

| | | |
|--------------|---------|------------------------------------------------------------------------------------------|
| SANYO | No.4958 | LC651104N/F/L, 651102N/F/L |
| | | Single-Chip 4-Bit Microcomputer For Small-Scale Control-Oriented Applications |

The LC651104N/F/L, LC651102N/F/L belong to our single-chip 4-bit microcomputer LC6500 series fabricated using CMOS process technology and are suited for use in small-scale control-oriented applications. Their basic architecture and instruction set are the same. The LC651104 and LC651102 comprise an eight-channel, 8-bit A/D converter. Application areas include audio equipment (tape deck, player, etc.), office equipment, communications equipment, car equipment, home appliances as well as circuits so far formed with the standard logic circuits and applications where the number of controls is small.

Features

- 1) CMOS technology for a low-power operation (with instruction-controlled standby function)
- 2) ROM/RAM
 - LC651104N/F/L ROM : 4K x 8bits, RAM : 256x 4bits
 - LC651102N/F/L ROM : 2K x 8bits, RAM : 256x 4bits
- 3) Instruction set : 80 instructions common to the LC6500 series
- 4) Wide operating voltage range from 2.5V to 6.0V (L version)
- 5) Instruction cycle time of 0.92 μ s (F version)
- 6) On-chip serial I/O port
- 7) Flexible I/O port
 - Number of ports : 6 ports/22 pins
 - All ports : Input/output common
 - Input/output voltage 15V max. (C,D,E,F at open drain)
 - Output current 20mA max. (sink current) (LED direct drivable)
 - Option selectable for your intended system
 - A. Open drain output, pull-up resistor : Single-bit select for all ports
 - B. Output level at the reset mode : 4-bit select of H/L level for port C/D
- 8) Interrupt function
 - Vectored interrupt by timer overflow (instruction-testable)
 - Vectored interrupt by $\overline{\text{INT}}$ pin or completion of transmit/receive at serial I/O port (instruction-testable)
- 9) Stack level : 8 levels (common with interrupt)
- 10) Timer : 4-bit prescaler + 8-bit programmable timer
- 11) Clock oscillation option selectable for your intended system
 - Oscillator option : 2-pin RC oscillation (N, L version)
 - 2-pin ceramic resonator oscillation (N,F,L version)
 - Predivider option : No predivider, 1/3 predivider, 1/4 predivider (N, L version)
- 12) Burst pulse (64 x cycle time) output function

- 13) A/D converter (sequential comparison type)
 - 8-bit Accuracy x 8 channels
- 14) Watchdog timer
 - External RC type
 - The external pin can be assigned the watchdog reset function by option.

Function Table

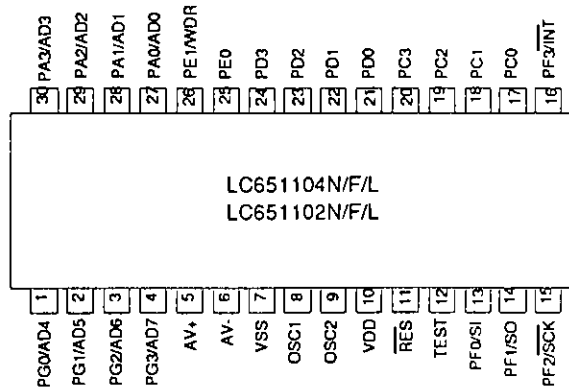
| Item | | LC651104N/1102N | LC651104F/1102F | LC651104L/1102L |
|-------------------|----------------------------|-----------------------------------------------------------------------------------|------------------------------------------------|---------------------------------------------------|
| Memory | ROM | 4096 x 8 bits (1104N) 2048 x 8 bits (1102N) | 4096 x 8 bits (1104F) 2048 x 8 bits (1102F) | 4096 x 8 bits (1104L) 2048 x 8 bits (1102L) |
| | RAM | 256 x 4 bits (1104N) 256 x 4 bits (1102N) | 256 x 4 bits (1104F) 256 x 4 bits (1102F) | 256 x 4 bits (1104L) 256 x 4 bits (1102L) |
| Instruction | Instruction set | 80 | 80 | 80 |
| | Table read | With | With | With |
| On-chip function | Interrupt | External 1, Internal 1 | External 1, Internal 1 | External 1, Internal 1 |
| | Timer | 4bit-prescaler + 8-bit timer | 4bit-prescaler + 8-bit timer | 4bit-prescaler + 8-bit timer |
| | Stack level | 8 | 8 | 8 |
| | Standby function | Standby available by HALT instruction | Standby available by HALT instruction | Standby available by HALT instruction |
| Input/output port | Number of ports | I/O 22 | I/O 22 | I/O 22 |
| | Serial port | 4/8-bit I/O | 4/8-bit I/O | 4/8-bit I/O |
| | I/O voltage | 15V max. | 15V max. | 15V max. |
| | Output current | 10mA typ. 20mA max. | 10mA typ. 20mA max. | 10mA typ. 20mA max. |
| | I/O circuit configuration | Open drain (N channel) or pull-up resistor-provided output selectable bit by bit. | | |
| | Output level at reset mode | "H" or "L" level selectable port by port (port C, D only) | | |
| | Burst pulse output | Available | Available | Available |
| Characteristic | Minimum cycle time | 2.77μs (VDD≥3V) | 0.92μs (VDD≥4V) | 3.84μs (VDD≥2.5V) |
| | Supply voltage | 3 to 6V | 4 to 6V | 2.5 to 6V |
| | Current dissipation | 1.5mA typ. | 2mA typ. | 1.5mA typ. |
| Oscillation | Resonator | RC (900kHz typ.) ceramic (400k, 800k, 1MHz, 4MHz) | ceramic 4MHz | RC (400kHz typ.) ceramic (400k, 800k, 1MHz, 4MHz) |
| | predivider option | 1/1, 1/3, 1/4 | 1/1 | 1/1, 1/3, 1/4 |
| Other | Package | DIP30S-D, MFP30S | DIP30S-D, MFP30S | DIP30S-D, MFP30S |

(Note) Information on the resonator and oscillation circuit constants will be presented as soon as the recommended circuit is determined.

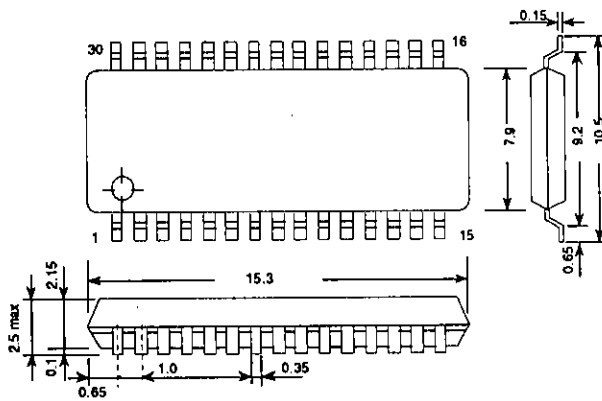
LC651104N/F/L, 651102N/F/L

Pin Assignment

Common to DIP • MFP

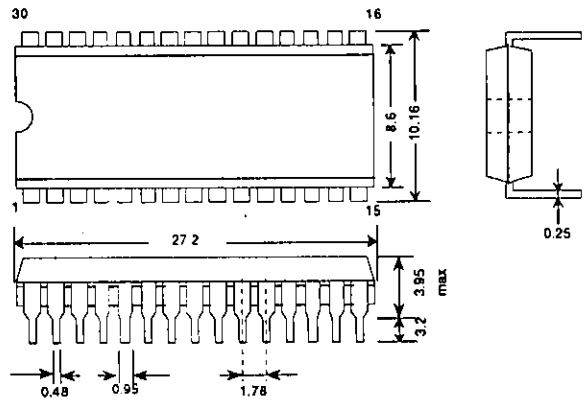


Case Outline 3073A (unit : mm)



SANYO : MFP30S

3061 (unit : mm)



SANYO : DIP30S-D

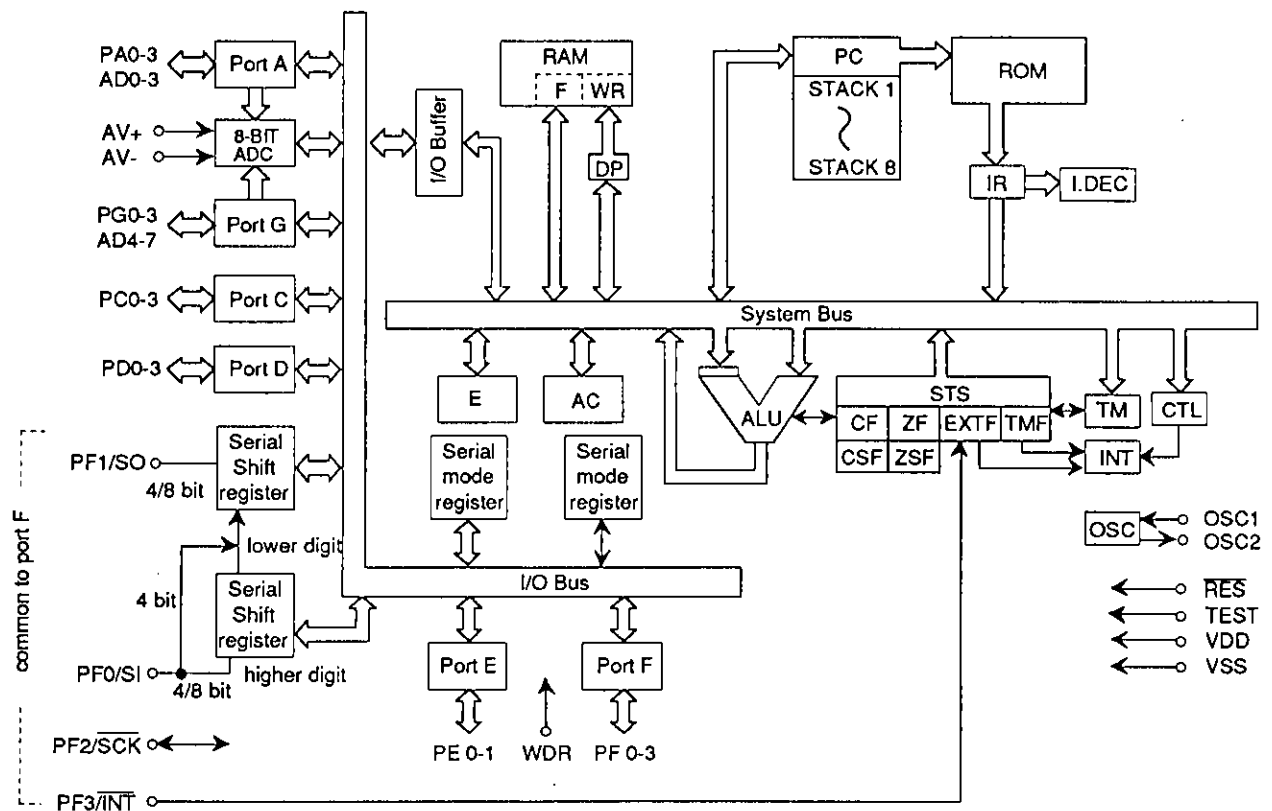
(Note) The package is the reference figure without the description of the rank. Please inquire us for the formal package.

Pin Name

| | | | |
|------------|---------------------------------------------------------------------------------|---------|----------------------------------------|
| OSC1, OSC2 | : C, R or ceramic resonator for OSC | TEST | : Test |
| RES | : Reset | INT | : Interrupt request pin |
| PA 0-3 | : Input/output common port A 0-3 | SI | : Serial input pin |
| PC 0-3 | : Input/output common port C 0-3 | SO | : Serial output pin |
| PD 0-3 | : Input/output common port D 0-3 | SCK | : Serial clock input/output pin |
| PE 0-1 | : Input/output common port E 0-1 | AD 0-7 | : AD converter input pin |
| PF 0-3 | : Input/output common port F 0-3 | AV+,AV- | : AD converter reference voltage input |
| PG 0-3 | : Input/output common port G 0-3 | WDR | : Watchdog reset pin |
| (Note) | • The SI, SO, SCK, and INT pins are common to the PF0 to PF3 pins respectively. | | |

System Block Diagram

LC651104N/F/L, LC651102N/F/L



| | | | |
|-----|-----------------------------|---------|-----------------------------------|
| RAM | : Data memory | ROM | : Program memory |
| F | : Flag | PC | : Program counter |
| WR | : Working register | INT | : Interrupt control |
| AC | : Accumulator | IR | : Instruction register |
| ALU | : Arithmetic and logic unit | I.DEC | : Instruction decoder |
| DP | : Data pointer | CF,CSF | : Carry flag, carry save flag |
| E | : E register | ZF, ZSF | : Zero flag, zero save flag |
| CTL | : Control register | EXT F | : External interrupt request flag |
| OSC | : Oscillator | TMF | : Internal interrupt request flag |
| TM | : Timer | | |
| STS | : Status register | | |

Development Support Tools

The following are available to support the program development for the LC651104, LC651102.

(1) User's Manual

"LC651104/1102 User's Manual"

(2) Development Tool Manual

For the EVA-800 system, refer to "EVA-800, LC651104/1102 Development Tool Manual".

(3) Development Tools

a. For program development (EVA-800 system)

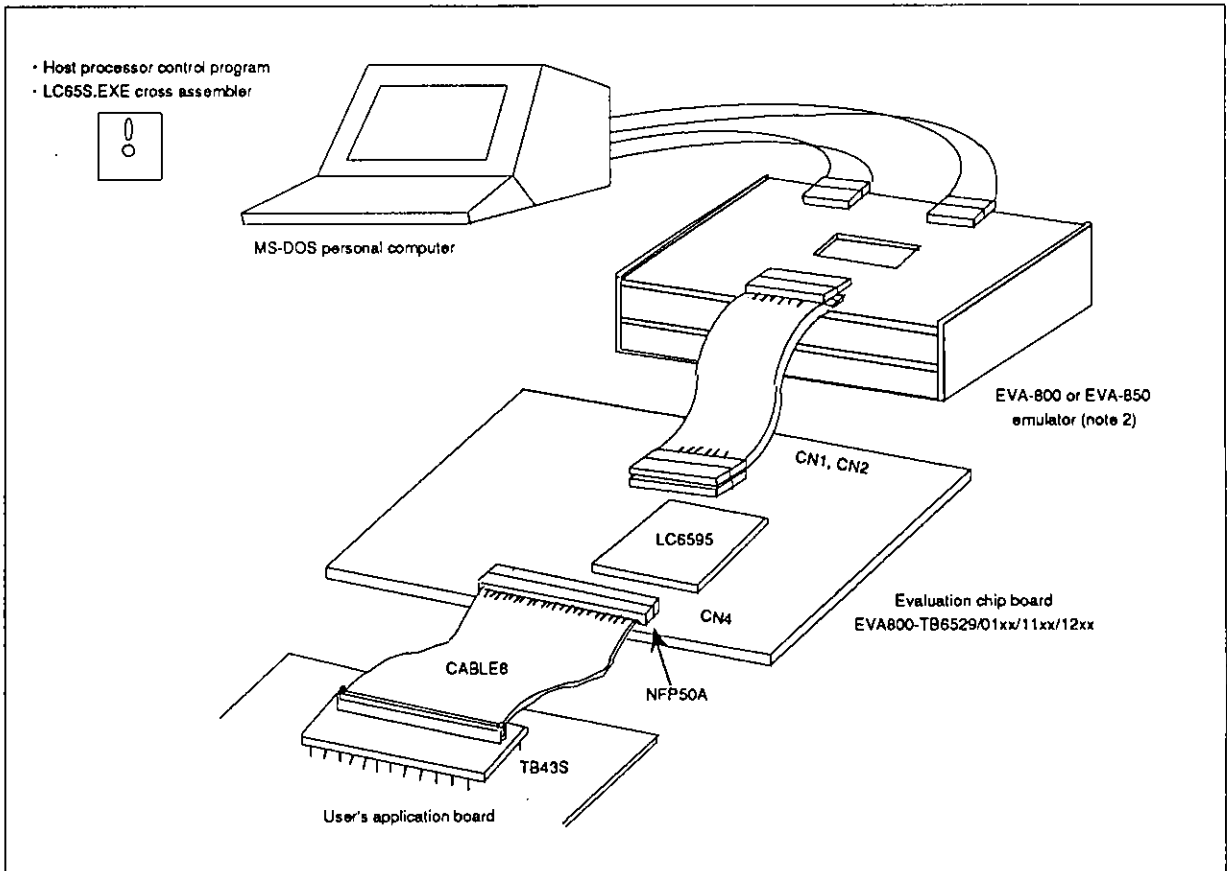
1. MS-DOS for host system (Note 1)
2. Cross assembler.....MS-DOS base cross assembler : <LC65S. EXE>
3. Evaluation chip : LC6595
4. Emulator : EVA-800 emulator and evaluation boards

b. For program development (EVA-86000 system) under development

c. For program evaluation During development EPROM built-in microcomputer (LC65E1104)

Appearance of Development Support System

EVA-800 System



(Note 1) MS-DOS : Trademark of Microsoft Corporation

(Note 2) The EVA-800 is a general term for emulator. A suffix (A, B,...) is added at the end of EVA-800 as the EVA-800 is improved to be a newer version. Do not use the EVA-800 with no suffix added.

Pin Description

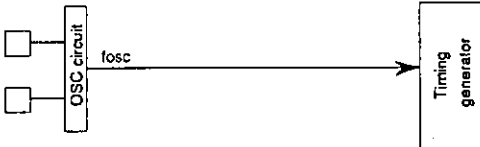
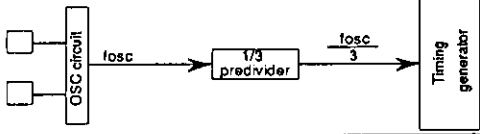
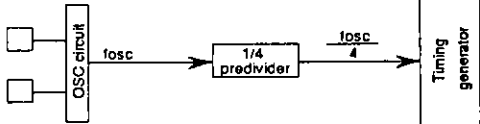
| Pin Name | Pins | I/O | Function | Option | Reset Mode | Unused Pin Handling |
|-----------------------------|--------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|
| VDD VSS | 1 1 | — — | Power supply | — | — | — |
| OSC1 OSC2 | 1 1 | Input Output | <ul style="list-style-type: none"> Pin for externally connecting RC, ceramic resonator for system clock generation. If external clock input is used, leave the OSC2 pin open. | 1) 2-pin RC OSC 2) 2-pin ceramic resonator OSC 3) Predivider option 1. No predivider 2. 1/3 predivider 3. 1/4 predivider | — | — |
| PA 0 to PA 3 /AD0 to AD3 | 4 | Input/ output | <ul style="list-style-type: none"> I/O port A0 to 3 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instruction) Single-bit set/reset (SPB, RPB instruction) Standby is controlled by PA3 The PA3 pin must be free from chattering during the HALT instruction execution cycle. All these four port pins can be used for two purposes <div style="border: 1px solid black; padding: 2px; margin-top: 5px;"> PA0/AD0 : AD converter input pin AD0 PA1/AD1 : AD converter input pin AD1 PA2/AD2 : AD converter input pin AD2 PA3/AD3 : AD converter input pin AD3 </div> | 1) Open drain type output 2) With pull-up resistor 1), 2) : Specified bit by bit | <ul style="list-style-type: none"> "H" output (Out-put Nch transistor : OFF) | Should be set to the open drain output type and then connected to the VSS pin. |
| PC 0 to PC 3 | 4 | Input/ output | <ul style="list-style-type: none"> I/O port C0 to 3 Same as for PA0 to 3 (Note) Option permits output at the reset mode to be "H" or "L". (Note) No standby control function is provided. | 1) Open drain type output 2) With pull-up resistor 3) Output at reset mode:"H" 4) Output at reset mode:"L" • 1), 2): Specified bit by bit • 3), 4): Specified in a group of 4 bits | <ul style="list-style-type: none"> "H" output "L" output (Option - selectable) | Same as for PA0 to 3 |
| PD 0 to PD 3 | 4 | Input/ output | <ul style="list-style-type: none"> I/O port D0 to 3 Same as for PC0 to 3 | Same as for PC0 to 3 | Same as for PC0 to 3 | Same as for PA0 to 3 |
| PE 0 to PE 1/WDR | 2 | Input/ output | <ul style="list-style-type: none"> I/O port E0 to 1 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit set/reset (SPB, RPB instruction) Single-bit decision (BP, BNP instruction) PE0 : With burst pulse (64Tcyc) output function PE1 pin can be switched WDR. | 1) Open drain type output 2) With pull-up resistor 1), 2) : Specified bit by bit 3) Normal port PE1 4) Watchdog reset :WDR 3), 4) : can be specified | <ul style="list-style-type: none"> "H" output (Out- put Nch transistor : OFF) | Same as for PA0 to 3 |

| Pin Name | Pins | I/O | Function | Option | Reset Mode | Unused Pin Handling |
|--------------------------------------------------------------------------------------------|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|----------------------------------|
| PF 0 / SI PF 1 / SO PF 2 / $\overline{\text{SCK}}$ PF 3 / $\overline{\text{INT}}$ | 4 | Input/output | <ul style="list-style-type: none"> I/O port F0 to 3 Same as for PE0 to 1 (Note) PF0 to 3 : Common with serial interface, $\overline{\text{INT}}$ input. <p>Program-selectable</p> <ul style="list-style-type: none"> SI •••• Serial input port SO ••• Serial output port $\overline{\text{SCK}}$ •• Serial clock input/output $\overline{\text{INT}}$ ••• Interrupt request input <p>4-bit/8-bit serial input/output is program-selectable. (Note) No burst pulse output function is provided.</p> | Same as for PA0 to 3 | Same as for PA0 to 3 | Same as for PA0 to 3 |
| PG 0 to PG 3 / AD4 to AD7 | 4 | Input/output | <ul style="list-style-type: none"> I/O port G0 to 3 Same as for PE0 to 1 (Note) (Note) No burst pulse output function is provided. All these four pins can be used for two purposes <div style="border: 1px solid black; padding: 2px; width: fit-content;"> PG0/AD4 : AD converter input pin AD4 PG1/AD5 : AD converter input pin AD5 PG2/AD6 : AD converter input pin AD6 PG3/AD7 : AD converter input pin AD7 </div> | Same as for PA0 to 3 | Same as for PA0 to 3 | Same as for PA0 to 3 |
| AV+ | 1 | — | <ul style="list-style-type: none"> Reference voltage input pin for A/D conversion. | — | — | Always connected to the VSS pin. |
| AV- | 1 | — | | | | |
| RES | 1 | Input | <ul style="list-style-type: none"> System reset input For power-up reset, C is connected externally. For reset restart, "L" level is applied for 4 clock cycles or more. | — | — | — |
| TEST | 1 | Input | <ul style="list-style-type: none"> LSI test pin Normally connected to VSS | — | — | Always connected to the VSS pin. |

Oscillator circuit option

| Option Name | Circuit | Conditions, etc. |
|--------------------------|---------|--------------------------|
| 1. External clock | | Leave the OSC2 pin open. |
| 2. 2-pin RC OSC | | |
| 3. Ceramic resonator OSC | | |

Predivider Option

| Option Name | Circuit | Conditions, etc. |
|---------------------------|-----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1. No predivider (1/1) |  | <ul style="list-style-type: none"> • Applicable to all of 3 OSC options. • The OSC frequency, external clock do not exceed 1444kHz. (LC651104N, 651102N) • The OSC frequency, external clock do not exceed 4330kHz. (LC651104F, 651102F) • The OSC frequency, external clock do not exceed 1040kHz. (LC651104L, 651102L) |
| 2. 1/3 predivider |  | <ul style="list-style-type: none"> • Applicable to only 2 OSC options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330kHz. |
| 3. 1/4 predivider |  | <ul style="list-style-type: none"> • Applicable to only 2 OSC options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330kHz. |

Note : The OSC option and predivider option are summarized below. Full care must be exercised.

Table of OSC, predivider Option of LC651104N/1102N, 1104F/1102F and 1104L/1102L

LC651104N, LC651102N

| Circuit Configuration | Frequency | Predivider Option (Cycle Time) | VDD Range | Remarks |
|---------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|--------------------|-----------------------------------|
| Ceramic resonator OSC | 400kHz | 1/1 (10 μs) | 3 to 6V | Unusable with 1/3, 1/4 predivider |
| | 800kHz | 1/1 (5 μs) | 3 to 6V | |
| | | 1/3 (15 μs) | 3 to 6V | |
| | | 1/4 (20 μs) | 3 to 6V | |
| 1MHz | 1/1 (4 μs) | 3 to 6V | | |
| | 1/3 (12 μs) | 3 to 6V | | |
| | 1/4 (16 μs) | 3 to 6V | | |
| 4MHz | 1/3 (3 μs) | 3 to 6V | | Unusable with 1/1 predivider |
| | 1/4 (4 μs) | 3 to 6V | | |
| | External clock by 2-pin RC OSC circuit | 200k to 1444kHz | 1/1 (20 to 2.77μs) | 3 to 6V |
| | 600k to 4330kHz | 1/3 (20 to 2.77μs) | 3 to 6V | |
| | 800k to 4330kHz | 1/4 (20 to 3.70μs) | 3 to 6V | |
| 2-pin RC | Used with 1/1predivider, recommended constants. If used with other than recommended constants, the frequency, VDD range must be the same as for external clock. | | 3 to 6V | |
| External clock input to the ceramic oscillation circuit | The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the 2-pin RC option. | | | |

LC651104F, LC651102F

| Circuit Configuration | Frequency | Predivider Option (Cycle Time) | VDD Range | Remarks |
|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-----------|---------|
| Ceramic resonator OSC | 4MHz | 1/1 (1μs) | 4 to 6V | |
| External clock by 2-pin RC OSC circuit | 200k to 4330kHz | 1/1 (20 to 0.92μs) | 4 to 6V | |
| External clock input to the ceramic oscillation circuit | The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the 2-pin RC option. | | | |

LC651104L, LC651102L

| Circuit Configuration | Frequency | Predivider Option (Cycle Time) | VDD Range | Remarks |
|---------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|-----------------------------------|-----------------------------------|
| Ceramic resonator OSC | 400kHz | 1/1 (10 μ s) | 2.5 to 6V | Unusable with 1/3, 1/4 predivider |
| | 800kHz | 1/1 (5 μ s) | 2.5 to 6V | |
| | | 1/3 (15 μ s) | 2.5 to 6V | |
| | | 1/4 (20 μ s) | 2.5 to 6V | |
| 1MHz | 1/1 (4 μ s) | 2.5 to 6V | | |
| | 1/3 (12 μ s) | 2.5 to 6V | | |
| | 1/4 (16 μ s) | 2.5 to 6V | | |
| 4MHz | 1/4 (4 μ s) | 2.5 to 6V | Unusable with 1/1, 1/3 predivider | |
| External clock by 2-pin RC OSC circuit | 200k to 1040kHz | 1/1 (20 to 3.84 μ s) | 2.5 to 6V | |
| | 600k to 3120kHz | 1/3 (20 to 3.84 μ s) | 2.5 to 6V | |
| | 800k to 4160kHz | 1/4 (20 to 3.84 μ s) | 2.5 to 6V | |
| 2-pin RC | Used with 1/1 predivider, recommended constants. If used with other than recommended constants, the frequency, VDD range must be the same as for external clock. | | 2.5 to 6V | |
| External clock input to the ceramic oscillation circuit | The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the 2-pin RC option. | | | |

Option of ports C, D Output Level at the Reset Mode

For input/output common ports C, D either of the following two output levels may be selected in a group of 4 bits during reset by option.

| Option Name | Conditions, etc. |
|-----------------------------------------|-----------------------------|
| 1. Output at the reset mode : "H" level | All of 4 bits of ports C, D |
| 2. Output at the reset mode : "L" level | All of 4 bits of ports C, D |

Option of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option .

| Option Name | Circuit | Applied ports |
|---------------------------------|---------|-----------------------------|
| 1. Open drain output | | • Ports A, C, D, E, F and G |
| 2. Output with pull-up resistor | | |

Watchdog reset option

This option can select the uses of PE1/WDR terminal. One is the normal port PE1, the other is the watchdog reset terminal WDR.

LC651104N, 651102N**1. Absolute Maximum Ratings at Ta=25°C, VSS=0V**

| Parameter | Symbol | Conditions | Pins | Limits | unit |
|-----------------------------|-----------|----------------------------------------------------|----------------------------------|-----------------------------------|------|
| Maximum supply voltage | VDD max | | VDD | -0.3 to +7.0 | V |
| Output voltage | VO | | OSC2 | Allowable up to voltage generated | V |
| Input voltage | VI(1) | | OSC1 (*1) | -0.3 to VDD+0.3 | V |
| | VI(2) | | TEST, RES, AV+, AV- | -0.3 to VDD+0.3 | V |
| Input/output voltage | VIO(1) | Port of OD type | PC0 - 3, PD0 - 3 | -0.3 to +15 | V |
| | VIO(2) | Port of PU type | PE0,1, PF0 - 3 | -0.3 to VDD+0.3 | V |
| | VIO(3) | | PA0 - 3, PG0 - 3 | -0.3 to VDD+0.3 | V |
| Peak output current | IOP | | I/O port | -2 to +20 | mA |
| Average output current | IOA | Per pin over the period of 100 ms | I/O Port | -2 to +20 | mA |
| | ΣIOA(1) | Total current of PC0 to 3, PD0 to 3, PE0 to 1 (*2) | PC0 to 3 PD0 to 3 PE0 to 1 | -15 to +100 | mA |
| | ΣIOA(2) | Total current of PF0 to 3, PG0 to 3, PA0 to 3 (*2) | PF0 to 3 PG0 to 3 PA0 to 3 | -15 to +100 | mA |
| Allowable power dissipation | Pd max(1) | Ta=-40 to +85°C (DIP package) | | 250 | mW |
| | Pd max(2) | Ta=-40 to +85°C (MFP package) | | 150 | mW |
| Operating temperature | Topg | | | -40 to +85 | °C |
| Storage temperature | Tstg | | | -55 to +125 | °C |

2. Allowable Operating Conditions at Ta=-40 to +85°C, VSS=0V, VDD=3.0 to 6.0V

| Parameter | Symbol | Conditions | VDD [V] | Pins | Limits | | | unit |
|--------------------------|--------|-------------------------|--------------|----------------------------|--------|------|---------|------|
| | | | | | min. | typ. | max. | |
| Operating supply voltage | VDD | | | VDD | 3.0 | | 6.0 | V |
| Standby supply voltage | VST | RAM, register hold (*3) | | VDD | 1.8 | | 6.0 | V |
| "H"-level input voltage | VIH(1) | Output Nch Tr.OFF | | Port C, D, E, F of OD type | 0.7VDD | | +13.5 | V |
| | VIH(2) | Output Nch Tr.OFF | | Port C, D, E, F of PU type | 0.7VDD | | VDD | V |
| | VIH(3) | Output Nch Tr.OFF | | Port A, G | 0.7VDD | | VDD | V |
| | VIH(4) | Output Nch Tr.OFF | | INT, SCK, SI of OD type | 0.8VDD | | +13.5 | V |
| | VIH(5) | Output Nch Tr.OFF | | INT, SCK, SI of PU type | 0.8VDD | | VDD | V |
| | VIH(6) | | VDD=1.8 to 6 | RES | 0.8VDD | | VDD | V |
| | VIH(7) | External clock mode | | OSC1 | 0.8VDD | | VDD | V |
| "L"-level input voltage | VIL(1) | Output Nch Tr.OFF | VDD=4 to 6 | Port | VSS | | 0.3VDD | V |
| | VIL(2) | Output Nch Tr.OFF | 3 to 6 | Port | VSS | | 0.25VDD | V |

| Parameter | Symbol | Conditions | VDD [V] | Pins | Limits | | | |
|-----------------------------------------------------|--------------|-----------------------------------------------------------------------------------|------------|--------------------------------------------------------|----------|--------------|-------------|----------------|
| | | | | | min. | typ. | max. | unit |
| "L"-level input voltage | VIL(3) | Output Nch Tr.OFF | VDD=4 to 6 | $\overline{\text{INT}}$, $\overline{\text{SCK}}$, SI | VSS | | 0.25VDD | V |
| | VIL(4) | Output Nch Tr.OFF | 3 to 6 | $\overline{\text{INT}}$, $\overline{\text{SCK}}$, SI | VSS | | 0.2VDD | V |
| | VIL(5) | External clock mode | VDD=4 to 6 | OSC1 | VSS | | 0.25VDD | V |
| | VIL(6) | External clock mode | 3 to 6 | OSC1 | VSS | | 0.2VDD | V |
| | VIL(7) | | VDD=4 to 6 | TEST | VSS | | 0.3VDD | V |
| | VIL(8) | | 3 to 6 | TEST | VSS | | 0.25VDD | V |
| | VIL(9) | | VDD=4 to 6 | $\overline{\text{RES}}$ | VSS | | 0.25VDD | V |
| | VIL(10) | | 3 to 6 | $\overline{\text{RES}}$ | VSS | | 0.2VDD | V |
| Operating frequency (cycle time) | fop (Tcyc) | When the 1/3 or 1/4 predivider option is selected, clock must not exceed 4.33MHz. | VDD=3 to 6 | | 200 (20) | | 1444 (2.77) | kHz (μ s) |
| External clock conditions | text | Fig.1. When clock exceeds 1.444 | VDD=3 to 6 | OSC1 | 200 | | 4330 | kHz |
| Pulse width | textH, textL | MHz, the 1/3 or 1/4 predivider | VDD=3 to 6 | OSC1 | 69 | | | ns |
| Rise/Fall time | textR, textF | option is selected. | VDD=3 to 6 | OSC1 | | | 50 | ns |
| Oscillation guaranty constants 2-pin RC oscillation | Cext | Fig.2 | VDD=3 to 6 | OSC1, OSC2 | | 270 \pm 5% | | pF |
| | Cext | Fig.2 | VDD=4 to 6 | OSC1, OSC2 | | 270 \pm 5% | | pF |
| | Rext | Fig.2 | VDD=3 to 6 | OSC1, OSC2 | | 12 \pm 1% | | k Ω |
| | Rext | Fig.2 | VDD=4 to 6 | OSC1, OSC2 | | 4.7 \pm 1% | | k Ω |
| Ceramic | | Fig.3 | | | | Table 1 | | |

3. Electrical Characteristics at Ta=-40 to +85°C, VSS=0V, VDD=3.0V to 6.0V

| Parameter | Symbol | Conditions | Pins | Limits | | | |
|-------------------------|---------------------|-----------------------------------------------------------------------|----------------------------|--------|-------|------|---------|
| | | | | min. | typ. | max. | unit |
| "H"-level input current | I _{IH} (1) | Output Nch Tr. OFF (including OFF leak current of Nch Tr.) VIN=+13.5V | Port C, D, E, F of OD type | | | +5.0 | μ A |
| | I _{IH} (2) | Output Nch Tr. OFF (including OFF leak current of Nch Tr.) VIN=VDD | Port A, G of OD type | | | +1.0 | μ A |
| | I _{IH} (3) | External clock mode, VIN=VDD | OSC1 | | | +1.0 | μ A |
| "L"-level input current | I _{IL} (1) | Output Nch Tr. OFF VIN=VSS | Port of OD type | -1.0 | | | μ A |
| | I _{IL} (2) | Output Nch Tr. OFF VIN=VSS | Port of PU type | -1.3 | -0.35 | | mA |
| | I _{IL} (3) | VIN=VSS | $\overline{\text{RES}}$ | -45 | -10 | | μ A |
| | I _{IL} (4) | External clock mode, VIN=VSS | OSC1 | -1.0 | | | μ A |

| Parameter | | Symbol | Conditions | Pins | Limits | | | |
|------------------------------------------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|----------------------------|----------------------------|--------------------------|----------|
| | | | | | min. | typ. | max. | unit |
| "H"-level output voltage | VOH(1) | | IOH=-50μA VDD=4.0 to 6.0V | Port of PU type | VDD-1.2 | | | V |
| | VOH(2) | | IOH=-10μA VDD=3.0 to 6.0V | Port of PU type | VDD-0.5 | | | V |
| "L"-level output voltage | VOL(1) | | IOL=10mA, VDD=4.0 to 6.0V | Port | | | 1.5 | V |
| | VOL(2) | | IOL=1mA, IOL of each port: 1mA or less VDD=3.0 to 6.0V | Port | | | 0.5 | V |
| Schmitt characteristics | Hysteresis voltage | VHIS | | RES, INT, SCK, SI, OSC1 of schmitt type(*4) | | 0.1VDD | | V |
| | 'H' level threshold voltage | VtH | | | 0.4VDD | | 0.8VDD | V |
| | 'L' level threshold voltage | VtL | | | 0.2VDD | | 0.6VDD | V |
| Current dissipation 2-pin RC oscillation | | IDDOP(1) | Output Nch Tr. OFF at operating, Port=VDD Fig.2 fosc=900kHz (TYP) | VDD | | 1.5 | 4 | mA |
| Ceramic resonator oscillation | | IDDOP(2) | Fig.3 4MHz, 1/3 predivider | VDD | | 1.5 | 5 | mA |
| | | IDDOP(3) | Fig.3 4MHz, 1/4 predivider | VDD | | 1.5 | 4 | mA |
| External clock | | IDDOP(4) | Fig.3 400kHz | VDD | | 1.0 | 2.5 | mA |
| | | IDDOP(5) | Fig.3 800kHz | VDD | | 1.5 | 4 | mA |
| | | IDDOP(6) | 200kHz to 1444kHz, 1/1 predivider 600kHz to 4330kHz, 1/3 predivider 800kHz to 4330kHz, 1/4 predivider | VDD | | 1.5 | 5 | mA |
| | Standby mode | IDDst | Output Nch Tr.OFF VDD=6V Port=VDD VDD=3V | VDD VDD | | 0.05 0.025 | 10 5 | μA μA |
| Oscillation characteristics Ceramic OSC Frequency | fCFOSC (*5) | Fig.3 fo=400kHz Fig.3 fo=800kHz Fig.3 fo=1MHz Fig.3 fo=4MHz,1/3 predivider 1/4 predivider | OSC1, OSC2 OSC1, OSC2 OSC1, OSC2 OSC1, OSC2 | 384 768 960 3840 | 400 800 1000 4000 | 416 832 1040 4160 | kHz kHz kHz kHz | |
| Stable time | tCFS | Fig.4 fo=400kHz Fig.4 fo=800kHz,1MHz,4MHz, 1/3 predivider,1/4 predivider | | | | 10 10 | ms ms | |

| Parameter | Symbol | Conditions | Pins | Limits | | | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------|-----------|-------------------|------|------|----|
| | | | | min. | typ. | max. | unit | |
| Oscillation characteristics 2-pin RC oscillation Frequency | fMOSC | Fig.2 Cext=270PF±5% Fig.2 Rext=4.7kΩ±1% VDD=4 to 6V | OSC1, OSC2 | 634 | 900 | 1278 | kHz | |
| | | Fig.2 Cext=270PF±5% Fig.2 Rext=12kΩ±1% VDD=3 to 6V | OSC1, OSC2 | 276 | 400 | 742 | | |
| Pull-up resistance I/O port | RPP | Output N-ch Tr. OFF VIN=VSS VDD=5V | Port of PU | 8 type | 14 | 30 | kΩ | |
| | RES | VIN=VSS VDD=5V | RES | 300 | 500 | 700 | | |
| External reset characteristics Reset time | tRST | | | | See Fig.5. | | | |
| Pin capacitance | Cp | f=1MHz Other than pins to be tested, VIN=VSS | | | 10 | | pF | |
| Serial Clock Input clock cycle time Output clock cycle time Input clock "L" level pulse width Onput clock "L" level pulse width Input clock "H" level pulse width Onput clock "H" level pulse width | tCKCY(1) | Fig.6 | SCK | 3.0 | | | μs | |
| | tCKCY(2) | Fig.6 | SCK | | 64 x tCYC (*6) | | μs | |
| | tCKL(1) | Fig.6 | SCK | 1.0 | | | μs | |
| | tCKL(2) | Fig.6 | SCK | | 32 x tCYC | | μs | |
| | tCKH(1) | Fig.6 | SCK | 1.0 | | | μs | |
| | tCKH(2) | Fig.6 | SCK | | 32 x tCYC | | μs | |
| | Serial input Data setup time Data hold time | tICK | Specified for ↑ of SCK Fig.6 | SI | 0.4 | | | μs |
| | | tCKI | | SI | 0.4 | | | μs |
| Serial output Output delay time | tCKO | Specified for ↓ of SCK Nch OD only, External 1kΩ, External 50pF, Fig.6 | SO | | | 0.6 | μs | |
| Pulse output Period "H"-level pulse width "L"-level pulse width | tPCY | Fig.7 tCYC=4 x System clock Period, Nch OD only, External 1kΩ, External 50pF | PE0 | | 64 x tCYC | | μs | |
| | tPH | | PE0 | | 32 x tCYC ±10% | | μs | |
| | tPL | | PE0 | | 32 x tCYC ±10 | | μs | |

| Parameter | Symbol | Conditions | Pins | Limits | | | |
|-------------------------------|--------------------------|--------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|--------------------------|------|------------------------|------|
| | | | | min. | typ. | max. | unit |
| AD conversion characteristics | | | | | | | |
| Resolution | | VDD=4 to 6 | | | 8 | | Bit |
| Absolute accuracy | | AV+=VDD AV-=VSS VDD=4 to 6 | | | ±1 | ±2 | LSB |
| Conversion time | TCAD | AD speed 1/1 At 26 x tCYC VDD=4 to 6 | | 72 (tCYC= 2.77µs) | | 312 (tCYC= 12µs) | µs |
| | | AD speed 1/2 At 51 x tCYC VDD=4 to 6 | | 141 (tCYC= 2.77µs) | | 612 (tCYC= 12µs) | |
| Reference input voltage | AV+ | VDD=4 to 6 | AV+ | AV- | | VDD | V |
| | AV- | | AV- | VSS | | AV+ | |
| Reference input current range | IRIF | AV+=VDD VDD=4 to 6 AV-=VSS | AV+, AV- | 75 | 150 | 300 | µA |
| Analog input voltage range | VAIN | VDD=4 to 6 | AD0 to AD7 | AV- | | AV+ | V |
| Analog port input current | IAIN | Including output OFF leakage current. VAIN=VDD VDD=4 to 6 | Port pins AD0 to AD7 (with the output circuit of the input/output multi-functional port pins set to OD type) | | | 1 | µA |
| | | VAIN=VSS VDD=4 to 6 | | -1 | | | |
| Watchdog Timer | Guaranteed constant (*7) | Cw | PE1 at open drain output VDD=3 to 6V | WDR | | 0.1±5% | µF |
| | | Rw | PE1 at open drain output VDD=3 to 6V | WDR | | 680±1% | kΩ |
| | | Rl | PE1 at open drain output VDD=3 to 6V | WDR | | 100±1% | Ω |
| | Clear time (discharge) | tWCT | Fig. 8 VDD=3 to 6V | WDR | 100 | | µs |
| | Clear time (charge) | tWCCY | Fig. 8 VDD=3 to 6V | WDR | 36 | | ms |
| | Guaranteed constant (*7) | Cw | PE1 at open drain output VDD=4 to 6V | WDR | | 0.047±5% | µF |
| | | Rw | PE1 at open drain output VDD=4 to 6V | WDR | | 680±1% | kΩ |
| | | Rl | PE1 at open drain output VDD=4 to 6V | WDR | | 100±1% | Ω |
| | Clear time (discharge) | tWCT | Fig. 8 VDD=4 to 6V | WDR | 40 | | µs |
| | Clear time (charge) | tWCCY | Fig. 8 VDD=4 to 6V | WDR | 18 | | ms |

- (*1) When oscillated internally under the oscillating conditions in Fig.4, up to the oscillation amplitude generated is allowable.
- (*2) Average over the period of 100ms.
- (*3) Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
- (*4) The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option or external clock oscillation option has been selected.
- (*5) fCFOSC: oscillation frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.
- (*6) TCYC=4 x system clock period
- (*7) If using under the wet environment, give care to the leak of the pin adjoined PE1, and the leak of the external RC constant.

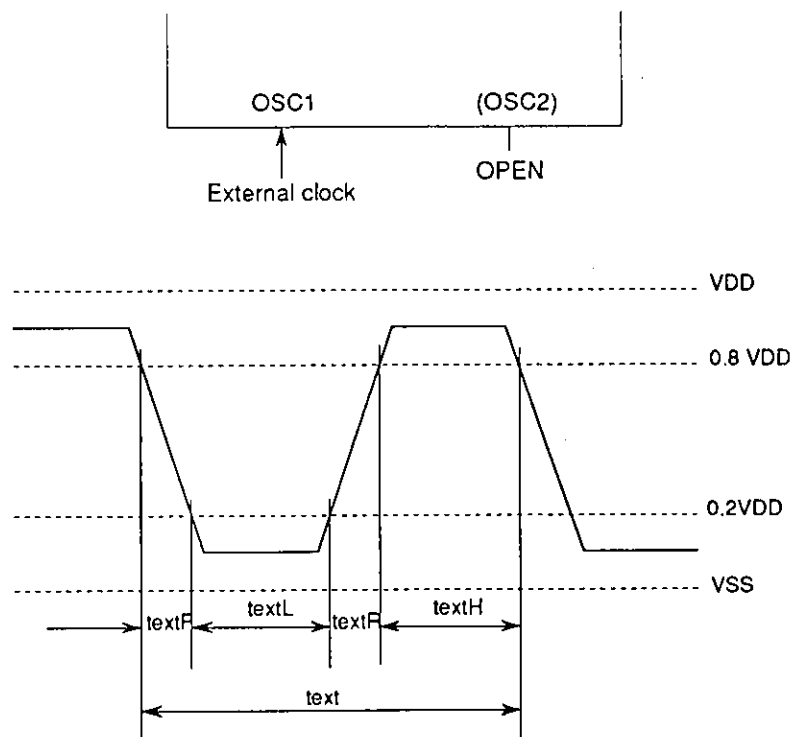


Fig. 1 External Clock Input Waveform

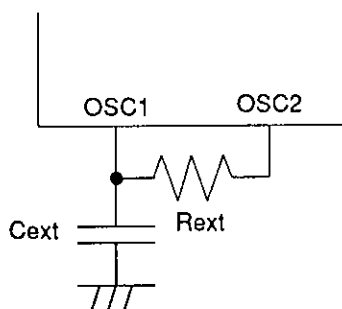


Fig. 2 2-pin RC Oscillation Circuit

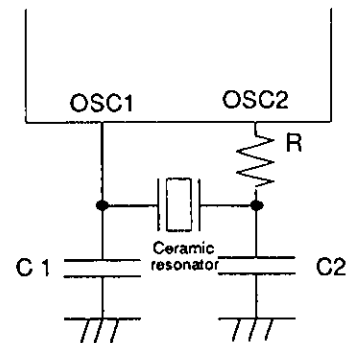


Fig. 3 Ceramic Resonator Oscillation Circuit

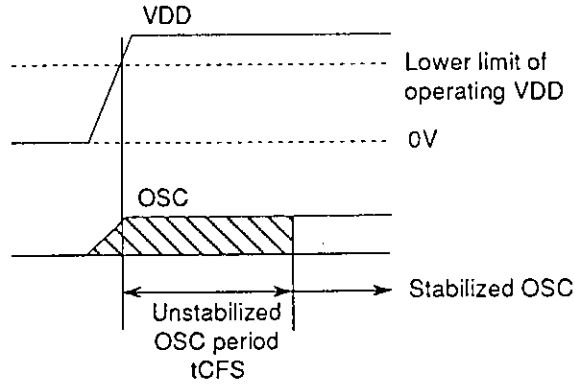


Fig. 4 Oscillation Stabilizing Period

Table 1 Constants Guaranteed for Ceramic Resonator OSC

| | | |
|-------------------------|----|-----------|
| 4MHz (Murata) | C1 | 33pF±10% |
| CSA4.00MG | C2 | 33pF±10% |
| CST4.00MGW (built-in C) | R | 0Ω |
| 4MHz (Kyocera) | C1 | 33pF±10% |
| KBR4.0MSA | C2 | 33pF±10% |
| KBR4.0MKS (built-in C) | R | 0Ω |
| 1MHz (Murata) | C1 | 100pF±10% |
| CSB1000J | C2 | 100pF±10% |
| | R | 2.2kΩ |
| 1MHz (Kyocera) | C1 | 100pF±10% |
| KBR1000F | C2 | 100pF±10% |
| | R | 0Ω |
| 800kHz (Murata) | C1 | 100pF±10% |
| CSB800J | C2 | 100pF±10% |
| | R | 2.2kΩ |
| 800kHz (Kyocera) | C1 | 220pF±10% |
| KBR800F | C2 | 220pF±10% |
| | R | 0Ω |
| 400kHz (Murata) | C1 | 220pF±10% |
| CSB400P | C2 | 220pF±10% |
| | R | 2.2kΩ |
| 400kHz (Kyocera) | C1 | 330pF±10% |
| KBR400BK | C2 | 330pF±10% |
| | R | 0Ω |

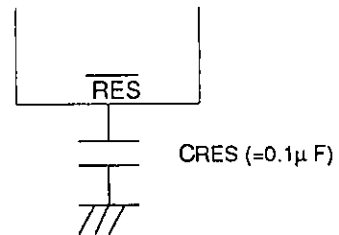


Fig. 5 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at $C_{RES}=0.1\mu F$. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

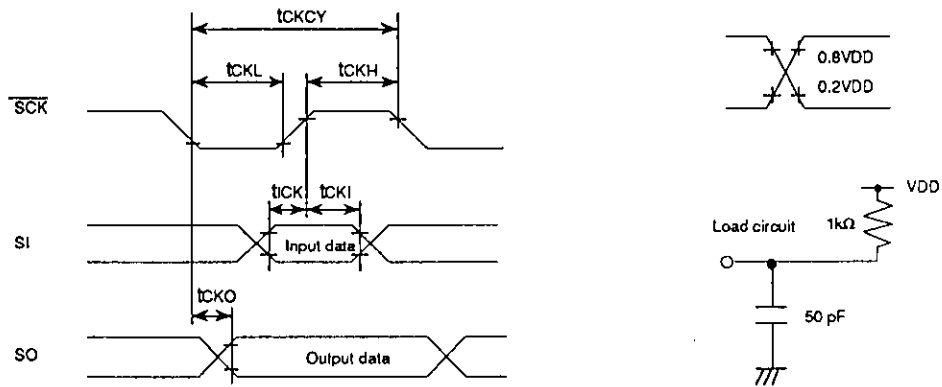
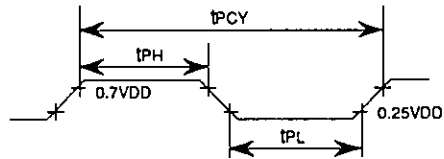
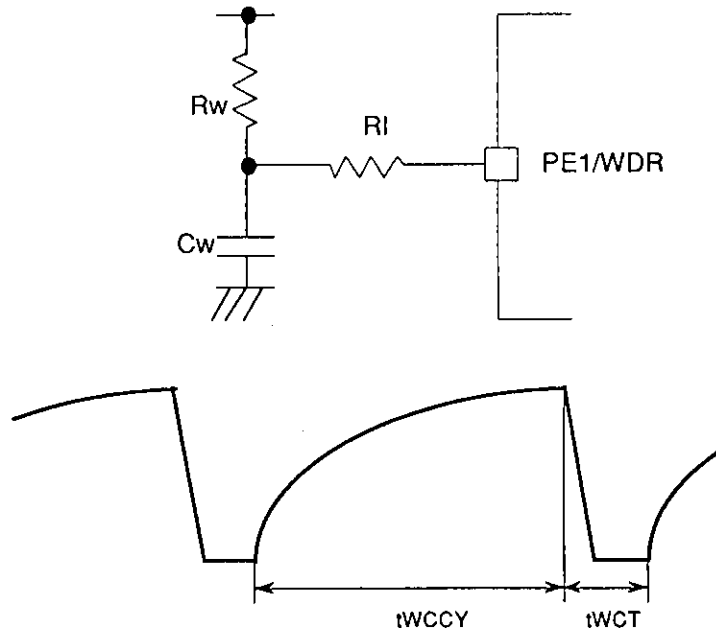


Fig. 6 Serial Input/Output Timing



The load conditions are the same as in Fig. 6.

Fig. 7 Pulse Output Timing at Port PE0



t_{WCCY} : The charge time by the time constant of the external C_w , R_w , R_i
 t_{WCT} : The discharge time by program operation

Fig. 8 Wave form of the watchdog timer

RC Oscillation Characteristics of the LC651104N, LC651102N
To be determined.

LC651104F, LC651102F

1. Absolute Maximum Ratings at Ta=25°C, VSS=0V

| Parameter | Symbol | Conditions | Pin | Limits | unit |
|-----------------------------|-----------|----------------------------------------------------|----------------------------------|-----------------------------------|------|
| Maximum supply voltage | VDD max | | VDD | -0.3 to +7.0 | V |
| Output voltage | VO | | OSC2 | Allowable up to voltage generated | V |
| Input voltage | VI(1) | | OSC1 (*1) | -0.3 to VDD+0.3 | V |
| | VI(2) | | TEST, RES, AV+, AV- | -0.3 to VDD+0.3 | V |
| Input/output voltage | VIO(1) | Port of OD type | PC0-3, PD0-3, | -0.3 to +15 | V |
| | VIO(2) | Port of PU type | PE0, 1, PF0-3 | -0.3 to VDD+0.3 | V |
| | VIO(3) | | PA0-3, PG0-3 | -0.3 to VDD+0.3 | V |
| Peak output current | IOP | | I/O Port | -2 to +20 | mA |
| Average output current | IOA | Per pin over the period of 100ms | I/O Port | -2 to +20 | mA |
| | ΣIOA(1) | Total current of PC0 to 3, PD0 to 3, PE0 to 1 (*2) | PC0 to 3 PD0 to 3 PE0 to 1 | -15 to +100 | mA |
| | ΣIOA(2) | Total current of PF0 to 3, PG0 to 3, PA0 to 3 (*2) | PF0 to 3 PG0 to 3 PA0 to 3 | -15 to +100 | mA |
| Allowable power dissipation | Pd max(1) | Ta=-40 to +85°C (DIP package) | | 250 | mW |
| | Pd max(2) | Ta=-40 to +85°C (MFP package) | | 150 | mW |
| Operating temperature | Topg | | | -40 to +85 | °C |
| Storage temperature | Tstg | | | -55 to +125 | °C |

2. Allowable Operating Conditions at Ta=-40 to +85°C, VSS=0V, VDD=4.0 to 6.0V

| Parameter | Symbol | Conditions | Pin | Limits | | | | |
|--------------------------|--------|-------------------------|----------------------------|--------|--------|-------|------|---|
| | | | | min. | typ. | max. | unit | |
| Operating supply voltage | VDD | | VDD | 4.0 | | 6.0 | V | |
| Standby supply voltage | VST | RAM, register hold (*3) | VDD | 1.8 | | 6.0 | V | |
| "H"-level input voltage | VIH(1) | Output Nch Tr. OFF | Port C, D, E, F of OD type | 0.7VDD | | +13.5 | V | |
| | VIH(2) | Output Nch Tr. OFF | Port C, D, E, F of PU type | 0.7VDD | | VDD | V | |
| | VIH(3) | Output Nch Tr. OFF | Port A, G | 0.7VDD | | VDD | V | |
| | VIH(4) | Output Nch Tr. OFF | INT, SCK, SI of OD type | 0.8VDD | | +13.5 | V | |
| | VIH(5) | Output Nch Tr. OFF | INT, SCK, SI of PU type | 0.8VDD | | VDD | V | |
| | VIH(6) | | VDD=1.8 to 6.0V | RES | 0.8VDD | | VDD | V |
| | VIH(7) | | External clock mode | OSC1 | 0.8VDD | | VDD | V |

| Parameter | Symbol | Conditions | Pin | Limits | | | |
|--------------------------------------------------------|--------------|---------------------|--------------|--------------|------|-------------|----------|
| | | | | min. | typ. | max. | unit |
| "L"-level input voltage | VIL(1) | Output Nch Tr. OFF | Port | VSS | | 0.3VDD | V |
| | VIL(2) | Output Nch Tr. OFF | INT, SCK, SI | VSS | | 0.25VDD | V |
| | VIL(3) | External clock mode | OSC1 | VSS | | 0.25VDD | V |
| | VIL(4) | | TEST | VSS | | 0.3VDD | V |
| | VIL(5) | | RES | VSS | | 0.25VDD | V |
| Operating frequency (Cycle time) | fOP (Tcyc) | | | 200 (20) | | 4330 (0.92) | kHz (μs) |
| External clock conditions | | | | | | | |
| Frequency | text | } Fig. 1 | OSC1 | 200 | | 4330 | kHz |
| Pulse width | textH, textL | | OSC1 | 69 | | | ns |
| Rise/fall time | textR, textF | | OSC1 | | | 50 | ns |
| Oscillation guaranteed constants ceramic resonator OSC | | Fig. 2 | | See Table 1. | | | |

3. Electrical Characteristics at Ta=-40 to +85°C, VSS=0V, VDD=4.0 to 6.0V

| Parameter | Symbol | Conditions | Pin | Limits | | | |
|--------------------------|-----------------------------|-----------------------------------------------------------------------|---------------------------------------------|---------|--------|--------|------|
| | | | | min. | typ. | max. | unit |
| "H"-level input current | IIH(1) | Output Nch Tr. OFF (including OFF leak current of Nch Tr.) VIN=+13.5V | Port C, D, E, F of OD type | | | +5.0 | μA |
| | IIH(2) | Output Nch Tr. OFF (including OFF leak current of Nch Tr.) VIN=VDD | Port A, G, of OD type | | | +1.0 | μA |
| | IIH(3) | External clock mode, VIN=VDD | OSC1 | | | +1.0 | μA |
| "L"-level input current | IIL(1) | Output Nch Tr. OFF VIN=VSS | Port of OD type | -1.0 | | | μA |
| | IIL(2) | Output Nch Tr. OFF VIN=VSS | Port of PU type | -1.3 | -0.35 | | mA |
| | IIL(3) | VIN=VSS | RES | -45 | -10 | | μA |
| | IIL(4) | External clock mode, VIN=VSS | OSC1 | -1.0 | | | μA |
| "H"-level output voltage | VOH(1) | IOH=-50μA | Port of PU type | VDD-1.2 | | | V |
| | VOH(2) | IOH=-10μA | Port of PU type | VDD-0.5 | | | V |
| "L"-level output voltage | VOL(1) | IOL=10mA | Port | | | 1.5 | V |
| | VOL(2) | IOL=1mA, IOL of each port : 1mA or less | Port | | | 0.5 | V |
| Schmitt characteristics | Hysteresis voltage | VHIS | RES, INT, SCK, SI, OSC1 of schmitt type(*4) | | 0.1VDD | | V |
| | 'H' level threshold voltage | VtH | | 0.4VDD | | 0.8VDD | V |
| | 'L' level threshold voltage | VtL | | 0.25VDD | | 0.6VDD | V |

| Parameter | Symbol | Conditions | Pin | Limits | | | |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------------------------------------------------------------------------|-------------------------|--------|----------------|-----------|------------|
| | | | | min. | typ. | max. | unit |
| Current dissipation Ceramic resonator OSC External clock | IDDOP(1) | Fig. 2 4MHz | VDD | | 2 | 6 | mA |
| | IDDOP(2) | 200kHz to 4330kHz *1 Output Nch Tr. OFF at Operating mode Port=VDD | VDD | | 2 | 6 | mA |
| Standby mode | IDDst | Output Nch Tr. OFF VDD=6V Port=VDD VDD=3V | VDD | | 0.05 | 10 | μ A |
| | | | VDD | | 0.025 | 5 | μ A |
| Oscillation characteristics Ceramic resonator OSC Frequency Stable time | fCFOSC | Fig.2 fo=4MHz (*5) | OSC1, OSC2 | 3840 | 4000 | 4160 | kHz |
| | tCFS | Fig.3 fo=4MHz | | | | 10 | ms |
| Pull-up resistance I/O port $\overline{\text{RES}}$ | RPP | Output Nch Tr. OFF VIN=VSS VDD=5V | Port of PU type | 8 | 14 | 30 | k Ω |
| | RU | VIN=VSS VDD=5V | $\overline{\text{RES}}$ | 300 | 500 | 700 | k Ω |
| External reset characteristics Reset time | tRST | | | | See Fig. 4 | | |
| Pin capacitance | Cp | f=1MHz, other than pins to be tested, VIN=VSS | | | 10 | | pF |
| Serial clock Input clock Cycle time Output clock Cycle time Input clock "L"-level pulse width Output clock "L"-level pulse width Input clock "H"-level pulse width Output clock "H"-level pulse width | tCKCY(1) | Fig. 5 | $\overline{\text{SCK}}$ | 2.0 | | | μ s |
| | tCKCY(2) | Fig. 5 | $\overline{\text{SCK}}$ | | 64 x tCYC (*6) | | μ s |
| | tCKL(1) | Fig. 5 | SCK | 0.6 | | | μ s |
| | tCKL(2) | Fig. 5 | $\overline{\text{SCK}}$ | | | 32 x tCYC | μ s |
| | tCKH(1) | Fig. 5 | $\overline{\text{SCK}}$ | | 0.6 | | μ s |
| | tCKH(2) | Fig. 5 | SCK | | | 32 x tCYC | μ s |
| Serial input Data setup time Data hold time | tICK | Specified for \uparrow of $\overline{\text{SCK}}$ | SI | 0.2 | | | μ s |
| | tCKI | Fig. 5 | SI | 0.2 | | | μ s |

LC651104N/F/L, 651102N/F/L

| Parameter | Symbol | Conditions | Pin | Limits | | | | |
|--------------------------------------------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------|------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-------------------|------------------------|------|----|
| | | | | min. | typ. | max. | unit | |
| Serial output Output delay time | tCKO | Specified for ↓ of \overline{SCK} Nch OD only, External 1kΩ External 50pF, Fig.5 | SO | | | 0.4 | μs | |
| Pulse output Period "H"-level Pulse width "L"-level Pulse width | tPCY | Fig. 6 TCYC=4 x System clock Period Nch OD only, External 1kΩ External 50pF | PE0 | | 64 x tCYC | | μs | |
| | tPH | | PE0 | | 32 x tCYC ±10% | | μs | |
| | tPL | | PE0 | | 32 x tCYC ±10% | | μs | |
| AD conversion characteristics Resolution Absolute accuracy | | VDD=4 to 6 | | | 8 | | Bit | |
| | | AV+=VDD AV-=VSS | VDD=4.5 to 6 AD speed 1/1 | | ±1 | ±2 | LSB | |
| | | | VDD=4 to 6 AD speed 1/2 | | ±1 | ±2 | LSB | |
| Conversion time | TCAD | AD speed 1/1 At 26 x tCYC VDD=4.5 to 6 | | 24 (tCYC= 0.92μs) | | 312 (tCYC= 12μs) | μs | |
| | | AD speed 1/2 At 51 x tCYC VDD=4 to 6 | | 47 (tCYC= 0.92μs) | | 612 (tCYC= 12μs) | μs | |
| Reference input voltage | AV+ | VDD=4 to 6 | AV+ | AV- | | VDD | V | |
| | AV- | | AV- | VSS | | AV+ | | |
| Reference input current range | IRIF | AV+=VDD AV-=VSS | VDD=4 to 6 | AV+, AV- | 75 | 150 | 300 | μA |
| Analog input voltage range | VAIN | VDD=4 to 6 | | AD0 to AD7 | AV- | | AV+ | V |
| Analog port input current | IAIN | Including output OFF leakage current. VAIN=VDD | VDD=4 to 6 | Port pins AD0 to AD7 (with the output circuit of the input/output multi-functional port pins set to OD type) | | | 1 | μA |
| | | VAIN=VSS | VDD=4 to 6 | | -1 | | | |
| Watchdog Timer | Guaranteed constant (*7) | Cw | PE1 at open drain output | WDR | | 0.01 ±5% | | μF |
| | | Rw | PE1 at open drain output | WDR | | 680 ±1% | | kΩ |
| | | Rl | PE1 at open drain output | WDR | | 100 ±1% | | Ω |
| | Clear time (discharge) | tWCT | Fig. 7 | WDR | 10 | | | μs |
| | Clear time (charge) | tWCCY | Fig. 7 | WDR | 4.2 | | | ms |

(*1) When oscillated internally under the oscillating conditions in Fig.2, up to the oscillation amplitude generated is allowable.

(*2) Average over the period of 100ms.

(*3) Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.

- (*4) The OSC1 pin can be schmitt-triggered when the external clock oscillation option has been selected.
- (*5) f_{CFOSC} : Oscillatable frequency.
- (*6) $TCYC=4 \times$ System clock period
- (*7) If using under the wet environment, give care to the leak of the pin adjoined PE1, and the leak of the external RC constant.

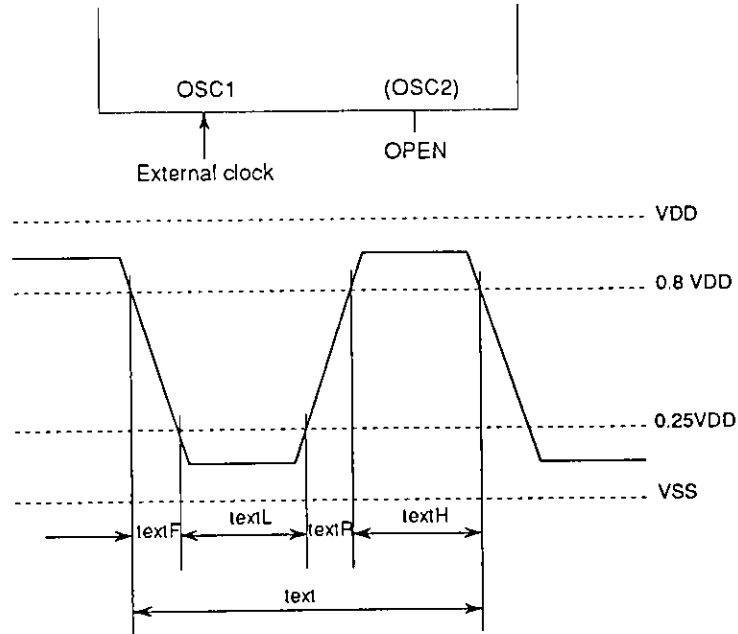


Fig. 1 External Clock Input Waveform

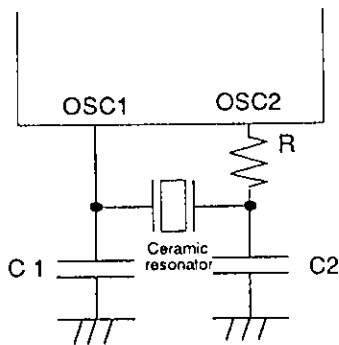


Fig. 2 Ceramic resonator OSC circuit

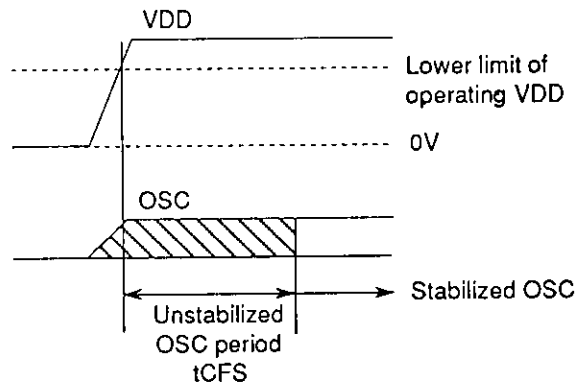


Fig. 3 OSC Stabilizing Period

Table 1. Constants Guaranteed for Ceramic Resonator OSC

| | | |
|-----------------------------|----|----------------|
| 4MHz (Murata) CSA4.00MG | C1 | 33pF \pm 10% |
| | C2 | 33pF \pm 10% |
| CST4.00MGW (built-in C) | R | 0 Ω |
| 4MHz (Kyocera) KBR4.0MSA | C1 | 33pF \pm 10% |
| | C2 | 33pF \pm 10% |
| KBR4.0MKS (built-in C) | R | 0 Ω |

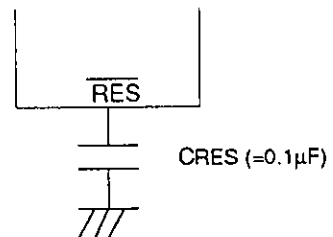


Fig. 4 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at $CRES=0.1\mu F$. If the rise time of the power supply is long, the value of $CRES$ must be increased so that the reset time becomes 10ms or more.

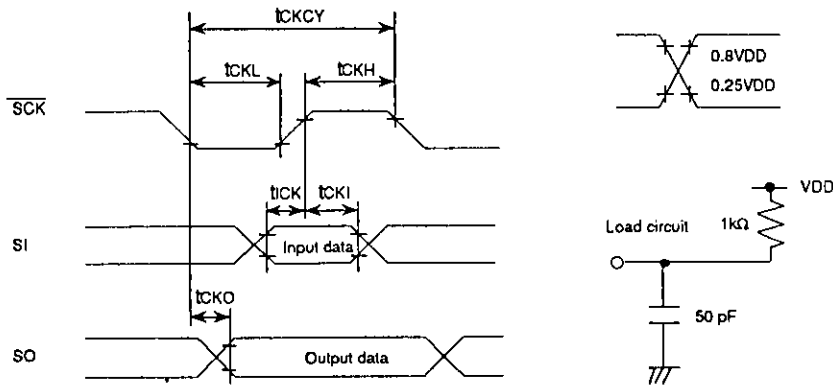
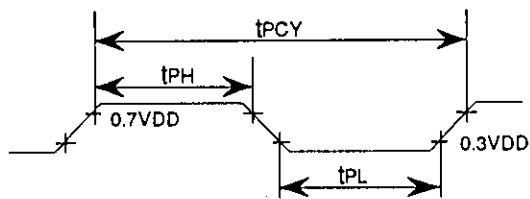
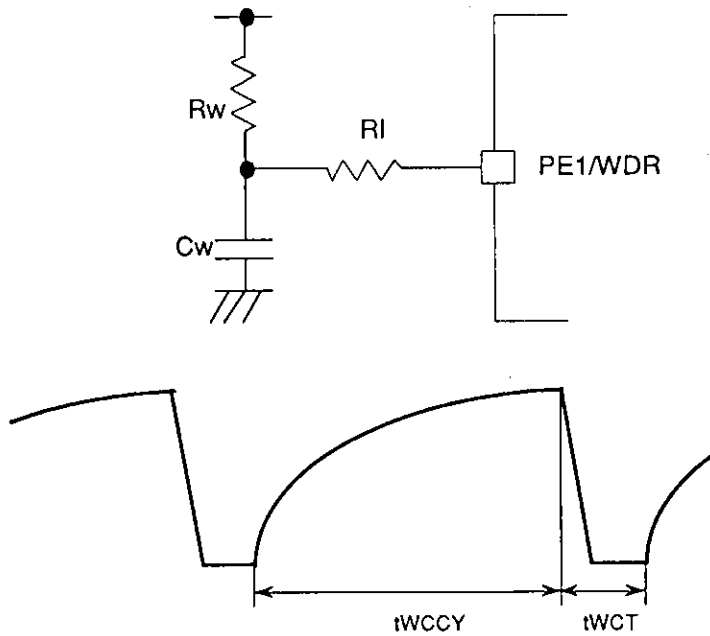


Fig. 5 Serial Input/Output Timing



The load conditions are the same as in Fig. 5.

Fig. 6 Pulse Output Timing at Port PE0



t_{WCCY} : The charge time by the time constant of the external C_w , R_w , R_l
 t_{WCT} : The discharge time by program operation

Fig. 7 Wave form of the watchdog timer

LC651104L, LC651102L

1. Absolute Maximum Ratings at Ta=25°C, VSS=0V

| Parameter | Symbol | Conditions | Pin | Limits | unit |
|-----------------------------|-----------------|---------------------------------------------------|----------------------------------|-----------------------------------|------|
| Maximum supply voltage | VDD max | | VDD | -0.3 to 7.0 | V |
| Output voltage | VO | | OSC2 | Allowable up to voltage generated | V |
| Input voltage | VI(1) | | OSC1 (*1) | -0.3 to VDD+0.3 | V |
| | VI(2) | | TEST, RES, AV+, AV- | -0.3 to VDD+0.3 | V |
| Input/output voltage | VIO(1) | Port of OD type | PC0-3, PD0-3 | -0.3 to +15 | V |
| | VIO(2) | Port of PU type | PE0, 1, PF0-3 | -0.3 to VDD+0.3 | V |
| | VIO(3) | | PA0-3, PG0-3 | -0.3 to VDD+0.3 | V |
| Peak output current | IOP | | I/O Port | -2 to +20 | mA |
| Average output current | IOA | Per pin over the period of 100ms | I/O Port | -2 to +20 | mA |
| | Σ IOA(1) | Total curren of PC0 to 3, PD0 to 3, PE0 to 1 (*2) | PC0 to 3 PD0 to 3 PE0 to 1 | -15 to +100 | mA |
| | Σ IOA(2) | Total curren of PF0 to 3, PG0 to 3, PA0 to 3 (*2) | PF0 to 3 PG0 to 3 PA0 to 3 | -15 to +100 | mA |
| Allowable power dissipation | Pd max(1) | Ta=-40 to +85°C (DIP package) | | 250 | mW |
| | Pd max(2) | Ta=-40 to +85°C (MFP package) | | 150 | mW |
| Operating temperature | Topg | | | -40 to +85 | °C |
| Storage temperature | Tstg | | | -55 to +125 | °C |

2. Allowable Operating Conditions at Ta=-40°C to 85°C, VSS=0V, VDD=2.5 to 6.0V

| Parameter | Symbol | Conditions | Pin | Limits | | | unit |
|--------------------------|--------|-------------------------|----------------------------------------------|--------|------|-------|------|
| | | | | min. | typ. | max. | |
| Operating supply voltage | VDD | | VDD | 2.5 | | 6.0 | V |
| Standby supply voltage | VST | RAM, register hold (*3) | VDD | 1.8 | | 6.0 | V |
| "H"-level input voltage | VIH(1) | Output Nch Tr. OFF | Port C, D, E, F of OD type | 0.7VDD | | +13.5 | V |
| | VIH(2) | Output Nch Tr. OFF | Port C, D, E, F of PU type | 0.7VDD | | VDD | V |
| | VIH(3) | Output Nch Tr. OFF | Port A, G | 0.7VDD | | VDD | V |
| | VIH(4) | Output Nch Tr. OFF | $\overline{\text{INT}}$, SCK, SI of OD type | 0.8VDD | | +13.5 | V |
| | VIH(5) | Output Nch Tr. OFF | $\overline{\text{INT}}$, SCK, SI of PU type | 0.8VDD | | VDD | V |
| | VIH(6) | VDD=1.8 to 6.0V | RES | 0.8VDD | | VDD | V |
| | VIH(7) | External clock | OSC1 | 0.8VDD | | VDD | V |

| Parameter | Symbol | Conditions | Pin | Limits | | | |
|----------------------------------|----------------------|----------------------------------------------------------------------------------|--------------|------------|--------|----------------|------|
| | | | | min. | typ. | max. | unit |
| "L"-level input voltage | VIL(1) | Output Nch Tr. OFF | Port | VSS | | 0.2VDD | V |
| | VIL(2) | Output Nch Tr. OFF | INT, SCK, SI | VSS | | 0.15VDD | V |
| | VIL(3) | External clock | OSC1 | VSS | | 0.15VDD | V |
| | VIL(4) | | TEST | VSS | | 0.2VDD | V |
| | VIL(5) | | RES | VSS | | 0.15VDD | V |
| Operating frequency (cycle time) | fOP (Tcyc) | When the 1/4 predivider option is selected, clock must not exceed 4.16MHz. | | 200 (20) | | 1040kHz (3.84) | (μs) |
| External Clock conditions | Frequency | Fig.1 When clock exceeds 1.040MHz, the 1/3 or 1/4 predivider option is selected. | OSC1 | 200 | | 4160 | kHz |
| | Pulse width | | OSC1 | 100 | | | ns |
| | Rise/fall time | | OSC1 | | | 100 | ns |
| Oscillation guaranteed constants | 2-pin RC oscillation | Cext Rext | Fig.2 | OSC1, OSC2 | 270±5% | | pF |
| | | | | | 12±1% | | kΩ |
| | Ceramic oscillation | | Fig.3 | | | See Table 1. | |

3. Electrical Characteristics at Ta=-40 to +85°C, VSS=0V, VDD=2.5 to 6.0V

| Parameter | Symbol | Conditions | Pin | Limits | | | |
|--------------------------|--------|-----------------------------------------------------------------------|----------------------------|---------|-------|------|------|
| | | | | min. | typ. | max. | unit |
| "H"-level input current | IIH(1) | Output Nch Tr. OFF (including OFF leak current of Nch Tr.) VIN=+13.5V | Port C, D, E, F of OD type | | | +5.0 | μA |
| | IIH(2) | Output Nch Tr. OFF (including OFF leak current of Nch Tr.) VIN=VDD | Port A, G of OD type | | | +1.0 | μA |
| | IIH(3) | External clock mode, VIN=VDD | OSC1 | | | +1.0 | μA |
| "L"-level input current | IIL(1) | Output Nch Tr. OFF VIN=VSS | Port of OD type | -1.0 | | | μA |
| | IIL(2) | Output Nch Tr. OFF VIN=VSS | Port of PU type | -1.3 | -0.35 | | mA |
| | IIL(3) | VIN=VSS | RES | -45 | -10 | | μA |
| | IIL(4) | External clock mode, VIN=VSS | OSC1 | -1.0 | | | μA |
| "H"-level output voltage | VOH | IOH=-10μA | Port of PU type | VDD-0.5 | | | V |
| "L"-level output voltage | VOL(1) | IOL=3mA | Port | | | 1.5 | V |
| | VOL(2) | IOL=1mA, IOL of each port: 1mA or less | Port | | | 0.4 | V |

| Parameter | | Symbol | Conditions | Pin | Limits | | | |
|----------------------------------------------------|-----------------------------|---------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|-----------|--------|------------|------|
| | | | | | min. | typ. | max. | unit |
| Schmitt Characteristics | Hysteresis voltage | VHIS | | \overline{RES} , \overline{INT} , \overline{SCR} , SI, OSC1 of schmitt type(*4) | | 0.1VDD | | V |
| | 'H' level threshold voltage | VtH | | | 0.4VDD | | 0.8VDD | V |
| | 'L' level threshold voltage | VtL | | | 0.2VDD | | 0.6VDD | V |
| Current dissipation 2-pin RC OSC Ceramic OSC | | IDDOP(1) | Output Nch Tr. OFF at operating, Port=VDD Fig.2 fOSC=400kHz (TYP) | VDD | | 1.0 | 4 | mA |
| | | IDDOP(2) | Fig.3 4MHz, 1/4predivider | VDD | | 1.5 | 4 | mA |
| | | IDDOP(3) | Fig.3 4MHz, 1/4predivider VDD=2.5V | VDD | | 0.5 | 1 | mA |
| | | IDDOP(4) | Fig.3 400kHz | VDD | | 1.0 | 2.5 | mA |
| | | IDDOP(5) | Fig.3 800kHz | VDD | | 1.5 | 4.0 | mA |
| | External clock | IDDOP(6) | 200kHz to 1024kHz, 1/1 predivider 600kHz to 3120kHz, 1/3 predivider 800kHz to 4160kHz, 1/4 predivider | VDD | | 1.5 | 4 | mA |
| Standby mode | IDDst | Output Nch Tr. OFF VDD=6V | VDD | | 0.05 | 10 | μ A | |
| | | Port=VDD VDD=2.5V | VDD | | 0.020 | 4 | μ A | |
| Oscillation characteristics Ceramic OSC | | | | | | | | |
| Frequency | fCFOSC (*5) | Fig.3 fo=400kHz | OSC1, OSC2 | 384 | 400 | 416 | kHz | |
| | | Fig.3 fo=800kHz | OSC1, OSC2 | 768 | 800 | 832 | kHz | |
| | | Fig.3 fo=1MHz | OSC1, OSC2 | 960 | 1000 | 1040 | kHz | |
| | | Fig.3 fo=4MHz, 1/4 predivider | OSC1, OSC2 | 3840 | 4000 | 4160 | kHz | |
| Stable time | tCFS | Fig.4 fo=400kHz | | | | 10 | ms | |
| | | Fig.4 fo=800kHz, 1MHz, 4MHz, 1/4 predivider | | | | 10 | ms | |
| 2-pin RC OSC Frequency | fMOSC | Fig.2 Cext=270PF \pm 5% Fig.2 Rext=12k Ω \pm 1% | OSC1, OSC2 | 276 | 400 | 742 | kHz | |
| Pull-up resistance I/O port | RPP | Output Nch Tr. OFF VIN=VSS VDD=5V | Port of PU type | 8 | 14 | 30 | k Ω | |
| | RES | VIN=VSS VDD=5V | \overline{RES} | 300 | 500 | 700 | k Ω | |
| External reset characteristics | | | | | | | | |
| Reset time | tRST | | | | See Fig.5 | | | |
| Pin capacitance | Cp | f=1MHz, Other than pins to be tested, VIN=VSS | | | 10 | | pF | |

| Parameter | Symbol | Conditions | Pin | Limits | | | |
|-------------------------------------------|----------|------------------------------------------------------------------------------------------------------------|------------------|---------------------------------|-------------------------|-------------------------------|---------|
| | | | | min. | typ. | max. | unit |
| Serial clock Input clock Cycle time | tCKCY(1) | Fig.6 | \overline{SCK} | 6.0 | | | μs |
| Output clock Cycle time | tCKCY(2) | Fig.6 | \overline{SCK} | | 64 x tCYC (*6) | | μs |
| Input clock "L"-level pulse width | tCKL(1) | Fig.6 | \overline{SCK} | 2.0 | | | μs |
| Output clock "L"-level pulse width | tCKL(2) | Fig.6 | \overline{SCK} | | 32 x tCYC | | μs |
| Input clock "H"-level pulse width | tCKH(1) | Fig.6 | \overline{SCK} | 2.0 | | | μs |
| Output clock "H"-level pulse width | tCKH(2) | Fig.6 | \overline{SCK} | | 32 x tCYC | | μs |
| Serial Input Data setup time | tICK | Specified for \uparrow of \overline{SCK} | SI | 0.5 | | | μs |
| Data hold time | tCKI | Fig.6 | SI | 0.5 | | | μs |
| Serial Output Output delay time | tCKO | Specified for \downarrow of \overline{SCK} Nch OD only, External 1k Ω Fig.6 External 50pF | SO | | | 1.0 | μs |
| Pulse output Period | tPCY | Fig.7 | PE0 | | 64 x tCYC | | μs |
| "H"-level pulse width | tPH | TCYC=4 x System clock Period | PE0 | | 32 x tCYC $\pm 10\%$ | | μs |
| "L"-level pulse width | tPL | Nch OD only, External 1k Ω External 50pF | PE0 | | 32 x tCYC $\pm 10\%$ | | μs |
| AD conversion characteristics | | | | | | | |
| Resolution | | VDD=4 to 6 | | | 8 | | Bit |
| Absolute accuracy | | AV+=VDD AV-=VSS VDD=4 to 6 | | | ± 1 | ± 2 | LSB |
| Conversion time | TCAD | AD speed 1/1 At 26 x tCYC VDD=4 to 6 | | 99 (tCYC= 3.84 μs) | | 312 (tCYC= 12 μs) | μs |
| | | AD speed 1/2 At 51 x tCYC VDD=4 to 6 | | 195 (tCYC= 3.84 μs) | | 612 (tCYC= 12 μs) | μs |
| Reference input voltage | AV+ | VDD=4 to 6 | AV+ | AV- | | VDD | V |
| | AV- | | AV- | VSS | | AV+ | |
| Reference input current range | IRIF | AV+=VDD VDD=4 to 6 AV-=VSS | AV+, AV- | 75 | 150 | 300 | μA |
| Analog input voltage range | VAIN | VDD=4 to 6 | AD0 to AD7 | AV- | | AV+ | V |

| Parameter | Symbol | Conditions | Pin | Limits | | | |
|-------------------------------|--------------------------|--------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|--------|------|-----------------|------------------|
| | | | | min. | typ. | max. | unit |
| AD conversion characteristics | | | | | | | |
| Analog port input current | IAIN | Including output OFF leakage current. VAIN=VDD VDD=4 to 6 | Port pins AD0 to AD7 (with the output circuit of the input/output multi-functional port pins set to OD type) | | | 1 | μA |
| | | VAIN=VSS VDD=4 to 6 | | -1 | | | |
| Watchdog Timer | Guaranteed constant (*7) | Cw | PE1 at open drain output VDD=2.5V to 6V | WDR | | $0.1 \pm 5\%$ | μF |
| | | Rw | PE1 at open drain output VDD=2.5V to 6V | WDR | | $680 \pm 1\%$ | $\text{k}\Omega$ |
| | | RI | PE1 at open drain output VDD=2.5V to 6V | WDR | | $100 \pm 1\%$ | Ω |
| | Clear time (discharge) | tWCT | Fig. 8 VDD=2.5V to 6V | WDR | 100 | | μs |
| | Clear time (charge) | tWCCY | Fig. 8 VDD=2.5V to 6V | WDR | 31 | | ms |
| | Guaranteed constant (*7) | Cw | PE1 at open drain output VDD=2.5V to 6V | WDR | | $0.047 \pm 5\%$ | μF |
| | | Rw | PE1 at open drain output VDD=2.5V to 6V | WDR | | $680 \pm 1\%$ | $\text{k}\Omega$ |
| | | RI | PE1 at open drain output VDD=2.5V to 6V | WDR | | $100 \pm 1\%$ | Ω |
| | Clear time (discharge) | tWCT | Fig. 8 VDD=2.5V to 6V | WDR | 40 | | μs |
| | Clear time (charge) | tWCCY | Fig. 8 VDD=2.5V to 6V | WDR | 14 | | ms |

(*1) When oscillated internally under the oscillating conditions in Fig.3, up to the oscillation amplitude generated is allowable.

(*2) Average over the period of 100ms.

(*3) Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction.

The PA3 pin must be free from chattering during the HALT instruction execution cycle.

(*4) The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option, or external clock oscillation option has been selected.

(*5) fCOSC : Oscillatable frequency.

(*6) TCYC=4 x System clock period

(*7) If using under the wet environment, give care to the leak of the pin adjoined PE1, and the leak of the external RC constant.

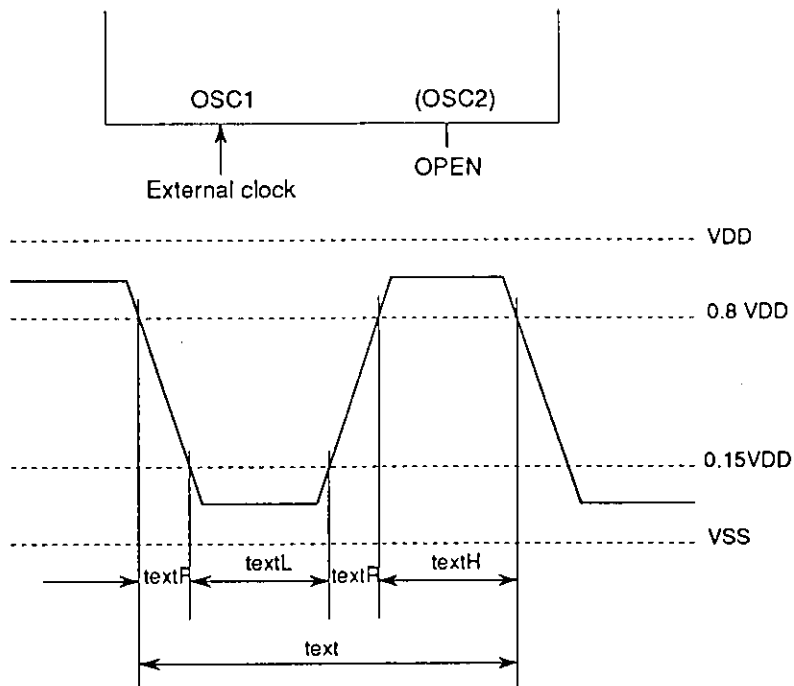


Fig. 1 External Clock Input Waveform

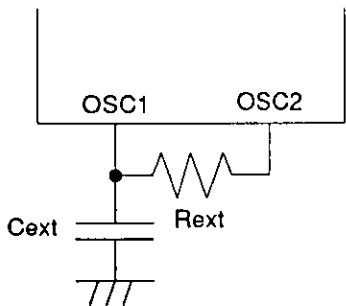


Fig. 2 2-pin RC Oscillation Circuit

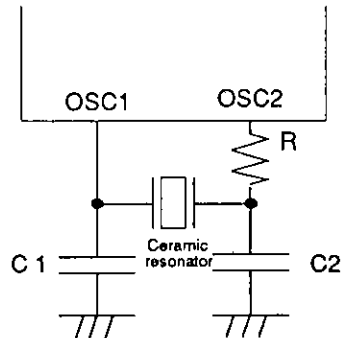


Fig. 3 Ceramic Resonator Oscillation Circuit

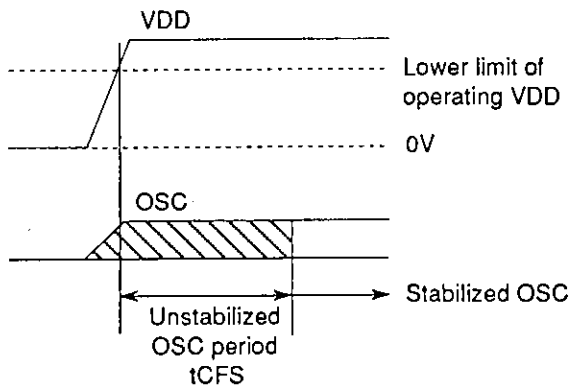


Fig. 4 Oscillation Stabilizing Period

Table 1 Constants Guaranteed for Ceramic Resonator OSC

| | | |
|---------------------------------------------------------|----|-----------|
| 4MHz (Murata) CSA4.00MGU CST4.00MGWU (built-in C) | C1 | 33pF±10% |
| | C2 | 33pF±10% |
| | R | 0Ω |
| 1MHz (Murata) CSB1000J | C1 | 100pF±10% |
| | C2 | 100pF±10% |
| | R | 2.2kΩ |
| 1MHz (Kyocera) KBR1000F | C1 | 100pF±10% |
| | C2 | 100pF±10% |
| | R | 0Ω |
| 800kHz (Murata) CSB800J | C1 | 100pF±10% |
| | C2 | 100pF±10% |
| | R | 2.2kΩ |
| 800kHz (Kyocera) KBR800F | C1 | 220pF±10% |
| | C2 | 220pF±10% |
| | R | 0Ω |
| 400kHz (Murata) CSB400P | C1 | 220pF±10% |
| | C2 | 220pF±10% |
| | R | 2.2kΩ |
| 400kHz (Kyocera) KBR400BK | C1 | 330pF±10% |
| | C2 | 330pF±10% |
| | R | 0Ω |

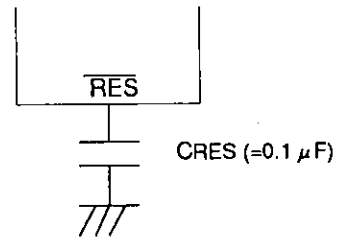


Fig. 5 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at CRES=0.1μF. If the rise time of the power supply is long, the value of CRES must be increased so that the reset time becomes 10ms or more.

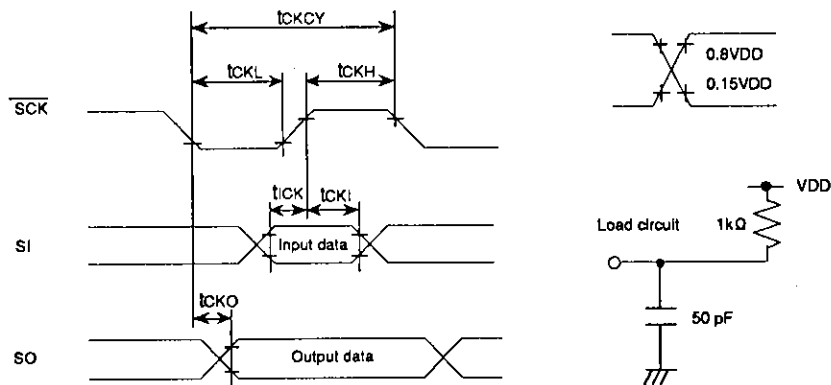


Fig. 6 Serial Input/Output Timing

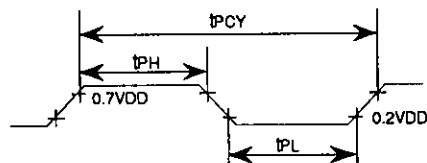
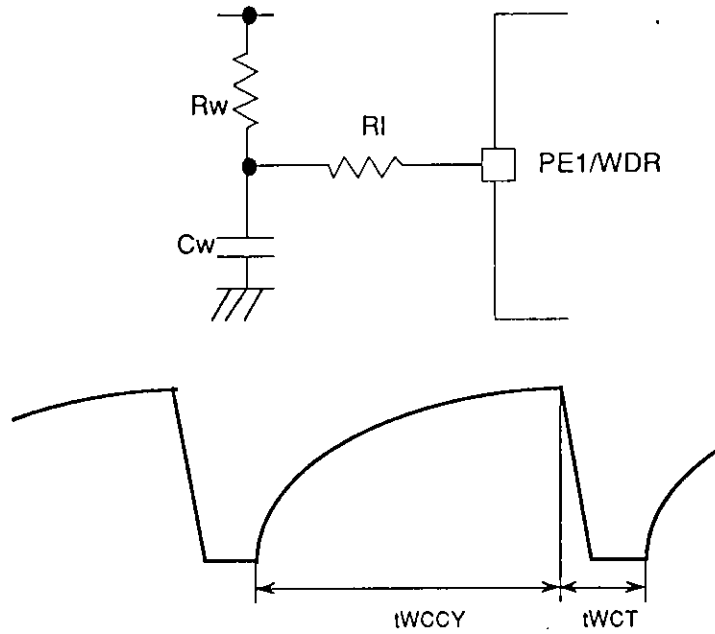


Fig.7 Pulse Output Timing at Port PE0

The load conditions are the same as in Fig. 6.



t_{WCCY} : The charge time by the time constant of the external C_w , R_w , R_I
 t_{WCT} : The discharge time by program operation

Fig. 8 Wave form of the watchdog timer

RC Oscillation Characteristic of the LC651104L, 651102L
 To be determined.

LC651104, LC651102 SERIES INSTRUCTION SET (BY FUNCTIONS)

| | | | | | |
|----------------|-----------------------------------|---------------------|--------------------------------------------------|-----|--------------------------|
| Symbol | Description | M(DP) | : Memory addressed by DP | () | : Contents |
| AC | : Accumulator | P(DP _L) | : Input/output port addressed by DP _L | - | : Transfer and direction |
| ACt | : Accumulator bit t | PC | : Program counter | + | : Addition |
| CF | : Carry flag | STACK | : Stack register | - | : Subtraction |
| CTL | : Control register | TM | : Timer | ∧ | : AND |
| DP | : Data pointer | TMF | : Timer (internal) interrupt request flag | ∨ | : OR |
| E | : E register | At, Ha, La | : Working register | ⊕ | : Exclusive OR |
| EXTF | : External interrupt request flag | ZF | : Zero flag | | |
| F _n | : Flag bit n | | | | |
| M | : Memory | | | | |

| Instruction group | Mnemonic | | Instruction code | | Bytes | Cycles | Function | Description | Status flag affected | Remarks | | | | | | | | | | | |
|----------------------------------------------|---------------------------------------------|---------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------|-------|--------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------------------------------------------------------------------------------------------------------|--------------------------|----------------|---|--------------------------|----------------|---|--------------------------|----------------|---|-------|-------|
| | | | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | | | | | | | | | | | | | | | | | |
| Accumulator manipulation instructions | CLA | Clear AC | 1 1 0 0 | 0 0 0 0 | 1 | 1 | AC ← 0 | The AC contents are cleared. | ZF | * 1 | | | | | | | | | | | |
| | CLC | Clear CF | 1 1 1 0 | 0 0 0 1 | 1 | 1 | CF ← 0 | The CF contents are cleared. | CF | | | | | | | | | | | | |
| | STC | Set CF | 1 1 1 1 | 0 0 0 1 | 1 | 1 | CF ← 1 | The CF is set. | CF | | | | | | | | | | | | |
| | CMA | Complement AC | 1 1 1 0 | 1 0 1 1 | 1 | 1 | AC ← \overline{AC} | The AC contents are complemented. | ZF | | | | | | | | | | | | |
| | INC | Increment AC | 0 0 0 0 | 1 1 1 0 | 1 | 1 | AC ← (AC) + 1 | The AC contents are incremented +1. | ZF CF | | | | | | | | | | | | |
| | DEC | Decrement AC | 0 0 0 0 | 1 1 1 1 | 1 | 1 | AC ← (AC) - 1 | The AC contents are decremented -1. | ZF CF | | | | | | | | | | | | |
| | RAL | Rotate AC left through CF | 0 0 0 0 | 0 0 0 1 | 1 | 1 | AC ₀ ← (CF), AC _{n+1} ← (AC) _n , CF ← (AC) ₃ | The AC contents are shifted left through the CF. | ZF CF | | | | | | | | | | | | |
| | TAE | Transfer AC to E | 0 0 0 0 | 0 0 1 1 | 1 | 1 | E ← (AC) | The AC contents are transferred to the E. | | | | | | | | | | | | | |
| XAE | Exchange AC with E | 0 0 0 0 | 1 1 0 1 | 1 | 1 | (AC) ↔ (E) | The AC contents and the E contents are exchanged. | | | | | | | | | | | | | | |
| Memory manipulation instructions | INM | Increment M | 0 0 1 0 | 1 1 1 0 | 1 | 1 | M(DP) ← (M(DP)) + 1 | The M(DP) contents are incremented +1. | ZF CF | | | | | | | | | | | | |
| | DEM | Decrement M | 0 0 1 0 | 1 1 1 1 | 1 | 1 | M(DP) ← (M(DP)) - 1 | The M(DP) contents are decremented -1. | ZF CF | | | | | | | | | | | | |
| | SMB bit | Set M data bit | 0 0 0 0 | 1 0 B ₁ B ₀ | 1 | 1 | M(DP, B ₁ B ₀) ← 1 | A single bit of the M(DP) specified with B ₁ B ₀ is set. | | | | | | | | | | | | | |
| | RMB bit | Reset M data bit | 0 0 1 0 | 1 0 B ₁ B ₀ | 1 | 1 | M(DP, B ₁ B ₀) ← 0 | A single bit of the M(DP) specified with B ₁ B ₀ is reset. | ZF | | | | | | | | | | | | |
| Arithmetic operation/comparison instructions | AD | Add M to AC | 0 1 1 0 | 0 0 0 0 | 1 | 1 | AC ← (AC) + (M(DP)) | Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC. | ZF CF | | | | | | | | | | | | |
| | ADC | Add M to AC with CF | 0 0 1 0 | 0 0 0 0 | 1 | 1 | AC ← (AC) + (M(DP)) + (CF) | Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC. | ZF CF | | | | | | | | | | | | |
| | DAA | Decimal adjust AC in addition | 1 1 1 0 | 0 1 1 0 | 1 | 1 | AC ← (AC) + 6 | 6 is added to the AC contents. | ZF | | | | | | | | | | | | |
| | DAS | Decimal adjust AC in subtraction | 1 1 1 0 | 1 0 1 0 | 1 | 1 | AC ← (AC) + 10 | 10 is added to the AC contents. | ZF | | | | | | | | | | | | |
| | EXL | Exclusive or M to AC | 1 1 1 1 | 0 1 0 1 | 1 | 1 | AC ← (AC) ∨ (M(DP)) | The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC. | ZF | | | | | | | | | | | | |
| | AND | And M to AC | 1 1 1 0 | 0 1 1 1 | 1 | 1 | AC ← (AC) ∧ (M(DP)) | The AC contents and the M(DP) contents are ANDed and the result is stored in the AC. | ZF | | | | | | | | | | | | |
| | OR | Or M to AC | 1 1 1 0 | 0 1 0 1 | 1 | 1 | AC ← (AC) ∨ (M(DP)) | The AC contents and the M(DP) contents are ORed and the result is stored in the AC. | ZF | | | | | | | | | | | | |
| | CM | Compare AC with M | 1 1 1 1 | 1 0 1 1 | 1 | 1 | (M(DP)) + (AC) + 1 | The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>Comparison result</td> <td>CF</td> <td>ZF</td> </tr> <tr> <td>(M(DP)) > (AC)</td> <td>0</td> <td>0</td> </tr> <tr> <td>(M(DP)) = (AC)</td> <td>1</td> <td>1</td> </tr> <tr> <td>(M(DP)) < (AC)</td> <td>1</td> <td>0</td> </tr> </table> | Comparison result | CF | ZF | (M(DP)) > (AC) | 0 | 0 | (M(DP)) = (AC) | 1 | 1 | (M(DP)) < (AC) | 1 | 0 | ZF CF |
| Comparison result | CF | ZF | | | | | | | | | | | | | | | | | | | |
| (M(DP)) > (AC) | 0 | 0 | | | | | | | | | | | | | | | | | | | |
| (M(DP)) = (AC) | 1 | 1 | | | | | | | | | | | | | | | | | | | |
| (M(DP)) < (AC) | 1 | 0 | | | | | | | | | | | | | | | | | | | |
| CI data | Compare AC with immediate data | 0 0 1 0 0 1 0 0 | 1 1 0 0 1 3 1 2 1 1 0 | 2 | 2 | ($1_3 1_2 1_1 1_0$) + (AC) + 1 | The AC contents and the immediate data $1_3 1_2 1_1 1_0$ are compared and the ZF and CF are set/reset. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>Comparison result</td> <td>CF</td> <td>ZF</td> </tr> <tr> <td>$1_3 1_2 1_1 1_0 > (AC)$</td> <td>0</td> <td>0</td> </tr> <tr> <td>$1_3 1_2 1_1 1_0 = (AC)$</td> <td>1</td> <td>1</td> </tr> <tr> <td>$1_3 1_2 1_1 1_0 < (AC)$</td> <td>1</td> <td>0</td> </tr> </table> | Comparison result | CF | ZF | $1_3 1_2 1_1 1_0 > (AC)$ | 0 | 0 | $1_3 1_2 1_1 1_0 = (AC)$ | 1 | 1 | $1_3 1_2 1_1 1_0 < (AC)$ | 1 | 0 | ZF CF | |
| Comparison result | CF | ZF | | | | | | | | | | | | | | | | | | | |
| $1_3 1_2 1_1 1_0 > (AC)$ | 0 | 0 | | | | | | | | | | | | | | | | | | | |
| $1_3 1_2 1_1 1_0 = (AC)$ | 1 | 1 | | | | | | | | | | | | | | | | | | | |
| $1_3 1_2 1_1 1_0 < (AC)$ | 1 | 0 | | | | | | | | | | | | | | | | | | | |
| CLI data | Compare DP _L with immediate data | 0 0 1 0 0 1 0 1 | 1 1 0 0 1 3 1 2 1 1 0 | 2 | 2 | (DP _L) ∨ ($1_3 1_2 1_1 1_0$) | The DP _L contents and the immediate data $1_3 1_2 1_1 1_0$ are compared. | ZF | | | | | | | | | | | | | |
| Load/store instructions | LI data | Load AC with immediate data | 1 1 0 0 | 1 3 1 2 1 1 0 | 1 | 1 | AC ← $1_3 1_2 1_1 1_0$ | The immediate data $1_3 1_2 1_1 1_0$ is loaded in the AC. | ZF | * 1 | | | | | | | | | | | |
| | S | Store AC to M | 0 0 0 0 | 0 0 1 0 | 1 | 1 | M(DP) ← (AC) | The AC contents are stored in the M(DP). | | | | | | | | | | | | | |
| | L | Load AC from M | 0 0 1 0 | 0 0 0 1 | 1 | 1 | AC ← (M(DP)) | The M(DP) contents are loaded in the AC. | ZF | | | | | | | | | | | | |
| | XM data | Exchange AC with M, then modify DP _H with immediate data | 1 0 1 0 | 0 M ₂ M ₁ M ₀ | 1 | 2 | (AC) ↔ (M(DP)) DP _H ← (DP _H) ∨ (M ₂ M ₁ M ₀) | The AC contents and the M(DP) contents are exchanged and then the DP _H contents are modified with the contents of (DP _H) ∨ (M ₂ M ₁ M ₀). | ZF | The ZF is set/reset according to the result of (DP _H) ∨ (M ₂ M ₁ M ₀). | | | | | | | | | | | |
| | X | Exchange AC with M | 1 0 1 0 | 0 0 0 0 | 1 | 2 | (AC) ↔ (M(DP)) | The AC contents and the M(DP) contents are exchanged. | ZF | The ZF is set/reset according to the DP _H contents at the time of instruction execution. | | | | | | | | | | | |
| | XI | Exchange AC with M, then increment DP _L | 1 1 1 1 | 1 1 1 0 | 1 | 2 | (AC) ↔ (M(DP)) DP _L ← (DP _L) + 1 | The AC contents and the M(DP) contents are exchanged and then the DP _L contents are incremented +1. | ZF | The ZF is set/reset according to the result of (DP _L) + 1. | | | | | | | | | | | |
| | XD | Exchange AC with M, then decrement DP _L | 1 1 1 1 | 1 1 1 1 | 1 | 2 | (AC) ↔ (M(DP)) DP _L ← (DP _L) - 1 | The AC contents and the M(DP) contents are exchanged and then the DP _L contents are decremented -1. | ZF | The ZF is set/reset according to the result of (DP _L) - 1. | | | | | | | | | | | |
| RTBL | Read table data from program ROM | 0 1 1 0 | 0 0 1 1 | 1 | 2 | AC, E ← ROM (PC, E, AC) | The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E. | | | | | | | | | | | | | | |

LC651104N/F/L, 651102N/F/L

| Instruction group | Mnemonic | Instruction code | | Bytes | Cycles | Function | Description | Status flag affected | Remarks | |
|--------------------------------------------|---------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|--------|----------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | | | | | | | |
| Data pointer manipulation instructions | LDZ data | Load DP _H with Zero and DP _L with immediate data respectively | 1 0 0 0 | 1 3 1 2 1 1 1 0 | 1 | 1 | DP _H ← 0 DP _L ← 1 3 1 2 1 1 1 0 | The DP _H and DP _L are loaded with 0 and the immediate data 1 3 1 2 1 1 1 0 respectively. | | |
| | LHI data | Load DP _H with immediate data | 0 1 0 0 | 1 3 1 2 1 1 1 0 | 1 | 1 | DP _H ← 1 3 1 2 1 1 1 0 | The DP _H is loaded with the immediate data 1 3 1 2 1 1 1 0. | | |
| | IND | Increment DP _L | 1 1 1 0 | 1 1 1 1 0 | 1 | 1 | DP _L ← (DP _L) + 1 | The DP _L contents are incremented +1. | ZF | |
| | DED | Decrement DP _L | 1 1 1 0 | 1 1 1 1 1 | 1 | 1 | DP _L ← (DP _L) - 1 | The DP _L contents are decremented -1. | ZF | |
| | TAL | Transfer AC to DP _L | 1 1 1 1 | 0 1 1 1 | 1 | 1 | DP _L ← (AC) | The AC contents are transferred to the DP _L | | |
| | TAL | Transfer DP _L to AC | 1 1 1 0 | 1 0 0 1 | 1 | 1 | AC ← (DP _L) | The DP _L contents are transferred to the AC | ZF | |
| | XAH | Exchange AC with DP _H | 0 0 1 0 | 0 0 1 1 | 1 | 1 | (AC) ↔ (DP _H) | The AC contents and the DP _H contents are exchanged. | | |
| Working register manipulation instructions | XA _i | Exchange AC with working register A _i | 1 1 1 0 | 0 0 0 0 | 1 | 1 | (AC) ↔ (A ₀) | The AC contents and the contents of working register A _i are exchanged. A _i is assigned one of A ₀ , A ₁ , A ₂ , A ₃ according to t ₁ ¹⁰ . | | |
| | XAO | | 1 1 1 0 | 0 0 1 0 | 1 | 1 | (AC) ↔ (A ₀) | | | |
| | XA1 | | 1 1 1 0 | 0 1 0 0 | 1 | 1 | (AC) ↔ (A ₁) | | | |
| | XA2 | | 1 1 1 0 | 1 0 0 0 | 1 | 1 | (AC) ↔ (A ₂) | | | |
| | XA3 | | 1 1 1 0 | 1 1 0 0 | 1 | 1 | (AC) ↔ (A ₃) | | | |
| | XHa | Exchange DP _H with working register Ha | 1 1 1 1 | 1 0 0 0 | 1 | 1 | (DP _H) ↔ (H ₀) | The DP _H contents and the contents of working register Ha are exchanged. Ha is assigned either of H ₀ or H ₁ according to a. | | |
| XHO | | 1 1 1 1 | 1 1 0 0 | 1 | 1 | (DP _H) ↔ (H ₁) | | | | |
| XL _a | Exchange DP _L with working register La | 1 1 1 1 | 0 0 0 0 | 1 | 1 | (DP _L) ↔ (L ₀) | The DP _L contents and the contents of working register La are exchanged. La is assigned either of L ₀ or L ₁ according to a. | | | |
| | XLO | | 1 1 1 1 | 0 1 0 0 | 1 | 1 | (DP _L) ↔ (L ₀) | | | |
| | XL1 | | 1 1 1 1 | 0 1 1 0 | 1 | 1 | (DP _L) ↔ (L ₁) | | | |
| Flag manipulation instructions | SFB flag | Set flag bit | 0 1 0 1 | B ₃ B ₂ B ₁ B ₀ | 1 | 1 | F _n ← 1 | The flag specified with B ₃ B ₂ B ₁ B ₀ is set. | | |
| | RFB flag | Reset flag bit | 0 0 0 1 | B ₃ B ₂ B ₁ B ₀ | 1 | 1 | F _n ← 0 | The flag specified with B ₃ B ₂ B ₁ B ₀ is reset. | ZF | The flags are divided into 4 groups of F ₀ to F ₃ , F ₄ to F ₇ , F ₈ to F ₁₁ , F ₁₂ to F ₁₅ . The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data B ₃ B ₂ B ₁ B ₀ . |
| Jump/subroutine instructions | JMP addr | Jump in the current bank | 0 1 1 0 | 1 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ | 2 | 2 | PC ← P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ | A jump to the address specified with immediate data P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ occurs. | | |
| | JPEA | Jump in the current page modified by E and AC | 1 1 1 1 | 1 0 1 0 | 1 | 1 | PC ₇₋₀ ← (E, AC) | A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs. | | |
| | CZP addr | Call subroutine in the zero page | 1 0 1 1 | P ₃ P ₂ P ₁ P ₀ | 1 | 1 | STACK ← (PC) + 1 PC ₁₀₋₆ , PC ₁₋₀ ← 0 PC ₅₋₂ ← P ₃ P ₂ P ₁ P ₀ | A subroutine in page 0 of bank 0 is called. | | |
| | CAL addr | Call subroutine in the zero bank | 1 0 1 0 | 1 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ | 2 | 2 | STACK ← (PC) + 2 PC ₁₀₋₀ ← 0 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ | A subroutine in bank 0 is called. | | |
| | RT | Return from subroutine | 0 1 1 0 | 0 0 1 0 | 1 | 1 | PC ← (STACK) | A return from a subroutine occurs. | | |
| | RTI | Return from interrupt routine | 0 0 1 0 | 0 0 1 0 | 1 | 1 | PC ← (STACK) CF ZF ← CSF, ZSF | A return from an interrupt service routine occurs. | ZF CF | |
| | BANK | Change bank | 1 1 1 1 | 1 1 0 1 | 1 | 1 | | The bank is changed. A pseudo I/O port is specified. | | Effective only when used immediately before an I/O instruction or branch instruction. |
| Branch instructions | BA _t addr | Branch on AC bit | 0 1 1 1 | 0 0 1 1 1 0 P ₇ P ₆ P ₅ P ₄ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC _t = 1 | If a single bit of the AC specified with the immediate data t ₁ t ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | Mnemonic is BA0 to BA3 according to the value of t. |
| | BNA _t addr | Branch on no AC bit | 0 0 1 1 | 0 0 1 1 1 0 P ₇ P ₆ P ₅ P ₄ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC _t = 0 | If a single bit of the AC specified with the immediate data t ₁ t ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | Mnemonic is BNA0 to BNA3 according to the value of t. |
| | BM _t addr | Branch on M bit | 0 1 1 1 | 0 1 1 1 1 0 P ₇ P ₆ P ₅ P ₄ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (M(DP _L t ₁ t ₀)) = 1 | If a single bit of the M(DP _L) specified with the immediate data t ₁ t ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | Mnemonic is BM0 to BM3 according to the value of t. |
| | BNM _t addr | Branch on no M bit | 0 0 1 1 | 0 1 1 1 1 0 P ₇ P ₆ P ₅ P ₄ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (M(DP _L t ₁ t ₀)) = 0 | If a single bit of the M(DP _L) specified with the immediate data t ₁ t ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | Mnemonic is BNM0 to BNM3 according to the value of t. |
| | BP _t addr | Branch on Port bit | 0 1 1 1 | 1 0 1 1 1 0 P ₇ P ₆ P ₅ P ₄ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DP _L t ₁ t ₀)) = 1 | If a single bit of port P(DP _L) specified with the immediate data t ₁ t ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | Mnemonic is BP0 to BP3 according to the value of t. |
| | BNP _t addr | Branch on no Port bit | 0 0 1 1 | 1 0 1 1 1 0 P ₇ P ₆ P ₅ P ₄ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DP _L t ₁ t ₀)) = 0 | If a single bit of port P(DP _L) specified with the immediate data t ₁ t ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | Mnemonic is BNP0 to BNP3 according to the value of t. |
| | BTM addr | Branch on timer | 0 1 1 1 | 1 1 0 0 | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if TMF = 1 then TMF ← 0 | If the TMF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The TMF is reset. | TMF | |

| Instruction group | Mnemonic | Instruction code | | Bytes | Cycles | Function | Description | Status flag affected | Remarks | |
|---------------------------|-----------|-------------------------------------------------------------|------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------------------------------------------------------------------|
| | | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | | | | | | | |
| Branch instructions | BNTM addr | Branch on no timer | 0 0 1 1 P ₇ P ₆ P ₅ P ₄ | 1 1 0 0 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if TMF = 0 then TMF ← 0 | If the TMF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The TMF is reset. | TMF | |
| | BI addr | Branch on interrupt | 0 1 1 1 P ₇ P ₆ P ₅ P ₄ | 1 1 0 1 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if EXTF = 1 then EXTF ← 0 | If the EXTF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The EXTF is reset. | EXTF | |
| | BNI addr | Branch on no interrupt | 0 0 1 1 P ₇ P ₆ P ₅ P ₄ | 1 1 0 1 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if EXTF = 0 then EXTF ← 0 | If the EXTF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The EXTF is reset. | EXTF | |
| | BC addr | Branch on CF | 0 1 1 1 P ₇ P ₆ P ₅ P ₄ | 1 1 1 1 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 1 | If the CF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | |
| | BNC addr | Branch on no CF | 0 0 1 1 P ₇ P ₆ P ₅ P ₄ | 1 1 1 1 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 0 | If the CF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | |
| | BZ addr | Branch on ZF | 0 1 1 1 P ₇ P ₆ P ₅ P ₄ | 1 1 1 0 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 1 | If the ZF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | |
| | BNZ addr | Branch on no ZF | 0 0 1 1 P ₇ P ₆ P ₅ P ₄ | 1 1 1 0 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 0 | If the ZF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | |
| | BFn addr | Branch on flag bit | 1 1 0 1 P ₇ P ₆ P ₅ P ₄ | n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if Fn = 1 | If the flag bit of the 16 flags specified with the immediate data n ₃ n ₂ n ₁ n ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | Mnemonic is BFO to #P 16 according to the value of n. |
| | BNFn addr | Branch on no flag bit | 1 0 0 1 P ₇ P ₆ P ₅ P ₄ | n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if Fn = 0 | If the flag bit of the 16 flags specified with the immediate data n ₃ n ₂ n ₁ n ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. | | Mnemonic is BNFO to #P 16 according to the value of n. |
| Input/Output instructions | IP | Input port to AC | 0 0 0 0 | 1 1 0 0 | 1 | 1 | AC ← (P(DP _L)) | Port P(DP _L) contents are loaded in the AC. | ZF | |
| | OP | Output AC to port | 0 1 1 0 | 0 0 0 1 | 1 | 1 | P(DP _L) ← (AC) | The AC contents are outputted to port P(DP _L). | | |
| | SPB bit | Set port bit | 0 0 0 0 | 0 1 B ₁ B ₀ | 1 | 2 | P(DP _L , B ₁ B ₀) ← 1 | A single bit in port P(DP _L) specified with the immediate data B ₁ B ₀ is set. | | When this instruction is executed, the E contents are destroyed. |
| | RPB bit | Reset port bit | 0 0 1 0 | 0 1 B ₁ B ₀ | 1 | 2 | P(DP _L , B ₁ B ₀) ← 0 | A single bit in port P(DP _L) specified with the immediate data B ₁ B ₀ is reset. | ZF | When this instruction is executed, the E contents are destroyed. |
| Other instructions | SCTL bit | Set control register bit(S) | 0 0 1 0 1 0 0 0 | 1 1 0 0 B ₃ B ₂ B ₁ B ₀ | 2 | 2 | CTL ← (CTL) V B ₃ B ₂ B ₁ B ₀ | The bits of the control register specified with the immediate data B ₃ B ₂ B ₁ B ₀ are set. | | |
| | RCTL bit | Reset control register bit(S) | 0 0 1 0 1 0 0 1 | 1 1 0 0 B ₃ B ₂ B ₁ B ₀ | 2 | 2 | CTL ← (CTL) A B ₃ B ₂ B ₁ B ₀ | The bits of the control register specified with the immediate data B ₃ B ₂ B ₁ B ₀ are reset. | ZF | |
| | WTTM | Write timer | 1 1 1 1 | 1 0 0 1 | 1 | 1 | TM ← (E), (AC) TMF ← 0 | The E and AC contents are loaded in the timer. The TMF is reset. | TMF | |
| | HALT | Halt | 1 1 1 1 | 0 1 1 0 | 1 | 1 | Halt | All operations stop. | | Only when all pins of port PA are set at L, stop |
| | NOP | No operation | 0 0 0 0 | 0 0 0 0 | 1 | 1 | No operation | No operation is performed, but 1 machine cycle is consumed. | | |

*1 If the CLA instruction is used continuously in such a manner as CLA, CLA, -----, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.

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