Ordering number : EN*5190

CMOS LSI

LC651204N/F/L, LC651202N/F/L

4-Bit Single-Chip Microcontrollers for Small-Scale Control Applications

Preliminary

Overview

The LC651204N/F/L and LC651202N/F/L are small-scale application microcontroller products in Sanyo's LC6500 series of 4-bit single-chip CMOS microcontrollers, and as such they fully support the basic architecture and instruction set of that series. These microcontrollers are provided in a 30-pin package and include 2 kilobytes (KB) and 4 KB of on-chip ROM. These products are appropriate for use in a wide range of applications, from applications that use a small number of controls and circuits that were previously implemented in standard logic to larger scale applications including audio equipment such as decks and players, office equipment, communications equipment, automotive equipment, and home appliances. Except for the lack of an A/D converter, these microcontrollers provide the same functionality as the LC651104, 02N/F/L.

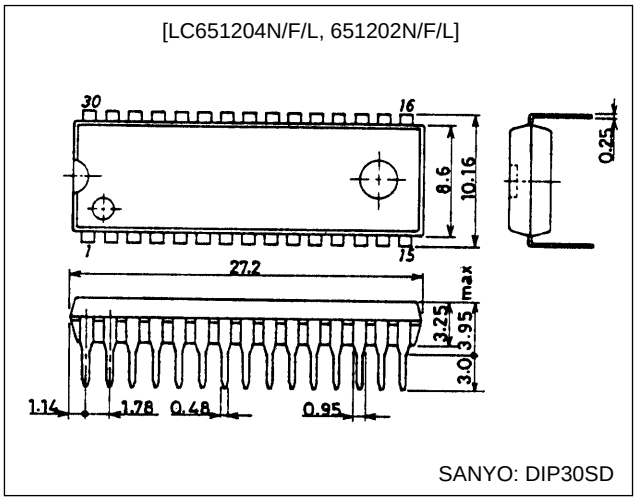
Features

- Fabricated in a CMOS process for low power (An instruction-controlled standby function is provided.)
- ROM/RAM
  LC651204N/F/L - ROM: 4K × 8 bits, RAM: 256 × 4 bits
  LC651202N/F/L - ROM: 2K × 8 bits, RAM: 256 × 4 bits
- Instruction set: The 80-instruction set provided by all members of the LC6500 series.
- Wide operating power-supply voltage range of 2.5 to 5.5 volts (L version)
- Instruction cycle time: 0.92 µs (F version)
- On-chip serial I/O circuit
- Highly flexible I/O ports
  — Number of ports: 6 ports with a total of 22 pins
  — All ports: Can be used for both input and output
    I/O voltage: 15 V maximum (Only for C, D, E, and F ports with open-drain output specifications)
    Output current: 20 mA maximum sink current (Capable of directly driving LEDs.)
  — Options that allow specifications to be customized to match those of the application system.
    Specification of open-drain output or built-in pull-up resistor: can be specified for all ports in bit units.
    Specification of the output level at reset: Can be specified to be high or low for ports C and D in port units.
- Interrupt functions
  — Timer overflow vector interrupt (The interrupt state can be tested by the CPU.)
  — Vector interrupts initiated by the $\overline{\text{INT}}$ pin or full/empty states of the serial I/O circuit. (The interrupt state can be tested by the CPU.)
- Stack levels: 8 levels (shared with interrupts)
- Timers: 4-bit prescaler plus 8-bit programmable timers
- Clock oscillator options to match application system specifications.
  — Oscillator circuit options: 2-pin ceramic oscillator (N, F, and L versions)
  — Divider circuit option: No divider, built-in divide-by-three circuit, built-in divide-by-four circuit (N and L versions)
- Supports continuous output of a square wave signal (with a period 64 times the cycle time)
- Watchdog timer
  — RC time constant scheme
  — A watchdog timer function can be allocated to one of the external pins as an option.
- EP version: LC65E1104, OTP version: LC65P1104

Package Dimensions

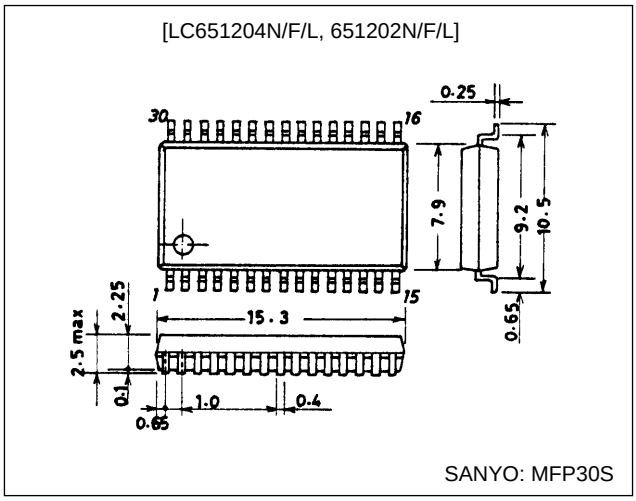
unit : mm

3196-DIP30SD



unit : mm

3073A-MFP30S



Note: The package drawings shown above are provided without error tolerances and are for reference purposes only. Contact Sanyo for official package drawings.

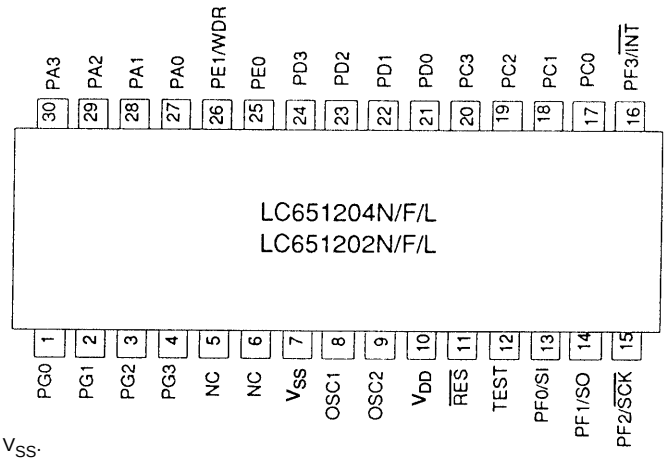
Function Overview

Item		LC651204N/1202N	LC651204F/1202F	LC651204L/1202L
Memory	ROM	4096 × 8 bits (1204N)	4096 × 8 bits (1204F)	4096 × 8 bits (1204L)
		2048 × 8 bits (1202N)	2048 × 8 bits (1202F)	2048 × 8 bits (1202L)
	RAM	256 × 4 bits (1204/1202N)	256 × 4 bits (1204/1202F)	256 × 4 bits (1204/1202L)
Instruction	Instruction set	80	80	80
	Table reference	Supported	Supported	Supported
Built-in functions	Interrupts	1 external, 1 internal	1 external, 1 internal	1 external, 1 internal
	Timers	4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer
	Stack levels	8	8	8
	Standby function	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction
I/O ports	Number of ports	22 I/O pins	22 I/O pins	22 I/O pins
	Serial ports	4-bit or 8-bit I/O	4-bit or 8-bit I/O	4-bit or 8-bit I/O
	I/O voltage	15 V max.	15 V max.	15 V max.
	Output current	10 mA typ. 20 mA max.	10 mA typ. 20 mA max.	10 mA typ. 20 mA max.
	I/O circuit types	Open drain (n-channel) or built-in pull-up resistor output selectable on a per-bit basis.		
	Output levels at reset	High or low can be selected in port units. (ports C and D only)		
	Square wave output	Supported	Supported	Supported
Characteristics	Minimum cycle time	2.77 µs (V_{DD} ≥ 3 V)	0.92 µs (V_{DD} ≥ 3 V)	3.84 µs (V_{DD} ≥ 2.5 V)
	Power-supply voltage	3 to 5.5 V	3 to 5.5 V	2.5 to 5.5 V
	Power-supply current	1.5 mA typ.	2 mA typ.	1.5 mA typ.
Oscillator	Oscillator	Ceramic (800 kHz, 1 MHz, 4 MHz)	Ceramic (4 MHz)	Ceramic (800 kHz, 1 MHz, 4 MHz)
	Divider circuit option	1/1, 1/3, 1/4	1/1	1/1, 1/3, 1/4
Other functions	Package	DIP30S-D MFP30S	DIP30S-D MFP30S	DIP30S-D MFP30S

Note: Sanyo will announce details on oscillator elements and oscillator circuit constants as recommended application circuits are developed. Customers should check with Sanyo for the latest information as the development process progresses.

Pin Assignment

Common assignments for the DIP and MFP packages



Note: NC pins must be connected to V_{SS}.

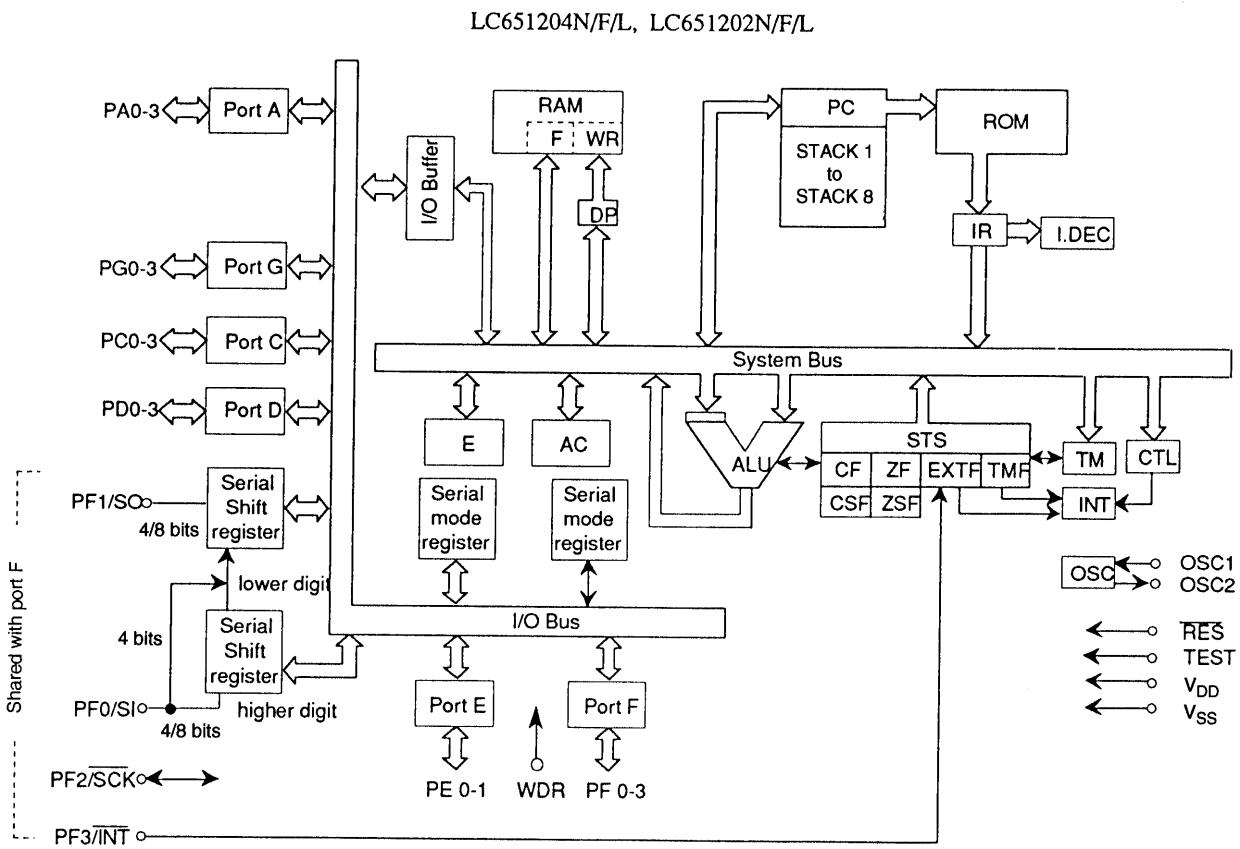
Top view

Pin Functions

Pin	Function
OSC1, OSC2	Connections for a ceramic oscillator element
$\overline{\text{RES}}$	Reset
PA0 to 3	I/O dual-function port A0 to A3
PC0 to 3	I/O dual-function port C0 to C3
PD0 to 3	I/O dual-function port D0 to D3
PE0 to 1	I/O dual-function port E0 to E1
PF0 to 3	I/O dual-function port F0 to F3
PG0 to 3	I/O dual-function port G0 to G3
TEST	Test
$\overline{\text{INT}}$	Interrupt request
SI	Serial input
SO	Serial output
$\overline{\text{SCK}}$	Serial clock input and output
NC	No connection
WDR	Watchdog reset

Note: The SI, SO, $\overline{\text{SCK}}$, and $\overline{\text{INT}}$ pins are shared function pins that are also used as PF0 to PF3.

System Block Diagram



RAM:	Data memory	ROM:	Program memory
F:	Flag	PC:	Program counter
WR:	Working register	INT:	Interrupt control
AC:	Accumulator	IR:	Instruction register
ALU:	Arithmetic and logic unit	I.DEC:	Instruction decoder
DP:	Data pointer	CF, CSF:	Carry flag, carry save flag
E:	E register	ZF, ZSF:	Zero flag, zero save flag
CTL:	Control register	EXTF:	External interrupt request flag
OSC:	Oscillator circuit	TMF:	Internal interrupt request flag
TM:	Timer		
STS:	Status register		

Development Support

Sanyo provides the following items to support application development using the LC651204 and LC651202.

1. User's manual

   The "LC651104/1102 User's Manual" is used with these microcontrollers.

2. Development tool manual

   See the "EVA800 - LC651104/1102 Development Tool Manual" for details on use of the EVA-800 system.

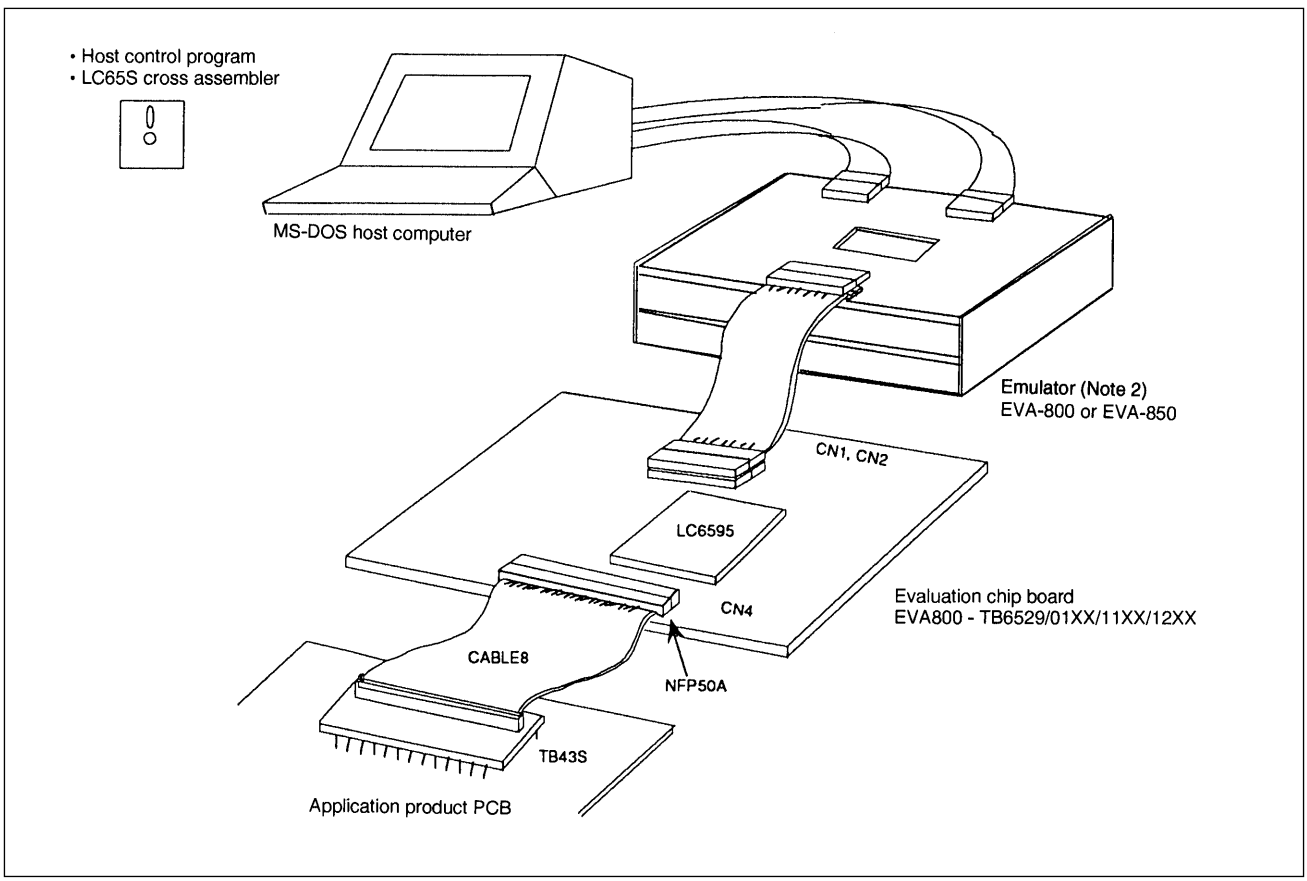
3. Development tool

- Program development (using the EVA-800 system)
  - — MS-DOS host computer system *1
  - — Cross assembler ... MS-DOS-based cross assembler: LC65S.EXE
  - — Evaluation chip: LC6595
  - — Emulator: The EVA-800 main unit plus the evaluation chip
- Program development (using the EVA-86000 system): Use the EVA86K-ECB651100.
- Program evaluation

  The <LC65E1104> on-chip EPROM microcontroller

Development Support System

EVA-800 System



Note: 1. MS-DOS is a registered trademark of Microsoft Corporation

2. Here, "EVA-800" is a generic term for several emulators. Suffixes (A, B, etc.) will be attached to the name as new versions are developed. Note that the EVA-800 emulator (i.e., the model with no suffix) is an old version and cannot be used.

Pin Functions

Pin	Pin no.	I/O	Function	Options	State at reset	Handling when unused
V_{DD} V_{SS}	1 1	— —	Power supply	—	—	—
OSC1 OSC2	1 1	Input Output	• System clock oscillator Connect an external ceramic oscillator element to these pins • Leave OSC2 open if an external clock is supplied.	(1) External clock (2) Two-pin ceramic oscillator (3) Divider circuit option 1. No divider circuit 2. Divide-by-three circuit 3. Divide-by-four circuit	—	—
PA0 to PA3	4	I/O	• I/O port A0 to A3 Input in 4-bit units using the IP instruction Output in 4-bit units using the OP instruction Port bits can be tested in bit units using the BP and BNP instructions. Port bits can be set or cleared in bit units using the SPB and RPB instructions. • PA3 is used for standby control. • Applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.	(1) Output open drain (2) Built-in pull-up resistor • Options (1) and (2) can be specified in bit units.	High-level output (i.e., the output n-channel transistor will be off.)	Open drain output select the options, connect to V_{SS}.
PC0 to PC3	4	I/O	• I/O port C0 to C3 The PC0 to PC3 pin functions are identical to those of the PA0 to 3 pins.* • High or low can be specified as the output at reset as an option. Note: These pins do not have a standby control function.	(1) Output open drain (2) Built-in pull-up resistor (3) High-level output at reset (4) Low-level output at reset • Options (1) and (2) can be specified in bit units. • Option (3) and (4) are specified in 4-bit units.	• High-level output • Low-level output (Depending on the option specified.)	The same as PA0 to PA3.
PD0 to PD3	4	I/O	• I/O port D0 to D3 The PD0 to PD3 pin functions and options are identical to those of the PC0 to PC3 pins.	The same as PC0 to PC3.	The same as PC0 to PC3.	The same as PA0 to PA3.

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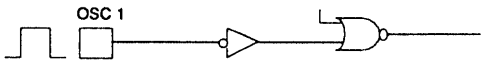
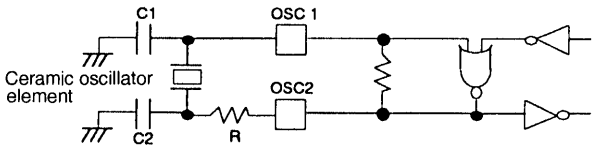
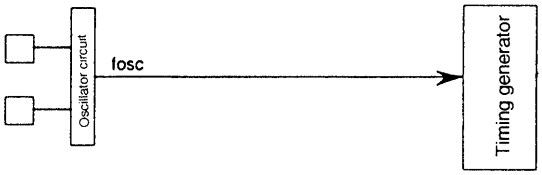
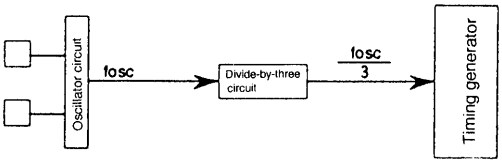
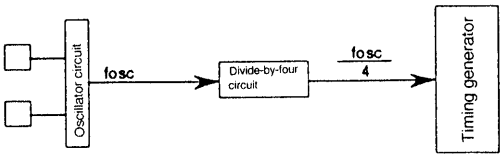
Pin	Pin no.	I/O	Function	Options	State at reset	Handling when unused
PE0 to PE1 /WDR	2	I/O	• I/O port E0 to E1 Input in 4-bit units using the IP instruction Output in 4-bit units using the OP instruction Port bits can be set or cleared in bit units using the SPB and RPB instructions. Port bits can be tested in bit units using the BP and BNP instructions. • The PE0 pin also has a continuous pulse (64·Tcyc) output function. • The PE1 pin can be set to function as the WDR watchdog timer reset pin as an option.	(1) Output open drain (2) Built-in pull-up resistor • Options (1) and (2) can be specified in bit units. (3) Normal port PE1 (4) Watchdog timer reset WDR (5) (3) or (4) can be specified.	High-level output (i.e., the output n-channel transistor will be off.)	The same as PA0 to PA3.
PF0/SI PF1/SO PF2/$\overline{\text{SCK}}$ PF3/$\overline{\text{INT}}$	4	I/O	• I/O port F0 to F3 This port has the same functions and options as PE0 to PE1. * • The pins PF0 to PF3 are also used as the serial interface and the $\overline{\text{INT}}$ pin. The function used can be selected under program control. SI ·····Serial input port SO····Serial output port $\overline{\text{SCK}}$ ··Serial clock input or output $\overline{\text{INT}}$ ···Interrupt request input Serial I/O can be switched between 4-bit and 8-bit operation under program control. Note: This port does not provide a continuous pulse output function.	The same as PA0 to PA3.	The same as PA0 to PA3. The serial port function is disabled. The interrupt source is $\overline{\text{INT}}$.	The same as PA0 to PA3.
PG0 to PG3	4	I/O	• I/O port G0 to G3 This port has the same functions and options as PE0 to PE1. * Note: This port does not provide a continuous pulse output function.	The same as PA0 to PA3.	The same as PA0 to PA3.	The same as PA0 to PA3.
NC	2		• NC pin. This pin must be connected to V_{SS} in the EP and OTP versions.	—	—	Connect to V_{SS}.
$\overline{\text{RES}}$	1	Input	• System reset input • Connect an external capacitor for the power up reset. • A low level must be applied for at least four clock cycles for the reset startup sequence to operate correctly.	—	—	—
TEST	1	Input	• LSI test pin Must be connected to V_{SS}.	—	—	Must be connected to V_{SS}.

Oscillator Circuit Options

Option	Circuit	Conditions and notes
External clock		The OSC2 pin must be left open.
Ceramic oscillator		

Divider Options

Option	Circuit	Conditions and notes
No divider (1/1)		• Supports both oscillator options. • The oscillator frequency or the external clock frequency must not exceed 1444 kHz (LC651204N and LC651202N) • The oscillator frequency or the external clock frequency must not exceed 4330 kHz (LC651204F and LC651202F) • The oscillator frequency or the external clock frequency must not exceed 1040 kHz (LC651204L and LC651202L)
Built-in divide-by-three circuit		• Supports both oscillator options. • The oscillator frequency or the external clock frequency must not exceed 4330 kHz
Built-in divide-by-four circuit		• Supports both oscillator options. • The oscillator frequency or the external clock frequency must not exceed 4330 kHz

Caution: The oscillator and divider options are summarized in the following tables. The information presented in those tables is crucial when using these products.

Divider Options for the LC651204N/1202N, LC651204F/1202F, and LC651204L/1202L

LC651204N, LC651202N

Circuit type	Frequency	Divider option (cycle time)	V_{DD} range	Notes
Ceramic oscillator	800 kHz	1/1 (5 µs)	3 to 5.5 V	
	1 MHz	1/1 (4µs)	3 to 5.5 V	
	4 MHz	1/3 (3µs) 1/4 (4µs)	3 to 5.5 V 3 to 5.5 V	This frequency cannot be used with the 1/1 divider (i.e., no divider circuit) option.
External clock generated by a two-terminal RC oscillator circuit	670 k to 1444 kHz 2000 k to 4330 kHz 2600 k to 4330 kHz	1/1 (6 to 2.77 µs) 1/3 (6 to 2.77 µs) 1/4 (6 to 3.70 µs)	3 to 5.5 V 3 to 5.5 V 3 to 5.5 V	
Use of an external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

LC651204F, LC651202F

Circuit type	Frequency	Divider option (cycle time)	V_{DD} range	Notes
Ceramic oscillator	4 MHz	1/1 (1 µs)	3 to 5.5 V	
External clock generated by a two-terminal RC oscillator circuit	670 k to 4330 kHz	1/1 (6 to 0.92 µs)	3 to 5.5 V	
Use of an external clock with the ceramic oscillator circuit	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

LC651204L LC651202L

Circuit type	Frequency	Divider option (cycle time)	V_{DD} range	Notes
Ceramic oscillator	800 kHz	1/1 (5 µs)	2.5 to 5.5 V	
	1 MHz	1/1 (4µs)	2.5 to 5.5 V	
	4 MHz	1/4 (4µs)	2.5 to 5.5 V	This frequency cannot be used with the 1/1, 1/3 divider (i.e., no divider circuit) option.
External clock generated by a two-terminal RC oscillator circuit	670 k to 1040 kHz 2000 k to 3120 kHz 2600 k to 4160 kHz	1/1 (6 to 3.84 µs) 1/3 (6 to 3.84 µs) 1/4 (6 to 3.84 µs)	2.5 to 5.5 V 2.5 to 5.5 V 2.5 to 5.5 V	
Use of an external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

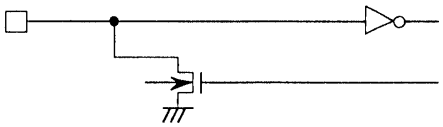
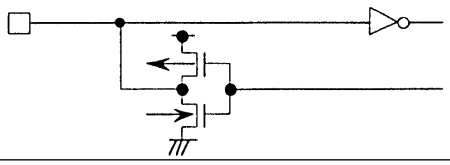
Port C and D Output State at Reset Options

The output levels at reset of the I/O ports C and D can be selected from the following two options, which are specified in 4-bit units.

Option	Conditions and notes
High-level output at reset	Ports C and D in 4-bit units
Low-level output at reset	Ports C and D in 4-bit units

Port Output Circuit Type Option

The output circuit types of the I/O ports can be selected from the following two options in bit units.

Option	Circuit	Conditions and notes
Open drain output		Ports A, C, D, E, F, and G
Pull-up resistor output		

Watchdog Timer Reset Option

Whether the PE1/WDR pin functions as the normal port PE1 or as the WDR watchdog timer reset pin can be selected as an option.

LC651204N, 651202N

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Voltages up to any generated voltage are allowed.	V
Input voltage	V_I (1)		OSC1 *1	–0.3 to V_{DD} +0.3	V
	V_I (2)		TEST, $\overline{RES}$	–0.3 to V_{DD} +0.3	V
I/O voltage	V_{IO} (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	–0.3 to + 15	V
	V_{IO} (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	–0.3 to V_{DD} +0.3	V
	V_{IO} (3)	PA0 to 3, PG0 to 3		–0.3 to V_{DD} +0.3	V
Peak output current	I_{OP}		I/O ports	–2 to +20	mA
Average output current	I_{OA}	Average value per pin over a 100-ms period	I/O ports	–2 to +20	mA
	ΣI_{OA} (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1*2	PC0 to PC3 PD0 to PD3 PE0 to PE1	–15 to +100	mA
	ΣI_{OA} (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to PF3 PG0 to PG3 PA0 to PA3	–15 to +100	mA
Allowable power dissipation	Pd max (1)	Ta = –40 to +85°C (DIP package)		250	mW
	Pd max (2)	Ta = –40 to +85°C (MFP package)		150	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to 85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Operating power-supply voltage	V_{DD}		V_{DD}	3.0		5.5	V
Standby power-supply voltage	V_{ST}	RAM and register values retained *3	V_{DD}	1.8		5.5	V
Input high-level voltage	V_{IH} (1)	Output n-channel transistors off	OD specification ports C, D, E, and F	0.7 V_{DD}		13.5	V
	V_{IH} (2)	Output n-channel transistors off	PU specification ports C, D, E, and F	0.7 V_{DD}		V_{DD}	V
	V_{IH} (3)	Output n-channel transistors off	Port A, G	0.7 V_{DD}		V_{DD}	V
	V_{IH} (4)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with OD specifications	0.8 V_{DD}		13.5	V
	V_{IH} (5)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with PU specifications	0.8 V_{DD}		V_{DD}	V
	V_{IH} (6)	V_{DD} = 1.8 to 5.5 V	$\overline{RES}$	0.8 V_{DD}		V_{DD}	V
	V_{IH} (7)	External clock specifications	OSC1	0.8 V_{DD}		V_{DD}	V

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Parameter	Symbol	Conditions		Applicable pins/notes	Ratings			
					min	typ	max	Unit
Input low-level voltage	V_{IL} (1)	Output n-channel transistor off	V_{DD} = 4 to 5.5 V	Port	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (2)	Output n-channel transistor off	V_{DD} = 3 to 5.5 V	Port	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (3)	Output n-channel transistor off	V_{DD} = 4 to 5.5 V	$\overline{INT}$, $\overline{SCk}$, SI	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (4)	Output n-channel transistor off	V_{DD} = 3 to 5.5 V	$\overline{INT}$, $\overline{SCk}$, SI	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (5)	External clock specifications	V_{DD} = 4 to 5.5 V	OSC1	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (6)	External clock specifications	V_{DD} = 3 to 5.5 V	OSC1	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (7)		V_{DD} = 4 to 5.5 V	TEST	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (8)		V_{DD} = 3 to 5.5 V	TEST	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (9)		V_{DD} = 4 to 5.5 V	$\overline{RES}$	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (10)		V_{DD} = 3 to 5.5 V	$\overline{RES}$	V_{SS}		$0.2V_{DD}$	V
Operating frequency (cycle time)	fop (Tcyc)	Frequencies up to 4.33 MHz are supported if the divide-by-three or divide-by-four divider circuit option is used.	V_{DD} = 3 to 5.5 V		670 (6)		1444 (2.77)	kHz (µs)
External clock conditions Frequency	text	Figure 1. The divide-by-three or divide-by-four divider circuit option must be used if the clock frequency exceeds 1.444 MHz.	V_{DD} = 3 to 5.5 V	OSC1	670		4330	kHz
Pulse width	textH, textL		V_{DD} = 3 to 5.5 V	OSC1	69			ns
Rise and fall times	textR, textF		V_{DD} = 3 to 5.5 V	OSC1			50	ns
Guaranteed oscillator constants Ceramic oscillator		Figure 2				See Table 1.		

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V (unless otherwise specified)

Parameter		Symbol	Conditions	Applicable pins/notes	Ratings			
					min	typ	max	Unit
Input high-level current		I_{IH} (1)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V_{IN} = 13.5 V	Ports C, D, E, and F with open-drain specifications			5.0	µA
		I_{IH} (2)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V_{IN} = V_{DD}	Ports A and G with open-drain specifications			1.0	µA
		I_{IH} (3)	External clock mode, V_{IN} = V_{DD}	OSC1			1.0	µA
Input low-level current		I_{IL} (1)	Output n-channel transistor off V_{IN} = V_{SS}	Ports with open-drain specifications	–1.0			µA
		I_{IL} (2)	Output n-channel transistor off V_{IN} = V_{SS}	Ports with pull-up resistor specifications	–1.3	–0.35		mA
		I_{IL} (3)	V_{IN} = V_{SS}	$\overline{RES}$	–45	–10		µA
		I_{IL} (4)	External clock mode, V_{IN} = V_{SS}	OSC1	–1.0			µA
Output high-level voltage		V_{OH} (1)	I_{OH} = –50 µA V_{DD} = 4.0 to 5.5 V	Ports with pull-up resistor specifications	V_{DD} –1.2			V
		V_{OH} (2)	I_{OH} = –10 µA V_{DD} = 3.0 to 5.5 V	Ports with pull-up resistor specifications	V_{DD} –0.5			V
Output low-level voltage		V_{OL} (1)	I_{OL} = 10 mA, V_{DD} = 4.0 to 5.5 V	Port			1.5	V
		V_{OL} (2)	I_{OL} = 1 mA, with the I_{OL} for all ports no more than 1 mA. V_{DD} = 3.0 to 5.5 V	Port			0.5	V
Schmitt characteristics	Hysteresis voltage	V_{HIS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, and SI OSC1 with Schmitt specifications *4		0.1 V_{DD}		V
	High-level threshold voltage	V_{tH}			0.4 V_{DD}		0.8 V_{DD}	V
	Low-level threshold voltage	V_{tL}			0.2 V_{DD}		0.6 V_{DD}	V
Current drain Ceramic oscillator		I_{DDOP} (1)	Operating, output n-channel transistors off, Ports = V_{DD} Figure 2, 4 MHz, divide-by-three circuit	V_{DD}		1.5	5	mA
		I_{DDOP} (2)	Figure 2, 4 MHz, divide-by-four circuit	V_{DD}		1.5	4	mA
		I_{DDOP} (3)	Figure 2, 800 kHz	V_{DD}		1.5	4	mA
External clock		I_{DDOP} (4)	670 to 1444 kHz, no divider circuit 2000 to 4330 kHz, divide-by-three circuit 2600 to 4330 kHz, divide-by-four circuit	V_{DD}		1.5	5	mA
Standby mode		I_{DDst}	Output n-channel transistor off, V_{DD} = 5.5 V Ports = V_{DD}, V_{DD} = 3 V	V_{DD} V_{DD}		0.05 0.025	10 5	µA µA

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC} *5	Figure 2, fo = 800 kHz Figure 2, fo = 1 MHz Figure 2, fo = 4 MHz, divide-by-three or divide-by-four circuit	OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	768 960 3840	800 1000 4000	832 1040 4160	kHz kHz kHz
Oscillator stabilization time	t_{CFS}	Figure 3, fo = 800 kHz, 1 MHz, 4 MHz Divide-by-three or divide-by-four circuit				5	ms
Pull-up resistors I/O ports	R_{PP}	Output n-channel transistor off $V_{in} = V_{SS}$, V_{DD} = 5 V	Ports with pull-up resistor specifications	8	14	30	kΩ
$\overline{RES}$	Ru	$V_{in} = V_{SS}$, V_{DD} = 5 V	$\overline{RES}$	100	250	400	kΩ
External reset characteristics Reset time	t_{RST}				See Figure 4.		
Pin capacitance	Cp	f = 1 MHz With all pins other than the pin being measured at $V_{IN} = V_{SS}$			10		pF
Serial clock Input clock cycle time	t_{CKCY} (1)	Figure 5	$\overline{SCK}$	3.0			µs
Output clock cycle time	t_{CKCY} (2)	Figure 5	$\overline{SCK}$		$64 \times T_{CYC}$ *6		µs
Input clock low-level pulse width	t_{CKL} (1)	Figure 5	$\overline{SCK}$	1.0			µs
Output clock low-level pulse width	t_{CKL} (2)	Figure 5	$\overline{SCK}$		$32 \times T_{CYC}$		µs
Input clock high-level pulse width	t_{CKH} (1)	Figure 5	$\overline{SCK}$	1.0			µs
Output clock high-level pulse width	t_{CKH} (2)	Figure 5	$\overline{SCK}$		$32 \times T_{CYC}$		µs

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Parameter		Symbol	Conditions	V_{DD} (v)	Applicable pins/notes	Ratings			
						min	typ	max	Unit
Serial input Data setup time		t_{ICK}	Stipulated with respect to the rising edge of $\overline{SCK}$.		SI	0.4			µs
Data hold time		t_{CKI}	Figure 5		SI	0.4			µs
Serial output Output delay time		t_{CKO}	Stipulated with respect to the falling edge of $\overline{SCK}$. For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF Figure 5	SO				0.6	µs
Pulse output Period		t_{PCY}	Figure 6 Tcyc = 4 x the system clock period For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF		PE0		$64 \times T_{CYC}$		µs
High-level pulse width		t_{PH}			PE0		$32 \times T_{CYC}$ ±10%		µs
Low-level pulse width		t_{PL}			PE0		$32 \times T_{CYC}$ ±10%		µs
Watchdog timer	Guaranteed constants *7	C_W	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.1±5%		µF
		R_W	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		R_I	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t_{WCT}	See Figure 7.		WDR	100			µs
	Clear period (charge)	t_{WCCY}	See Figure 7.		WDR	29			ms
	Guaranteed constants *7	C_W	When PE1 has open-drain output specifications	4 to 5.5	WDR		0.047±5%		µF
		R_W	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		R_I	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t_{WCT}	See Figure 7.		WDR	40			µs
	Clear period (charge)	t_{WCCY}	See Figure 7.		WDR	15			ms

Note: 1. When driven internally using the oscillator circuit shown in Figure 3 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.

2. The average over a 100-ms period

3. The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.

4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.

5. The values shown for fCFOSC are the frequencies for which oscillation is possible. The center frequency when a ceramic oscillator is used may differ by about 1% from the nominal value listed by the manufacturer of the ceramic oscillator element. See the specifications of the ceramic oscillator element for details.

6. Tcyc = 4 × the system clock period

7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

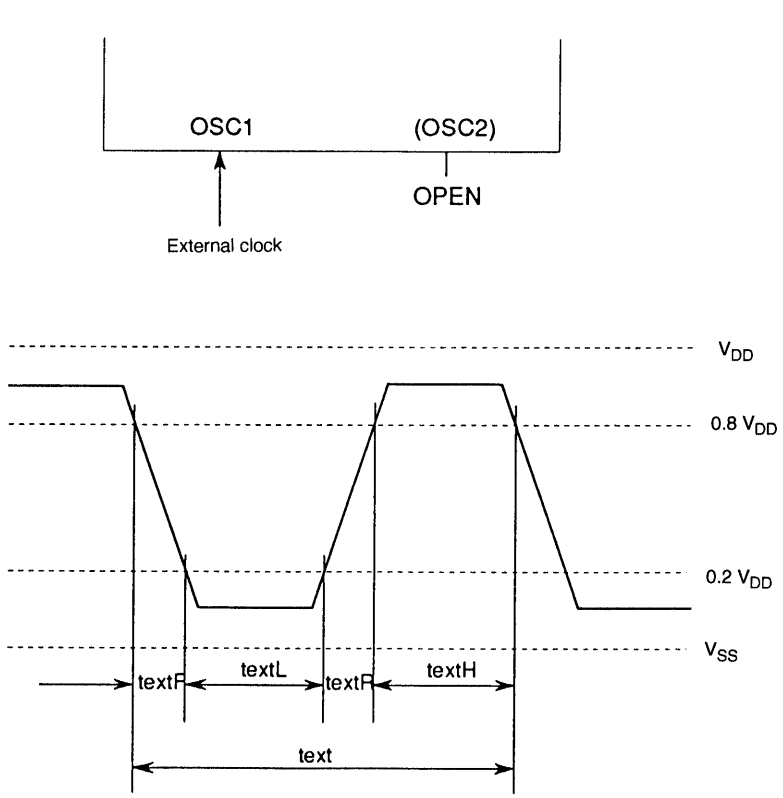


Figure 1 External Clock Input Waveform

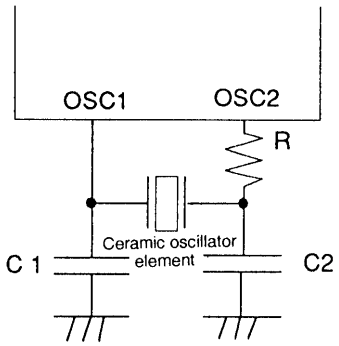


Figure 2 Ceramic Oscillator Circuit

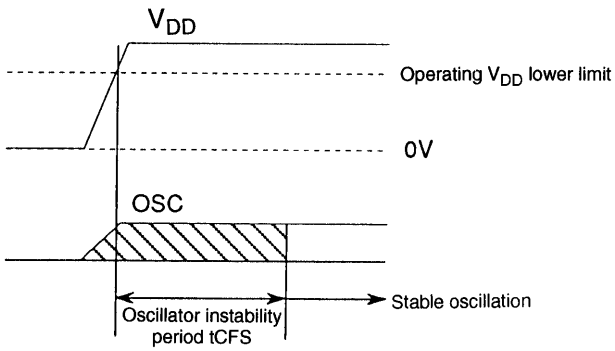


Figure 3 Oscillator Stabilization Period

Table 1: Guaranteed Ceramic Oscillator Constants

4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MG CST4.00MGW (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
4 MHz (Kyocera Corporation) KBR4.0MSA KBR4.0MKS (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
1 MHz (Murata Mfg. Co., Ltd.) CSB1000J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
1 MHz (Kyocera Corporation) KBR1000F	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	0 Ω
800 kHz (Murata Mfg. Co., Ltd.) CSB800J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
800 kHz (Kyocera Corporation) KBR800F	C1	220 pF ± 10%
	C2	220 pF ± 10%
	R	0 Ω

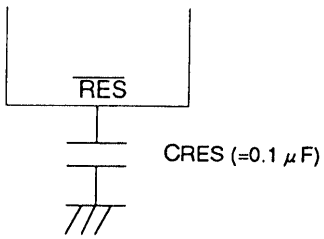


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1 µF will be between 5 and 50 ms.
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

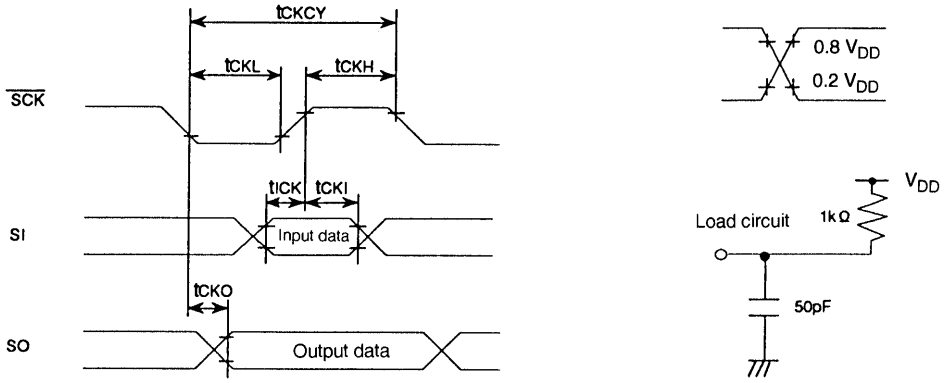
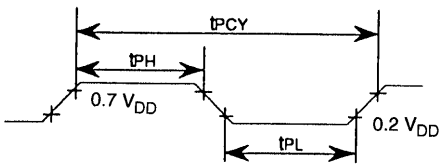
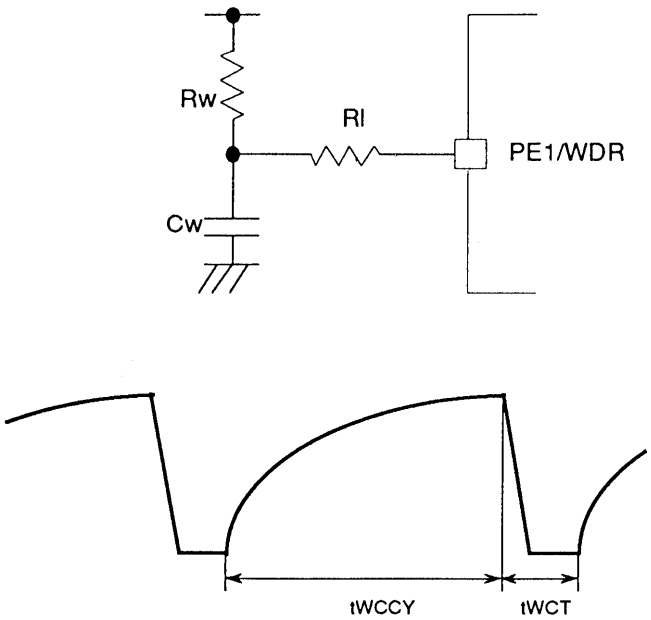


Figure 5 Serial I/O Timing



With load conditions identical to those shown in Figure 5

Figure 6 Port PE0 Pulse Output Timing



t_{WCCY}: Charge time due to the external components C_W, R_W, and RI.
t_{WCT}: Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

LC651204F, 651202F

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Voltages up to any generated voltage are allowed.	V
Input voltage	V_I (1)		OSC1 *1	–0.3 to V_{DD} +0.3	V
	V_I (2)		TEST, $\overline{RES}$	–0.3 to V_{DD} +0.3	V
I/O voltage	V_{IO} (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	–0.3 to + 15	V
	V_{IO} (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	–0.3 to V_{DD} +0.3	V
	V_{IO} (3)	PA0 to 3, PG0 to 3		–0.3 to V_{DD} +0.3	V
Peak output current	I_{OP}		I/O ports	–2 to +20	mA
Average output current	I_{OA}	Average value per pin over a 100-ms period	I/O ports	–2 to +20	mA
	Σ I_{OA} (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1 *2	PC0 to 3 PD0 to 3 PE0 to 1	–15 to +100	mA
	Σ I_{OA} (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to 3 PG0 to 3 PA0 to 3	–15 to +100	mA
Allowable power dissipation	Pd max (1)	Ta = –40 to +85°C (DIP package)		250	mW
	Pd max (2)	Ta = –40 to +85°C (MFP package)		150	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Operating power-supply voltage	V_{DD}		V_{DD}	3.0		5.5	V
Standby power-supply voltage	V_{ST}	RAM and register values retained *3	V_{DD}	1.8		5.5	V
Input high-level voltage	V_{IH} (1)	Output n-channel transistors off	OD specification ports C, D, E, and F	0.7 V_{DD}		13.5	V
	V_{IH} (2)	Output n-channel transistors off	PU specification ports C, D, E, and F	0.7 V_{DD}		V_{DD}	V
	V_{IH} (3)	Output n-channel transistors off	Port A, G	0.7 V_{DD}		V_{DD}	V
	V_{IH} (4)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with OD specifications	0.8 V_{DD}		13.5	V
	V_{IH} (5)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with PU specifications	0.8 V_{DD}		V_{DD}	V
	V_{IH} (6)	V_{DD} = 1.8 to 5.5 V	$\overline{RES}$	0.8 V_{DD}		V_{DD}	V
	V_{IH} (7)	External clock specifications	OSC1	0.8 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL} (1)	Output n-channel transistors off	Port	V_{SS}		0.2 V_{DD}	V
	V_{IL} (2)	Output n-channel transistors off	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.2 V_{DD}	V
	V_{IL} (3)	External clock specifications	OSC1	V_{SS}		0.2 V_{DD}	V
	V_{IL} (4)		TEST	V_{SS}		0.2 V_{DD}	V
	V_{IL} (5)		$\overline{RES}$	V_{SS}		0.2 V_{DD}	V

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Operating frequency (cycle time)	fop (T cyc)			670 (6)		4330 (0.97)	kHz (µs)
External clock conditions							
Frequency	text		OSC1	670		4330	kHz
Pulse width	textH, textL	Figure 1	OSC1	69			ns
Rise and fall times	textR, textF		OSC1			50	ns
Guaranteed oscillator constants Ceramic oscillator		Figure 2		See table 1.			

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V (unless otherwise specified)

Parameter		Symbol	Conditions		Applicable pins/notes	Ratings			
						min	typ	max	Unit
Input high-level current		I_{IH} (1)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V_{IN} = 13.5 V		Ports C, D, E, and F with open-drain specifications			5.0	µA
		I_{IH} (2)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V_{IN} = V_{DD}		Ports A and G with open-drain specifications			1.0	µA
		I_{IH} (3)	External clock mode, V_{IN} = V_{DD}		OSC1			1.0	µA
Input low-level current		I_{IL} (1)	Output n-channel transistor off V_{IN} = V_{SS}		Ports with open-drain specifications	–1.0			µA
		I_{IL} (2)	Output n-channel transistor off V_{IN} = V_{SS}		Ports with pull-up resistor specifications	–1.3	–0.35		mA
		I_{IL} (3)	V_{IN} = V_{SS}		$\overline{RES}$	–45	–10		µA
		I_{IL} (4)	External clock mode, V_{IN} = V_{SS}		OSC1	–1.0			µA
Output high-level voltage		V_{OH} (1)	I_{OH} = –50 µA		Ports with pull-up resistor specifications	V_{DD} –1.2			V
		V_{OH} (2)	I_{OH} = –10 µA		Ports with pull-up resistor specifications	V_{DD} –0.5			V
Output low-level voltage		V_{OL} (1)	I_{OL} = 10 mA		Port			1.5	V
		V_{OL} (2)	I_{OL} = 1 mA, with the I_{OL} for all ports no more than 1 mA.		Port			0.5	V
Schmitt characteristics	Hysteresis voltage	V_{HIS}			$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, and SI OSC1 with Schmitt specifications *4		0.1 V_{DD}		V
	High-level threshold voltage	V_{tH}				0.4 V_{DD}		0.8 V_{DD}	V
	Low-level threshold voltage	V_{tL}				0.25V_{DD}		0.6 V_{DD}	V
Current drain Ceramic oscillator		I_{DDOP} (1)	Figure 2, 4 MHz		V_{DD}		2	6	mA
External clock		I_{DDOP} (2)	670 to 1444 kHz *1 Operating, output n-channel transistors off, Ports = V_{DD}		V_{DD}		2	6	mA
Standby mode		I_{DDst}	Output n-channel transistor off, Ports = V_{DD}	V_{DD} = 5.5 V	V_{DD}		0.05	10	µA
				V_{DD} = 3 V	V_{DD}		0.025	5	µA

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC}	Figure 2, fo = 4 MHz *5	OSC1, OSC2	3840	4000	4160	kHz
Oscillator stabilization time	t_{CFS}	Figure 3, fo = 4 MHz				5	ms
Pull-up resistors I/O ports	R_{PP}	Output n-channel transistor off $V_{in} = V_{SS}$, V_{DD} = 5 V	Ports with pull-up resistor specifications	8	14	30	kΩ
$\overline{RES}$	Ru	$V_{in} = V_{SS}$, V_{DD} = 5 V	$\overline{RES}$	100	250	400	kΩ
External reset characteristics Reset time	t_{RST}				See Figure 4.		
Pin capacitance	Cp	f = 1 MHz With all pins other than the pin being measured at $V_{IN} = V_{SS}$			10		pF
Serial clock Input clock cycle time	t_{CKCY} (1)	Figure 5	$\overline{SCK}$	2.0			µs
Output clock cycle time	t_{CKCY} (2)	Figure 5	$\overline{SCK}$		$64 \times T_{CYC}$ *6		µs
Input clock low-level pulse width	t_{CKL} (1)	Figure 5	$\overline{SCK}$	0.6			µs
Output clock low-level pulse width	t_{CKL} (2)	Figure 5	$\overline{SCK}$		$32 \times T_{CYC}$		µs
Input clock high-level pulse width	t_{CKH} (1)	Figure 5	$\overline{SCK}$	0.6			µs
Output clock high-level pulse width	t_{CKH} (2)	Figure 5	$\overline{SCK}$		$32 \times T_{CYC}$		µs
Serial input Data setup time	t_{ICK}	Stipulated with respect to the rising edge of $\overline{SCK}$.	SI	0.2			µs
Data hold time	t_{CKI}	Figure 5	SI	0.2			µs
Serial output Output delay time	t_{CKO}	Stipulated with respect to the falling edge of $\overline{SCK}$. For n-channel open-drain outputs only. External resistance: 1 kΩ, external capacitance: 50 pF. Figure 5	SO			0.4	µs
Pulse output Period	t_{PCY}	Figure 6	PE0		$64 \times T_{CYC}$		µs
High-level pulse width	t_{PH}	Tcyc = 4 × the system clock period For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF	PE0		$32 \times T_{CYC}$ ±10%		µs
Low-level pulse width	t_{PL}		PE0		$32 \times T_{CYC}$ ±10%		µs

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Parameter		Symbol	Conditions	V_{DD} (v)	Applicable pins/notes	Ratings			
						min	typ	max	Unit
Watchdog timer	Guaranteed constants *7	C_W	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.01±5%		µF
		R_W	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		R_I	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t_{WCT}	See Figure 7.		WDR	10			µs
	Clear period (charge)	t_{WCCY}	See Figure 7.		WDR	3.0			ms
	Guaranteed constants *7	C_W	When PE1 has open-drain output specifications	4.5 to 5.5	WDR		0.01±5%		µF
		R_W	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		R_I	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t_{WCT}	See Figure 7.		WDR	10			µs
	Clear period (charge)	t_{WCCY}	See Figure 7.		WDR	3.3			ms

Note: 1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.

2. The average over a 100-ms period

3. The operating power-supply voltage V_{DD} must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.

4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.

5. The values shown for f_{CFOSC} are the frequencies for which oscillation is possible.

6. Tcyc = 4 × the system clock period

7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

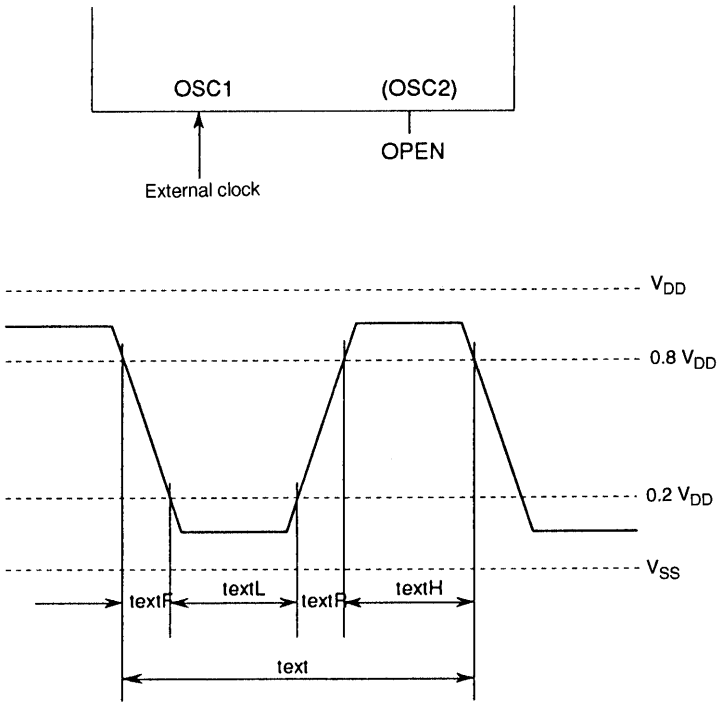


Figure 1 External Clock Input Waveform

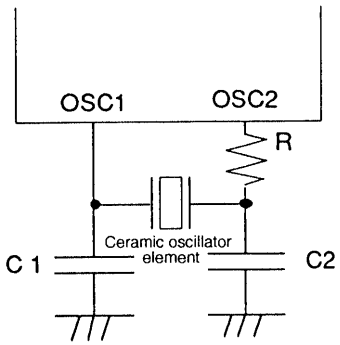


Figure 2 Ceramic Oscillator Circuit

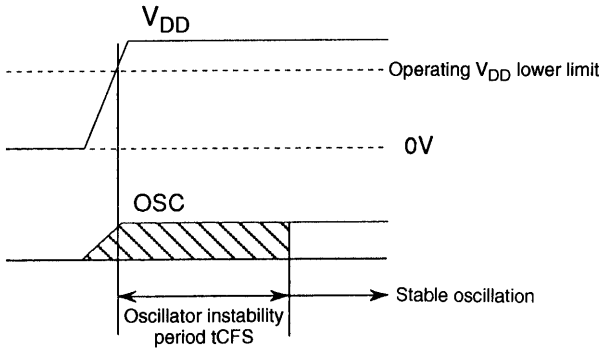


Figure 3 Oscillator Stabilization Period

Table 1: Guaranteed Ceramic Oscillator Constants

4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MG CST4.00MGW (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
4 MHz (Kyocera Corporation) KBR4.0MSA KBR4.0MKS (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω

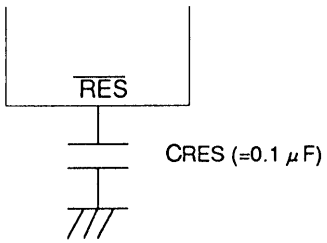


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1 μF will be between 5 and 50 ms.
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

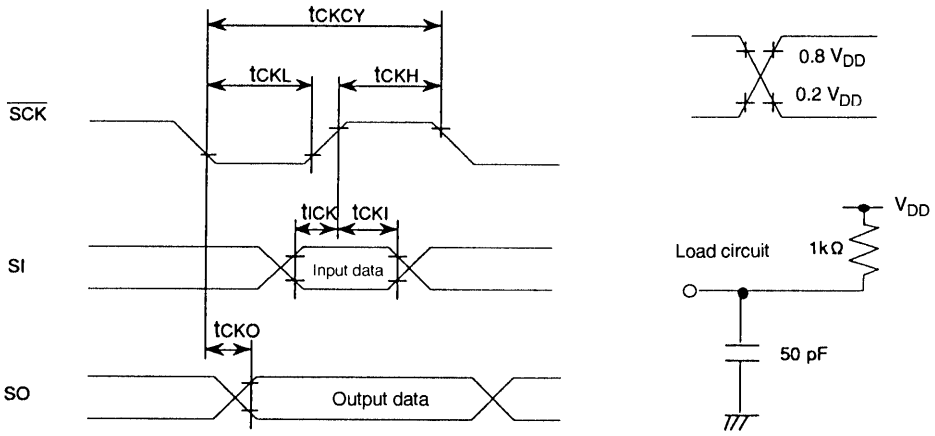
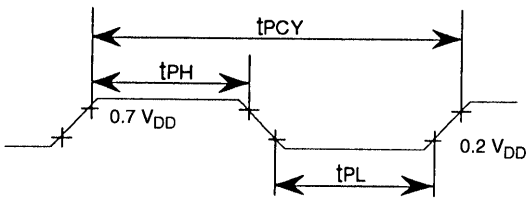
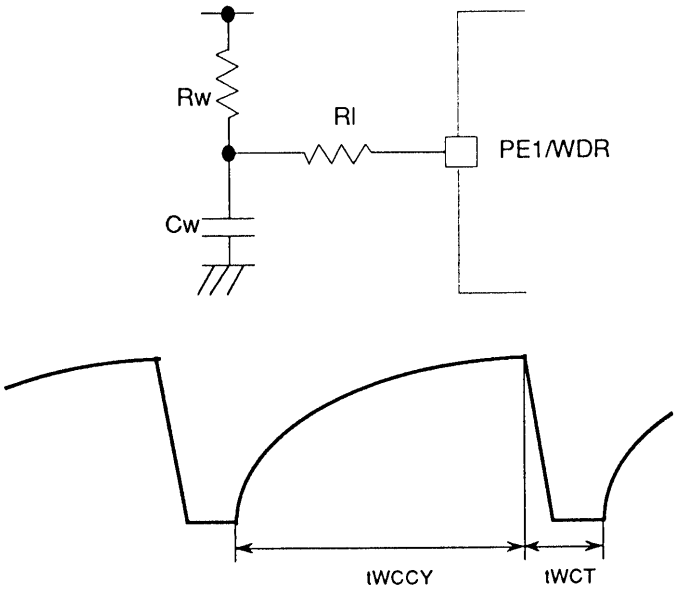


Figure 5 Serial I/O Timing



With load conditions identical to those shown in Figure 5

Figure 6 Port PE0 Pulse Output Timing



t_{WCCY}: Charge time due to the external components C_W, R_W, and RI.
t_{WCT}: Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

LC651204L, 651202L

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Voltages up to any generated voltage are allowed.	V
Input voltage	V_I (1)		OSC1*1	–0.3 to V_{DD} +0.3	V
	V_I (2)		TEST, $\overline{RES}$	–0.3 to V_{DD} +0.3	V
I/O voltage	V_{IO} (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	–0.3 to + 15	V
	V_{IO} (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	–0.3 to V_{DD} +0.3	V
	V_{IO} (3)	PA0 to 3, PG0 to 3		–0.3 to V_{DD} +0.3	V
Peak output current	I_{OP}		I/O ports	–2 to +20	mA
Average output current	I_{OA}	Average value per pin over a 100-ms period	I/O ports	–2 to +20	mA
	ΣI_{OA} (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1 *2	PC0 to 3 PD0 to 3 PE0 to 1	–15 to +100	mA
	ΣI_{OA} (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3 *2	PF0 to 3 PG0 to 3 PA0 to 3	–15 to +100	mA
Allowable power dissipation	Pd max (1)	Ta = –40 to +85°C (DIP package)		250	mW
	Pd max (2)	Ta = –40 to +85°C (MFP package)		150	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.5 to 5.5 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Operating power-supply voltage	V_{DD}		V_{DD}	2.5		5.5	V
Standby power-supply voltage	V_{ST}	RAM and register values retained *3	V_{DD}	1.8		5.5	V
Input high-level voltage	V_{IH} (1)	Output n-channel transistors off	OD specification ports C, D, E, and F	0.7 V_{DD}		13.5	V
	V_{IH} (2)	Output n-channel transistors off	PU specification ports C, D, E, and F	0.7 V_{DD}		V_{DD}	V
	V_{IH} (3)	Output n-channel transistors off	Port A, G	0.7 V_{DD}		V_{DD}	V
	V_{IH} (4)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with OD specifications	0.8 V_{DD}		13.5	V
	V_{IH} (5)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with PU specifications	0.8 V_{DD}		V_{DD}	V
	V_{IH} (6)	V_{DD} = 1.8 to 5.5 V	$\overline{RES}$	0.8 V_{DD}		V_{DD}	V
	V_{IH} (7)	External clock specifications	OSC1	0.8 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL} (1)	Output n-channel transistors off	Port	V_{SS}		0.2 V_{DD}	V
	V_{IL} (2)	Output n-channel transistors off	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.15 V_{DD}	V
	V_{IL} (3)	External clock specifications	OSC1	V_{SS}		0.15 V_{DD}	V
	V_{IL} (4)		TEST	V_{SS}		0.2 V_{DD}	V
	V_{IL} (5)		$\overline{RES}$	V_{SS}		0.15 V_{DD}	V

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Operating frequency (cycle time)	fop (Tcyc)	Frequencies up to 4.16 MHz are supported if the divide-by-four divider circuit option is used.		670 (6)		1040 (3.84)	kHz (µs)
External clock conditions Frequency Pulse width Rise and fall times	 text textH, textL textR, textF	Figure 1. The divide-by- three or divide-by-four divider circuit option must be used if the clock frequency exceeds 1.040 MHz.	 OSC1 OSC1 OSC1	 670 150		 4160 100	 kHz ns ns
Guaranteed oscillator constants Ceramic oscillator		Figure 2		See table 1.			

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.5 to 5.5 V (unless otherwise specified)

Parameter		Symbol	Conditions	Applicable pins/notes	Ratings			
					min	typ	max	Unit
Input high-level current		I_{IH} (1)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V_{IN} = 13.5 V	Ports C, D, E, and F with open drain specifications			5.0	µA
		I_{IH} (2)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V_{IN} = V_{DD}	Ports A and G with open drain specifications			1.0	µA
		I_{IH} (3)	External clock mode, V_{IN} = V_{DD}	OSC1			1.0	µA
Input low-level current		I_{IL} (1)	Output n-channel transistor off V_{IN} = V_{SS}	Ports with open drain specifications	–1.0			µA
		I_{IL} (2)	Output n-channel transistor off V_{IN} = V_{SS}	Ports with pull-up resistor specifications	–1.3	–0.35		mA
		I_{IL} (3)	V_{IN} = V_{SS}	$\overline{RES}$	–45	–10		µA
		I_{IL} (4)	External clock mode, V_{IN} = V_{SS}	OSC1	–1.0			µA
Output high-level voltage		V_{OH} (1)	I_{OH} = –10 µA	Ports with pull-up resistor specifications	V_{DD} –0.5			V
Output low-level voltage		V_{OL} (1)	I_{OL} = 3 mA	Port			1.5	V
		V_{OL} (2)	I_{OL} = 1 mA, with the I_{OL} for all ports no more than 1 mA.	Port			0.4	V
Schmitt characteristics	Hysteresis voltage	V_{HIS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, and SI OSC1 with Schmitt specifications *4		0.1 V_{DD}		V
	High-level threshold voltage	V_{tH}			0.4 V_{DD}		0.8 V_{DD}	V
	Low-level threshold voltage	V_{tL}			0.2 V_{DD}		0.6 V_{DD}	V

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Parameter	Symbol	Conditions		Applicable pins/notes	Ratings			
					min	typ	max	Unit
Current drain Ceramic oscillator	I_{DDOP} (1)	Operating, output n-channel transistors off, Ports = V_{DD} Figure 2, 4 MHz, divide-by-four circuit		V_{DD}		1.5	4	mA
	I_{DDOP} (2)	Figure 2, 4 MHz, divide-by-four circuit V_{DD} = 2.5 V		V_{DD}		0.5	1	mA
	I_{DDOP} (3)	Figure 2, 800 kHz		V_{DD}		1.5	4.0	mA
External clock	I_{DDOP} (4)	670 to 1024 kHz, no divider circuit 2000 to 3120 kHz, divide-by-three circuit 2600 to 4160 kHz, divide-by-four circuit		V_{DD}		1.5	4	mA
Standby mode	I_{DDst}	Output n-channel transistor off, Ports = V_{DD}	V_{DD} = 5.5 V	V_{DD}		0.05	10	µA
			V_{DD} = 2.5 V	V_{DD}		0.020	4	µA
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC} *5	Figure 2, fo = 800 kHz Figure 2, fo = 1 MHz Figure 2, fo = 4 MHz, divide-by-four circuit		OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	768 960 3840	800 1000 4000	832 1040 4160	kHz kHz kHz
Oscillator stabilization time	t_{CFS}	Figure 3, fo = 800 kHz, 1 MHz, 4 MHz, divide-by-four circuit					5	ms
Pull-up resistors I/O ports	R_{PP}	Output n-channel transistor off V_{in} = V_{SS}, V_{DD} = 5 V		Ports with pull-up resistor specifications	8	14	30	kΩ
$\overline{RES}$	Ru	V_{in} = V_{SS}, V_{DD} = 5 V		$\overline{RES}$	100	250	400	kΩ
External reset characteristics Reset time	t_{RST}				See Figure 4.			
Pin capacitance	Cp	f = 1 MHz With all pins other than the pin being measured at V_{IN} = V_{SS}				10		pF

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Serial clock Input clock cycle time	t_{CKCY} (1)	Figure 5	$\overline{SCK}$	6.0			µs
Output clock cycle time	t_{CKCY} (2)	Figure 5	$\overline{SCK}$		$64 \times T_{CYC}$ *6		µs
Input clock low-level pulse width	t_{CKL} (1)	Figure 5	$\overline{SCK}$	2.0			µs
Output clock low-level pulse width	t_{CKL} (2)	Figure 5	$\overline{SCK}$		$32 \times T_{CYC}$		µs
Input clock high-level pulse width	t_{CKH} (1)	Figure 5	$\overline{SCK}$	2.0			µs
Output clock high-level pulse width	t_{CKH} (2)	Figure 5	$\overline{SCK}$		$32 \times T_{CYC}$		µs
Serial input Data setup time	t_{ICK}	Stipulated with respect to the rising edge of $\overline{SCK}$.	SI	0.5			µs
Data hold time	t_{CKI}	Figure 5	SI	0.5			µs
Serial output Output delay time	t_{CKO}	Stipulated with respect to the falling edge of $\overline{SCK}$. For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF. Figure 5	SO			1.0	µs
Pulse output period	t_{PCY}	Figure 6	PE0		$64 \times T_{CYC}$		µs
High-level pulse width	t_{PH}	Tcyc = 4 × the system clock period For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF	PE0		$32 \times T_{CYC}$ ±10%		µs
Low-level pulse width	t_{PL}		PE0		$32 \times T_{CYC}$ ±10%		µs

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Parameter		Symbol	Conditions	V_{DD} (v)	Applicable pins/notes	Ratings			
						min	typ	max	Unit
Watchdog timer	Guaranteed constants *7	C_W	When PE1 has open-drain output specifications	2.5 to 5.5	WDR		0.1±5%		µF
		R_W	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		R_I	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t_{WCT}	See Figure 7.		WDR	100			µs
	Clear period (charge)	t_{WCCY}	See Figure 7.		WDR	26			ms
	Guaranteed constants *7	C_W	When PE1 has open-drain output specifications	2.5 to 5.5	WDR		0.047±5%		µF
		R_W	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		R_I	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t_{WCT}	See Figure 7.		WDR	40			µs
	Clear period (charge)	t_{WCCY}	See Figure 7.		WDR	12			ms

Note: 1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.

2. The average over a 100-ms period

3. The operating power-supply voltage V_{DD} must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.

4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.

5. The values shown for f_{CFOSC} are the frequencies for which oscillation is possible.

6. $T_{cyc} = 4 \times$ the system clock period

7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

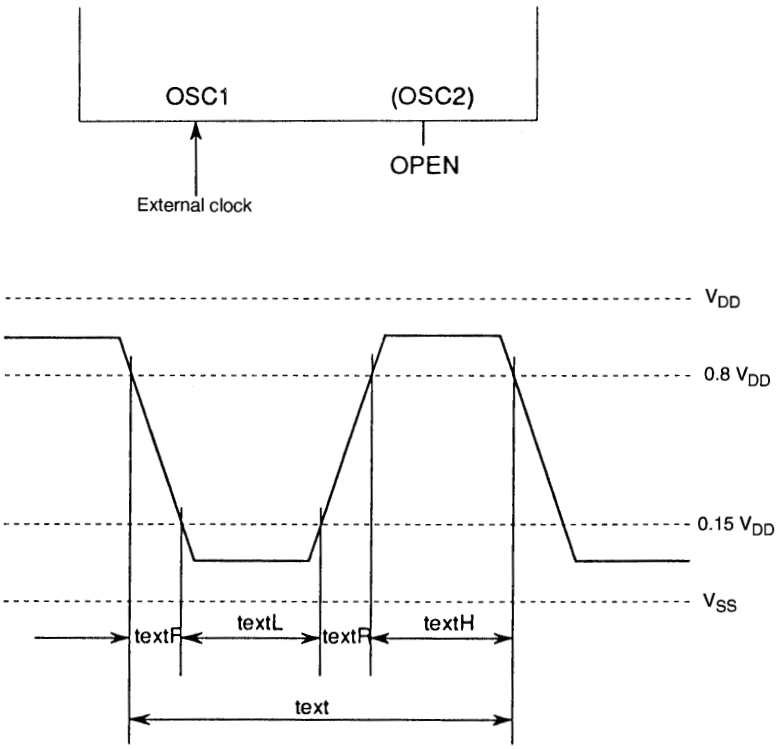


Figure 1 External Clock Input Waveform

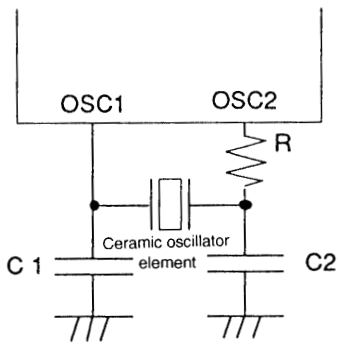


Figure 2 Ceramic Oscillator Circuit

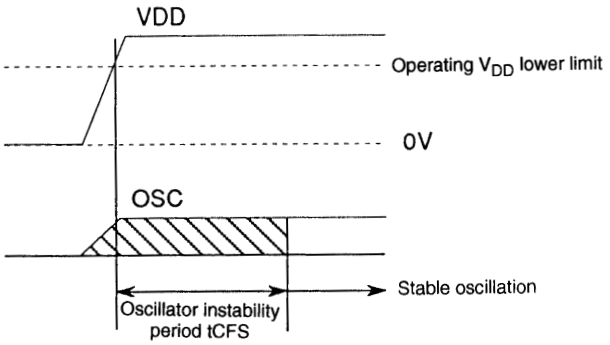


Figure 3 Oscillator Stabilization Period

Table 1: Guaranteed Ceramic Oscillator Constants

4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MGU CST4.0MGWU (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
1 MHz (Murata Mfg. Co., Ltd.) CSB1000J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
1 MHz (Kyocera Corporation) KBR1000F	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	0 Ω
800 kHz (Murata Mfg. Co., Ltd.) CSB800J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
800 kHz (Kyocera Corporation) KBR800F	C1	220 pF ± 10%
	C2	220 pF ± 10%
	R	0 Ω

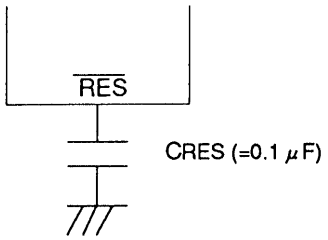


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1 μF will be between 5 and 50 ms.
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

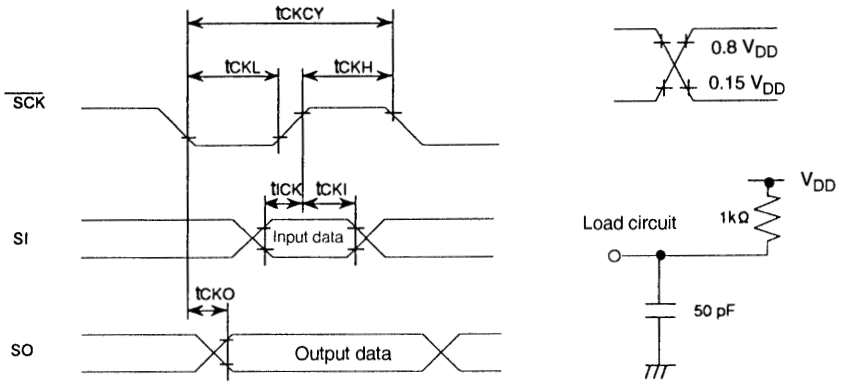
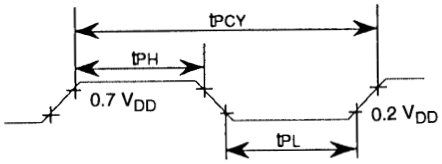
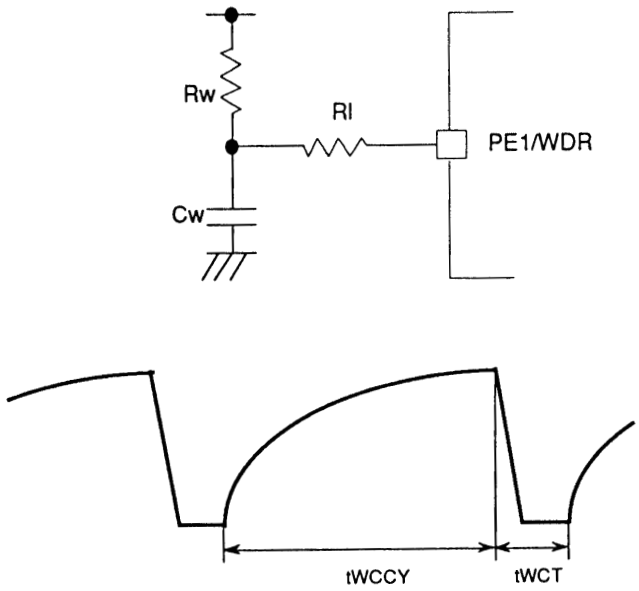


Figure 5 Serial I/O Timing



With load conditions identical to those shown in Figure 5

Figure 6 Port PE0 Pulse Output Timing



t_{WCCY}: Charge time due to the external components C_W, R_W, and Rl
t_{WCT}: Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

LC651204/1202 Instruction Set (by function)

Abbreviations

AC:	Accumulator	M:	Memory	ZF :	Zero flag
ACt:	Accumulator bit t	M(DP):	Memory addressed by DP	( )[ ]:	Indicates the contents of the item enclosed.
CF:	Carry flag	P(DPL):	I/O port specified by DPL	← :	Transfer and direction
CTL:	Control register	PC:	Program counter	+ :	Addition
DP:	Data pointer	STACK:	Stack pointer	– :	Subtraction
E:	E register	TM:	Timer	^ :	Logical AND
EXTF:	External interrupt request flag	TMF:	Timer (internal) interrupt request flag	∨ :	Logical OR
Fn:	Flag bit n	At, Ha, La:	Working registers	⩛ :	Logical exclusive OR

Instruction group	Mnemonic		Instruction code								Number of bytes	Number of cycles	Operation	Description	Modified status flags	Notes
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0						
Accumulator manipulation instructions	CLA	Clear AC	1	1	0	0	0	0	0	0	1	1	AC ← 0	Clears AC.	ZF	*1
	CIC	Clear CF	1	1	1	0	0	0	0	1	1	1	CF ← 0	Clears CF.	CF	
	STC	Set CF	1	1	1	1	0	0	0	1	1	1	CF ← 1	Sets CF.	CF	
	CMA	Complement AC	1	1	1	0	1	0	1	1	1	1	AC ← $(\overline{AC})$	Sets AC to the one's	ZF	
	INC	Increment AC	0	0	0	0	1	1	1	0	1	1	AC ← (AC) + 1	Increments AC.	ZF CF	
	DEC	Decrement AC	0	0	0	0	1	1	1	1	1	1	AC ← (AC) – 1	Decrements AC.	ZF CF	
	RAL	Rotate AC left through CF	0	0	0	0	0	0	0	1	1	1	$AC_0 \leftarrow (CF)$, $AC_{n+1} \leftarrow (AC_n)$, $CF \leftarrow (AC_3)$	Shifts AC together with CF left.	ZF CF	
	TAE	Transfer AC to E	0	0	0	0	0	0	1	1	1	1	E ← (AC)	Moves the contents of AC to E.		
	XAE	Exchange AC with E	0	0	0	0	1	1	0	1	1	1	(AC) ↔ (E)	Exchanges the contents of AC and E.		
Memory manipulation instructions	INM	Increment M	0	0	1	0	1	1	1	0	1	1	M(DP) ← [M(DP)] + 1	Increments M(DP).	ZF CF	
	DEm	Decrement M	0	0	1	0	1	1	1	1	1	1	M(DP) ← [M(DP)] – 1	Decrements M(DP).	ZF CF	
	SmB bit	Set M data bit	0	0	0	0	1	0	B_1	B_0	1	1	M(DP, B_1 B_0) ← 1	Sets the bit in M(DP) specified by B1B0 to 1.		
	RMB bit	Reset M data bit	0	0	1	0	1	0	B_1	B_0	1	1	M(DP, B_1 B_0) ← 0	Clears the bit in M(DP) specified by B1B0 to 0.		
Arithmetic and comparison instructions	AD	Add M to AC	0	1	1	0	0	0	0	0	1	1	AC ← (AC) + [M(DP)]	Adds the contents of AC and M(DP) as two's complement quantities and stores the result in AC.	ZF CF	
	ADC	Add M to AC with CF	0	0	1	0	0	0	0	0	1	1	AC ← (AC) + [M(DP)] + (CF)	Adds the contents of AC, CF, and M(DP) as two's complement quantities and stores the result in AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1	1	1	0	0	1	1	0	1	1	AC ← (AC) + 3	Adds 6 to AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1	1	1	0	1	0	1	0	1	1	AC ← (AC) + 10	Adds 10 to AC.	ZF	
	EXL	Exclusive or M to AC	1	1	1	1	0	1	0	1	1	1	AC ← (AC) ⩛ [M(DP)]	Takes the logical exclusive OR of AC and M(DP) and stores the result in AC.	ZF	
	AND	And M to AC	1	1	1	0	0	1	1	1	1	1	AC ← (AC) ^ [M(DP)]	Takes the logical AND of AC and M(DP) and stores the result in AC.	ZF	
	OR	Or M to AC	1	1	1	0	0	1	0	1	1	1	AC ← (AC) ∨ [M(DP)]	Takes the logical OR of AC and M(DP) and stores the result in AC.	ZF	
	CM	Compare AC with M	1	1	1	1	1	0	1	1	1	1	$\overline{[M(DP)]}$ + (AC) + 1	Compares the contents of AC and M(DP) and sets or clears CF and ZF accordingly. (Magnitude relationship / CF / ZF: [M(DP)] > (AC) 0 0; [M(DP)] = (AC) 1 1; [M(DP)] < (AC) 1 0)	ZF CF	
	CI data	Compare AC with immediate data	0	0	1	0	1	1	0	0	2	2	$\overline{I_3\ I_2\ I_1\ I_0}$ + (AC) + 1	Compares the contents of AC and the immediate data I_3 I_2 I_1 I_0 and sets or clears CF and ZF accordingly. (Magnitude relationship / CF / ZF: I_3 I_2 I_1 I0 > (AC) 0 0; I_3 I_2 I_1 I0 = (AC) 1 1; I_3 I_2 I_1 I0 < (AC) 1 0)	ZF CF	
			0	1	0	0	I_3	I_2	I_1	I_0						
	CLI data	Compare DP_L with immediate data	0	0	1	0	1	1	0	0	2	2	$(DP_L) \vee I_3\ I_2\ I_1\ I_0$	Compares the contents of DPL and the immediate data.	ZF	
			0	1	0	1	I_3	I_2	I_1	I_0						
Load and store instructions	LI data	Load AC with immediate data	1	1	0	0	I_3	I_2	I_1	I_0	1	1	AC ← I_3 I_2 I_1 I_0	Loads AC with the immediate data I_3 I_2 I_1 I_0.	ZF	*1
	S	Store AC to M	0	0	0	0	0	0	1	0	1	1	M(DP) ← (AC)	Stores the contents of AC at M(DP).		
	L	Load AC from M	0	0	1	0	0	0	0	1	1	1	AC ← [M(DP)]	Loads the contents of M(DP) into AC.	ZF	
	XM data	Exchange AC with M then modify DP_H with immediate data	1	0	1	0	0	M_2	M_1	M_0	1	2	(AC) ↔ [M(DP)] $DP_H \leftarrow (DP_H) \vee 0\ M_2\ M_1\ M_0$	Exchanges the contents of AC and M(DP). Then, replaces the contents of DPH with $(DP_H) \vee 0\ M_2\ M_1\ M_0$.	ZF	ZF is set to indicate the result of the (DPH) ⩛ 0 M_2 M_1 M_0 operation.
	X	Exchange AC with M	1	0	1	0	0	0	0	0	1	2	(AC) ↔ [M(DP)]	Exchanges the contents of AC and M(DP).	ZF	ZF is set according to the contents of DPH at the point the instruction was executed.
	XI	Exchange AC with M then increment DP_L	1	1	1	1	1	1	1	0	1	2	(AC) ↔ [M(DP)] $DP_L \leftarrow (DP_L) + 1$	Exchanges the contents of AC and M(DP). Then, increments the contents of DP_L.	ZF	ZF is set to indicate the result of the DP_L +1 operation.
	XD	Exchange AC with M then Decrement DP_L	1	1	1	1	1	1	1	1	1	2	(AC) ↔ [M(DP)] $DP_L \leftarrow (DP_L) – 1$	Exchanges the contents of AC and M(DP). Then, Decrements the contents of DP_L.	ZF	ZF is set to indicate the result of the DP_L –1 operation.
	RTBI	Read table data from program ROM	0	1	1	0	0	0	1	1	1	2	AC, E ↔ ROM (PCh, E, AC)	Loads into AC and E the ROM data stored at the location given by the lower 8 bits of the PC, E and AC.		

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Instruction group	Mnemonic		Instruction code								Number of bytes	Number of cycles	Operation	Description	Modified status flags	Notes
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0						
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1	0	0	0	I_3	I_2	I_1	I_0	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3\ I_2\ I_1\ I_0$	Loads 0 into DP_H and the immediate data I3I2I1I0 into DP_L.		
	LHI data	Load DPH with immediate data	0	1	0	0	I_3	I_2	I_1	I_0	1	1	$DP_H \leftarrow I_3\ I_2\ I_1\ I_0$	Loads the immediate data $I_3\ I_2\ I_1\ I_0$ into DP_H.		
	IND	Increment DP_L	1	1	1	0	1	1	1	0	1	1	$DP_L \leftarrow (DP_L) + 1$	Increments the contents of DP_L.	ZF	
	DED	Decrement DP_L	1	1	1	0	1	1	1	1	1	1	$DP_L \leftarrow (DP_L) - 1$	Decrements the contents of DP_L.	ZF	
	TAL	Transfer AC to DP_L	1	1	1	1	0	1	1	1	1	1	$DP_L \leftarrow (AC)$	Moves the contents of AC to DP_L.		
	TLA	Transfer DPL to AC	1	1	1	0	1	0	0	1	1	1	$AC \leftarrow (DP_L)$	Moves the contents of DPL to AC.	ZF	
	XAH	Exchange AC with DPH	0	0	1	0	0	0	1	1	1	1	$(AC) \leftrightarrow (DP_H)$	Exchanges the contents of AC and DP_H.		
Working register manipulation instructions	XAt	Exchange AC with working register At					t1	t0						Exchanges the contents of AC		
	XA0		1	1	1	0	0	0	0	0	1	1	$(AC) \leftrightarrow (A0)$	and the working register A0, A1,		
	XA1		1	1	1	0	0	1	0	0	1	1	$(AC) \leftrightarrow (A1)$	A2, or A3 specified by t1t0.		
	XA2		1	1	1	0	1	0	0	0	1	1	$(AC) \leftrightarrow (A2)$			
	XA3		1	1	1	0	1	1	0	0	1	1	$(AC) \leftrightarrow (A3)$			
	XHa	Exchange DPH with working register Ha						a						Exchanges the contents of DP_H		
	XH0		1	1	1	1	1	0	0	0	1	1	$(DP_H) \leftrightarrow (H0)$	and the working register H0 or H1		
	XH1		1	1	1	1	1	1	0	0	1	1	$(DP_H) \leftrightarrow (H1)$	specified by a.		
	XLa	Exchange DPH with working register Ha						a						Exchanges the contents of DP_L		
	XL0		1	1	1	1	1	0	0	0	1	1	$(DP_L) \leftrightarrow (L0)$	and the working register L0 or L1		
	XL1		1	1	1	1	1	1	0	0	1	1	$(DP_L) \leftrightarrow (L1)$	specified by a.		
Memory manipulation instructions	SFB flag	Set flag bit	0	1	0	1	B_3	B_2	B_1	B_0	1	1	$Fn \leftarrow 1$	Sets the flag specified by $B_3\ B_2\ B_1\ B_0$ to 1.		
	RFB flag	Reset flag bit	0	0	0	1	B_3	B_2	B_1	B_0	1	1	$Fn \leftarrow 0$	Clears the flag specified by $B_3\ B_2\ B_1\ B_0$ to 0.	ZF	The flags are divided into four groups, F0 to F3, F4 to F7, F8 to F11, and F12 to F15. ZF is set or cleared according to the 4 bits included in the specified flags.
Jump and subroutine instructions	JMP addr	Jumping in the current bank	0 P_7	1 P_6	1 P_5	0 P_4	1 P_3	P_{10} P_2	P_9 P_1	P_8 P_0	2	2	$PC \leftarrow P_{10}\ P_9\ P_8\ P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$	Jumps to the location specified by the immediate data $P_{10}\ P_9\ P_8\ P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$.		
	JPEA	Jumping current page modified by E and AC	1	1	1	1	1	0	1	0	1	1	PC_0 to $_7 \leftarrow$ (E, AC)	Jumps to the location given by replacing the lower 8 bits of the PC with E and AC.		
	CZP addr	Call subroutine in the zero page	1	0	1	1	P_3	P_2	P_1	P_0	1	1	STACK $\leftarrow$ (PC) + 1 PC_{10} to $_6$, PC_1 to $_0 \leftarrow 0$ PC_5 to $_2 \leftarrow P_3\ P_2\ P_1\ P_0$	Calls a subroutine on page 0.		
	CAL addr	Call subroutine	1	0	1	0	1	P_{10}	P_9	P_8	2	2	STACK $\leftarrow$ (PC) + 2	Calls a subroutine.		
	RT	Return from subroutine	0	1	1	0	0	0	1	0	1	1	PC $\leftarrow$ (STACK)	Returns from a subroutine.		
	RTI	Return from interrupt routine	0	0	1	0	0	0	1	0	1	1	PC $\leftarrow$ (STACK) CF, ZF $\leftarrow$ CSF, ZSF	Returns from an interrupt handling routine.	ZF CF	
	BANK	Change bank	1	1	1	1	1	1	0	1	1	1		Specifies a pseudo I/O port and changes the bank.		Only valid for the immediately following JMP, I/O, or branch instruction.
Branch instructions	BAt addr	Change bank	0 P_7	1 P_6	1 P_5	1 P_4	0 P_3	0 P_2	t_1 P_1	t_0 P_0	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if ACt = 1	Branches to the location on the same page specified by P_7 to P_0 if the bit in AC specified by the immediate data t1t0 is 1.		The mnemonics are BA0 to BA3, reflecting the value of t.
	BNAt addr	Branch on no AC bit	0 P_7	0 P_6	1 P_5	1 P_4	0 P_3	0 P_2	t_1 P_1	t_0 P_0	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if ACt = 0	Branches to the location on the same page specified by P_7 to P_0 if the bit in AC specified by the immediate data t1t0 is 0.		The mnemonics are BNA0 to BNA3, reflecting the value of t.
	BMt addr	Branch on M bit	0 P_7	1 P_6	1 P_5	1 P_4	0 P_3	1 P_2	t_1 P_1	t_0 P_0	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if [M(DP, $t_1\ t_0$)] = 1	Branches to the location on the same page specified by P_7 to P_0 if the bit in M(DP) specified by the immediate data $t_1\ t_0$ is 1.		The mnemonics are BM0 to BM3, reflecting the value of t.
	BNMt addr	Branch on no M bit	0 P_7	0 P_6	1 P_5	1 P_4	0 P_3	1 P_2	t_1 P_1	t_0 P_0	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if [M(DP, $t_1\ t_0$)] = 0	Branches to the location on the same page specified by P_7 to P_0 if the bit in M(DP) specified by the immediate data $t_1\ t_0$ is 0.		The mnemonics are BNM0 to BNM3, reflecting the value of t.
	BPt addr	Branch on Port bit	0 P_7	1 P_6	1 P_5	1 P_4	1 P_3	0 P_2	t_1 P_1	t_0 P_0	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if [P(DP_L, $t_1\ t_0$)] = 1	Branches to the location on the same page specified by P_7 to P_0 if the bit in port P(DPL) specified by the immediate data $t_1\ t_0$ is 1.		The mnemonics are BP0 to BP3, reflecting the value of t.
	BNPt addr	Branch on no Port bit	0 P_7	0 P_6	1 P_5	1 P_4	1 P_3	0 P_2	t_1 P_1	t_0 P_0	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if [P(DP_L, $t_1\ t_0$)] = 0	Branches to the location on the same page specified by P_7 to P_0 if the bit in port P(DPL) specified by the immediate data $t_1\ t_0$ is 0.		The mnemonics are BNP0 to BNP3, reflecting the value of t.
	BTM addr	Branch on timer	0 P_7	1 P_6	1 P_5	1 P_4	1 P_3	0 P_2	0 P_1	0 P_0	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if TMF = 0 then TMF $\leftarrow$ 0	Branches to the location on the same page specified by P_7 to P_0 if TMF is 1. Also clears TMF.	TMF	

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Instruction group	Mnemonic		Instruction code D_7 D_6 D_5 D_4	Instruction code D_3 D_2 D_1 D_0	Number of bytes	Number of cycles	Operation	Description	Modified status flags	Notes
Branch instructions	BNTM addr	Branch on no timer	0 0 1 1 P_7 P_6 P_5 P_4	1 1 0 0 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if TMF = 0 then TMF ← 0	Branches to the location on the same page specified by P_7 to P_0 if TMF is 0. Also clears TMF.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 P_7 P_6 P_5 P_4	1 1 0 1 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if EXTF = 1 then EXTF ← 0	Branches to the location on the same page specified by P_7 to P_0 if EXTF is 1. Also clears EXTF.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 P_7 P_6 P_5 P_4	1 1 0 1 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if EXTF = 0 then EXTF ← 0	Branches to the location on the same page specified by P_7 to P_0 if EXTF is 0. Also clears EXTF.	EXTF	
	BC addr	Branch on CF	0 1 1 1 P_7 P_6 P_5 P_4	1 1 1 1 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if EXTF = 0	Branches to the location on the same page specified by P_7 to P_0 if CF is 1.		
	BNC addr	Branch on no CF	0 0 1 1 P_7 P_6 P_5 P_4	1 1 1 1 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if CF = 0	Branches to the location on the same page specified by P_7 to P_0 if CF is 0.		
	BZ addr	Branch on ZF	0 1 1 1 P_7 P_6 P_5 P_4	1 1 1 0 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if ZF = 1	Branches to the location on the same page specified by P_7 to P_0 if ZF is 1.		
	BNZ addr	Branch on no ZF	0 0 1 1 P_7 P_6 P_5 P_4	1 1 1 0 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if ZF = 0	Branches to the location on the same page specified by P_7 to P_0 if ZF is 0.		
	BFn addr	Branch on flag bit	1 1 0 1 P_7 P_6 P_5 P_4	n_3 n_2 n_1 n_0 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if Fn = 1	Branches to the location on the same page specified by P_7 to P_0 if the bit in the 16 flags specified by n_3 n_2 n_1 n_0 is 1.		The mnemonics are BF0 to BF15, reflecting the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 P_7 P_6 P_5 P_4	n_3 n_2 n_1 n_0 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if Fn = 0	Branches to the location on the same page specified by P_7 to P_0 if the bit in the 16 flags specified by n_3 n_2 n_1 n_0 iis 0.		The mnemonics are BFN0 to BFN15, reflecting the value of n.
I/O instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← [P(DP_L)]	Inputs the contents of port P(DP_L) to AC.	ZF	
	OP	Output port to AC	0 1 1 0	0 0 0 1	1	1	P(DP_L, B1 B0) ← (AC)	Outputs the contents of AC to port P(DP_L).		
	SPB bit	Set port bit	0 0 0 0	0 1 B_1 B_0	1	2	P(DP_L, B1 B0) ← 1	Sets to 1 the bit in port P(DP_L) specified by the immediate data B_1 B_0.		Executing this instruction destroys the contents of the E register.
	RPB bit	Reset port bit	0 0 1 0	0 1 B_1 B_0	1	2	P(DP_L, B1 B0) ← 1	Clears to 0 the bit in port P(DP_L) specified by the immediate data B_1 B_0.	ZF	Executing this instruction destroys the contents of the E register.
Other instructions	SCTL bit	Set control register bit (S)	0 0 1 0	1 1 0 0	2	2	CTL ← (CTL) ∨ B_3 B_2 B_1 B_0	Sets the bit (or bits) in the control register specified by B_3 B_2 B_1 B_0.		
	RCTL bit	Reset control register bit (S)	0 0 1 0 1 0 0 1	1 1 0 0 B_3 B_2 B_1 B_0	2	2	CTL ← (CTL) ∨ B_3 B_2 B_1 B_0	Clears the bit (or bits) in the control register specified by B_3 B_2 B_1 B_0.	ZF	
	WTTM	Write timer	1 1 1 1	1 0 1 1	1	1	TM ← (E), (AC) TMF ← 0	Loads the contents of E and AC into the timer. Also clears TMF.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	Stops all operations.		This instruction is disabled only when all bits in port PA are 0.
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	Consumes one machine cycle while performing no operation.		