Ordering number: EN2367B

CMOS LSI

No.2367B

SANYO

LC6512A, 6513A

SINGLE-CHIP 4-BIT MICROCOMPUTER FOR CONTROL-ORIENTED APPLICATIONS (LOW-THRESHOLD INPUT, ON-CHIP FLT DRIVER)

General Description

The LC6512A, 6513A are microcomputers that are indentical with FLT driver-contained microcomputers LC6502D, 6505D in instruction set but are further enhanced in performance, such as shorter cycle time, more stack levels, increased FLT drive capacity, and are partially changed in specifications for standby function. Since the LC6512A, 6513A are also pin-compatible with the LC6502D, 6505D, they can be used as similar replacements for the LC6502D, 6505D. The LC6512A, 6513A can replace the LC6502B/6502D, 6505B/6505D to enhance performances of equipment in which these microcomputers have been applied so far.

Features

- Low power dissipation CMOS single-chip microcomputer
- Instruction set with 79 instructions common to the LC6502C, 6502B, 6502D/LC6505C, 6505B, 6505D
- 2-source, 2-level interrupt function (external interrupt/internal timer interrupt)
- 8-level stack
- 4-bit prescaler-contained 8-bit programmable timer
- FLT driver-contained output ports and low-threshold input ports
  (1) Digits driving output ports: 10 pins
  (2) Segments driving output ports: 8 pins
  (3) Normal voltage input ports: 8 pins (4 pins: Low-threshold input port)
  (4) Normal voltage input/output ports: 8-pins
- ROM, RAM
  (1) LC6512A ROM: 2048 bytes, RAM: 128 x 4 bits
  (2) LC6513A ROM: 1024 bytes, RAM: 64 x 4 bits
- Cycle time 1.33μs min.
  400kHz, 800kHz, 1MHz, 3MHz ceremic resonator OSC
- Power-down by 2 standby modes
  (1) HALT mode: Power dissipation saving by program standby during normal operation
  (2) HOLD mode: Power supply backup during power failure
  (3) The standby function is the same as for the LC6514B and its using method is different from that of the LC6502D, 6505D, etc.
- Differences among LC6512D, 6513D, and LC6512A, 6513A
  The LC6512D, 6513D and LC6512A, 6513A are different in the OSC circuit only and are the same in the basic features. The differences are shown below.

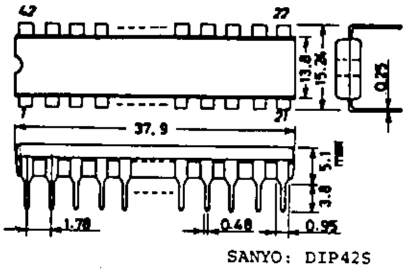
Item	LC6512A, 6513A	LC6512D, 6513D
OSC circuit configuration	1-stage inverter	5-stage inverter
OSC mode	Ceramic resonator OSC	Ceramic resonator OSC, CR OSC, application of external clock
OSC waveform	Sine wave	Rectangular wave
Operating frequency	Ceramic resonator OSC: 500kHz, 800kHz, 1MHz, 3MHz	Ceramic resonator OSC: 400kHz, 800kHz, 1MHz CR OSC: 400kHz typ, 800kHz typ External clock: 222kHz to 1290kHz

Technical Data

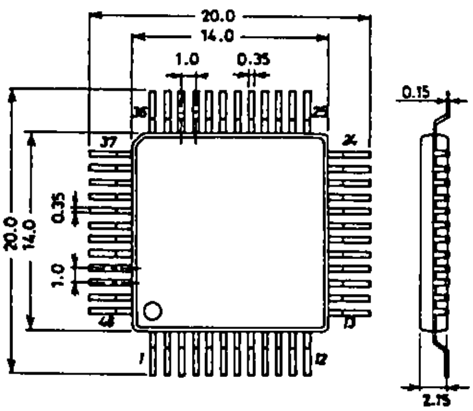
The LC6512A, 6513A are members of our LC6500 series of CMOS microcomputers. For their internal functions, refer to the LC6500 SERIES USER'S MANUAL. Those which differ from the description in the USER'S MANUAL are described in this catalog. Carefully study features and Appendix 4 Standby Function in this catalog before using the LC6512A, 6513A.

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg.,1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

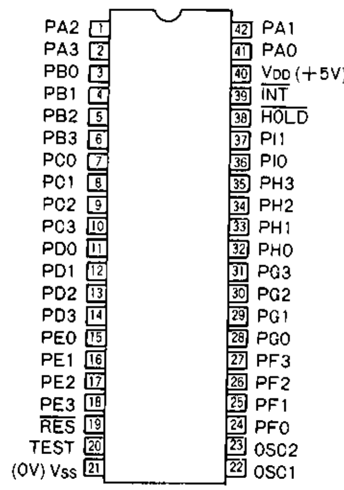
Package Dimensions 3025B-D42SIC
(unit: mm)



Package Dimensions 3052A-Q48AIC
(unit: mm)



Pin Assignment



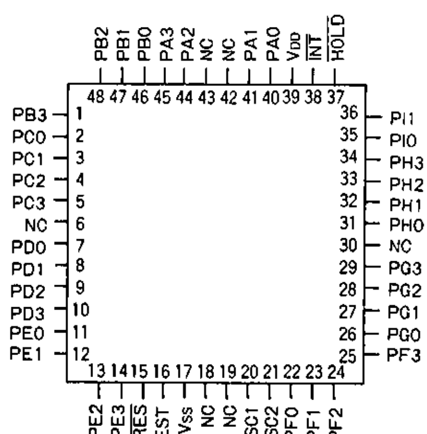
DIP42S

Pin Name

OSC1, OSC2	: Ceramic resonator for OSC	
$\overline{\text{INT}}$	: Interrupt	
$\overline{\text{RES}}$	: Reset	
$\overline{\text{HOLD}}$	: Hold	
PA0–3	: Input port	A0–3
PB0–3	: Input port	B0–3
PC0–3	: Input/output common port	C0–3
PD0–3	: Input/output common port	D0–3
PE0–3	: Output port (High-voltage port)	E0–3
PF0–3	: Output port (High-voltage port)	F0–3
PG0–3	: Output port (High-voltage port)	G0–3
PH0–3	: Output port (High-voltage port)	H0–3
PI0, 1	: Output port (High-voltage port)	I0, 1
TEST	: Test	

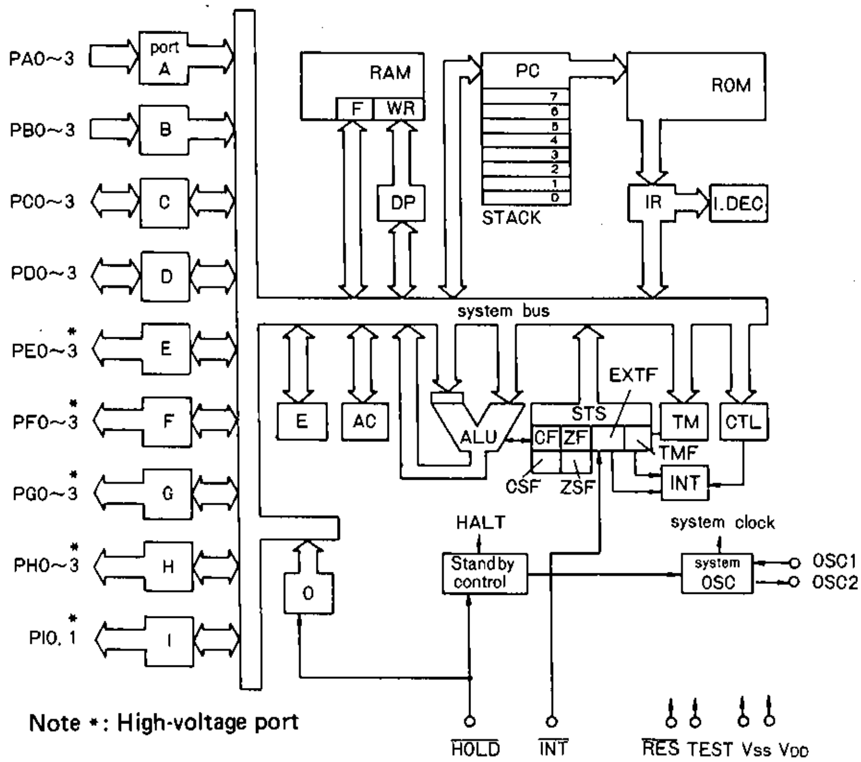
(Note) Nothing must be connected to NC pins internally or externally.

When mounting the QIP version on the board, do not dip it in solder.



QIP48

System Block Diagram



Note *: High-voltage port

RAM	: Data memory	STS	: Status register
F	: Flag	ROM	: Program memory
WR	: Working register	PC	: Program counter
AC	: Accumulator	INT	: Interrupt control
ALU	: Arithmetic and logic unit	IR	: Instruction register
DP	: Data pointer	I.DEC	: Instruction decoder
E	: E register	CF, CSF	: Carry flag, carry save flag
CTL	: Control register	ZF, ZSF	: Zero flag, zero save flag
OSC	: Oscillation circuit	EXTF	: External interrupt request flag
TM	: Timer	TMF	: Internal interrupt request flag

Pin Description

Pin Name	Input/Output	Function
$\overline{INT}$	Input	Interrupt request input pin
$\overline{HOLD}$	Input	HOLD mode request input pin (The LC6502, 6505 differ in function.) Capable of being used as a general-purpose single-bit input port unless the standby mode is used.
$\overline{RES}$	Input	Reset input pin
PA_{0-3}	Input	Input port A_0 to A_3 (Normal voltage, low-threshold input) Capable of 4-bit input and single-bit decision for branch Use also for HALT mode release request input

(Continued on next page)

(Continued from preceding page.)

PB_{0-3}	Input	Input port B_0 to B_3 (Normal voltage) Capable of 4-bit input and single-bit decision for branch
PC_{0-3}	Input/Output	Input/output common port C_0 to C_3 (Normal voltage) Capable of 4-bit input and single-bit decision for branch during input Capable of 4-bit output and single-bit set/reset during output
PD_{0-3}	Input/Output	Input/output common port D_0 to D_3 (Normal voltage) Capable of 4-bit input and single-bit decision for branch during input Capable of 4-bit output and single-bit set/reset during output
PE_{0-3}	Output	Output port E_0 to E_3 (Digit driver output) Capable of 4-bit output and single-bit set/reset Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch
PF_{0-3}	Output	Output port F_0 to F_3 (Digit driver output) Capable of 4-bit output and single-bit set/reset Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch
PG_{0-3}	Output	Output port G_0 to G_3 (Segment driver output) Capable of 4-bit output and single-bit set/reset Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch
PH_{0-3}	Output	Output port H_0 to H_3 (Segment driver output) Capable of 4-bit output and single-bit set/reset Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch
$PI_{0,1}$	Output	Output port I_0, I_1 (Digit driver output) Capable of 2-bit output and single-bit set/reset Capable of 2-bit input of output latch contents and single-bit decision of output latch for branch
OSC1	Input	A ceramic resonator is connected to this pin and pin OSC2 in the internal clock mode.
OSC2	Output	Pin for externally connecting a resonance circuit for the internal clock mode
V_{DD}	Input	Power supply pin Normally connected to +5V
V_{SS}	–	Connected to 0V power supply
TEST	Input	LSI test pin Normally connected to V_{SS}(0V)

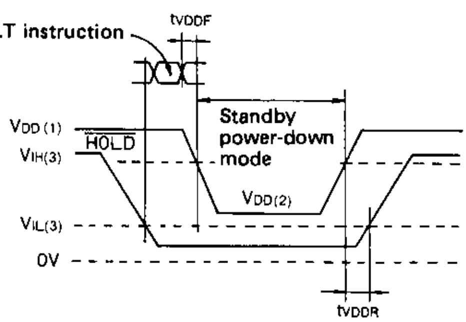
Absolute Maximum Ratings/T_a = 25°C, V_{SS} = 0V

				unit
Maximum Supply Voltage	V_{DD}		–0.3 to +7.0	V
Input Voltage	V_{IN}	Input pins other than OSC1	–0.3 to V_{DD}+0.3(Note1)	V
Output Voltage	$V_{OUT(1)}$	Ports C, D OSC 2	–0.3 to V_{DD}+0.3	V
	$V_{OUT(2)}$	Ports E, F, G, H, I	V_{DD}–45 to V_{DD}+0.3	V
Peak Output Current	$I_{O(1)}$	Ports C, D: Each pin	–2.0 to +2.0	mA
	$I_{O(2)}$	Ports E, F, I: Each pin	–15 to 0	mA
	$I_{O(3)}$	Ports G, H: Each pin	–10 to 0	mA
	$I_{O(4)}$	All pins of ports C to I	–90 to +16	mA
Allowable Power Dissipation	P_d max(1)	T_a=–30 to +70°C(Flat package)	350	mW
	P_d max(2)	T_a=–30 to +70°C (DIP)	600	mW
Operating Temperature	Topr		–30 to +70	°C
Storage Temperature	T_{stg}		–55 to +125	°C

(Note 1) For pin OSC1, up to oscillation amplitude generated when internally oscillated under the recommended oscillation conditions in Fig. 2 is allowable.

[Note] When mounting the QIP package version on the board, do not dip it in solder.

Allowable Operating Conditions/T_a = –30 to +70°C, V_{DD} = 5V±10%, V_{SS} = 0V			min	typ	max	unit
Operating Supply Voltage	$V_{DD(1)}$		4.5	5.0	5.5	V
Power-down Supply Voltage	$V_{DD(2)}$	HOLD mode: $\overline{HOLD}$ = $V_{IL(3)}$	1.8		5.5	V
"H"-Level Input Voltage	$V_{IH(1)}$	Port A	1.9		V_{DD}	V
	$V_{IH(2)}$	Ports B, C, D	$0.7V_{DD}$		V_{DD}	V
	$V_{IH(3)}$	$\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$ and OSC1	$0.8V_{DD}$		V_{DD}	V
"L"-Level Input Voltage	$V_{IL(1)}$	Ports B, C, D	V_{SS}		$0.3V_{DD}$	V
	$V_{IL(2)}$	$\overline{INT}$, $\overline{RES}$, OSC1	V_{SS}		$0.2V_{DD}$	V
	$V_{IL(3)}$	$\overline{HOLD}$, TEST: V_{DD}=1.8 to 5.5V	V_{SS}		$0.2V_{DD}$	V
	$V_{IL(4)}$	Port A	V_{SS}		0.5	V
External Capacitance for Ceramic	C1	See Fig. 2.				
Resonator OSC	C2	See Fig. 2.				
Allowable Delay in Key Scan	t_{DH}	See Figs. 3-3, 3-4 in Appendix 3.			(N-2) Xtcyc	µs
Circuit	t_{DL}				(N-2) Xtcyc	µs
		(Note) tcyc: Cycle time at microcomputer running mode				
Standby Timing	t_{VDDF}	V_{DD}=1.8 to 5.5V, See Fig. 1.	0			µs
	t_{VDDR}	V_{DD}=1.8 to 5.5V, See Fig. 1.	0			µs



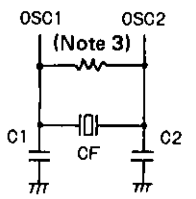
[Note]
No chattering shall be applied to the $\overline{HOLD}$ pin and PA_0 to 3 pins during the HALT instruction execution cycle.

Fig. 1 Standby mode timing

Electrical Characteristics/T_a = –30 to +70°C, V_{DD} = 5.0V±10%, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	unit
"H"-Level Input Current	I_{IH}	Each input pin: V_{IN}=V_{DD}			1.0	μA
"L"-Level Input Current	I_{IL}	Each input pin: V_{IN}=V_{SS}	–1.0			μA
"H"-Level Output Voltage	$V_{OH(1)}$	Ports C, D: I_{OH}=–1mA	V_{DD}–2.0			V
	$V_{OH(2)}$	Ports C, D: I_{OH}=–100μA	V_{DD}–0.5			V
	$V_{OH(3)}$	Ports E, F, I: I_{OH}=–10mA	V_{DD}–1.8			V
	$V_{OH(4)}$	Ports E, F, I: I_{OH}=–2mA	V_{DD}–1.0			V
	$V_{OH(5)}$	Ports E, F, I: I_{OH}=–1mA (Each port I_{OH}=Less than –1mA)	V_{DD}–0.5			V
	$V_{OH(6)}$	Ports G, H: I_{OH}=–2mA	V_{DD}–1.0			V
	$V_{OH(7)}$	Ports G, H: I_{OH}=–1mA (Each port I_{OH}=Less than –1mA)	V_{DD}–0.5			V
	$V_{OH(8)}$	OSC2: I_{OH}=–100μA	V_{DD}–0.5			V
"L"-Level Output Voltage	$V_{OL(1)}$	Ports C, D: I_{OL}=1mA			0.4	V
	$V_{OL(2)}$	OSC2: I_{OL}=100μA			0.4	V
Output OFF Leak Current	$I_{OFF(1)}$	Ports C, D: V_{OUT}=V_{DD}, HOLD mode			1.0	μA
	$I_{OFF(2)}$	Ports C, D: V_{OUT}=V_{SS}, HOLD mode	–1.0			μA
	$I_{OFF(3)}$	Ports E, F, G, H, I: V_{OUT}=V_{DD}			30	μA
	$I_{OFF(4)}$	Ports E, F, G, H, I: V_{OUT}=V_{DD}–40V	–30			μA
Clock OSC Frequency for Ceramic Resonator OSC	f_{CFOSC}	OSC circuit in Fig. 2: Recommended conditions for ceramic resonator OSC	392	Note 2	408	kHz
			784	Note 2	816	kHz
			980	Note 2	1020	kHz
			2940	Note 2	3060	kHz
Current Dissipation	$I_{DD(1)}$	Ceramic resonator OSC; f=400, 800, 1000kHz		1.0	2.0	mA
		Operating mode f=3MHz Recommended conditions for ceramic resonator OSC, output pin open, input pin V_{IN}=V_{SS}		2.7	4.0	mA
	$I_{DD(2)}$	HALT mode: V_{DD}=5V±10%, Test circuit in Fig. 3			10	μA
	$I_{DD(3)}$	HOLD mode: V_{DD}=1.8 to 5.5V, Test circuit in Fig. 4			10	μA
Input Capacitance	C_{IN}	Each input pin: Measure at f=1MHz. Pins not being measured: V_{SS}		5		pF
Output Capacitance	C_{OUT}	Ports E, F, G, H, I: Measure at f=1MHz Pins not being measured: V_{SS}		10		pF
Input/Output Capacitance	C_{IO}	Ports C, D: Measure at f=1MHz, Pins not being measured: V_{SS}		10		pF
Hysteresis Voltage	V_H	$\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$		0.1V_{DD}		V

Center frequency	Ceramic resonator	C1 (pF)	C2 (pF)
3MHz	CSA3.00MG (Murata)	33±10%	
	KBR3.0MS (Kyocera)	22±10%	
1MHz	CSB1000K, D (Murata)	180±10%	
	KBR1000H (Kyocera)	180±10%	
800kHz	CSB800K, D (Murata)	180±10%	
	KBR800H (Kyocera)	180±10%	
400kHz	CSB400P (Murata)	330±10%	
	KBR400B (Kyocera)	330±10%	

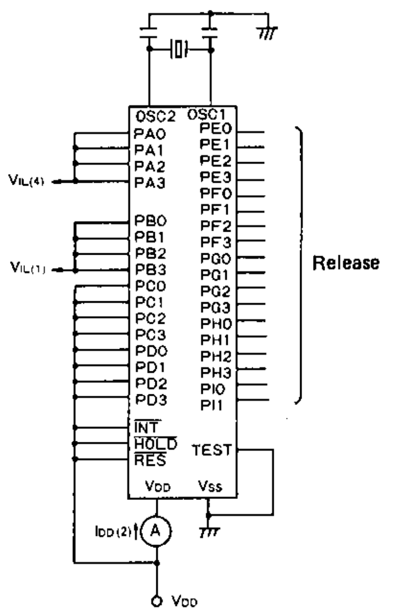


CF: Ceramic resonator
CSA3.00MG (Murata)
KBR3.0MS (Kyocera)
CSB1000K, D (Murata)
KBR1000H(Kyocera)
CSB800K, D (Murata)
KBR800H (Kyosera)
CSB400P (Murata)
KBR400B (Kyosera)

Fig. 2 Recommended OSC circuit, constants for ceramic resonator OSC

Note 2) There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.
The min., max. values of OSC frequency represent the oscillatable frequency range.

Note 3) When using the piggyback microcomputer, evaluation chip for evaluation, connect a feedback resistor (approximately 1Mohm).



Input/output common ports C, D: Output inhibit
HALT instruction is executed to provide HALT mode.

Fig. 3 $I_{DD(2)}$ test circuit

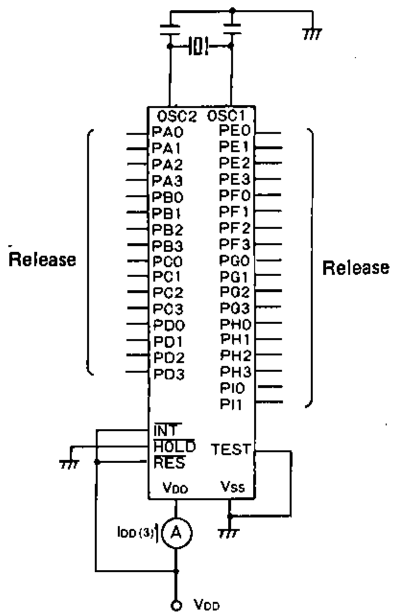
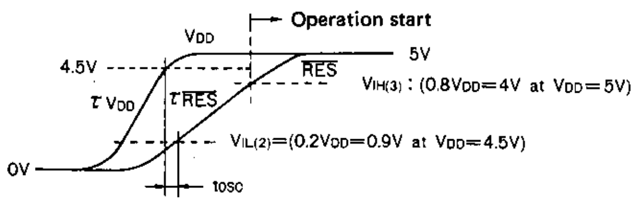
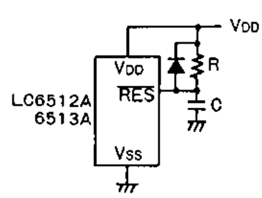


Fig. 4 $I_{DD(3)}$ test circuit





τV_{DD}: Power supply rise time constant
τRES: RES pin rise time constant
Fix C, R so that $\tau V_{DD} \leqq \tau RES$, $t_{OSC} \geqq 10$msec. is obtained.
t_{OSC}: OSC stabilized time

Fig. 5 Initial reset timing

Appendix 1. Support System

For application development of the LC6512A, 6513A, the support system for the LC6512A, 6513A is used.

1-1. Software support

The support system provides source editor, cross assembler. For cross assembler on CP/M, the "LC6502.COM", "LC6505.COM" are used, and on MS-DOS, the "LC6512.COM", "LC6513.COM" are used.

1-2. Hardware support

(1) Evaluation chip

Evaluation chip LC6597 is used. Level converters, drivers are connected to high-voltage ports (PE_0 to 3, PF_0 to 3, PG_0 to 3, PH_0 to 3, $PI_{0,\ 1}$) externally.

(A dedicated adaptor is available.)

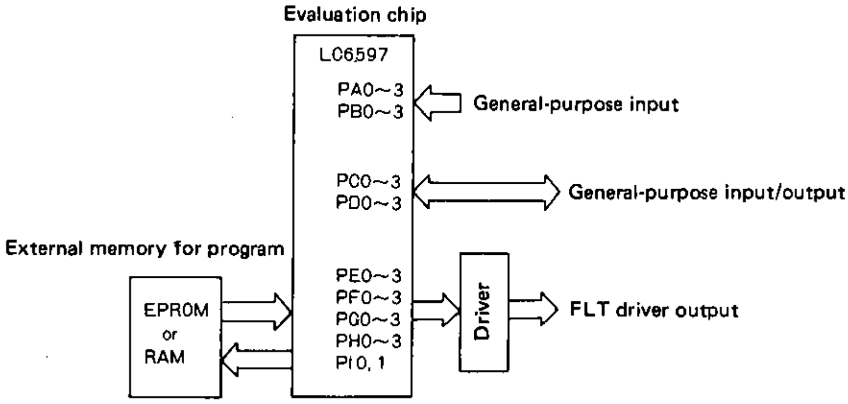


Fig. 1-1 Basic evaluation system using evaluation chip

(2) Simulation chip

Piggyback LC65PG12/13 and adaptor (EVA-97-12D/13D) for the LC6512A, 6513A are used jointly.

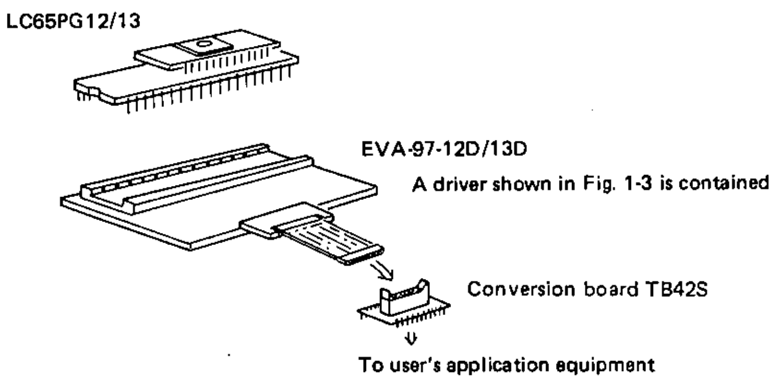


Fig. 1-2 How to use piggyback

(3) Evaluation kit
The EVA-410 and EVA-TB2 are used. For connecting with user's application equipment, adaptor (EVA-97-12D/13D) is used.

(4) Adaptor (EVA-97-12D/13D)
This is used when evaluating the LC6512A, 6513A with the aid of the evaluation chip and piggyback. This contains drivers for FLT. (See Figs. 1-3, 1-4.)

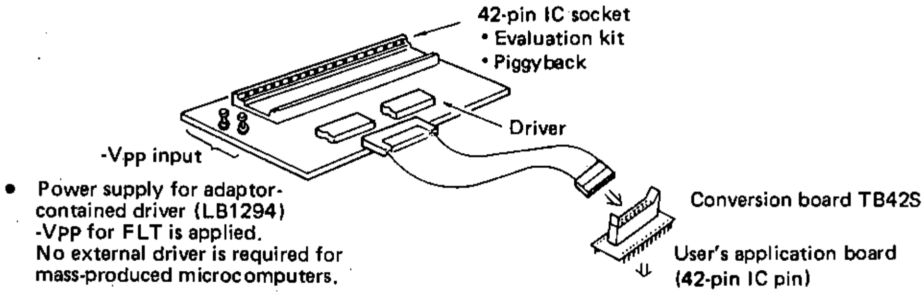


Fig. 1-3 Adaptor (EVA-97-12D/13D) for LC6512A, 6513A

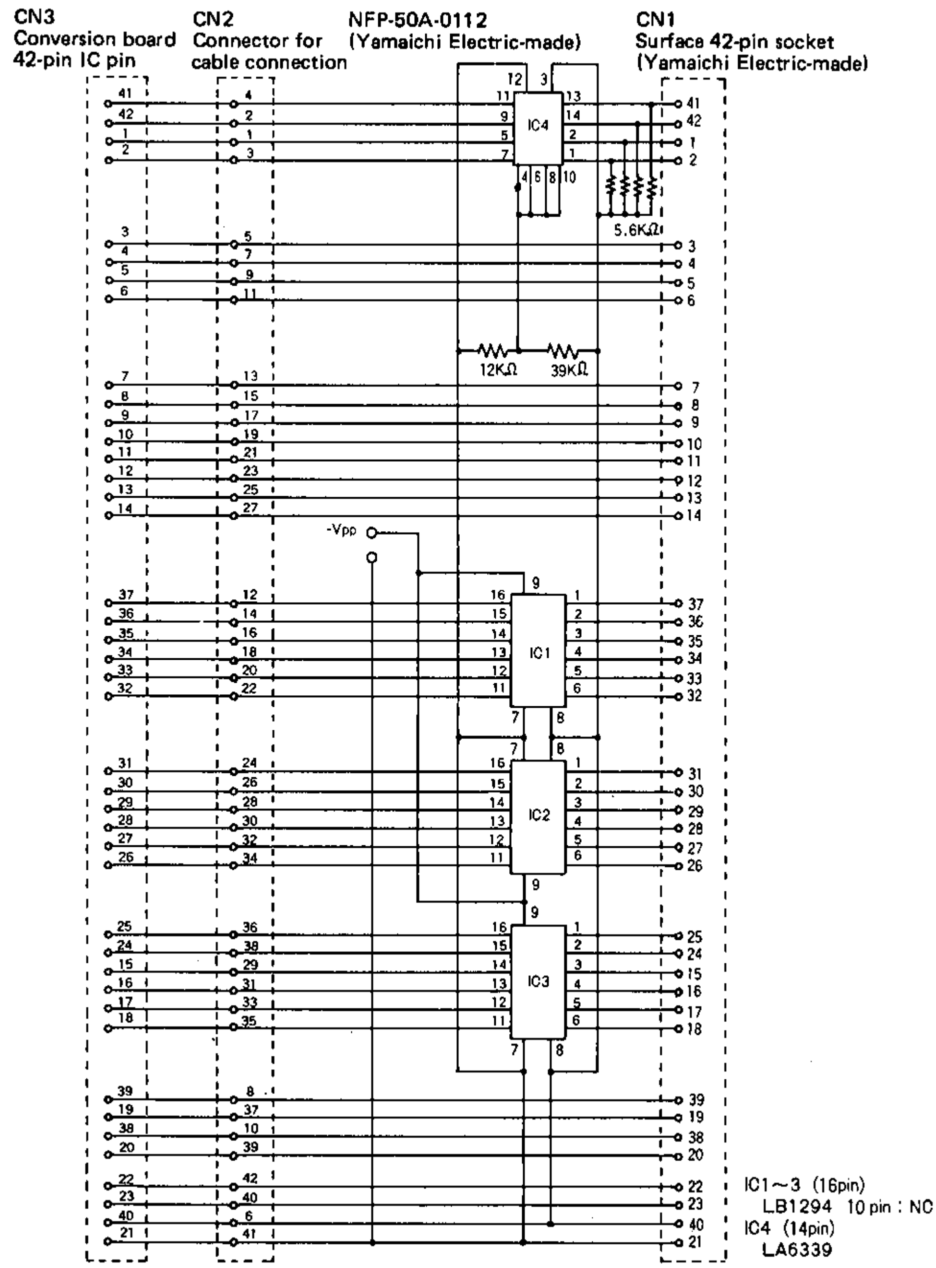


Fig. 1-4 EVA-97-12D/13D

Appendix 2. Internal Architecture of LC6512A, 6513A

The LC6512A, 6513A are identical with the LC6502C, 6505C in the internal architecture and instruction set except that output ports are of high-voltage type and port A is of low-threshold input type and the standby function is the same as for the LC6514B. For details, refer to "LC6500 SERIES USER'S MANUAL"; and for the standby function, refer to Appendix 4 "Standby Function".

2-1. PC

For the LC6512A, 6513A, this is organized with a 11-bit, 10-bit binary counter, respectively, which specifies the ROM address of an instruction to be executed next. The high-order 3(2) bits specify a page and the low-order 8 bits specify an address in the page. The page is updated automatically. ( ) is for the LC6513A.

2-2. ROM

This is used to store user programs. For the LC6512A, 6513A, this is organized with 2048 x 8 bits, 1024 x 8 bits, respectively. By using the ROM table read instruction, the whole area can be accessed and the display pattern can be programmed.

2-3. Stack

This is used to save the contents of the PC at the subroutine call or interrupt mode. This allows subroutine nesting up to 8 levels.

2-4. DP

This is a register organized with 4-bit DPL and 3-bit, 2-bit DPH for the LC6512A, 6513A, respectively. When accessing the data RAM, the DPL, DPH specify a column address, row address, respectively. When accessing input/output ports, the DPL specifies port A to port I. The DPL also specifies internal pseudo port O.

2-5. RAM

This is a static RAM used to store data. For the LC6512A, 6513A, this is organized with 128 x 4 bits, 64 x 4 bits, respectively. Row address 7H(3H) is allocated for 16 flags and 8 working registers which can be manipulated without being addressed by the DP. ( ) is for the LC6513A.

2-6. AC, E

The AC is a 4-bit register which stores data to be processed by instructions. The E register is an auxiliary register to be back up the AC and is used as a temporary register or general-purpose register at the instruction execution mode.

2-7. ALU

This is a circuit which performs arithmetic and logic operations specified by individual instructions. This outputs not only data of operation results but also the status of carry (C), zero (Z).

2-8. Status register

This is a 4-bit register which stores the status of carry, zero and the external interrupt, timer interrupt request. The contents of the status register can be tested by the branch instructions.

2-9. Timer

This consists of a 4-bit fixed prescaler and a 8-bit programmable timer. This counts the system clock and requests a timer interrupt when an overflow occurs.

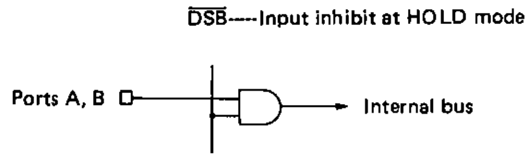
2-10. Control register

This is a 4-bit register, 2-bits of which control input/output of input/output common ports C, D and 2-bits of which enable/disable external interrupt, internal timer interrupt.

2-11. Input/output ports

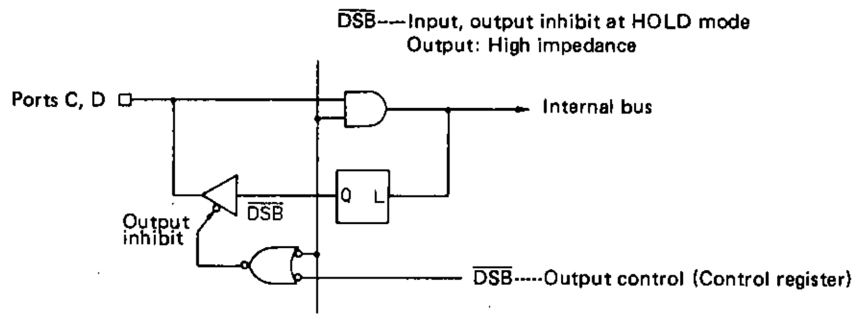
There are 9 ports/34 pins from port A to I. Each port is addressed by the DPL. Ports A, B are of normal-voltage input type, ports C, D are of normal-voltage input/output common type, and ports E, F, G, H, I contain FLT drivers. Port A is of low-threshold input type.

(1) Ports A_0 to 3, B_0 to 3



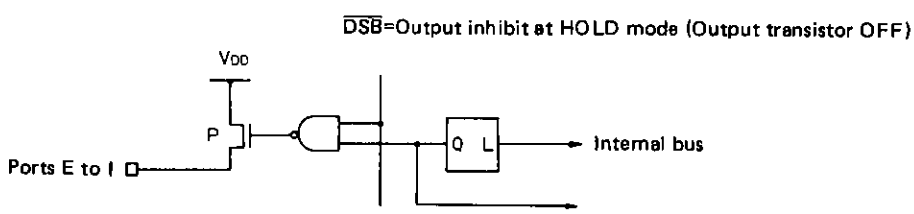
Functions
- 4-bit input (IP instruction)
- Single-bit test (BP, BNP instructions)
- Port A: Low-threshold input
- Port B: Normal-threshold input

(2) Ports C_0 to 3, D_0 to 3



Functions
1. Input mode (Output inhibit)
   - 4-bit input (IP instruction)
   - Single-bit test (BP, BNP instructions)
2. Output mode
   - 4-bit output (OP instruction)
   - Single-bit set, reset (SPB, RPB instructions)

(3) Ports E_0 to 3, F_0 to 3, G_0 to 3, H_0 to 3, I_0 to 1 (High-voltage ports)



Functions
- 4-bit (2-bit for port I) output (OP instruction)
- 4-bit (2-bit for port I) input of output latch contents (IP instruction)
- Single-bit set, reset (SPB, RPB instructions)
  Set: The output represents a 1. ----- Output transistor ON
  Reset: The output represents a 0. ----- Output transistor OFF
- Single-bit test of output latch contents (BP, BNP instructions)
- Ports E, F, I: FLT digits drive
- Ports G, H: FLT segments drive

2-12. External interrupt

The trailing edge of the signal on the $\overline{INT}$ pin is detected and the interrupt request flag in the status register is set. The occurrence of an interrupt is controlled by the enable/disable flag in the control register.

2-13. Reset

The system is initialized by setting the $\overline{RES}$ pin to "L" level. The contents to be initialized are as follows:

- PC — Address 000H
- Control register — 0000 → Interrupt disable, Ports C, D: Output inhibit
- Status register — Timer, external interrupt flag → Reset
- Output port — Output latch (0_H) → Output transistor OFF

Appendix 3. Proper Cares in Using LSI

3-1. Low-threshold input port A_0 to $_3$ provides the input characteristic shown in Fig. 3-1.

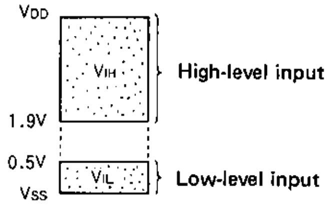


Fig. 3-1

3-2. FLT driver output

Ports E_0 to $_3$, F_0 to $_3$, I_0 to $_1$ (10 pins) are for high-current digits driver output; and ports G_0 to $_3$, H_0 to $_3$ (8 pins) are for intermediate-current segments driver outputs. Of course, digits driver outputs can be used as segments driver outputs. Fig. 3-2 shows a sample application.

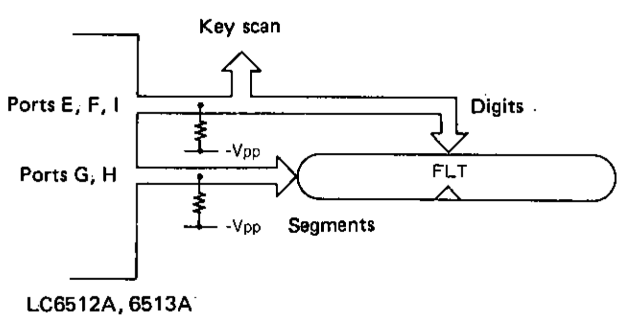


Fig. 3-2 FLT display application

Digit drive signal-used key scan

When key-scanning with the FLT digit drive signal in Fig. 3-3 and inputting the return signal to port A, the following must be observed.

(a) Estimate voltage drop (V_{ON}) in the output transistor using the current flowing in an FLT used and the V-I characteristic of the output port of the LC6512A, 6513A.

(b) Estimate voltage drop (V_{SW}) in the switch circuit.

(c) Check to see that V_{ON} + V_{SW} meets the V_{IH}/V_{IL} requirement of the input port in Fig. 3-1.

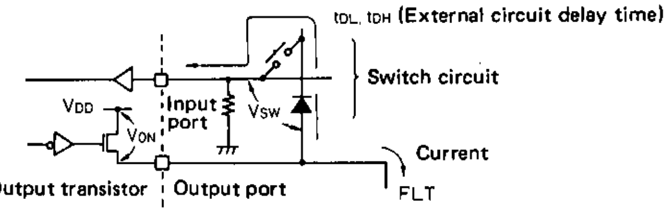


Fig. 3-3 Sample key scan application

For the key scan application in Fig. 3-3, make the program considering the delay in the external circuit and the input delay shown below.

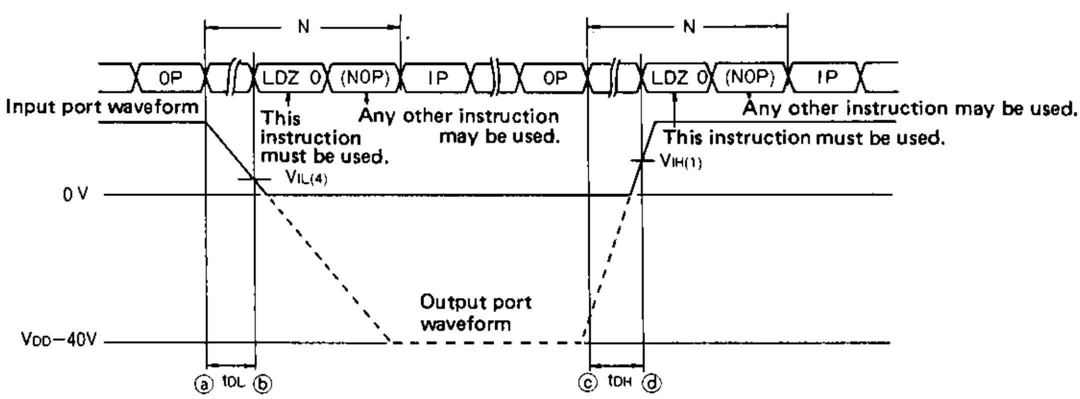


Fig. 3-4

When the IP instruction is used to input the return signal as shown above, the input delay must be considered and two instructions are placed between the IP instruction and the crossing of input port waveform and $V_{IL(4)}$, $V_{IH(1)}$, respectively. Some instructions must be placed additionally according to the length of delay (t_{DL}, t_{DH}) in the external circuit after the digit drive signal is delivered with the execution of the OP instruction (point a and point c).

N: Number of instruction cycles existing between instruction (OP, SPB, RPB) used to output data to output port and instruction (IP, BP, BNP) used to input data from input port.
(Number of instruction cycles to be programmed according to the length of t_{DL}, t_{DH})

t_{DL}, t_{DH}: Delay in external circuit from output port to input port.

Appendix 4. Standby Function

Two standby modes – HALT mode and HOLD mode – are available to minimize the power dissipation when the program is in the wait state or a power failure is backed up. Both modes are set with the execution of the HALT instruction. All the operations including the system clock generator are stopped at the standby mode. (For other models LC6502/05 of the LC6500 series, the HOLD mode is hardware-set with the $\overline{HOLD}$ pin = "L". Be careful of the difference in the mode setting method.)

The HALT mode and HOLD mode are used properly depending on the purposes. They are different in the mode setting conditions, I/O port state during standby operation, mode releasing method. The HALT mode is entered by executing the HALT instruction when the $\overline{HOLD}$ pin is at "H" level. The HALT mode is used to save the power dissipation when the program is in the wait state. The HOLD mode is entered by executing the HALT instruction when the $\overline{HOLD}$ pin is at "L" level. At the HOLD mode all I/O ports are disabled and there is no power dissipation in the interfaces with external circuits, permitting capacitor or battery-used power supply backup during power failure.

4-1. HALT mode setting

The HALT mode is entered by executing the HALT instruction when the $\overline{HOLD}$ pin is at "H" level and all pins for port A_0 to A_3 are at "L" level. When even one of pins for port A_0 to A_3 is at "H" level, the HALT instruction is disregarded and becomes equal to the NOP instruction.

The HALT mode causes individual blocks to be placed in the following states.

(1) Operation is stopped

- All the operations including the system clock generator are stopped.

(2) I/O port

- The state immediately before setting the HALT mode is held.

(3) Blocks to be cleared/reset

- Timer .... State where all bits are set to "1" (max. time).
- Status flag ..... The EXTF, TMF are reset (interrupt disable). The CF, ZF contents are held. An interrupt request at the HALT mode is disregarded.

(4) Blocks to be held

- For the registers, data RAM, port output latch, PC (except those in (3), the contents immediately before setting the HALT mode are held.

4-2. HOLD mode setting

The HOLD mode is entered by executing the HALT instruction when the $\overline{HOLD}$ pin is at "L" level. In this case, the contents of port A_0 to A_3 remain unaffected.

The state in the HOLD mode is the same as that in the HALT mode, except the state of I/O port. The HOLD mode permits the undermentioned power-down mode to be entered.

I/O port

- Input ports A, B: Input inhibit
- Input/output port C, D: Input inhibit, output high impedance
- Output ports E to I: Output Pch transistor OFF
- $\overline{INT}$, $\overline{RES}$ pins: Input inhibit

For the output latch of the output port, the contents immediately before setting the HOLD mode are held.

4-3. HOLD power-down mode setting

The HOLD mode permits the supply voltage to be lowered and also the power dissipation to be reduced after mode setting. The HOLD mode can be used in the capacitor or battery-used backup operation during power failure.

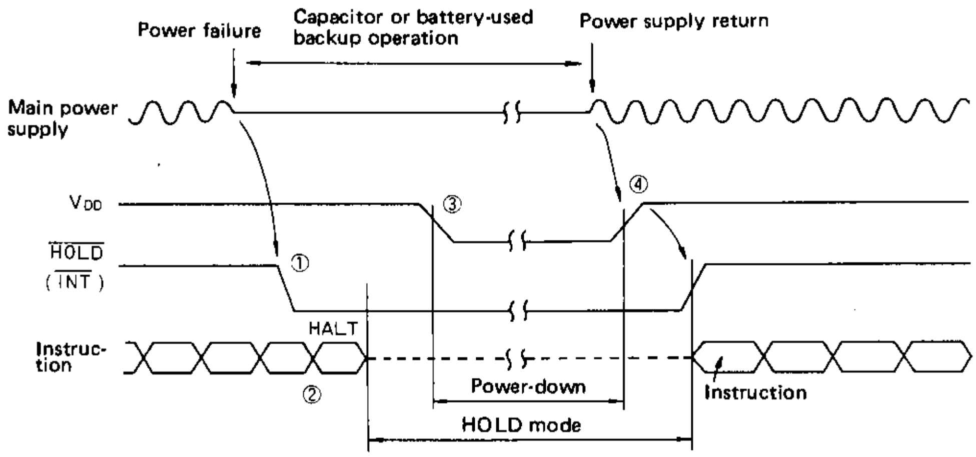


Fig. 4-1 HOLD mode and power-down

① A failure of the main power supply is detected and a standby request is made. This is hardware-controlled by the external circuit.
② The HOLD pin is software-polled or the same signal is applied to the INT pin to test the standby request by interrupt. Then, the HALT instruction is executed and the HOLD mode is entered. (Note)
③ After the HOLD mode is entered, power-down can be attained by lowering V_{DD}.
④ After V_{DD} returns to the prescribed voltage, the HOLD pin is set to "H" level and the normal operation returns.

(Note) The HOLD pin input signal is transferred to pseudo input port PO 0 (DPL = 0EH, 2^0 bit). Therefore, when polling the HOLD pin, the BP0 or BNP0 instruction is used at DPL = 0EH. (The IP instruction cannot be used.)
When the BP0 instruction is used for testing, a branch occurs when the input voltage is at high level in the same manner as for normal input ports.

4-4. HALT mode release

Release by reset
When "L" level is applied to the RES pin, the HALT mode is released and the system reset state is entered.
When the RES pin is set to "H" level again, the normal operation starts. Since the ceremic resonator mode is used for system clock generation, the release by reset must be performed.
– Notes –
- Since the ceramic resonator mode is used for system clock generation, "L" level must be applied to the RES pin for 5 to 10 msec (oscillation stabilizing time).

Mode change from HALT mode to HOLD Mode
The HALT mode is entered with the execution of the HALT instruction when the HOLD pin is at "H"level.
The HALT mode is changed to the HOLD mode automatically by setting the HOLD pin to "L" level.

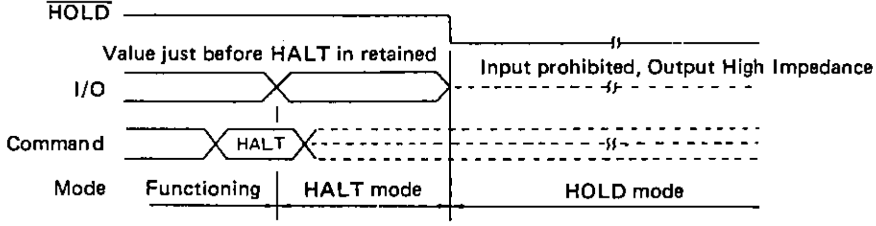


Fig. 4-2 Mode change from HALT mode to HOLD mode

4-5. HOLD mode release

Release by reset

The HOLD mode is released by setting the HOLD pin to "H" level while applying "L" level to the RES pin. When the RES pin is set to "H" level again, the normal operation starts. The contents of the memories remain unaffected except the PC, I/O ports, registers which are initialized by the reset operation.

Since the ceramic resonator mode is used, the reset state must be held until oscillation is fully stabilized (10 msec after oscillation start) after the HOLD mode is released.

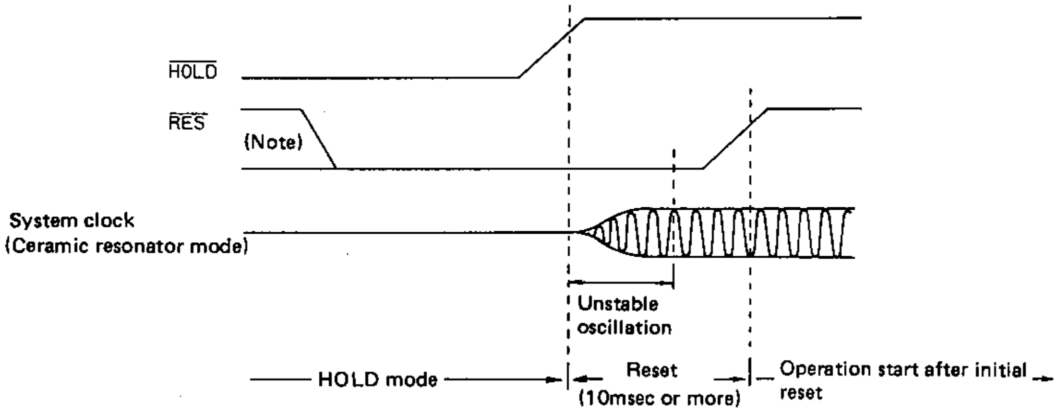


Fig. 4-3 HOLD mode release by reset

Note: With "L" level applied to the HOLD pin as shown above, the CPU is not reset even when the RES pin is set to "L" level. This is because the HOLD pin is given priority lest the CPU is reset unnecessarily when the capacitor or battery-used backup mode causes the CPU peripherals to operate unstably and the RES pin is set to "L" level. Be careful of the level of the HOLD pin and RES pin also at the initial reset mode when power is applied. When the HOLD pin is at "L" level, no reset occurs.

4-6. Proper cares in using standby function

When using the HOLD mode, an application circuit and program must be designed with the following in mind.

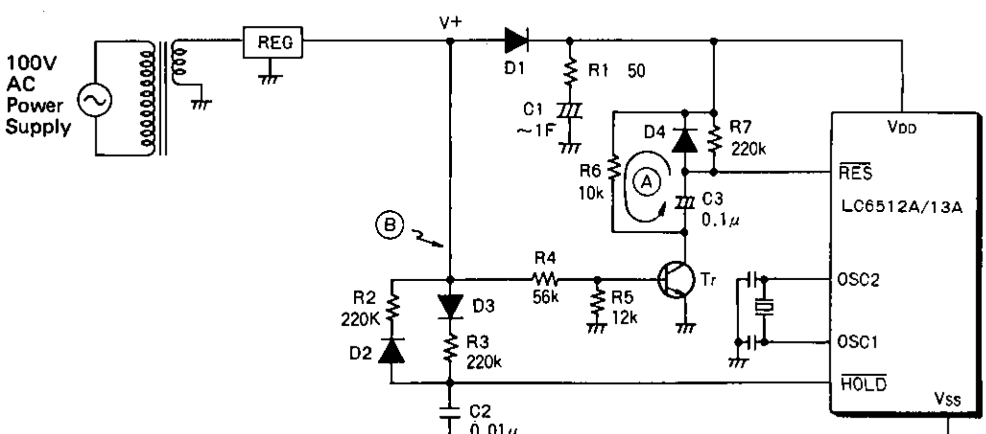
(1) The supply voltage at the standby state must not be less than specified.
(2) Input timing of each control signal (HOLD, RES, port A, INT, etc.) at the standby initiate/release state.
(3) Release operation must not be overlapped at the time of execution of the HALT instruction.

4-7. Sample application where the standby function is used for power failure backup

Power failure backup is an application where power failure of the main power source is detected by the HOLD pin, etc. to cause the HOLD mode to be entered so that the current dissipation is minimized and a backup capacitor is used to retain the contents of the internal registers even during power failure.

4-7-1. Sample application circuit (ceramic resonator OSC)

Fig. 4-4 shows a ceramic resonator OSC-applied circuit where the standby function is used for power failure backup.

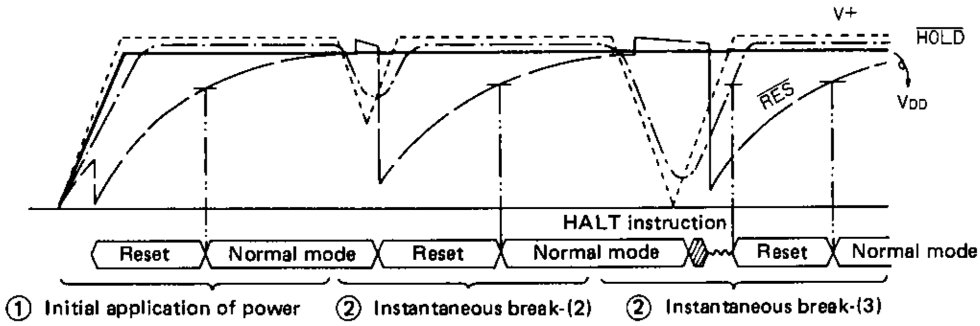


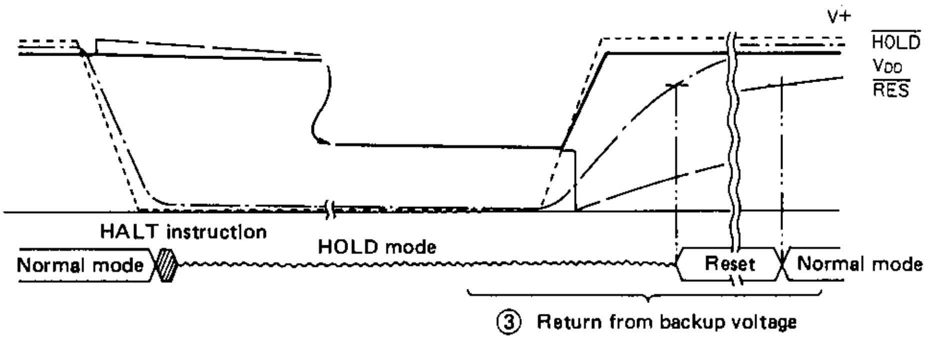
Unit (resistance: Ω, capacitance: F)

Fig. 4-4 Sample Application Circuit

4-7-2. Operating waveform

The operating waveform in the sample application circuit in Fig. 4-4 is shown below. The mode is roughly divided as follows:





4-7-3. Operation of sample application circuit

① At the time of initial application of power

A reset occurs and the execution of the program starts at address 000H of the program counter (PC).

② At the time of instantaneous break

(1) At the time of very short instantaneous break

The execution of the program continues.

(2) At the time of instantaneous break being a little longer than (1) (When the RES input voltage meets V_{IL} and the HOLD input voltage does not meet V_{IL}).

A reset occurs during the execution of the program and the execution of the program starts at address 000H of the program counter (PC).

Since the HOLD request signal is not applied to the HOLD pin, the HOLD mode is not entered.

(3) At the time of long instantaneous break (When both of the RES input voltage and HOLD input voltage meet V_{IL}).

The HOLD request signal is applied to the HOLD pin and the HOLD mode is entered.

When V+ rises after instantaneous break, a reset occurs to release the HOLD mode and the execution of the program starts at address 000H of the program counter (PC).

③ At the time of return from backup voltage

A reset occurs and the execution of the program starts at address 000H of the program counter (PC).

4-7-4. Notes for circuit design

① How to fix C3, R6, C2, R2
Fix closed loop (A) discharge time constants C3, R6 and $\overline{HOLD}$ pin charge time constants C2, R2 so that closed loop (A) fully discharges before the $\overline{HOLD}$ input voltage gets lower than V_{IL} at the time of instantaneous break and the $\overline{RES}$ input voltage is sure to get lower than V_{IL} (a reset occurs) when V+ rises after instantaneous break where the $\overline{HOLD}$ input voltage gets lower than V_{IL}.

② How to fix C3, R7
Fix $\overline{RES}$ pin charge time constants C3, R7 so that when power is applied initially or the HOLD mode is released the ceramic resonator OSC oscillates normally and the $\overline{RES}$ input voltage exceeds V_{IH} and the program starts running.

③ How to fix R4, R5
Fix Tr bias constants R4, R5 so that when V+ rises after instantaneous break the $\overline{RES}$ input voltage gets lower than V_{IL} (brought to "L" level) before the $\overline{HOLD}$ input voltage exceeds V_{IH} (brought to "H" level).

④ How to fix C2, R3
Fix $\overline{HOLD}$ pin charge time constants C2, R3 so that when the $\overline{HOLD}$ mode is released from the backup mode the $\overline{HOLD}$ input voltage does not exceed V_{OH} (not brought to "H" level) until the $\overline{RES}$ input voltage gets lower than V_{IL} (brought to "L" level).
Fix C3, R7 and C2, R3 so that the time interval from the moment the $\overline{HOLD}$ input voltage exceeds V_{IH} until the moment the $\overline{RES}$ input voltage exceeds V_{IH} is longer than the ceremic resonator OSC stabilizing time.

⑤ When the load is heavy or the polling interval is long
Since C1 discharges largely, increase the capacity of C1 or separate (B) detection from V+ and use a power supply or signal that rises faster than V+.

4-7-5. Notes for software design

When the HOLD request signal is detected, the HALT instruction is executed immediately. A concrete example is shown below.

(1) An interrupt is inhibited before polling the HOLD request pin ($\overline{HOLD}$ pin).
(2) Polling of the $\overline{HOLD}$ pin and the HALT instruction are programmed consecutively.

[Concrete example]

```
      :
    RCTL     3       ;EXTEN, TMEN ←0 (External, timer interrupt inhibit)
    BP0      AAA     ;Polling of the HOLD pin (If "H" level, a branch occurs to AAA.)
    HALT             ;The HOLD mode is entered.
      :
      :
 AAA:
```

Appendix   LC6500 Series Instruction Set (by Function)

Symbols	Meaning
AC:	Accumulator
ACt:	Accumulator bit t
CF:	Carry flag
CTL:	Control register
DP:	Data pointer
E:	E register
EXTF:	External interrupt request flag
Fn:	Flag bit n
M:	Memory
M(DP):	Memory addressed by DP
$P(DP_L)$:	Input/output port addressed by DP_L
PC:	Program counter
STACK:	Stack register
TM:	Timer
TMF:	Timer (internal) interrupt request flag
At, Ha, La:	Working register
ZF:	Zero flag
( ), [ ]:	Contents
←:	Transfer and direction
+:	Addition
−:	Subtraction
∧:	AND
∨:	OR
⊻:	Exclusive OR

Instruction	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	*1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF is reset.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $\overline{(AC)}$	The AC contents are complemented (zero bits become 1, one bits become 0).	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) − 1	The AC contents are decremented −1.	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0 ← (CF), AC_{n+1} ← (AC_n), CF ← (AC_3)	The AC contents are shifted left through the CF.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ⇆ (E)	The AC contents and the E contents are exchanged.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← [M(DP)] + 1	The M(DP) contents are incremented +1.	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← [M(DP)] − 1	The M(DP) contents are decremented −1.	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B_1B_0	1	1	M(DP, B_1B_0) ← 1	A single bit of the M(DP) specified by B_1B_0 is set.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B_1B_0	1	1	M(DP, B_1B_0) ← 0	A single bit of the M(DP) specified by B_1B_0 is reset.	ZF	
Operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)]	The AC contents and the M(DP) contents are binary-added and the result is placed in the AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)] + (CF)	The AC, CF, M(DP) contents are binary-added and the result is placed in the AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ⊻ [M(DP)]	The AC contents and the M(DP) contents are exelusive-ORed and the result is placed in the AC.	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ [M(DP)]	The AC contents and the M(DP) contents are ANDed and the result is placed in the AC.	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ [M(DP)]	The AC contents and the M(DP) contents are ORed and the result is placed in the AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	$\overline{[M(DP)]}$ + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset. Comparison result / CF / ZF [M(DP)] > (AC) / 0 / 0 [M(DP)] = (AC) / 1 / 1 [M(DP)] < (AC) / 1 / 0	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 $I_3I_2I_1I_0$	2	2	$\overline{I_3I_2I_1I_0}$ + (AC) + 1	The AC contents and immediate data $I_3I_2I_1I_0$ are compared and the ZF and CF are set/reset. Comparison result / CF / ZF $I_3I_2I_1I_0$ > (AC) / 0 / 0 $I_3I_2I_1I_0$ = (AC) / 1 / 1 $I_3I_2I_1I_0$ < (AC) / 1 / 0	ZF CF	
	CLI data	Compare DP_L with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 $I_3I_2I_1I_0$	2	2	(DP_L) ⊻ $I_3I_2I_1I_0$	The DP_L contents and immediate data $I_3I_2I_1I_0$ are compared.	ZF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	$I_3I_2I_1I_0$	1	1	AC ← $I_3I_2I_1I_0$	Immediate data $I_3I_2I_1I_0$ is loaded in the AC.	ZF	*1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← [M(DP)]	The M(DP) contents are loaded in the AC.	ZF	
	XM data	Exchange AC with M, then modify DP_H with immediate data	1 0 1 0	0 $M_2M_1M_0$	1	2	(AC) ⇆ [M(DP)] DP_H ← (DP_H) ⊻ $0M_2M_1M_0$	The AC contents and the M(DP) contents are exchanged. Then, the DP_H contents are modified with the contents of (DP_H) ⊻ $0M_2M_1M_0$.	ZF	The ZF is set/reset according to the result of (DP_H) ⊻ $0M_2M_1M_0$.
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ⇆ [M(DP)]	The AC contents and the M(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP_H contents at the time of instruction execution.
	XI	Exchange AC with M, then increment DP_L	1 1 1 1	1 1 1 0	1	2	(AC) ⇆ [M(DP)] DP_L ← (DP_L) + 1	The AC contents and the M(DP) contents are exchanged. Then, the DP_L contents are incremented +1.	ZF	The ZF is set/reset according to the result of $(DP_L + 1)$.
	XD	Exchange AC with M, then decrement DP_L	1 1 1 1	1 1 1 1	1	2	(AC) ⇆ [M(DP)] DP_L ← (DP_L) − 1	The AC contents and the M(DP) contents are exchanged. Then, the DP_L contents are decremented −1.	ZF	The ZF is set/reset according to the result of $(DP_L - 1)$.
	RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC E ← ROM (PCh, E, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.		

Instruction	Mnemonic		Instruction code $D_7 D_6 D_5 D_4$	Instruction code $D_3 D_2 D_1 D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1 0 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3 I_2 I_1 I_0$	The DP_H and DP_L are loaded with 0 and immediate data $I_3I_2I_1I_0$ respectively.		
	LHI data	Load DP_H with immediate data	0 1 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow I_3 I_2 I_1 I_0$	The DP_H is loaded with immediate data $I_3I_2I_1I_0$.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	$DP_L \leftarrow (DP_L)+1$	The DP_L contents are incremented +1.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	$DP_L \leftarrow (DP_L)-1$	The DP_L contents are decremented −1.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	$DP_L \leftarrow (AC)$	The AC contents are transferred to the DP_L.		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	$AC \leftarrow (DP_L)$	The DP_L contents are transferred to the AC.	ZF	
	XAH	Exchange AC with DP_H	0 0 1 0	0 0 1 1	1	1	$(AC) \leftrightarrows (DP_H)$	The AC contents and the DP_H contents are exchanged.		
Working register manipulation instructions	XAt XA0 XA1 XA2 XA3	Exchange AC with working register At	 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0	$t_1 t_0$ 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 0	 1 1 1 1	 1 1 1 1	 $(AC) \leftrightarrows (A0)$ $(AC) \leftrightarrows (A1)$ $(AC) \leftrightarrows (A2)$ $(AC) \leftrightarrows (A3)$	The AC contents and the contents of working register A0, A1, A2, or A3 specified by t_1t_0 are exchanged.		
	XHa XH0 XH1	Exchange DP_H with working register Ha	 1 1 1 1 1 1 1 1	a 1 0 0 0 1 1 0 0	 1 1	 1 1	 $(DP_H) \leftrightarrows (H0)$ $(DP_H) \leftrightarrows (H1)$	The DP_H contents and the contents of working register H0 or H1 specified by a are exchanged.		
	XLa XL0 XL1	Exchange DP_L with working register La	 1 1 1 1 1 1 1 1	a 0 0 0 0 0 1 0 0	 1 1	 1 1	 $(DP_L) \leftrightarrows (L0)$ $(DP_L) \leftrightarrows (L1)$	The DP_L contents and the contents of working register L0 or L1 specified by a are exchanged.		
Flag manipulation instructions	SFB flag	Set flag bit	0 1 0 1	$B_3 B_2 B_1 B_0$	1	1	$Fn \leftarrow 1$	A flag specified by $B_3B_2B_1B_0$ is set.		
	RFB flag	Reset flag bit	0 0 0 1	$B_3 B_2 B_1 B_0$	1	1	$Fn \leftarrow 0$	A flag specified by $B_3B_2B_1B_0$ is reset.	ZF	The flags are divided into 4 groups of F0 to F3, F4 to F7, F8 to F11, F12 to F15. The ZF is set/reset according to the 4 bits including a single bit specified by immediate data $B_3B_2B_1B_0$.
Jump/subroutine instructions	JMP addr	Jump in the current bank	0 1 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	$PC \leftarrow PC_{11}$ (又は $\overline{PC_{11}}$) $P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$	A jump to an address specified by the PC_{11} (or $\overline{PC_{11}}$) and immediate data P_{10} to P_0 occurs.		
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	$PC_{7\sim0} \leftarrow (E, AC)$	A jump to an address specified by the contents of the PC whose low-order 8 bits are replaced with the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	$P_3 P_2 P_1 P_0$	1	1	$STACK \leftarrow (PC)+1$ $PC_{11\sim6}, PC_{1\sim0} \leftarrow 0$ $PC_{5\sim2} \leftarrow P_3P_2P_1P_0$	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	$STACK \leftarrow (PC)+2$ $PC_{11\sim0} \leftarrow 0P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$	A subtoutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$ $CF, ZF \leftarrow CSF, ZSF$	A return from an interrupt servicing routine occurs.	ZF CF	
Branch instructions	BAt addr	Branch on AC bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if $AC_t = 1$	If a single bit of the AC specified by immediate data t_1t_0 is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if $AC_t = 0$	If a single bit of the AC specified by immediate data t_1t_0 is 0 a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMt addr	Branch on M bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if $(M(DP, t_1t_0)) = 1$	If a single bit of the M(DP) specified by immediate data t_1t_0 is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if $(M(DP, t_1t_0)) = 0$	If a single bit of the M(DP) specified by immediate data t_1t_0 is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if $(P(DP_L, t_1t_0)) = 1$	If a single bit of port $P(DP_L)$ specified by immediate data t_1t_0 is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNPt addr	Branch on no Port bit	0 0 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if $(P(DP_L, t_1t_0)) = 0$	If a single bit of port $P(DP_L)$ specified by immediate data t_1t_0 is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 0 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if $TMF = 1$ then $TMF \leftarrow 0$	If the TMF is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs. The TMF is reset.	TMF	

Instruction	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Branch instructions	BNTM addr	Branch on no timer	0 0 1 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs. The TMF is reset.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs. The EXTF is reset.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs. The EXTF is reset.	EXTF	
	BC addr	Branch on CF	0 1 1 1 $P_7P_6P_5P_4$	1 1 1 1 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if CF = 1	If the CF is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 $P_7P_6P_5P_4$	1 1 1 1 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if CF = 0	If the CF is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 $P_7P_6P_5P_4$	1 1 1 0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \sim P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if ZF = 1	If the ZF is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 $P_7P_6P_5P_4$	1 1 1 0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if ZF = 0	If the ZF is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		
	BFn addr	Branch on flag bit	1 1 0 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if Fn = 1	If a flag bit of the 16 flags specified by immediate data $n_3n_2n_1n_0$ is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BF0 to BF15 according to the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if Fn = 0	If a flag bit of the 16 flags specified by immediate data $n_3n_2n_1n_0$ is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BNF0 to BNF 15 according to the value of n.
Input/output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← [P(DP$_L$)]	The contents of port P(DP$_L$) are inputted to the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DP$_L$) ← (AC)	The AC contents are outputted to port P(DP$_L$)		
	SPB bit	Set port bit	0 0 0 0	0 1 B_1 B_0	1	2	P(DP$_L$, B_1B_0) ← 1	Immediate data B_1B_0-specified one bit in port P(DP$_L$) is set.		Mnemonic is BNF0 to BNF 15 according to the value of n.
	RPB bit	Reset port bit	0 0 1 0	0 1 B_1 B_0	1	2	P(DP$_L$, B_1B_0) ← 0	Immediate data B_1B_0-specified one bit in port P (DP$_L$) is reset.	ZF	When this instruction is executed, the E register contents are destroyed.
Other instructions	SCTL bit	Set control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 $B_3B_2B_1B_0$	2	2	CTL ← (CTL) V $B_3B_2B_1B_0$	Immediate data $B_3B_2B_1B_0$-specified bits in the control register are set.		
	RCTL bit	Reset control register bit(S)	0 0 1 0 1 0 0 1	1 1 0 0 $B_3B_2B_1B_0$	2	2	CTL ← (CTL) Λ $\overline{B_3B_2B_1B_0}$	Immediate data $B_3B_2B_1B_0$-specified bits in the control register are reset.	ZF	
	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	TM ← (E), (AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

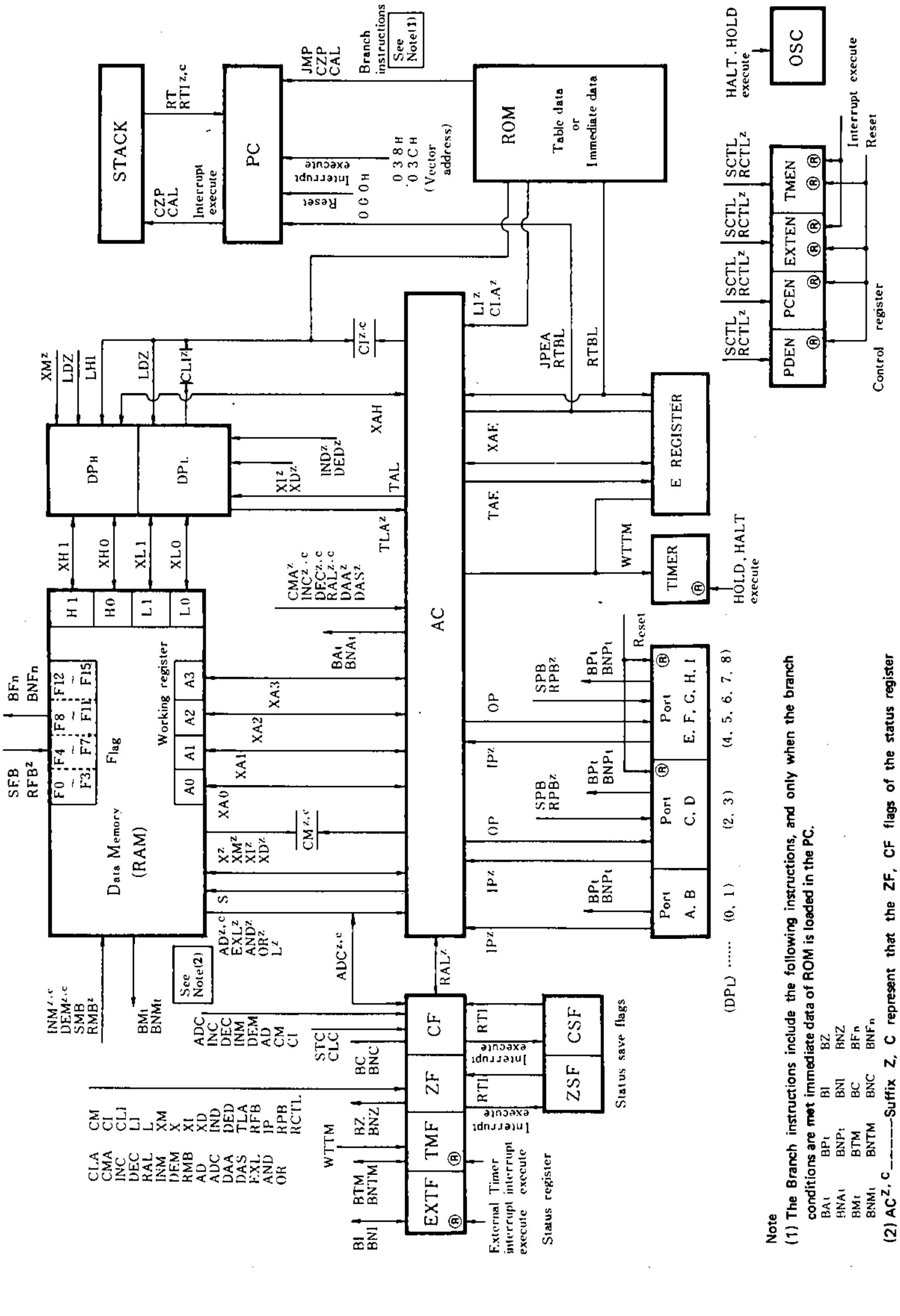
*1 If the LI instruction or CLA instruction is used consecutively in such a manner as LI, LI, LI, -----, or CLA, CLA, CLA, ------, the first LI instruction or CLA instruction only is effective and the following LI instructions or CLA instructions are changed to the NOP instructions.

LC6500 Series Instruction Map

	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1st byte	0	NOP	RAL	S	TAE	SPB				SMB				IP	XAE	INC	DEC
	1	RFB															
	2	ADC	L	RTI	XAH	RPB				RMB				RCTL, CLI SCTL, CI		INM	DEM
	3	BNA_t				BNM_t				BNP_t				BNTM	BNI	BNZ	BNC
	4	LHI															
	5	SFB															
	6	AD	OP	RT	RTBL					JMP							
	7	BA_t				BM_t				BP_t				BTM	BI	BZ	BC
	8	LDZ															
	9	BNF_n															
	A	X	XM							CAL							
	B	CZP															
	C	CLA	LI														
	D	BF_n															
	E	XA0	CLC			XA1	OR	DAA	AND	XA2	TLA	DAS	CMA	XA3		IND	DED
	F	XL0	STC			XL1	EXL	HALT	TAL	XH0	WTTM	JPEA	CM	XH1		XI	XD
2nd byte	4	CI															
	5	CLI															
	8	SCTL															
	9	RCTL															

1-cycle instruction
1-byte, 2-cycle instruction
2-byte instruction

LC6500 Series Programming Model



Note

(1) The Branch instructions include the following instructions, and only when the branch conditions are met immediate data of ROM is loaded in the PC.

BAt	BPt	BI	BZ
BNAt	BNPt	BNI	BNZ
BMt	BTM	BC	BFn
BNMt	BNTM	BNC	BNFn

(2) $AC^{Z,C}$———Suffix Z, C represent that the ZF, CF flags of the status register are affected.