

Ordering number: EN2076D

|  |                                       |          |
|--|---------------------------------------|----------|
| <b>SANYO</b>   | No. 2076D                             | CMOS LSI |
|  | <b>LC6520C, 6522C, LC6520H, 6522H</b> |          |
| Single-Chip 4-Bit Microcomputers for<br>Medium/Large-Scale Control-Oriented Applications |                                       |          |

The LC6520C/H are single-chip 4-bit microcomputers that contain a 4K-byte ROM, 1K-bit RAM, have 42 pins, and are fabricated using CMOS process technology. Besides 8 input/output common ports of 32 pins and an input port of 4 pins, the LC6520C/H have specific ports that are used to provide the interrupt function, 4-bit/8-bit serial input/output function, and burst pulse output function. All output ports are of the open drain type with a withstand voltage of 15 V and a drive current of 20 mA and have the option of containing a pull-up resistance bitwise.

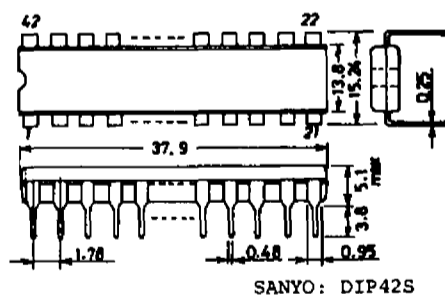
The LC6520C/H are the same as our LC6500 series in the basic architecture of the CPU and the instruction set, but are made more powerful in the stack level and the cycle time.

The LC6522C/H are the same as the LC6520C/H, except that they contain a 2k-byte ROM, 512-bit RAM.

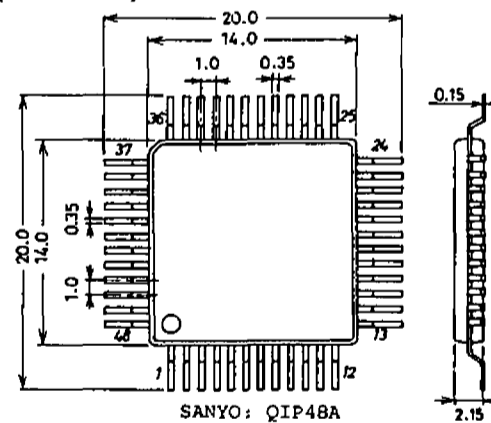
#### Features

- Instruction set with 80 instructions (Common to the LC6500 series)
- ROM/RAM
  - : 4096 bytes/1024 bits (LC6520C/H)
  - : 2048 bytes/512 bits (LC6522C/H)
- Instruction cycle time: 6  $\mu$ s (C version,  $V_{DD} = 3$  to 5.5V)  
2.77  $\mu$ s (C version,  $V_{DD} = 4$  to 5.5V)  
9.92  $\mu$ s (H version,  $V_{DD} = 4.5$  to 5.5V)
- Serial input/output interface x 1 (4 bits/8 bits program-selectable)
- I/O ports
  - Input port: 4 pins
  - Input/output common ports: 32 pins
  - Input/output withstand voltage: 15 V max (all input/output ports)
  - Output current: 20 mA max (all output ports)
  - Pull-up resistance: May be contained bitwise by option. (All output ports)
  - Output level during reset: For ports C, D, output (H or L) during reset may be specified portwise by option.

Package Dimensions 3025B-D42SIC  
(unit: mm)



Package Dimensions 3052A-Q48AIC  
(unit: mm)



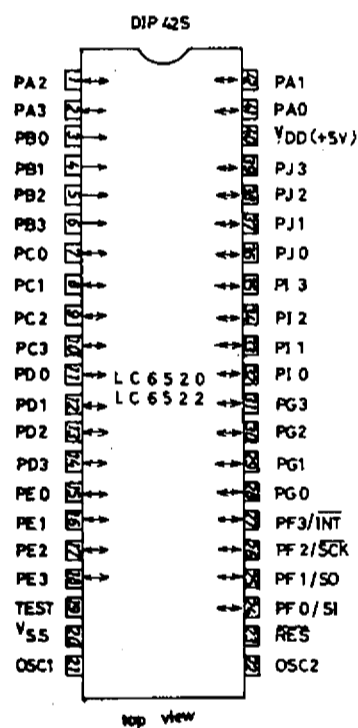
**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**  
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

5202HK / 4209TA / 7137KI / 4176KI, TS No.2076-1/29

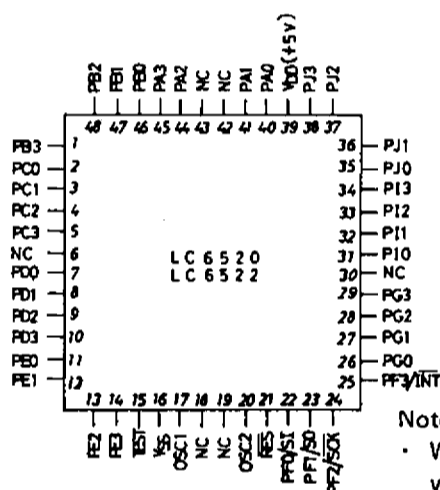
LC6520C,6520H,6522C,6522H

- Interrupt function
  - Timer interrupt: 1
  - $\overline{\text{INT}}$  pin or serial I/O interrupt: 1
- Stack level: 8 levels (common with interrupt)
- Timer: 4-bit prescaler + 8-bit programmable timer
- Burst pulse (64 x cycle time, duty 50%) output function
- Oscillator option
  - Circuit mode: Ceramic mode, RC mode, external clock mode (200 kHz to 4.2 MHz)
  - (Xtal OSC constants are being checked.)
  - Predivider option: 1/1, 1/3, 1/4
- Standby function: Standby function provided by the HALT instruction
- Supply Voltage: 3 to 5.5 V (C version)  
4.5 to 5.5 V (H version)
- Package: DIP42 shrink type, QIP48

Pin Assignment



QIP48



Note)

- When mounting the QIP version on the board, do not dip it in solder.
- Nothing must be connected to NC pin.

Pin Name

- OSC1, OSC2: RC, ceramic resonator, or X'tal for OSC
- $\overline{\text{INT}}$ : Interrupt
- RES: Reset
- PA0-3: Input/output common port
- PB0-3: Input port
- PC0-3: Input/output common port
- PD0-3: Input/output common port
- PE0-3: Input/output common port
- PF0-3: Input/output common port
- PG0-3: Input/output common port
- PI0-3: Input/output common port
- PJ0-3: Input/output common port
- SCK: Serial Input/output port
- SI: Serial Input/output port
- TEST: Test

LC6520C,6520H,6522C,6522H

Pin Description

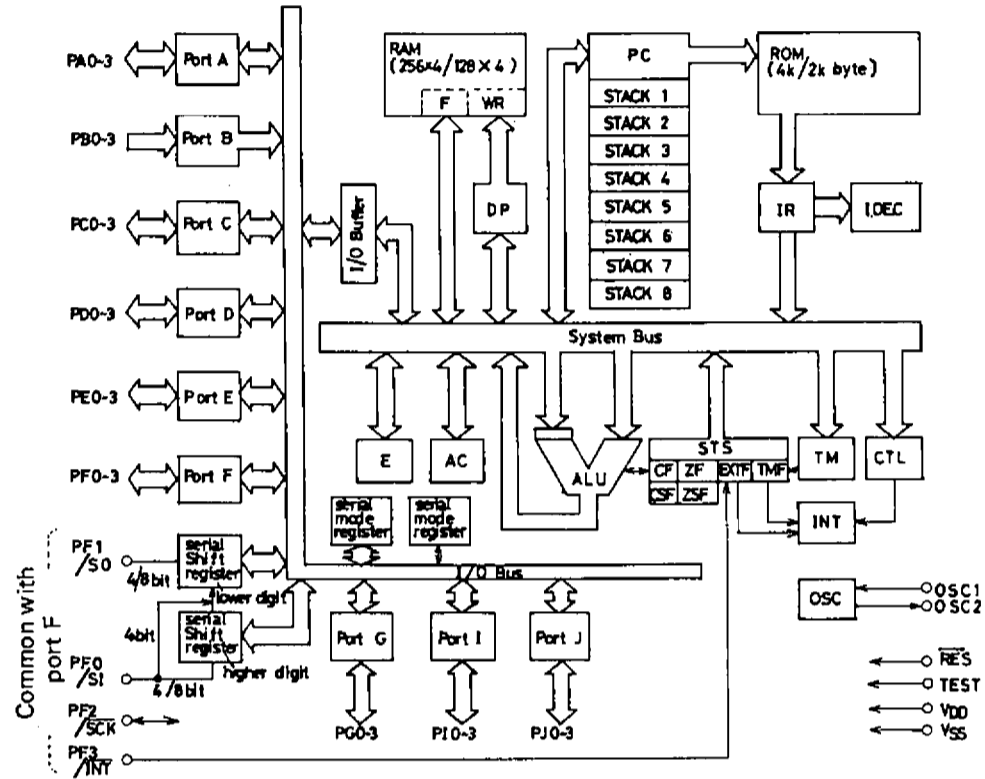
| Pin Name   | Pins   | I/O          | Functions   | Options  | During Reset   |
|--|--------|--------------|---|--|--|
| V <sub>DD</sub><br>V <sub>SS</sub>                                       | 1<br>1 |              | Power supply  |  |  |
| OSC1   | 1      | Input        | <ul style="list-style-type: none"> <li>Pin for externally connecting R, C or a ceramic resonator for system clock generation</li> </ul>   | <ol style="list-style-type: none"> <li>External clock input</li> <li>2-pin RC OSC</li> <li>2-pin ceramic resonator OSC</li> </ol>  |  |
| OSC2   | 1      | Output       | <ul style="list-style-type: none"> <li>For the external clock mode, the OSC2 pin is open.</li> </ul>  | <ol style="list-style-type: none"> <li>Predivider option                             <ol style="list-style-type: none"> <li>No. predivider</li> <li>1/3 predivider</li> <li>1/4 predivider</li> </ol> </li> </ol>  |  |
| PA <sub>0</sub><br>PA <sub>1</sub><br>PA <sub>2</sub><br>PA <sub>3</sub> | 4      | Input/output | <ul style="list-style-type: none"> <li>Input/output common port A<sub>0</sub> to 3.                             <ul style="list-style-type: none"> <li>4-bit input (IP instruction)</li> <li>4-bit output (OP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> <li>Single-bit set/reset (SPB, RPB instructions)</li> </ul> </li> <li>Standby is controlled by the PA<sub>3</sub> (or PA<sub>0</sub> to 3).</li> <li>The PA<sub>3</sub> (or PA<sub>0</sub> to 3) pin must be free from chattering during the HALT instruction execution cycle.</li> </ul> | <ol style="list-style-type: none"> <li>Open drain type output</li> <li>With pull-up resistance</li> </ol> (1), (2): Specified bit by bit.  | <ul style="list-style-type: none"> <li>"H" output (Output Nch transistor OFF)</li> </ul>             |
| PB <sub>0</sub><br>PB <sub>1</sub><br>PB <sub>2</sub><br>PB <sub>3</sub> | 4      | Input        | <ul style="list-style-type: none"> <li>Input Port B<sub>0</sub> to 3                             <ul style="list-style-type: none"> <li>4-bit input (IP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> </ul> </li> </ul>   |  |  |
| PC <sub>0</sub><br>PC <sub>1</sub><br>PC <sub>2</sub><br>PC <sub>3</sub> | 4      | Input/output | <ul style="list-style-type: none"> <li>Input/output common port C<sub>0</sub> to 3. The functions are the same as for the PA<sub>0</sub> to 3. (Note)</li> <li>Output ("H" or "L") during reset may be specified by option.</li> </ul> (Note) No standby control function is provided.  | <ol style="list-style-type: none"> <li>Open drain type output</li> <li>With pull-up resistance</li> <li>Output during reset: "H"</li> <li>Output during reset: "L"</li> </ol> <ul style="list-style-type: none"> <li>(1), (2): Specified bit by bit.</li> <li>(3), (4): Specified in a group of 4 bits.</li> </ul> | <ul style="list-style-type: none"> <li>"H" output</li> <li>"L" output (Option-selectable)</li> </ul> |
| PD <sub>0</sub><br>PD <sub>1</sub><br>PD <sub>2</sub><br>PD <sub>3</sub> | 4      | Input/output | <ul style="list-style-type: none"> <li>Input/output common port D<sub>0</sub> to 3</li> <li>The functions, options are the same as for the PC<sub>0</sub> to 3.</li> </ul>  | Same as for the PC <sub>0</sub> to 3.  | Same as for the PC <sub>0</sub> to 3.  |
| PE <sub>0</sub><br>PE <sub>1</sub><br>PE <sub>2</sub><br>PE <sub>3</sub> | 4      | Input/output | <ul style="list-style-type: none"> <li>Input/output common port E<sub>0</sub> to 3                             <ul style="list-style-type: none"> <li>4-bit input (IP instruction)</li> <li>4-bit output (OP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> <li>Single-bit set/reset (SPB, RPB instructions)</li> </ul> </li> <li>PE<sub>0</sub>: With burst pulse (64T<sub>cyc</sub>) output function</li> </ul>  | <ol style="list-style-type: none"> <li>Open drain type output</li> <li>With pull-up resistance</li> </ol> (1), (2): Specified bit by bit.  | <ul style="list-style-type: none"> <li>"H" output (Output Nch transistor OFF)</li> </ul>             |

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| Pin Name   | Pins | I/O          | Functions  | Options                               | During Reset   |
|--|------|--------------|--|---------------------------------------|--|
| PF <sub>0</sub> /SI<br>PF <sub>1</sub> /SO<br>PF <sub>2</sub> /SCK<br>PF <sub>3</sub> /INT | 4    | Input/output | <ul style="list-style-type: none"> <li>Input/output port F<sub>0</sub> to 3<br/>The functions, options are the same as for the PE<sub>0</sub> to 3. However, no burst pulse output function is provided.</li> <li>PF<sub>0</sub> to 3: Also used for serial interface, INT input. Program-selectable.<br/>4 bits/8 bits of serial input/output: Program-selectable<br/>SI: Serial input port<br/>SO: Serial output port<br/>SCK: Serial clock input/output<br/>INT: Interrupt request input</li> </ul> | Same as for the PE <sub>0</sub> to 3. | Same as for the PE <sub>0</sub> to 3.<br>Serial port:<br>Disable<br>Interrupt<br>source: INT |
| PG <sub>0</sub><br>PG <sub>1</sub><br>PG <sub>2</sub><br>PG <sub>3</sub>                   | 4    | Input/output | <ul style="list-style-type: none"> <li>Input/output common port G<sub>0</sub> to 3<br/>The functions, options are the same as for the PE<sub>0</sub> to 3. However, no burst pulse output function is provided.</li> </ul>   | Same as for the PE <sub>0</sub> to 3. | Same as for the PE <sub>0</sub> to 3.  |
| PI <sub>0</sub><br>PI <sub>1</sub><br>PI <sub>2</sub><br>PI <sub>3</sub>                   | 4    | Input/output | <ul style="list-style-type: none"> <li>Input/output common port I<sub>0</sub> to 3<br/>The functions, options are the same as for the PG<sub>0</sub> to 3.</li> </ul>  | Same as for the PG <sub>0</sub> to 3. | Same as for the PG <sub>0</sub> to 3.  |
| PJ <sub>0</sub><br>PJ <sub>1</sub><br>PJ <sub>2</sub><br>PJ <sub>3</sub>                   | 4    | Input/output | <ul style="list-style-type: none"> <li>Input/output common port J<sub>0</sub> to 3<br/>The functions, options are the same as for the PG<sub>0</sub> to 3.</li> </ul>  | Same as for the PG <sub>0</sub> to 3. | Same as for the PG <sub>0</sub> to 3.  |
| RES  | 1    | Input        | <ul style="list-style-type: none"> <li>System reset input</li> <li>For power-up reset, C is connected externally.</li> <li>For reset start, "L" level is applied for 4 clock cycles or more.</li> </ul>  |                                       |  |
| TEST   | 1    | Input        | <ul style="list-style-type: none"> <li>LSI test pin<br/>Normally connected to V<sub>SS</sub></li> </ul>  |                                       |  |

System Block Diagram



- |      |                           |          |                                 |
|------|---------------------------|----------|---------------------------------|
| RAM: | Data memory               | ROM:     | Program memory                  |
| F:   | Flag                      | PC:      | Program counter                 |
| WR:  | Working register          | INT:     | Interrupt control               |
| AC:  | Accumulator               | IR:      | Instruction register            |
| ALU: | Arithmetic and logic unit | i.DEC:   | Instruction decoder             |
| DP:  | Data pointer              | CF, CSF: | Carry flag, carry save flag     |
| E:   | E register                | ZF, ZSF: | Zero flag, zero save flag       |
| CTL: | Control register          | EXTF:    | External interrupt request flag |
| OSC: | Oscillator                | TMF:     | Internal interrupt request flag |
| TM:  | Timer                     |          |                                 |
| STS: | Status register           |          |                                 |

**Oscillator Circuit Option**

| Option Name              | Circuit | Conditions, etc.  |
|--------------------------|---------|---|
| 1. External Clock        |         | <ul style="list-style-type: none"> <li>Input: Schmitt type</li> </ul> |
| 2. 2-pin RC OSC          |         | <ul style="list-style-type: none"> <li>Input: Schmitt type</li> </ul> |
| 3. Ceramic Resonator OSC |         |   |

• **Predivider Option**

| Option Name       | Circuit | Conditions, etc.   |
|-------------------|---------|--|
| 1. No predivider  |         | <ul style="list-style-type: none"> <li>Applicable to all of 3 OSC options.</li> <li>The OSC frequency, external clock do not exceed 1444 kHz. (LC6520C, LC6522C)</li> <li>The OSC frequency, external clock do not exceed 4330 kHz. (LC6520H, LC6522H)</li> <li>Refer to Table of OSC, Predivider Option (Table 2).</li> </ul> |
| 2. 1/3 predivider |         | <ul style="list-style-type: none"> <li>Applicable to only 2 options of external clock, ceramic resonator OSC.</li> <li>The OSC frequency, external clock do not exceed 4330 kHz.</li> <li>Refer to Table of OSC, Predivider Option (Table-2).</li> </ul>   |
| 3. 1/4 predivider |         | <ul style="list-style-type: none"> <li>Applicable to only 2 options of external clock, ceramic resonator OSC.</li> <li>The OSC frequency, external clock do not exceed 4330 kHz.</li> <li>Refer to table of OSC, Predivider Option (Table 2).</li> </ul>   |

**Options of Ports C, D Output Level during Reset**

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

| Option Name                       | Conditions, etc.            |
|-----------------------------------|-----------------------------|
| 1. Output during reset: "H" level | All of 4 bits of ports C, D |
| 2. Output during reset: "L" level | All of 4 bits of ports C, D |

**Options of Port Output Configuration**

For each input/output-common port, either of the following two output configurations may be selected by option (bitwise).

| Option Name                       | Circuit | Conditions, etc. |
|-----------------------------------|---------|------------------|
| 1. Open drain type output         |         |                  |
| 2. Output with pull-up resistance |         |                  |

**Development Support**

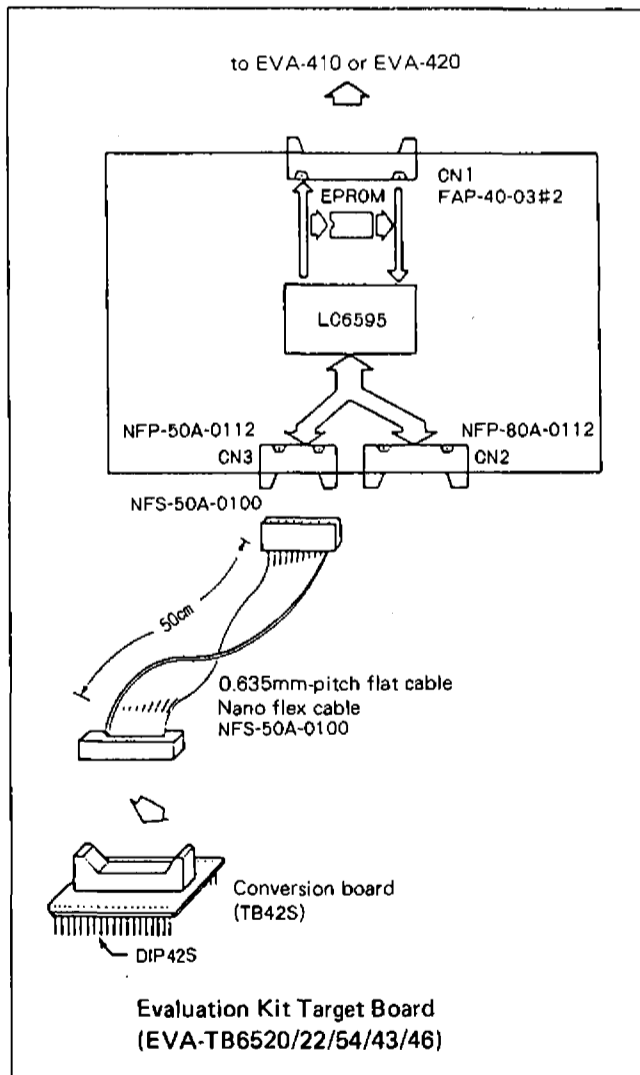
The following are available to support the LC6520, LC6522 program development.

- (1) User's Manual
  - "LC6554 Series User's Manual" No. E21B. (Issued in December, 1987)
- (2) Development Tool Manual
  - For the EVA-410 system, refer to the description of Development Support Tools in "LC6554 Series User's Manual". For the EVA-800 system, refer to "EVA-800-LC6554 Series Development Tool Manual".
- (3) Development Tools
  - 1) For program development (EVA-410 system)
    - i. MS-DOS host computer system (Note 1)
    - ii. MS-DOS base cross assembler (LC65S.EXE)
    - iii. Evaluation kit (EVA-410C or EVA-420)
    - iv. Evaluation kit target board (EVA-TB6520/22/54/43/46), evaluation chip (LC6595)
  - 2) For program evaluation
    - i. Piggyback (LC65PG20/22), with socket for conversion of number of piggyback pins

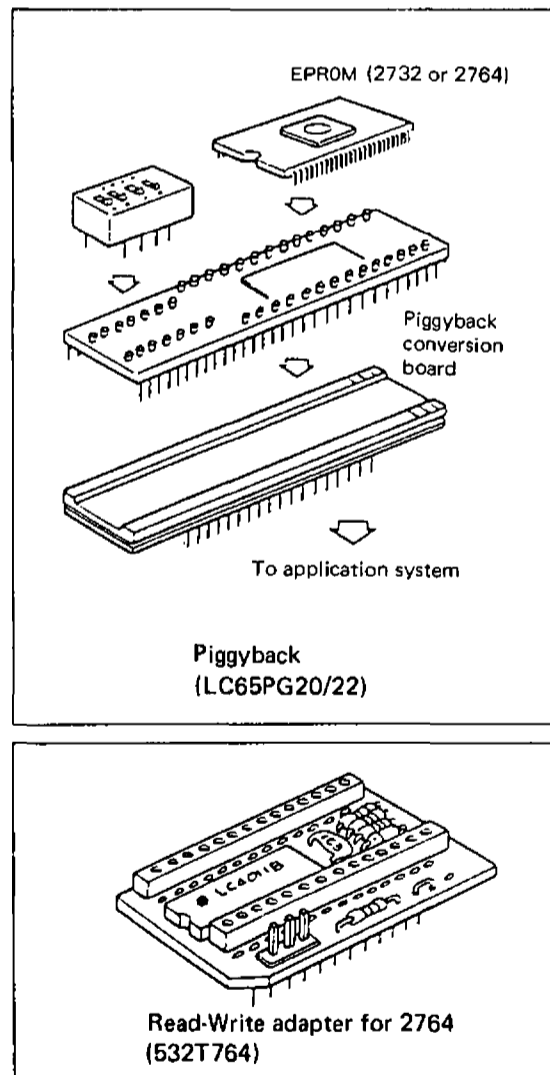
Note. For notes on program evaluation, do not fail to refer to "5-3-1. Notes on when evaluating programs for the LC6520/22" in "LC6554 Series User's Manual".

**Appearance of Application Development Tools**

**EVA-410 System**



**Piggyback**

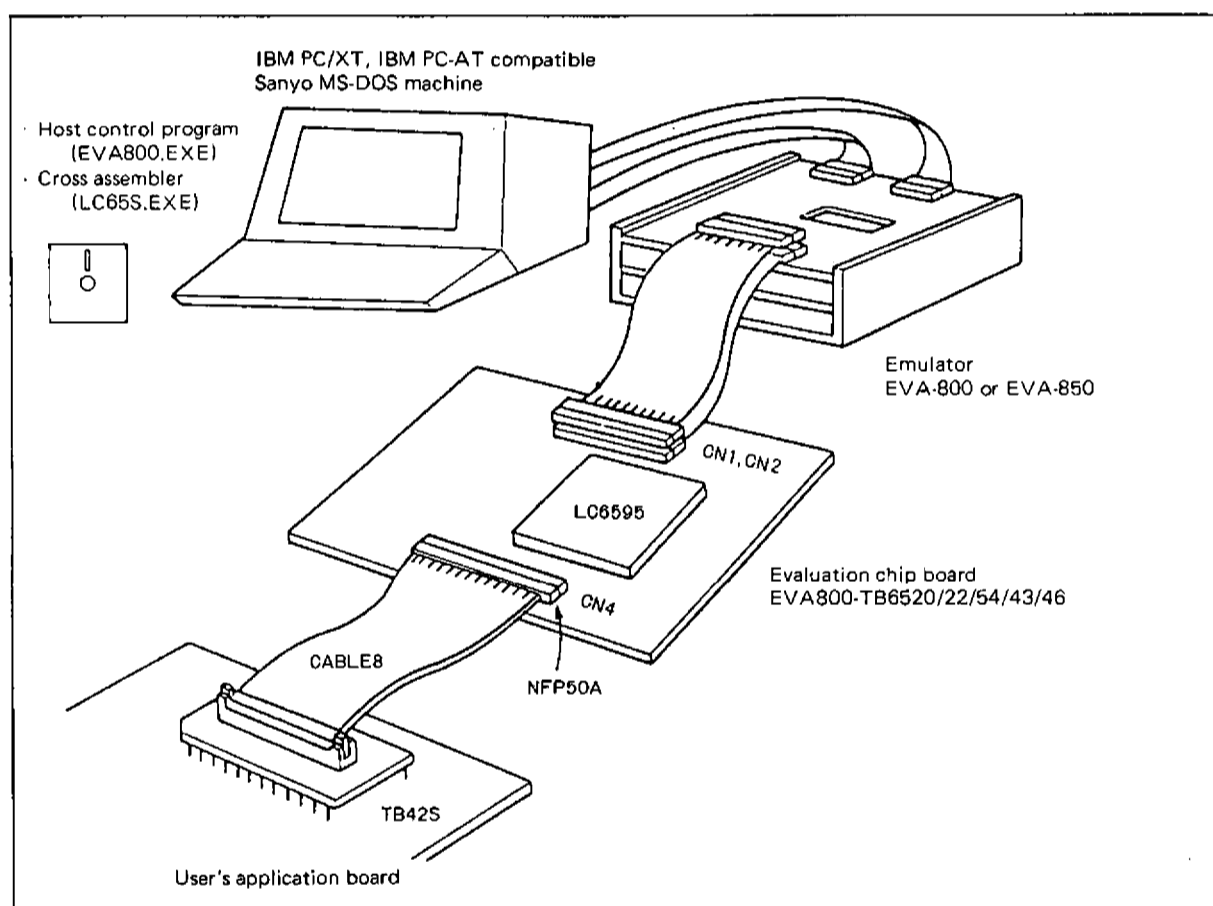




- 3) For program development (EVA-800 system)
- i. IBM PC/XT, IBM PC-AT (Note 1) compatible Sanyo MS-DOS machine
  - ii. Cross assembler .....MS-DOS base cross assembler: (LC65S.EXE)
  - iii. Host control program: (EVA800.EXE)
  - iv. Evaluation chip: LC6595
  - v. Emulator : EVA-800 or EVA-850 control board and evaluation chip board (Note 2)

**Appearance of Development Support System**

**EVA-800 System**



(Note 1) IBM PC/XT, IBM PC-AT: Products of IBM Corporation

MS-DOS: Trademark of Microsoft Corporation

(Note 2) The EVA-800 is a general term for emulator. A suffix (A, B ...) is added at the end of EVA-800 as the EVA-800 is improved to be a newer version. Do not use the EVA-800 with no suffix added.

LC6520C,6520H,6522C,6522H

Main Specifications of the LC6520C, 6522C

| Absolute Maximum Ratings/ $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{V}$   |                      |   |                                   | unit             |              |  |
|---|----------------------|---|-----------------------------------|------------------|--------------|--|
| Maximum Supply Voltage  | $V_{DD\text{ max}}$  | $V_{DD}$  | -0.3 to +7.0                      | V                |              |  |
| Output Voltage  | $V_o$                | OSC2  | Allowable up to voltage generated | V                |              |  |
| Input Voltage   | $V_i$ (1)            | OSC1 (Note 1)   | -0.3 to $V_{DD}+0.3$              | V                |              |  |
|   | $V_i$ (2)            | TEST, RES   | -0.3 to $V_{DD}+0.3$              | V                |              |  |
|   | $V_i$ (3)            | PB0 to 3  | -0.3 to +15                       | V                |              |  |
| Input/Output Voltage  | $V_{IO}$ (1)         | Port of OD type   | -0.3 to +15                       | V                |              |  |
|   | $V_{IO}$ (2)         | Port of PU type   | -0.3 to $V_{DD}+0.3$              | V                |              |  |
| Peak Output Current   | $I_{OP}$             | Input/output port   | -2 to +20                         | mA               |              |  |
| Average Output Current  | $I_{OA}$             | Input/output port:  | -2 to +20                         | mA               |              |  |
|   |                      | Per pin over the period of 100 msec.  |                                   |                  |              |  |
|   | $\Sigma I_{OA}$ (1)  | Total current of PA0 to 3, PC0 to 3, PD0 to 3 and PE0 to 3 (Note 2)                         | -30 to +140                       | mA               |              |  |
|   | $\Sigma I_{OA}$ (2)  | Total current of PF0 to 3, PG0 to 3, PI0 to 3 and PJ0 to 3.(Note 2)                         | -30 to +140                       | mA               |              |  |
| Allowable Power Dissipation   | $P_d\text{ max}$ (1) | DIP package, $T_a = -30$ to $+70^\circ\text{C}$   | 600                               | mW               |              |  |
|   | $P_d\text{ max}$ (2) | QIP package, $T_a = -30$ to $+70^\circ\text{C}$   | 400                               | mW               |              |  |
| Operating Temperature   | $T_{opr}$            |   | -30 to +70                        | $^\circ\text{C}$ |              |  |
| Storage Temperature   | $T_{stg}$            |   | -55 to +125                       | $^\circ\text{C}$ |              |  |
| Allowable Operating Conditions/ $T_a = -30$ to $+70^\circ\text{C}$ , $V_{SS} = 0\text{V}$ , $V_{DD} = 3.0$ to $5.5\text{V}$ |                      |   | min                               | typ              | max          | unit                                   |
| Operating Supply Voltage  | $V_{DD}$             | $V_{DD}$  | 3.0                               |                  | 5.5          | V                                      |
| Standby Supply Voltage  | $V_{st}$             | $V_{DD}$ : RAM, resistor hold (Note 3)  | 1.8                               |                  | 5.5          | V                                      |
| "H"-Level Input Voltage   | $V_{IH}$ (1)         | Port of OD type, PB0 to 3: Output Nch Tr OFF  | $0.7V_{DD}$                       |                  | +13.5        | V                                      |
|   | $V_{IH}$ (2)         | Port of PU type: Output Nch Tr OFF  | $0.7V_{DD}$                       |                  | $V_{DD}$     | V                                      |
|   | $V_{IH}$ (3)         | $\overline{SCK}$ , SI, $\overline{INT}$ of OD type: Output Nch Tr OFF                       | $0.8V_{DD}$                       |                  | +13.5        | V                                      |
|   | $V_{IH}$ (4)         | $\overline{SCK}$ , SI, $\overline{INT}$ of PU type: Output Nch Tr OFF                       | $0.8V_{DD}$                       |                  | $V_{DD}$     | V                                      |
|   | $V_{IH}$ (5)         | $\overline{RES}$  | $0.8V_{DD}$                       |                  | $V_{DD}$     | V                                      |
|   | $V_{IH}$ (6)         | OSC1: External clock mode   | $0.8V_{DD}$                       |                  | $V_{DD}$     | V                                      |
| "L"-Level Input Voltage   | $V_{IL}$ (1)         | PORT: $V_{DD} = 4$ to $5.5\text{V}$ , Output Nch Tr OFF                                     | $V_{SS}$                          |                  | $0.3V_{DD}$  | V                                      |
|   | $V_{IL}$ (2)         | PORT: Output Nch Tr OFF   | $V_{SS}$                          |                  | $0.25V_{DD}$ | V                                      |
|   | $V_{IL}$ (3)         | $\overline{INT}$ , $\overline{SCK}$ , SI: $V_{DD} = 4$ to $5.5\text{V}$ , Output Nch Tr OFF | $V_{SS}$                          |                  | $0.25V_{DD}$ | V                                      |
|   | $V_{IL}$ (4)         | $\overline{INT}$ , $\overline{SCK}$ , SI: Output Nch Tr OFF                                 | $V_{SS}$                          |                  | $0.2V_{DD}$  | V                                      |
|   | $V_{IL}$ (5)         | OSC1: $V_{DD} = 4$ to $5.5\text{V}$ , External clock mode                                   | $V_{SS}$                          |                  | $0.25V_{DD}$ | V                                      |
|   | $V_{IL}$ (6)         | OSC1: External clock mode   | $V_{SS}$                          |                  | $0.2V_{DD}$  | V                                      |
|   | $V_{IL}$ (7)         | TEST: $V_{DD} = 4$ to $5.5\text{V}$   | $V_{SS}$                          |                  | $0.3V_{DD}$  | V                                      |
|   | $V_{IL}$ (8)         | TEST  | $V_{SS}$                          |                  | $0.25V_{DD}$ | V                                      |
|   | $V_{IL}$ (9)         | $\overline{RES}$ : $V_{DD} = 4$ to $5.5\text{V}$  | $V_{SS}$                          |                  | $0.25V_{DD}$ | V                                      |
|   | $V_{IL}$ (10)        | $\overline{RES}$  | $V_{SS}$                          |                  | $0.2V_{DD}$  | V                                      |
| Operating Frequency (Cycle Time)  | $f_{op}$             |   |                                   | See Table 2.     |              |  |
|   | $(T_{cyc})$          | ( $V_{DD} = 4.0$ to $5.5\text{V}$ )   | (2.77)<br>(6.0)                   |                  | (20)<br>(20) | ( $\mu\text{s}$ )<br>( $\mu\text{s}$ ) |

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LC6520C, 6520H, 6522C, 6522H

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| External Clock Conditions (When the external clock or 2-pin RC OSC option is selected)   |                | min  | typ          | max   | unit         |
|--|----------------|--|--------------|-------|--------------|
| Frequency  | $f_{ext}$      |  | See Table 2. |       |              |
| Pulse Width  | $t_{extH}$     | 90   |              |       | ns           |
|  | $t_{extL}$     | 180  |              |       | ns           |
| Rise/Fall Time   | $t_{extR}$     |  |              | 30    | ns           |
|  | $t_{extF}$     |  |              | 100   | ns           |
| <b>Oscillation Guaranteed Constants</b>  |                |  |              |       |              |
| 2-Pin RC Oscillation   | $C_{ext}$      | OSC1, OSC2: $V_{DD} = 4$ to $5.5V$ , Fig. 2  | 220±5%       |       | pF           |
|  | $R_{ext}$      | OSC1, OSC2: $V_{DD} = 4$ to $5.5V$ , Fig. 2  | 6.8±1%       |       | kΩ           |
|  | $C_{ext}$      | OSC1, OSC2: Fig. 2   | 270±5%       |       | pF           |
|  | $R_{ext}$      | OSC1, OSC2: Fig. 2   | 15±1%        |       | kΩ           |
| Ceramic Resonator Oscillation  |                | Fig. 3   | See Table 1. |       |              |
| <b>Electrical Characteristics/<math>T_a = -30</math> to <math>+70^\circ C</math>, <math>V_{SS} = 0V</math>, <math>V_{DD} = 3.0</math> to <math>5.5V</math></b> |                |  |              |       |              |
| "H"-Level Input Current  | $I_{IH}$ (1)   | Port of open drain type, $PB_0$ to 3:<br>Output Nch Tr OFF, Including OFF leakage current of Nch Tr,<br>$V_{IN} = +13.5V$                                |              |       | +5.0 $\mu A$ |
| "L"-Level Input Current  | $I_{IH}$ (2)   | OSC1: External clock mode, $V_{IN} = V_{DD}$   |              |       | +1.0 $\mu A$ |
|  | $I_{IL}$ (1)   | Port of open drain type, $PB_0$ to 3:<br>Output Nch Tr OFF, $V_{IN} = V_{SS}$  | -1.0         |       | $\mu A$      |
|  | $I_{IL}$ (2)   | Port with pull-up resistance:<br>Output Nch Tr OFF, $V_{IN} = V_{SS}$  | -1.3         | -0.35 | mA           |
|  | $I_{IL}$ (3)   | $\overline{RES}$ : $V_{IN} = V_{SS}$   | -45          | -10   | $\mu A$      |
| "H"-Level Output Voltage   | $I_{IL}$ (4)   | OSC1: External clock mode,<br>$V_{IN} = V_{SS}$  | -1.0         |       | $\mu A$      |
|  | $V_{OH}$ (1)   | Port with pull-up resistance:<br>$V_{DD} = 4$ to $5.5V$ , $I_{OH} = -50 \mu A$   | $V_{DD}-1.2$ |       | V            |
| "L"-Level Output Voltage   | $V_{OH}$ (2)   | Port with pull-up resistance:<br>$I_{OH} = -10 \mu A$  | $V_{DD}-0.5$ |       | V            |
|  | $V_{OL}$ (1)   | Port: $V_{DD} = 4$ to $5.5V$ , $I_{OL} = 10$ mA  |              |       | 1.5 V        |
| Hysteresis Voltage   | $V_{OL}$ (2)   | Port: $I_{OL} = 1$ mA, When $I_{OL}$ of each port is 1 mA or less.   |              |       | 0.5 V        |
|  | $V_{Hys}$      | $\overline{RES}$ , $\overline{INT}$ , $\overline{SCR}$ , $SI$ ,<br>OSC1 of Schmitt type (Note 6)   | 0.1 $V_{DD}$ |       | V            |
| <b>Current Dissipation</b>   |                |  |              |       |              |
| 2-Pin RC Oscillation   | $I_{DDOP}$ (1) | Operation mode, Output Nch Tr OFF, Port = $V_{DD}$<br>$V_{DD}$ : $V_{DD} = 4$ to $5.5V$ , Fig. 2<br>$f_{osc} = 750$ kHz typ                              | 2            | 5     | mA           |
|  | $I_{DDOP}$ (2) | $V_{DD}$ : Fig. 2 $f_{osc} = 350$ kHz typ  | 1.5          | 4.5   | mA           |
| Ceramic Resonator Oscillation  | $I_{DDOP}$ (3) | $V_{DD}$ : Fig. 3 $V_{DD} = 4$ to $5.5V$ , 4MHz,<br>1/3 predivider   | 5            | 10    | mA           |
|  | $I_{DDOP}$ (4) | $V_{DD}$ : Fig. 3 $V_{DD} = 4$ to $5.5V$ , 4MHz,<br>1/4 predivider   | 5            | 10    | mA           |
| External Clock   | $I_{DDOP}$ (5) | $V_{DD}$ : Fig. 3 400kHz   | 1.5          | 4     | mA           |
|  | $I_{DDOP}$ (6) | $V_{DD}$ : $V_{DD} = 4$ to $5.5V$ , Fig. 3 800kHz  | 2            | 5     | mA           |
|  | $I_{DDOP}$ (7) | $V_{DD}$ : 200 kHz to 667 kHz,<br>1/1 predivider<br>600 kHz to 2000 kHz, 1/3 predivider<br>800 kHz to 2667 kHz, 1/4 predivider                           | 2            | 5     | mA           |
|  | $I_{DDOP}$ (8) | $V_{DD}$ : $V_{DD} = 4$ to $5.5V$ ,<br>200 kHz to 1444 kHz, 1/1 predivider<br>600 kHz to 4330 kHz, 1/3 predivider<br>800 kHz to 4330 kHz, 1/4 predivider | 3            | 10    | mA           |
| Standby Mode   | $I_{DDSt}$     | $V_{DD}$ : $V_{DD} = 5.5V$ (Output Nch Tr OFF,<br>Port = $V_{DD}$ )  | 0.05         | 10    | $\mu A$      |
|  |                | $V_{DD}$ : $V_{DD} = 3V$   | 0.025        | 5     | $\mu A$      |

Continued on next page.

LC6520C,6520H,6522C,6522H

Continued from preceding page.

|                                       |                                | min  | typ                        | max                        | unit                       |                          |
|---------------------------------------|--------------------------------|--|----------------------------|----------------------------|----------------------------|--------------------------|
| <b>Oscillation Characteristics</b>    |                                |  |                            |                            |                            |                          |
| <b>Ceramic Resonator Oscillation</b>  |                                |  |                            |                            |                            |                          |
| Oscillation Frequency                 | f <sub>CFOSC</sub><br>(Note 4) | OSC1, OSC2: Fig. 3 f <sub>o</sub> = 400 kHz<br>OSC1, OSC2: V <sub>DD</sub> = 4 to 5.5V,<br>Fig. 3 f <sub>o</sub> = 800 kHz<br>OSC1, OSC2: V <sub>DD</sub> = 4 to 5.5V,<br>Fig. 3 f <sub>o</sub> = 3 MHz, 1/3 predivider,<br>1/4 predivider<br>OSC1, OSC2: V <sub>DD</sub> = 4 to 5.5V,<br>Fig. 3 f <sub>o</sub> = 4 MHz, 1/3 predivider,<br>1/4 predivider | 392<br>784<br>2940<br>3920 | 400<br>800<br>3000<br>4000 | 408<br>816<br>3060<br>4080 | kHz<br>kHz<br>kHz<br>kHz |
| Oscillation Stabilizing Period        | t <sub>CFS</sub>               | Fig. 4 f <sub>o</sub> = 400 kHz<br>V <sub>DD</sub> = 4 to 5.5V, Fig. 4<br>f <sub>o</sub> = 4 MHz, 3 MHz, 800 kHz   |                            |                            | 10<br>10                   | ms<br>ms                 |
| <b>2-Pin RC Oscillation</b>           |                                |  |                            |                            |                            |                          |
| Oscillation Frequency                 | f <sub>MOSC</sub> (1)          | OSC1, OSC2: V <sub>DD</sub> = 4 to 5.5V, Fig. 2,<br>C <sub>ext</sub> = 220 pF±5%, R <sub>ext</sub> = 6.8 kΩ±1%   | 515                        | 750                        | 1156                       | kHz                      |
|                                       | f <sub>MOSC</sub> (2)          | OSC1, OSC2: Fig. 2,<br>C <sub>ext</sub> = 270 pF±5%, R <sub>ext</sub> = 15 kΩ±1%   | 222                        | 350                        | 609                        | kHz                      |
| <b>Pull-up Resistance</b>             |                                |  |                            |                            |                            |                          |
| I/O Port Pull-up Resistance           | R <sub>pp</sub>                | Port of PU type: V <sub>DD</sub> = 5V  |                            | 14                         |                            | kΩ                       |
| <b>External Reset Characteristics</b> |                                |  |                            |                            |                            |                          |
| "H"-Level Threshold                   | V <sub>tH</sub>                |  | 0.5V <sub>DD</sub>         | 0.8V <sub>DD</sub>         |                            | V                        |
| "L"-Level Threshold                   | V <sub>tL</sub>                |  | 0.2V <sub>DD</sub>         | 0.5V <sub>DD</sub>         |                            | V                        |
| Reset Time                            | T <sub>RST</sub>               |  |                            | See Fig. 5.                |                            |                          |
| Pin Capacitance                       | CP                             | f = 1 MHz, Other than pins to be tested, V <sub>IN</sub> = V <sub>SS</sub>   |                            | 10                         |                            | pF                       |
| <b>Serial Clock</b>                   |                                |  |                            |                            |                            |                          |
| Input Clock Cycle Time                | t <sub>CKCY</sub> (1)          | $\overline{SCK}$ : V <sub>DD</sub> = 4 to 5.5V, Fig. 6<br>$\overline{SCK}$   | 3.0<br>12.0                |                            |                            | μs<br>μs                 |
| Output Clock Cycle Time               | t <sub>CKCY</sub> (2)          | SCK (T <sub>CYC</sub> = 4 x System clock period), Fig. 6   |                            | 64 x T <sub>CYC</sub>      |                            | μs                       |
| Input Clock "L"-Level Pulse Width     | t <sub>CKL</sub> (1)           | $\overline{SCK}$ : V <sub>DD</sub> = 4 to 5.5V, Fig. 6<br>$\overline{SCK}$   | 1.0                        |                            |                            | μs                       |
|                                       | t <sub>CKL</sub> (2)           | $\overline{SCK}$ , Fig. 6  |                            | 32 x T <sub>CYC</sub>      |                            | μs                       |
| Output Clock "L"-Level Pulse Width    | t <sub>CKH</sub> (1)           | $\overline{SCK}$ : V <sub>DD</sub> = 4 to 5.5V, Fig. 6<br>$\overline{SCK}$   | 1.0                        |                            |                            | μs                       |
|                                       | t <sub>CKH</sub> (2)           | $\overline{SCK}$ : Fig. 6  |                            | 32 x T <sub>CYC</sub>      |                            | μs                       |
| <b>Serial Input</b>                   |                                |  |                            |                            |                            |                          |
| Data Setup Time                       | t <sub>ICK</sub>               | SI: Specified for ↑ of $\overline{SCK}$ , Fig. 6   | 0.5                        |                            |                            | μs                       |
| Data Hold Time                        | t <sub>CKI</sub>               | SI: Specified for ↑ of $\overline{SCK}$ , Fig. 6   | 0.5                        |                            |                            | μs                       |
| <b>Serial Output</b>                  |                                |  |                            |                            |                            |                          |
| Output Delay Time                     | t <sub>CKO</sub>               | SO: V <sub>DD</sub> = 4 to 5.5V,<br>Specified for ↓ of $\overline{SCK}$ ,<br>Nch OD only: External 1 kohm,<br>external 50 pF, Fig. 6<br>SO   |                            |                            | 0.5<br>2.0                 | μs<br>μs                 |
| <b>Pulse Output</b>                   |                                |  |                            |                            |                            |                          |
| Period                                | t <sub>PCY</sub>               | PE0: T <sub>CYC</sub> = 4 x System clock period,<br>Nch OD only: External 1 kohm,<br>external 50 pF, Fig. 7  |                            | 64 x T <sub>CYC</sub>      |                            | μs                       |
| "H"-Level Pulse Width                 | t <sub>PH</sub>                | PE0:   |                            | 32 x T <sub>CYC</sub> ±10% |                            | μs                       |
| "L"-Level Pulse Width                 | t <sub>PL</sub>                | PE0:   |                            | 32 x T <sub>CYC</sub> ±10% |                            | μs                       |

**Note 1:** When oscillated internally under the oscillating conditions in Fig. 3, up to the oscillation amplitude generated is allowable.

**Note 2:** Average over the period of 100 msec.

**Note 3:** Operating supply voltage V<sub>DD</sub> must be held until the standby mode is entered after the execution of the HALT instruction.  
The PA3 (or PA0 to 3) pin must be free from chattering during the HALT instruction execution cycle.

**Note 4:** f<sub>CFOSC</sub> represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

**Note 5:** When mounting the QIP version on the board, do not dip it in solder.

**Note 6:** The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.

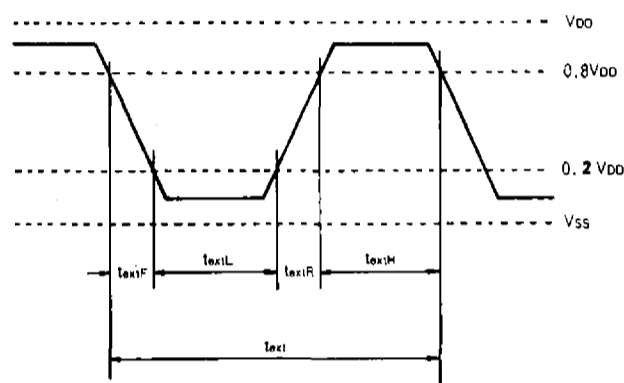
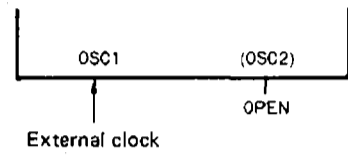


Fig. 1 External Clock Input Waveform

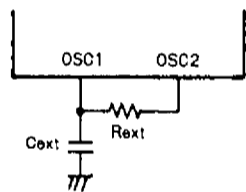


Fig. 2 2-Pin RC Oscillation Circuit

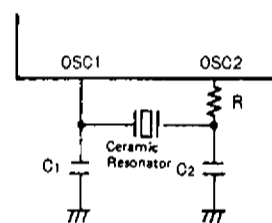


Fig. 3 Ceramic Resonator Oscillation Circuit

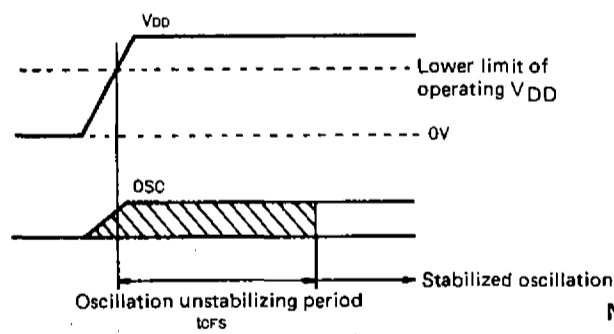


Fig. 4 Oscillation Stabilizing Period

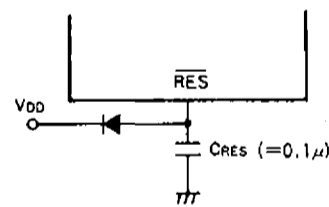


Fig. 5 Reset Circuit

**Note 7:** When the rise time of the power supply is 0, the reset time becomes 10 ms to 100 ms at  $C_{RES} = 0.1 \mu F$ . If the rise time of the power supply is long, the value of  $C_{RES}$  must be increased so that the reset time becomes 10 ms or greater.

|                            |    |            |                                       |    |             |
|----------------------------|----|------------|---------------------------------------|----|-------------|
| 4MHz (Murata)<br>CSA4.00MG | C1 | 33pF ± 10% | 800kHz (Murata)<br>CSB800D<br>CSB800K | C1 | 220pF ± 10% |
|                            | C2 | 33pF ± 10% |                                       | C2 | 220pF ± 10% |
|                            | R  | 0Ω         |                                       | R  | 0Ω          |
| 4MHz (Kyocera)<br>KBR4.0MS | C1 | 33pF ± 10% | 800kHz (Kyocera)<br>KBR800H           | C1 | 150pF ± 10% |
|                            | C2 | 33pF ± 10% |                                       | C2 | 150pF ± 10% |
|                            | R  | 0Ω         |                                       | R  | 0Ω          |
| 3MHz (Murata)<br>CSA3.00MG | C1 | 33pF ± 10% | 400kHz (Murata)<br>CSB400P            | C1 | 470pF ± 10% |
|                            | C2 | 33pF ± 10% |                                       | C2 | 470pF ± 10% |
|                            | R  | 0Ω         |                                       | R  | 0Ω          |
| 3MHz (Kyocera)<br>KBR3.0MS | C1 | 47pF ± 10% | 400kHz (Kyocera)<br>KBR400B           | C1 | 330pF ± 10% |
|                            | C2 | 47pF ± 10% |                                       | C2 | 330pF ± 10% |
|                            | R  | 0Ω         |                                       | R  | 0Ω          |

Table 1 Constants Guaranteed for Ceramic Resonator Oscillation

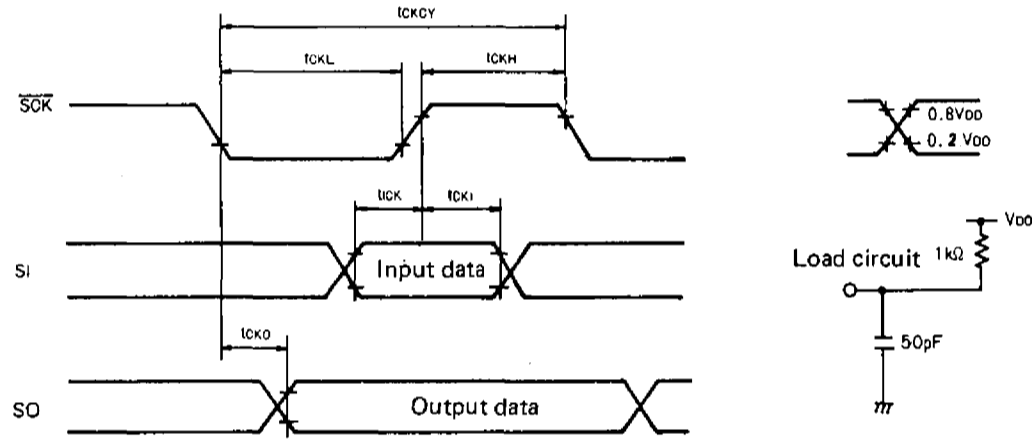


Fig. 6 Serial Input/Output Timing

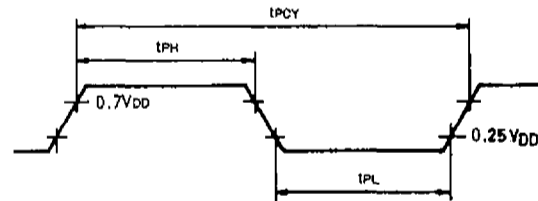


Fig. 7 Pulse Output Timing at Port PE0

The load conditions are the same as in Fig. 6.

LC6520C,6520H,6522C,6522H

| Circuit Configuration  | Frequency  | Predivider Option (Cycle Time)           | V <sub>DD</sub>                     | Remarks                           |
|--|--|--|-------------------------------------|-----------------------------------|
| Ceramic Resonator Option                                       | 400 kHz  | 1/1 (10 μs)                              | 3 to 5.5V                           | Unusable with 1/3, 1/4 predivider |
|  | 800 kHz  | 1/1 (5 μs)<br>1/3 (15 μs)<br>1/4 (20 μs) | 4 to 5.5V<br>4 to 5.5V<br>4 to 5.5V |                                   |
|  | 3 MHz  | 1/3 (4 μs)<br>1/4 (5.33 μs)              | 4 to 5.5V<br>4 to 5.5V              | Unusable with 1/1 predivider      |
|  | 4 MHz  | 1/3 (3 μs)<br>1/4 (4 μs)                 | 4 to 5.5V<br>4 to 5.5V              | Unusable with 1/1 predivider      |
| External Clock Option or External Clock Drive by RC OSC Option | 200 to 667 kHz   | 1/1 (20 to 6 μs)                         | 3 to 5.5V                           |                                   |
|  | 600 to 2000 kHz  | 1/3 (20 to 6 μs)                         | 3 to 5.5V                           |                                   |
|  | 800 to 2667 kHz  | 1/4 (20 to 6 μs)                         | 3 to 5.5V                           |                                   |
|  | 200 to 1444 kHz  | 1/1 (20 to 2.77 μs)                      | 4 to 5.5V                           |                                   |
|  | 600 to 4330 kHz  | 1/3 (20 to 2.77 μs)                      | 4 to 5.5V                           |                                   |
|  | 800 to 4330 kHz  | 1/4 (20 to 3.70 μs)                      | 4 to 5.5V                           |                                   |
| External Clock Drive by ceramic resonator OSC Option           | The external clock drive is impossible. When using the external clock drive, specify the external clock option or RC OSC option.   |  |                                     |                                   |
| RC OSC Option  | Used with 1/1 predivider, recommended constants (V <sub>DD</sub> = 4 to 5.5V, V <sub>DD</sub> = 3 to 5.5V).<br>If used with other than recommended constants, the predivider option, frequency, V <sub>DD</sub> range must be the same as for the external clock option. |  |                                     |                                   |

**Table 2 Table of Oscillation, Predivider Option** (All selectable combinations are shown. Do not use any other combinations than shown above.)

**RC Oscillation Characteristic of the LC6520C, 6522C**

Fig. 8 shows the RC oscillation characteristic of the LC6520C, 6522C. For the variation range of RC OSC frequency of the LC6520C, 6522C, the following are guaranteed at the external constants only shown below.

- 1) V<sub>DD</sub> = 3.0V to 5.5V, T<sub>a</sub> = -30°C to +70°C  
 External constants    C<sub>ext</sub> = 270 pF, R<sub>ext</sub> = 15 kohms  
 222 kHz ≤ f<sub>mosc</sub> ≤ 609 kHz
- 2) V<sub>DD</sub> = 4.0V to 5.5V, T<sub>a</sub> = -30°C to +70°C  
 External constants    C<sub>ext</sub> = 220 pF, R<sub>ext</sub> = 6.8 kohms  
 515 kHz ≤ f<sub>mosc</sub> ≤ 1156 kHz

If any other constants than specified above are used, the range of R<sub>ext</sub> = 4 kohms to 23 kohms, C<sub>ext</sub> = 150 pF to 400 pF must be observed. (See Fig. 8.)

**Note 8:** The oscillation frequency at V<sub>DD</sub> = 5.0V, T<sub>a</sub> = 25°C must be in the range of 350 kHz to 750 kHz.

**Note 9:** The oscillation frequency at V<sub>DD</sub> = 4.0V to 5.5V, T<sub>a</sub> = -30°C to +70°C and V<sub>DD</sub> = 3.0V to 5.5V, T<sub>a</sub> = -30°C to +70°C must be within the operation clock frequency range. (See Table 2.)

LC6520C, 6520H, 6522C, 6522H

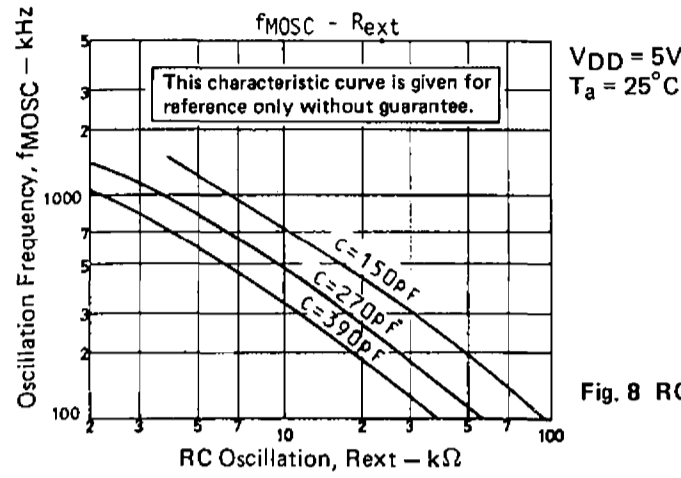


Fig. 8 RC Oscillation Frequency Data (Typ.)

Main Specifications of the LC6520H, 6522H

| Absolute Maximum Ratings/ $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{V}$   |                      |   |                                   | unit             |                   |
|---|----------------------|---|-----------------------------------|------------------|-------------------|
| Maximum Supply Voltage  | $V_{DD\text{ max}}$  | $V_{DD}$  | -0.3 to +7.0                      | V                |                   |
| Output Voltage  | $V_o$                | OSC2  | Allowable up to voltage generated | V                |                   |
| Input Voltage   | $V_i$ (1)            | OSC1 (Note 1)   | -0.3 to $V_{DD}+0.3$              | V                |                   |
|   | $V_i$ (2)            | TEST, $\overline{\text{RES}}$   | -0.3 to $V_{DD}+0.3$              | V                |                   |
|   | $V_i$ (3)            | PB0 to 3  | -0.3 to +15                       | V                |                   |
| Input/Output Voltage  | $V_{IO}$ (1)         | Port of OD type   | -0.3 to +15                       | V                |                   |
|   | $V_{IO}$ (2)         | Port of PU type   | -0.3 to $V_{DD}+0.3$              | V                |                   |
| Peak Output Current   | $I_{OP}$             | Input/output port   | -2 to +20                         | mA               |                   |
| Average Output Current  | $I_{OA}$             | Input/output port: Per pin over the period of 100 msec.                   | -2 to +20                         | mA               |                   |
|   | $\Sigma I_{OA}$ (1)  | Total current of PA0 to 3, PC0 to 3, PD0 to 3, and PE0 to 3 (Note 2)      | -30 to +140                       | mA               |                   |
|   | $\Sigma I_{OA}$ (2)  | Total current of PF0 to 3, PG0 to 3, and PI0 to 3, PJ0 to 3 (Note 2)      | -30 to +140                       | mA               |                   |
| Allowable Power Dissipation   | $P_D\text{ max}$ (1) | DIP package, $T_a = -30$ to $+70^\circ\text{C}$                           | 600                               | mW               |                   |
|   | $P_D\text{ max}$ (2) | QIP package, $T_a = -30$ to $+70^\circ\text{C}$                           | 400                               | mW               |                   |
| Operating Frequency   | $T_{opg}$            |   | -30 to +70                        | $^\circ\text{C}$ |                   |
| Storage Temperature   | $T_{stg}$            |   | -55 to +125                       | $^\circ\text{C}$ |                   |
| Allowable Operating Conditions/ $T_a = -30$ to $+70^\circ\text{C}$ , $V_{SS} = 0\text{V}$ , $V_{DD} = 4.5$ to $5.5\text{V}$ |                      | min   | typ                               | max              | unit              |
| Operating Supply Voltage  | $V_{DD}$             | $V_{DD}$  | 4.5                               | 5.5              | V                 |
| Standby Supply Voltage  | $V_{st}$             | $V_{DD}$ : RAM, resistor hold (Note 3)                                    | 1.8                               | 5.5              | V                 |
| "H"-Level Input Voltage   | $V_{IH}$ (1)         | Port of OD type, PB0 to 3: Output Nch Tr OFF                              | $0.7V_{DD}$                       | +13.5            | V                 |
|   | $V_{IH}$ (2)         | Port of PU type: Output Nch Tr OFF  | $0.7V_{DD}$                       | $V_{DD}$         | V                 |
|   | $V_{IH}$ (3)         | SCK, SI, INT: Output Nch Tr OFF   | $0.8V_{DD}$                       | +13.5            | V                 |
|   | $V_{IH}$ (4)         | $\overline{\text{SCK}}$ , SI, $\overline{\text{INT}}$ : Output Nch Tr OFF | $0.8V_{DD}$                       | $V_{DD}$         | V                 |
|   | $V_{IH}$ (5)         | $\overline{\text{RES}}$   | $0.8V_{DD}$                       | $V_{DD}$         | V                 |
|   | $V_{IH}$ (6)         | OSC1: External clock mode   | $0.8V_{DD}$                       | $V_{DD}$         | V                 |
| "L"-Level Input Voltage   | $V_{IL}$ (1)         | Port: Output Nch Tr OFF   | $V_{SS}$                          | $0.3V_{DD}$      | V                 |
|   | $V_{IL}$ (2)         | $\overline{\text{INT}}$ , $\overline{\text{SCK}}$ , SI: Output Nch Tr OFF | $V_{SS}$                          | $0.25V_{DD}$     | V                 |
|   | $V_{IL}$ (3)         | OSC1: External clock mode   | $V_{SS}$                          | $0.25V_{DD}$     | V                 |
|   | $V_{IL}$ (4)         | TEST  | $V_{SS}$                          | $0.3V_{DD}$      | V                 |
|   | $V_{IL}$ (5)         | $\overline{\text{RES}}$   | $V_{SS}$                          | $0.25V_{DD}$     | V                 |
| Operating Frequency (Cycle Time)  | $f_{op}$             |   | See Table 2.                      |                  |                   |
|   | $(T_{cyc})$          |   | (0.92)                            | (20)             | ( $\mu\text{s}$ ) |
| External Clock Conditions (When the external clock option is selected)  |                      |   |                                   |                  |                   |
| Frequency   | $f_{ext}$            | OSC1: Fig. 1  |                                   | See Table 2.     |                   |
| Pulse Width   | $t_{extH}$           | OSC1: Fig. 1  | 90                                |                  | ns                |
|   | $t_{extL}$           |   |                                   |                  |                   |
| Rise/Fall Time  | $t_{extR}$           | OSC1: Fig. 1  |                                   | 30               | ns                |
|   | $t_{extF}$           |   |                                   |                  |                   |
| Oscillation Guaranteed Constants  |                      |   |                                   |                  |                   |
| Ceramic Resonator Oscillation   |                      | Fig. 2  |                                   | See Table 1.     |                   |



LC6520C,6520H,6522C,6522H

| Electrical Characteristics/ $T_a = -30$ to $+70^\circ\text{C}$ , $V_{SS} = 0\text{V}$ , $V_{DD} = 4.5$ to $5.5\text{V}$ |                      | min   | typ   | max | unit   |
|---|----------------------|---|-------|-----|--|
| "H"-Level Input Current   | $I_{IH}$ (1)         | Port of open drain type, PB0 to 3: Output Nch Tr OFF, Including Nch Tr OFF leakage current, $V_{IN} = 13.5\text{V}$           |       |     | +5.0 $\mu\text{A}$                             |
| "L"-Level Input Current   | $I_{IH}$ (2)         | OSC1: External clock mode, $V_{IN} = V_{DD}$  |       |     | +1.0 $\mu\text{A}$                             |
|   | $I_{IL}$ (1)         | -1.0  |       |     | $\mu\text{A}$                                  |
|   | $I_{IL}$ (2)         | -1.3  | -0.35 |     | mA   |
|   | $I_{IL}$ (3)         | -45   | -10   |     | $\mu\text{A}$                                  |
| "H"-Level Output Voltage  | $V_{OH}$ (1)         | Port with pull-up resistance: $I_{OH} = -50 \mu\text{A}$  |       |     | $V_{DD}-1.2$ V                                 |
|   | $V_{OH}$ (2)         | Port with pull-up resistance: $I_{OH} = -10 \mu\text{A}$  |       |     | $V_{DD}-0.5$ V                                 |
| "L"-Level Output Voltage  | $V_{OL}$ (1)         | Port: $I_{OL} = 10 \text{mA}$   |       |     | 1.5 V  |
|   | $V_{OL}$ (2)         | Port: $I_{OL} = 1 \text{mA}$ , When $I_{OL}$ of each port is 1 mA or less.  |       |     | 0.5 V  |
| Hysteresis Voltage  | $V_{Hys}$            | RES, INT, SCK, SI, OSC1 of Schmitt type (Note 6)  |       |     | 0.1 $V_{DD}$ V                                 |
| Current Dissipation   |                      |   |       |     |  |
| Ceramic Resonator Oscillation   | $I_{DDOP}$ (1)       | $V_{DD}$ : Fig. 2, 4MHz, Operating mode, Output Nch Tr OFF, Port = $V_{DD}$   |       |     | 5 10 mA  |
| External Clock  | $I_{DDOP}$ (2)       | $V_{DD}$ : 200 kHz to 4330 kHz, Operating mode, Output Nch Tr OFF, Port = $V_{DD}$  |       |     | 5 10 mA  |
| Standby Mode  | $I_{DDST}$           | $V_{DD}$ : $V_{DD} = 5.5\text{V}$ (Output Nch Tr OFF, Port = $V_{DD}$ )<br>$V_{DD}$ : $V_{DD} = 3\text{V}$ (Port = $V_{DD}$ ) |       |     | 0.05 10 $\mu\text{A}$<br>0.025 5 $\mu\text{A}$ |
| Oscillation Characteristics   |                      |   |       |     |  |
| Ceramic Resonator Oscillation   |                      |   |       |     |  |
| Oscillation Frequency   | $f_{CFOSC}$ (Note 4) | OSC1, OSC2: Fig. 2 $f_o = 4 \text{MHz}$   |       |     | 3920 4000 4080 kHz                             |
| Oscillation Stabilizing Period  | $t_{CFS}$            | Fig. 3 $f_o = 4 \text{MHz}$   |       |     | 10 ms  |
| Pull-up Resistance  |                      |   |       |     |  |
| I/O Port Pull-up Resistance   | $R_{pp}$             | Port of PU type: $V_{DD} = 5\text{V}$   |       |     | 14 k $\Omega$                                  |
| External Reset Characteristics  |                      |   |       |     |  |
| "H"-Level Threshold   | $V_{tH}$             | 0.5 $V_{DD}$  |       |     | 0.8 $V_{DD}$ V                                 |
| "L"-Level Threshold   | $V_{tL}$             | 0.25 $V_{DD}$   |       |     | 0.5 $V_{DD}$ V                                 |
| Reset Time  | $T_{RST}$            | See Fig. 4.   |       |     |  |
| Pin Capacitance   | CP                   | f = 1 MHz, Other than pins to be tested, $V_{IN} = V_{SS}$  |       |     | 10 pF  |
| Serial Clock  |                      |   |       |     |  |
| Input Clock Cycle Time  | $t_{CKCY}$ (1)       | SCK: Fig. 5   |       |     | 3.0 $\mu\text{s}$                              |
| Output Clock Cycle Time   | $t_{CKCY}$ (2)       | SCK: ( $T_{CYC} = 4 \times$ System clock period), Fig. 5  |       |     | 64 x $T_{CYC}$ $\mu\text{s}$                   |
| Input Clock "L"-Level Pulse Width   | $t_{CKL}$ (1)        | SCK: Fig. 5   |       |     | 1.0 $\mu\text{s}$                              |
| Output Clock "L"-Level Pulse Width  | $t_{CKL}$ (2)        | SCK: Fig. 5   |       |     | 32 x $T_{CYC}$ $\mu\text{s}$                   |

Continued on next page.

Continued from preceding page.

|                                    |          |   | min | typ                  | max | unit    |
|------------------------------------|----------|---|-----|----------------------|-----|---------|
| Input Clock "H"-Level Pulse Width  | tCKH (1) | $\overline{SCK}$ : Fig. 5   | 1.0 |                      |     | $\mu s$ |
| Output Clock "H"-Level Pulse Width | tCKH (2) | $\overline{SCK}$ : Fig. 5   |     | 32 x TCYC            |     | $\mu s$ |
| Serial Input Data Setup Time       | tICK     | SI: Specified for $\uparrow$ of $\overline{SCK}$ , Fig. 5   | 0.5 |                      |     | $\mu s$ |
| Serial Input Data Hold Time        | tCKI     | SI: Specified for $\uparrow$ of $\overline{SCK}$ , Fig. 5   | 0.5 |                      |     | $\mu s$ |
| Serial Output Output Delay Time    | tCKO     | SO: Specified for $\downarrow$ of $\overline{SCK}$ , Nch OD only: External 1 kohm, external 50 pF, Fig. 5 |     |                      | 0.5 | $\mu s$ |
| Pulse Output Period                | tpCY     | PE0: TCYC = 4 x System clock period, Nch OD only: External 1 kohm, external 50 pF, Fig. 6                 |     | 64 x TCYC            |     | $\mu s$ |
| "H"-Level Pulse Width              | tpH      | PE0:  |     | 32 x TCYC $\pm 10\%$ |     | $\mu s$ |
| "L"-Level Pulse Width              | tpL      | PE0:  |     | 32 x TCYC $\pm 10\%$ |     | $\mu s$ |

**Note 1:** When oscillated internally under the oscillating conditions in Fig. 2, up to the oscillation amplitude generated is allowable.

**Note 2:** Average over the period of 100 msec.

**Note 3:** Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 (or PA0 to 3) pin must be free from chattering during the HALT instruction execution cycle.

**Note 4:** fCFOSC represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

**Note 5:** When mounting the QIP version on the board, do not dip it in solder.

**Note 6:** The OSC1 becomes the Schmitt type when the OSC option is the external clock OSC.

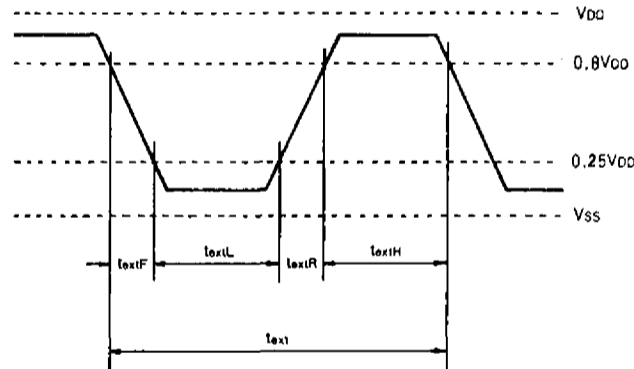
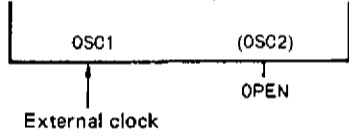


Fig. 1 External Clock Input Waveform

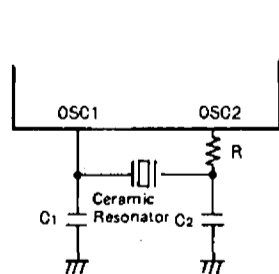


Fig. 2 Ceramic Resonator Oscillation Circuit

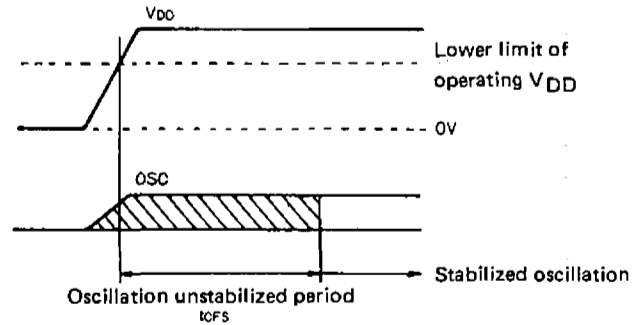
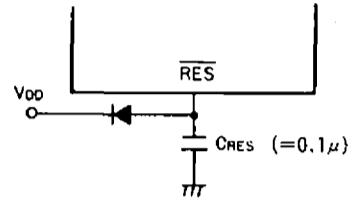


Fig. 3 Oscillation Stabilizing Period

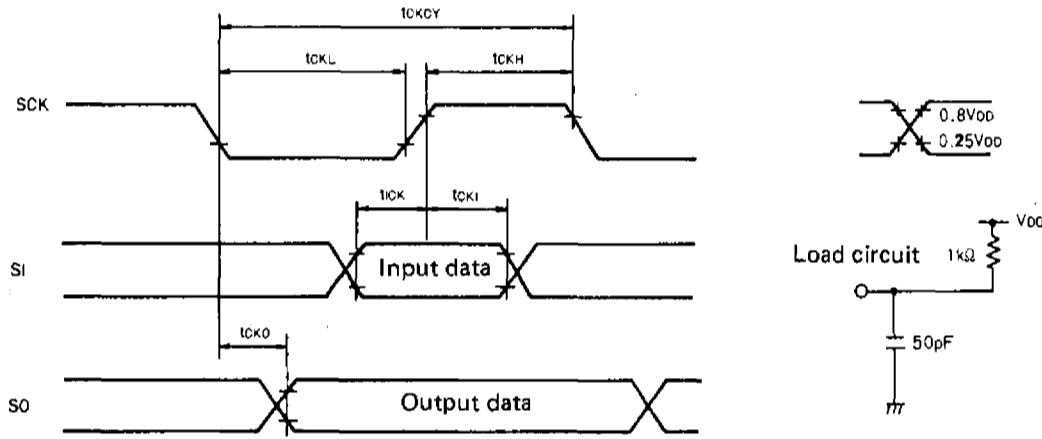
|                            |    |            |
|----------------------------|----|------------|
| 4MHz (Murata)<br>CSA4.00MG | C1 | 33pF ± 10% |
|                            | C2 | 33pF ± 10% |
|                            | R  | 0Ω         |
| 4MHz (Kyocera)<br>KBR4.0MS | C1 | 33pF ± 10% |
|                            | C2 | 33pF ± 10% |
|                            | R  | 0Ω         |

**Table 1 Constants Guaranteed for Ceramic Resonator Oscillation**

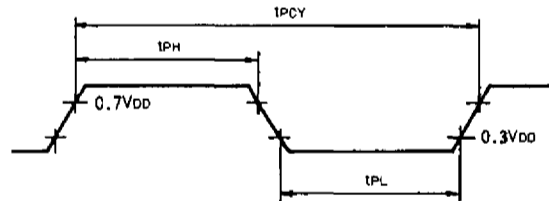


**Fig. 4 Reset Circuit**

**Note 7:** When the rise time of the power supply is 0, the reset time becomes 10 ms to 100 ms at  $C_{RES} = 0.1 \mu F$ . If the rise time of the power supply is long, the value of  $C_{RES}$  must be increased so that the reset time becomes 10 ms or greater.



**Fig. 5 Serial Input/Output Timing**



The load conditions are the same as in Fig. 5.

**Fig. 6 Pulse Output Timing at Port PEO**

| Circuit Configuration                                | Frequency   | Predivider Option (Cycle Time) | VDD         | Remarks |
|--|---|--------------------------------|-------------|---------|
| Ceramic Resonator OSC Option                         | 4 MHz   | 1/1 (1 μs)                     | 4.5 to 5.5V |         |
| External Clock Option                                | 200 to 4330 kHz   | 1/1 (20 to 0.92 μs)            | 4.5 to 5.5V |         |
| External Clock Drive by Ceramic Resonator OSC Option | The external clock drive is impossible. When using the external clock drive, specify the external clock option. |                                |             |         |

**Table 2 Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown above.)**

**Notes for Standby Function Application**

The LC6520, LC6522 provide the standby function called HALT mode to minimize the current dissipation when the program is in the wait state.

The standby function is controlled by the HALT instruction, PA pin,  $\overline{RES}$  pin, and serial transfer completion signal. A peripheral circuit and program must be so designed as to provide precise control of the standby function. In most applications where the standby function is performed, voltage regulation, instantaneous break of power, and external noise are not negligible. When designing an application circuit and program, whether or not to take some measures must be considered according to the extent to which these factors are allowed. This section mainly describes power failure backup for which the standby function is mostly used. A sample application circuit where the standby function is performed precisely is shown below and notes for circuit design and program design are also given below.

When using the standby function, the application circuit shown below must be used and the notes must be also fully observed.

If any other method than shown in this section is applied, it is necessary to fully check the environmental conditions such as power failure and the actual operation of an application equipment.

**1. HALT mode release conditions**

**1-1. Supplementary description of release by serial transfer completion signal**

On completion of serial transfer, the HALT mode is released and the execution of the program starts with an instruction immediately following the HALT instruction. This function can be used to execute the program only when serial transfer occurs, placing the program in the wait state when no serial transfer occurs. This function is effective in reducing the current dissipation or clock noise.

**— Notes —**

- Release by the serial transfer completion signal is available only when the RC mode is used for system clock generation; and unavailable when the ceramic mode is used.
- On completion of serial transfer, the HALT mode is released unconditionally. In an application, such as capacitor backup application, where the current dissipation must be kept as low as possible during backup and serial transfer by external clock is also used, the HALT mode is released when serial data is transferred externally during backup.

**1-2. Summary of HALT release conditions**

The HALT mode setting, release conditions are shown in Table 1.

**Table 1 HALT mode setting, release conditions**

| HALT mode setting conditions  | HALT mode release conditions  |
|---|---|
| HALT instruction<br>Provided that PA <sub>3</sub> , (PA <sub>3</sub> to PA <sub>0</sub> or PA <sub>3</sub> is program-selectable) is at high level. | 1 Reset (Low level is applied to $\overline{RES}$ .)<br>2 Low level is applied to PA <sub>3</sub> , (PA <sub>3</sub> to PA <sub>0</sub> or PA <sub>3</sub> is program-selectable.)<br>3 Serial transfer completion. |

Note) HALT mode release conditions (2), (3) are available only when the RC mode is used for system clock generation; and unavailable when the ceramic mode is used.

**2. Proper cares in using standby function**

When using the standby function, an application circuit and program must be designed with the following in mind.

- (1) The supply voltage at the standby state must not be less than specified.
- (2) Input timing and conditions of each control signal ( $\overline{RES}$ , port A, serial transfer) must be observed at the standby initiate/release state.
- (3) Release operation must not be overlapped at the time of execution of the HALT instruction.

A sample application where the standby function is used for power failure backup is shown below as a concrete method to observe these notes. A sample application circuit, its operation, and notes for program design are given below.

**Sample application where the standby function is used for power failure backup**

Power failure backup is an application where power failure of the main power source is detected and the HALT instruction is executed to cause the standby state to be entered. The current dissipation is minimized and a backup capacitor is used to retain the contents of the internal registers for a certain period of time. After power is restored, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC). Shown below are sample applications where the program selects or not between power-ON reset and reset after power is restored, notes, measures for instantaneous break of AC power, and notes for serial transfer.

**2-1. Sample application 1 where the standby function is used for power failure backup**

Shown below is a sample application where the program does not select between power-ON reset and reset after power is restored.

**2-1-1. Sample application circuit – (1)**

Fig. 2-1 shows a sample application where the standby function is used for power failure backup.

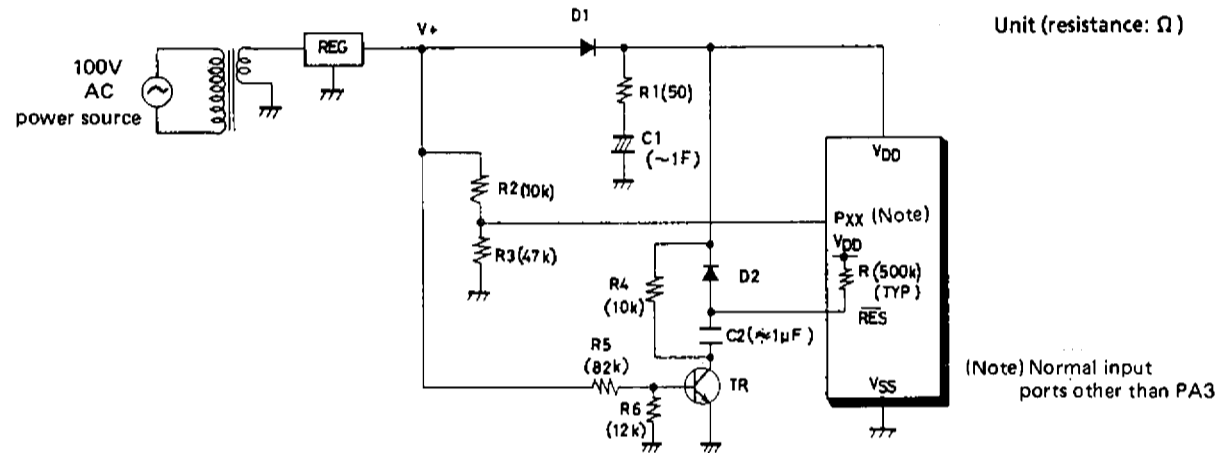


Fig. 2-1. Sample application – (1) where the standby function is used for power failure backup

**2-1-2. Operating waveform in sample application circuit – (1)**

The operating waveform in the sample application circuit in Fig. 2-1 is shown in Fig. 2-2. The mode is roughly divided as follows: a, Power-ON reset, b, Instantaneous break of main power, c, Return from power failure backup.

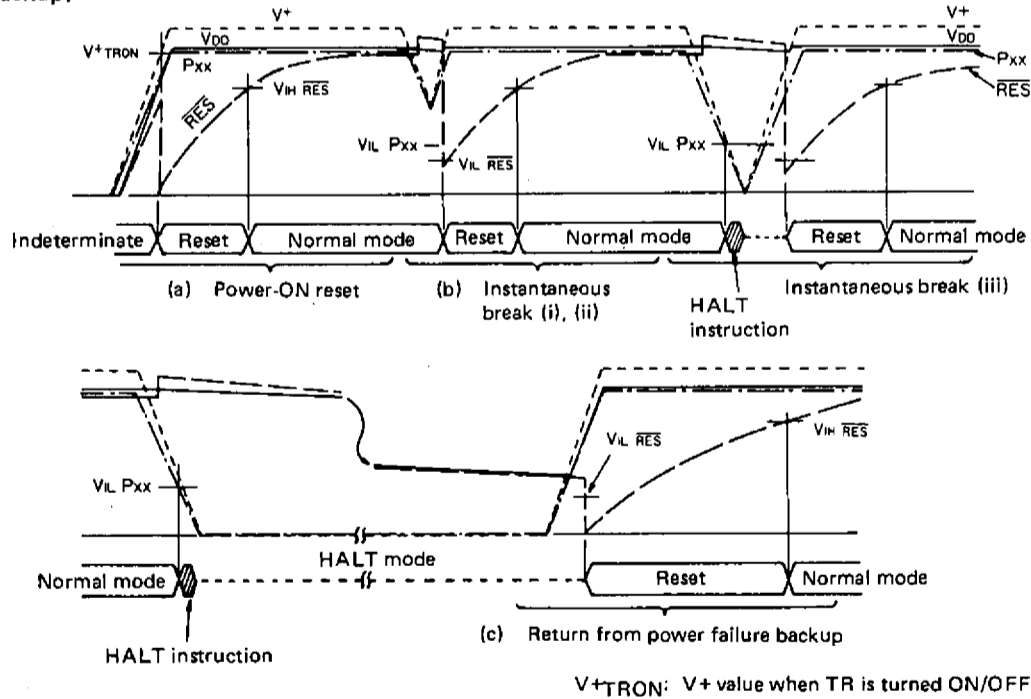


Fig. 2-2. Operating waveforms – (1) in sample application circuit

**2-1-3. Operation of sample application circuit – (1)**

(a) At the time of power-ON reset

After power rises, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC).

– Note –

This sample application circuit provides an indeterminate region where no reset occurs before the operating  $V_{DD}$  range is entered.

(b) At the time of instantaneous break

(i) When the  $P_{XX}$  input voltage does not meet  $V_{IL}$  (The  $P_{XX}$  input level does not get lower than input threshold level  $V_{IL}$ ) and the RES input voltage only meets  $V_{IL}$ :

A reset occurs in the normal mode, providing the same operation as power-ON reset.

(ii) When both of the  $P_{XX}$  input voltage and RES input voltage do not meet  $V_{IL}$ :

The program continues running in the normal mode.

(iii) When both of the  $P_{XX}$  input voltage and  $\overline{RES}$  input voltage meet  $V_{IL}$ :

When two pollings do not regard the  $P_{XX}$  input voltage as "L" level, the HALT mode is not entered and a reset occurs.

When two pollings regard the  $P_{XX}$  input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode.

(c) At the time of return from power failure backup

After power is restored, a reset occurs, releasing the standby mode.

**2-1-4. Notes for design of sample application circuit – (1)**

• V+rise time and  $C_2$

Make the time constant ( $C_2, R$ ) of the reset circuit 10 times as long as the V+rise time. (R: ON-chip resistor, 500 kohm typ.)

Make the V+rise time shorter (up to 20 ms).

•  $R_1$  and  $C_1$

Make the  $R_1$  value as small as possible. Make the  $C_1$  value as large as possible according to the backup time calculated, (Fix the  $R_1$  value so that the  $C_1$  charging current does not exceed the power source capacity.)

•  $R_2$  and  $R_3$

Make the "H"-level input voltage applied to the  $P_{XX}$  pin equal to  $V_{DD}$ .

•  $R_4$

Fix the time constant of  $C_2$  and  $C_4$  so that  $C_2$  can discharge during the period of time from when V+ gets lower than  $V_{TROM}$  (TR OFF) at the time of instantaneous break until the  $P_{XX}$  input voltage gets lower than  $V_{IL}$  (because release by reset is not available after the HALT mode is entered by instantaneous break).

•  $R_5$  and  $R_6$

Make V+ ( $V_{BE} \approx 0.6V$  is obtained by  $R_5$  and  $R_6$ ) when the reset circuit works (Tr ON) more than (operating  $V_{DD\ min} + V_F$  of diode  $D_1$ ). Observing this note, make V+ as low as possible to provide a reset early enough after power-ON.

• Backup time

The normal operation continues with a relatively high current dissipation from when power failure is detected by the  $P_{XX}$  until the HALT instruction is executed. Fix the  $C_1$  value so that the standby supply voltage is held during backup time of set + above-mentioned time.

**2-1-5. Notes for software design**

• Design the program so that port  $A_0$  to  $A_2$  cannot be used for standby release and port  $A_3$  is brought to "H" level at the standby mode.

• Input a standby request to a normal input port other than the  $PA_3$  and check by polling this input port twice.

(Example)

```

:
BP1      AAA      ; 1st polling
RCTL     3        ; Interrupt inhibit
BP1      AAA      ; 2nd polling
HALT
AAA:     :
```

2-2. Sample application 2 where the standby function is used for power failure backup  
 Shown below is a sample application where the program selects between power-ON reset and reset after power is restored.

2-2-1. Sample application circuit – (2) (No instantaneous break in power source)  
 Fig. 2-3 shows a sample application where the standby function is used for power failure backup.

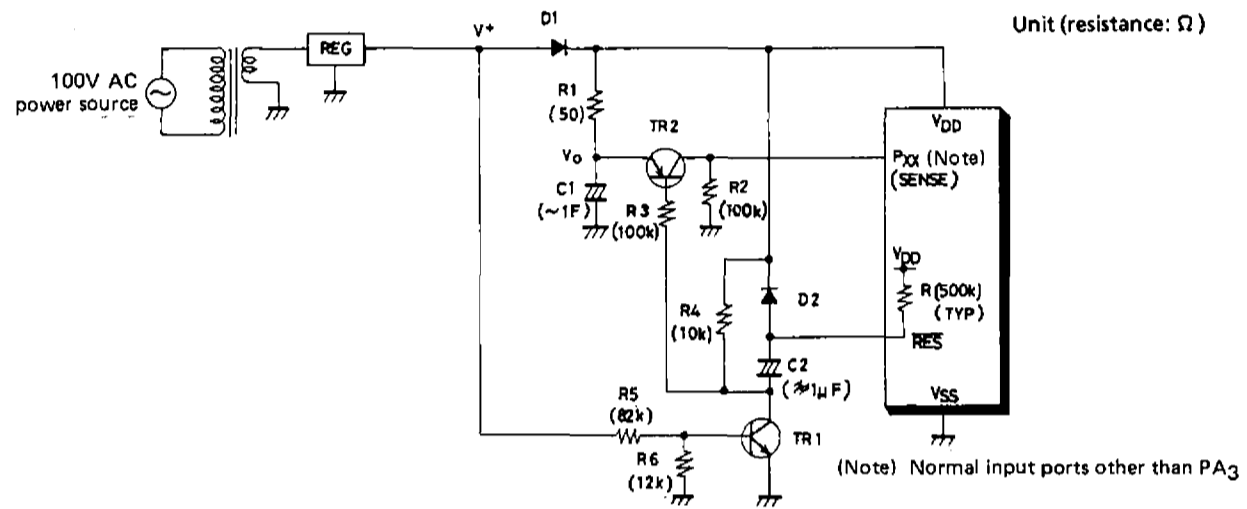


Fig. 2-3 Sample application – (2) where the standby function is used for power failure backup

2-2-2. Operating waveform in sample application circuit – (2)  
 The operating waveform in the sample application circuit in Fig. 2-3 is shown in Fig. 2-4. The mode is roughly divided as follows: a, Power-ON reset, b. Return from power failure backup.

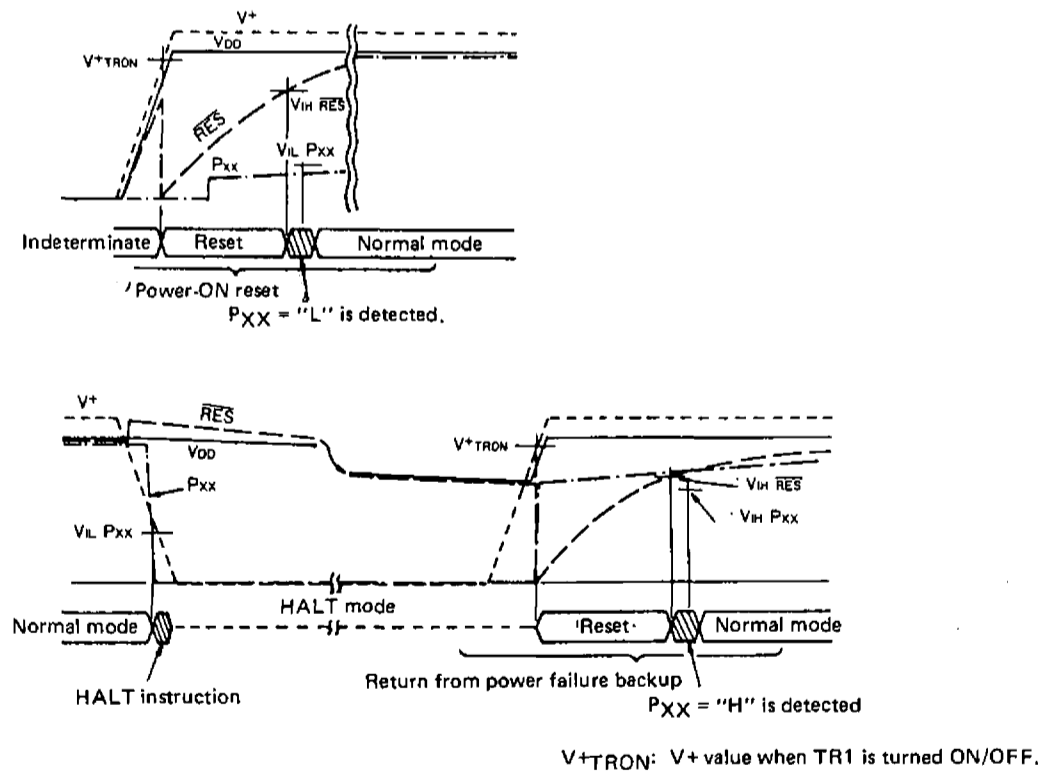


Fig. 2-4. Operating waveform – (2) in sample application circuit

**2-2-3. Operation of sample application circuit – (2)**

- (a) At the time of power-ON reset  
The operation and notes are the same as for sample application circuit – (1), except that after reset release P<sub>XX</sub> = "L" is program-detected to decide program start after initial reset.
- (b) Standby initiation  
When one polling regards the P<sub>XX</sub> input voltage as "L" level, the HALT mode is entered.
- (c) At the time of return from power failure backup  
After power is restored, a reset occurs, releasing the standby mode. After standby release P<sub>XX</sub> = "H" is program-detected, deciding program start after power is restored.

**– Note –**

If power is restored after V<sub>DD</sub> during power failure backup gets lower than V<sub>IH</sub> on the P<sub>XX</sub>, P<sub>XX</sub> = "L" may be program-detected, deciding program start after initial reset.

**2-2-4. Notes for design of sample application circuit – (2)**

- R<sub>2</sub> and R<sub>3</sub>  
Fix the R<sub>2</sub> value so that R<sub>2</sub> >> R<sub>1</sub> is yielded and fix the R<sub>3</sub> value so that I<sub>B</sub> of TR<sub>2</sub> is limited.
- R<sub>4</sub>  
There is no severe restriction on the R<sub>4</sub> value, but fix it so that C<sub>2</sub> can discharge quickly.  
Other notes are the same as for sample application circuit – (1).

**2-2-5. Notes for software design**

- Design the program so that port A<sub>0</sub> to A<sub>2</sub> cannot be used for standby release and port A<sub>3</sub> is brought to "H" level.
- Input a standby request to a normal input port other than the PA<sub>3</sub> and check by polling this input port once.

(Example)

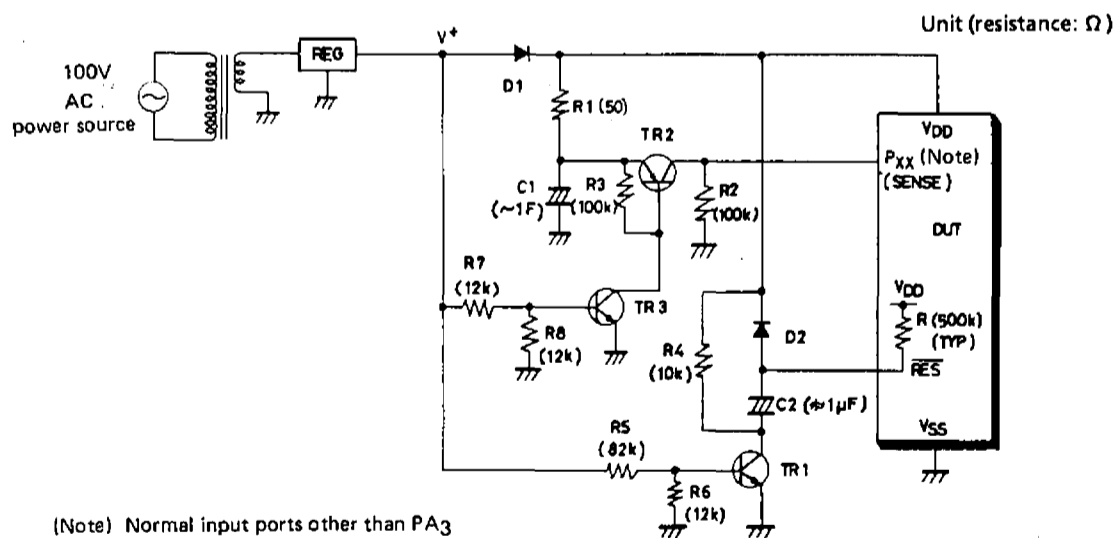
```

:
BP1      AAA      ; Polling
HALT     ; Standby
AAA:
:
    
```

**2-3. Sample application 3 where the standby function is used for power failure backup**

**2-3-1. Sample application circuit – (3) (There is an instantaneous break in power source.)**

Fig. 2-5. shows a sample application where the standby function is used for power failure backup.



(Note) Normal input ports other than PA<sub>3</sub>

**Fig. 2-5 Sample application – (3) where the standby function is used for power failure backup**



2-3-2. Operating waveform in sample application circuit – (3)

The operating waveform in the sample application circuit in fig. 2-5 is shown in Fig. 2-6. The mode is roughly divided as follows: a, Power-ON reset, b, Instantaneous break of main power, C, Return from power failure backup.

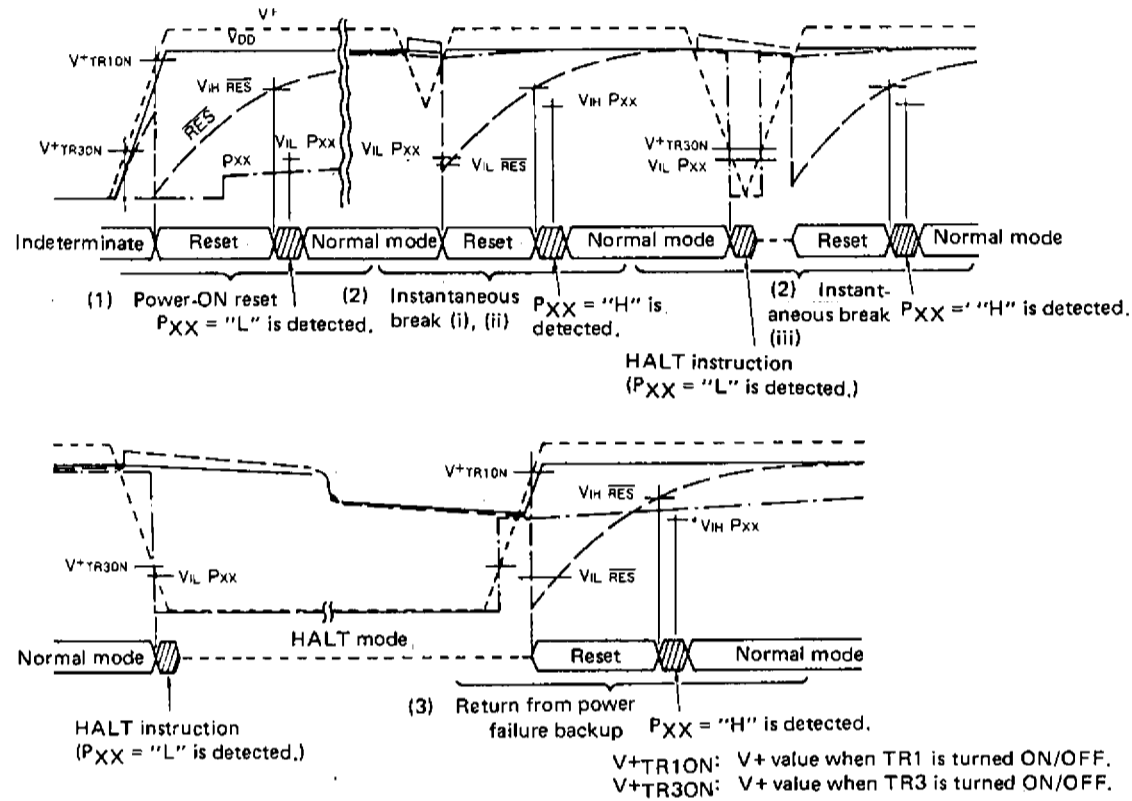


Fig. 2-6. Operating waveform in sample application circuit – (3)

2-3-3. Operation of sample application circuit – (3)

- (a) At the time of power-ON reset
 

The operation and notes are the same as for sample application circuit – (2)
- (b) At the time of instantaneous break
  - (i) When the  $P_{XX}$  input voltage does not meet  $V_{IL}$  (the  $P_{XX}$  input level does not get lower than input threshold level  $V_{IL}$ ) and the  $\overline{RES}$  input voltage only meets  $V_{IL}$ :  
A reset occurs in the normal mode. After reset release  $P_{XX} = "H"$  is program-detected, deciding program start after instantaneous break.
  - (ii) When both of the  $P_{XX}$  input voltage and  $\overline{RES}$  input voltage do not meet  $V_{IL}$ :  
The program continues running in the normal mode.
  - (iii) When both of the  $P_{XX}$  input voltage and  $\overline{RES}$  input voltage meet  $V_{IL}$ :  
When two pollings do not regard the  $P_{XX}$  input voltage as "L" level, the HALT mode is not entered and a reset occurs.  
When two pollings regard the  $P_{XX}$  input voltage as "L" level, the HALT mode is entered and after power is restored, a reset occurs, releasing the standby mode. After standby release  $P_{XX} = "H"$  is program-detected, deciding program start after instantaneous break.
- (c) At the time of return from power failure backup
 

The operation and notes are the same as for sample application circuit – (2)

**2-3-4. Notes for design of sample application circuit – (3)**

- R3  
Bias resistance of TR2
  - R7 and R8  
Fix the R7 and R8 values so that TR3 is turned ON/OFF at approximately 1.5V of V+.
- Other notes are the same as for sample application circuit – (1)

**2-3-5. Notes for software design**

Same as for sample application circuit – (1)

**2-4. Notes (1) for providing serial transfer**

Notes for providing power failure backup and serial transfer

This application assigns top priority to power failure backup. When power failure backup is provided, serial transfer may not be provided normally.

- (1) When the internal clock is used for the serial clock:  
Execute the serial transfer start instruction immediately before executing the HALT instruction. If this is done during serial transfer, the power failure backup mode is entered without normal transfer.
- (2) When the external clock is used for the serial clock:  
When power failure is detected, it is most prioritized that the HALT mode is entered, providing power failure backup. It is necessary to design an application system where no release signal by serial transfer completion is inputted to the HALT instruction executing cycle and no release signal is inputted during backup.

**2-5. Notes (2) for providing serial transfer**

Notes for providing HALT and serial transfer for program standby without power failure backup

This application assigns top priority to serial transfer. The following notes for system design must be observed.

- (1) When the internal clock is used for the serial clock:  
Transfer starts when it is ready on both sides. When transfer is not ready on the other side, the HALT instruction is executed to reduce the current dissipation. When transfer is ready, the HALT release signal ( $\overline{RES}$ , PA) causes return from the standby mode, starting serial transfer.
- (2) When the external clock is used for the serial clock:  
Synchronization must be provided between microcomputers to prevent the HALT instruction and HALT release signal (RSIOEND) from overlapping. When transfer is ready, the serial transfer start instruction is executed and the program is placed in the wait state. The other side adjusts thime so that no overlap occurs between the HALT instruction and transfer completion and starts serial transfer. On completion of transfer, the HALT mode is released and the program is executed with an instruction immediately following the HALT instruction.

LC6520C, 6520H, 6522C, 6522H

LC6520, LC6522 INSTRUCTION SET

Symbol Description

|      |                                   |                     |  |          |                          |
|------|-----------------------------------|---------------------|--|----------|--------------------------|
| AC   | : Accumulator                     | M(DP)               | : Memory addressed by DP                         | ( ), ( ) | : Contents               |
| ACt  | : Accumulator bit t               | P(DP <sub>L</sub> ) | : Input/output port addressed by DP <sub>L</sub> | -        | : Transfer and direction |
| CF   | : Carry flag                      | PC                  | : Program counter                                | +        | : Addition               |
| CTL  | : Control register                | STACK               | : Stack register                                 | -        | : Subtraction            |
| DP   | : Data pointer                    | TM                  | : Timer  | ∧        | : AND                    |
| E    | : E register                      | TMF                 | : Timer (internal) interrupt request flag        | ∨        | : OR                     |
| EXTF | : External interrupt request flag | At, Ma, La          | : Working register                               | ⊙        | : Exclusive OR           |
| Fn   | : Flag bit n                      | ZF                  | : Zero flag                                      |          |                          |
| M    | : Memory                          |                     |  |          |                          |

| Instruction group  | Mnemonic                                    | Instruction code  |   | Bytes  | Cycles | Function   | Description   | Status flag affected   | Remarks           |   |  |                |   |  |                |   |  |                |   |       |       |  |
|--|---|---|---|--|--------|--|---|--|-------------------|---|--|----------------|---|--|----------------|---|--|----------------|---|-------|-------|--|
|  |   | D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>         | D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub> |  |        |  |   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| Accumulator manipulation instructions                              | CLA   | Clear AC  | 1 1 0 0   | 0 0 0 0  | 1      | 1  | AC ← 0  | The AC contents are cleared.   | ZF                | * 1   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | CLC   | Clear CF  | 1 1 1 0   | 0 0 0 1  | 1      | 1  | CF ← 0  | The CF contents are cleared.   | CF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | STC   | Set CF  | 1 1 1 1   | 0 0 0 1  | 1      | 1  | CF ← 1  | The CF is set.   | CF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | CMA   | Complement AC   | 1 1 1 0   | 1 0 1 1  | 1      | 1  | AC ← $\overline{AC}$  | The AC contents are complemented.  | ZF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | INC   | Increment AC  | 0 0 0 0   | 1 1 1 0  | 1      | 1  | AC ← (AC) + 1   | The AC contents are incremented +1.  | ZF CF             |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | DEC   | Decrement AC  | 0 0 0 0   | 1 1 1 1  | 1      | 1  | AC ← (AC) - 1   | The AC contents are decremented -1.  | ZF CF             |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | RAL   | Rotate AC left through CF   | 0 0 0 0   | 0 0 0 1  | 1      | 1  | AC <sub>0</sub> ← (CF), AC <sub>n+1</sub> ← (AC <sub>n</sub> ), CF ← (AC <sub>0</sub> )   | The AC contents are shifted left through the CF.   | ZF CF             |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | TAE   | Transfer AC to E  | 0 0 0 0   | 0 0 1 1  | 1      | 1  | E ← (AC)  | The AC contents are transferred to the E.  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| XAE  | Exchange AC with E                          | 0 0 0 0   | 1 1 0 1   | 1  | 1      | (AC) ↔ (E)   | The AC contents and the E contents are exchanged.   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| Memory manipulation instructions                                   | INM   | Increment M   | 0 0 1 0   | 1 1 1 0  | 1      | 1  | M(DP) ← (M(DP)) + 1   | The M(DP) contents are incremented +1.   | ZF CF             |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | DEM   | Decrement M   | 0 0 1 0   | 1 1 1 1  | 1      | 1  | M(DP) ← (M(DP)) - 1   | The M(DP) contents are decremented -1.   | ZF CF             |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | SMB bit                                     | Set M data bit  | 0 0 0 0   | 1 0 B <sub>1</sub> B <sub>0</sub>              | 1      | 1  | M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 1   | A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is set.   |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | RMB bit                                     | Reset M data bit  | 0 0 1 0   | 1 0 B <sub>1</sub> B <sub>0</sub>              | 1      | 1  | M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 0   | A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is reset.   | ZF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
| Arithmetic operation/comparison instructions                       | AD  | Add M to AC   | 0 1 1 0   | 0 0 0 0  | 1      | 1  | AC ← (AC) + (M(DP))   | Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.   | ZF CF             |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | ADC   | Add M to AC with CF   | 0 0 1 0   | 0 0 0 0  | 1      | 1  | AC ← (AC) + (M(DP)) + (CF)  | Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.   | ZF CF             |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | DAA   | Decimal adjust AC in addition                                       | 1 1 1 0   | 0 1 1 0  | 1      | 1  | AC ← (AC) + 6   | 6 is added to the AC contents.   | ZF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | DAS   | Decimal adjust AC in subtraction                                    | 1 1 1 0   | 1 0 1 0  | 1      | 1  | AC ← (AC) + 10  | 10 is added to the AC contents.  | ZF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | EXL   | Exclusive OR M to AC  | 1 1 1 1   | 0 1 0 1  | 1      | 1  | AC ← (AC) ∨ (M(DP))   | The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.  | ZF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | AND   | And M to AC   | 1 1 1 0   | 0 1 1 1  | 1      | 1  | AC ← (AC) ∧ (M(DP))   | The AC contents and the M(DP) contents are ANDed and the result is stored in the AC.   | ZF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | OR  | Or M to AC  | 1 1 1 0   | 0 1 0 1  | 1      | 1  | AC ← (AC) ∨ (M(DP))   | The AC contents and the M(DP) contents are ORed and the result is stored in the AC.  | ZF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | CM  | Compare AC with M   | 1 1 1 1   | 1 0 1 1  | 1      | 1  | (M(DP)) - (AC) + 1  | The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset.<br><table border="1"> <tr><th>Comparison result</th><th>CF</th><th>ZF</th></tr> <tr><td>(M(DP)) &gt; (AC)</td><td>0</td><td>0</td></tr> <tr><td>(M(DP)) = (AC)</td><td>1</td><td>1</td></tr> <tr><td>(M(DP)) &lt; (AC)</td><td>1</td><td>0</td></tr> </table> | Comparison result | CF  | ZF   | (M(DP)) > (AC) | 0 | 0  | (M(DP)) = (AC) | 1 | 1  | (M(DP)) < (AC) | 1 | 0     | ZF CF |  |
|  | Comparison result                           | CF  | ZF  |  |        |  |   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | (M(DP)) > (AC)                              | 0   | 0   |  |        |  |   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| (M(DP)) = (AC)   | 1   | 1   |   |  |        |  |   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| (M(DP)) < (AC)   | 1   | 0   |   |  |        |  |   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| CI data  | Compare AC with immediate data              | 0 0 1 0<br>0 1 0 0  | 1 1 0 0<br>1 3 1 2 1 1 0                                    | 2  | 2      | (DP <sub>L</sub> ) + (AC) + 1  | The AC contents and the immediate data I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> are compared and the ZF and CF are set/reset.<br><table border="1"> <tr><th>Comparison result</th><th>CF</th><th>ZF</th></tr> <tr><td>I<sub>3</sub>I<sub>2</sub>I<sub>1</sub>I<sub>0</sub> &gt; (AC)</td><td>0</td><td>0</td></tr> <tr><td>I<sub>3</sub>I<sub>2</sub>I<sub>1</sub>I<sub>0</sub> = (AC)</td><td>1</td><td>1</td></tr> <tr><td>I<sub>3</sub>I<sub>2</sub>I<sub>1</sub>I<sub>0</sub> &lt; (AC)</td><td>1</td><td>0</td></tr> </table> | Comparison result  | CF                | ZF  | I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> > (AC) | 0              | 0 | I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> = (AC) | 1              | 1 | I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> < (AC) | 1              | 0 | ZF CF |       |  |
| Comparison result  | CF  | ZF  |   |  |        |  |   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> > (AC) | 0   | 0   |   |  |        |  |   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> = (AC) | 1   | 1   |   |  |        |  |   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> < (AC) | 1   | 0   |   |  |        |  |   |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| CLI data   | Compare DP <sub>L</sub> with immediate data | 0 0 1 0<br>0 1 0 1  | 1 1 0 0<br>1 3 1 2 1 1 0                                    | 2  | 2      | (DP <sub>L</sub> ) ∨ I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> | The DP <sub>L</sub> contents and the immediate data I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> are compared.   | ZF   |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
| Load/store instructions  | LI data                                     | Load AC with immediate data   | 1 1 0 0   | 1 3 1 2 1 1 0                                  | 1      | 1  | AC ← I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>  | The immediate data I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> is loaded in the AC.  | ZF                | * 1   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | S   | Store AC to M   | 0 0 0 0   | 0 0 1 0  | 1      | 1  | M(DP) ← (AC)  | The AC contents are stored in the M(DP).   |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | L   | Load AC from M  | 0 0 1 0   | 0 0 0 1  | 1      | 1  | AC ← (M(DP))  | The M(DP) contents are loaded in the AC.   | ZF                |   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | XM data                                     | Exchange AC with M, then modify DP <sub>H</sub> with immediate data | 1 0 1 0   | 0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub> | 1      | 2  | (AC) ↔ (M(DP))<br>DP <sub>H</sub> ← (DP <sub>H</sub> ) ∨ 0M <sub>2</sub> M <sub>1</sub> M <sub>0</sub>  | The AC contents and the M(DP) contents are exchanged and then the DP <sub>H</sub> contents are modified with the contents of (DP <sub>H</sub> ) ∨ 0M <sub>2</sub> M <sub>1</sub> M <sub>0</sub> .  | ZF                | The ZF is set/reset according to the result of (DP <sub>H</sub> ) ∨ 0M <sub>2</sub> M <sub>1</sub> M <sub>0</sub> . |  |                |   |  |                |   |  |                |   |       |       |  |
|  | X   | Exchange AC with M  | 1 0 1 0   | 0 0 0 0  | 1      | 2  | (AC) ↔ (M(DP))  | The AC contents and the M(DP) contents are exchanged.  | ZF                | The ZF is set/reset according to the DP <sub>H</sub> contents at the time of instruction execution.                 |  |                |   |  |                |   |  |                |   |       |       |  |
|  | XI  | Exchange AC with M, then increment DP <sub>L</sub>                  | 1 1 1 1   | 1 1 1 0  | 1      | 2  | (AC) ↔ (M(DP))<br>DP <sub>L</sub> ← (DP <sub>L</sub> ) + 1  | The AC contents and the M(DP) contents are exchanged and then the DP <sub>L</sub> contents are incremented +1.   | ZF                | The ZF is set/reset according to the result of (DP <sub>L</sub> + 1).   |  |                |   |  |                |   |  |                |   |       |       |  |
|  | XO  | Exchange AC with M, then decrement DP <sub>L</sub>                  | 1 1 1 1   | 1 1 1 1  | 1      | 2  | (AC) ↔ (M(DP))<br>DP <sub>L</sub> ← (DP <sub>L</sub> ) - 1  | The AC contents and the M(DP) contents are exchanged and then the DP <sub>L</sub> contents are decremented -1.   | ZF                | The ZF is set/reset according to the result of (DP <sub>L</sub> - 1).   |  |                |   |  |                |   |  |                |   |       |       |  |
| RTBL   | Read table data from program ROM            | 0 1 1 0   | 0 0 1 1   | 1  | 2      | AC, E ← ROM (PCh E AC)   | The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.  |  |                   |   |  |                |   |  |                |   |  |                |   |       |       |  |

LC6520C, 6520H, 6522C, 6522H

| Instruction group                          | Mnemonic                              | Instruction code  |             | Bytes                   | Cycles | Function     | Description   | Status flag affected   | Remarks |   |
|--|---------------------------------------|---|-------------|-------------------------|--------|--------------|---|--|---------|---|
|  |                                       | D7 D6 D5 D4   | D3 D2 D1 D0 |                         |        |              |   |  |         |   |
| Data pointer manipulation instructions     | LDZ data                              | Load DPH with Zero and DPL with immediate data respectively | 1 0 0 0     | 13 12 11 10             | 1      | 1            | DPH ← 0<br>DPL ← 13 12 11 10  | The DPH and DPL are loaded with 0 and the immediate data 13 12 11 10 respectively.   |         |   |
|  | LHI data                              | Load DPH with immediate data                                | 0 1 0 0     | 13 12 11 10             | 1      | 1            | DPH ← 13 12 11 10   | The DPH is loaded with the immediate data 13 12 11 10.   |         |   |
|  | IND                                   | Increment DPL   | 1 1 1 0     | 1 1 1 0                 | 1      | 1            | DPL ← (DPL) + 1   | The DPL contents are incremented +1.   | ZF      |   |
|  | DED                                   | Decrement DPL   | 1 1 1 0     | 1 1 1 1                 | 1      | 1            | DPL ← (DPL) - 1   | The DPL contents are decremented -1.   | ZF      |   |
|  | TAL                                   | Transfer AC to DPL  | 1 1 1 1     | 0 1 1 1                 | 1      | 1            | DPL ← (AC)  | The AC contents are transferred to the DPL.  |         |   |
|  | TLA                                   | Transfer DPL to AC  | 1 1 1 0     | 1 0 0 1                 | 1      | 1            | AC ← (DPL)  | The DPL contents are transferred to the AC.  | ZF      |   |
|  | XAH                                   | Exchange AC with DPH  | 0 0 1 0     | 0 0 1 1                 | 1      | 1            | (AC) ↔ (DPH)  | The AC contents and the DPH contents are exchanged.  |         |   |
| Working register manipulation instructions | XAt                                   | Exchange AC with working register At                        | 1 1 1 0     | 11 10                   | 1      | 1            | (AC) ↔ (A0)   | The AC contents and the contents of working register At are exchanged. At is assigned one of A0, A1, A2, A3 according to t1 t0.  |         |   |
|  | XA1                                   |   | 1 1 1 0     | 0 1 0 0                 |        |              | (AC) ↔ (A1)   |  |         |   |
|  | XA2                                   |   | 1 1 1 0     | 1 0 0 0                 |        |              | (AC) ↔ (A2)   |  |         |   |
|  | XA3                                   |   | 1 1 1 0     | 1 1 0 0                 |        |              | (AC) ↔ (A3)   |  |         |   |
|  | XHa                                   | Exchange DPH with working register Ha                       | 1 1 1 1     | 1 0 0 0                 | 1      | 1            | (DPH) ↔ (H0)  | The DPH contents and the contents of working register Ha are exchanged. Ha is assigned either of H0 or H1 according to a.  |         |   |
|  | XH1                                   |   | 1 1 1 1     | 1 1 0 0                 |        |              | (DPH) ↔ (H1)  |  |         |   |
| XLa  | Exchange DPL with working register La | 1 1 1 1   | 0 0 0 0     | 1                       | 1      | (DPL) ↔ (L0) | The DPL contents and the contents of working register La are exchanged. La is assigned either of L0 or L1 according to a. |  |         |   |
| XL1  |                                       | 1 1 1 1   | 0 1 0 0     |                         |        | (DPL) ↔ (L1) |   |  |         |   |
| Flag manipulation instructions             | SFB flag                              | Set flag bit  | 0 1 0 1     | B3 B2 B1 B0             | 1      | 1            | F <sub>n</sub> ← 1  | The flag specified with B3 B2 B1 B0 is set.  |         |   |
|  | RFB flag                              | Reset flag bit  | 0 0 0 1     | B3 B2 B1 B0             | 1      | 1            | F <sub>n</sub> ← 0  | The flag specified with B3 B2 B1 B0 is reset.  | ZF      | The flags are divided into 4 groups of F0 to F3, F4 to F7, F8 to F11, F12 to F15. The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data B3 B2 B1 B0. |
| Jump/subroutine instructions               | JMP addr                              | Jump in the current bank                                    | 0 1 1 0     | 1 P10 P9 P8 P7 P6 P5 P4 | 2      | 2            | PC ← PC11 (又 ← PC11) P10 P9 P8 P7 P6 P5 P4 P3 P2 P1 P0  | A jump to the address specified with the PC11 (or PC11) and immediate data P10 P9 P8 P7 P6 P5 P4 P3 P2 P1 P0 occurs.   |         | If the BANK and JMP instructions are executed consecutively, PC11 → PC11  |
|  | JPEA                                  | Jump in the current page modified by E and AC               | 1 1 1 1     | 1 0 1 0                 | 1      | 1            | PC7 ~ 0 ← (E, AC)   | A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.   |         |   |
|  | CZP addr                              | Call subroutine in the zero page                            | 1 0 1 1     | P3 P2 P1 P0             | 1      | 1            | STACK ← (PC) + 1<br>PC11 ~ 6, PC1 ~ 0 ← 0<br>PC5 ~ 2 ← P3 P2 P1 P0  | A subroutine in page 0 of bank 0 is called.  |         |   |
|  | CAL addr                              | Call subroutine in the zero bank                            | 1 0 1 0     | 1 P10 P9 P8 P7 P6 P5 P4 | 2      | 2            | STACK ← (PC) + 2<br>PC11 ~ 0 ← 0 P10 P9 P8 P7 P6 P5 P4 P3 P2 P1 P0  | A subroutine in bank 0 is called.  |         |   |
|  | RT                                    | Return from subroutine                                      | 0 1 1 0     | 0 0 1 0                 | 1      | 1            | PC ← (STACK)  | A return from a subroutine occurs.   |         |   |
|  | RTI                                   | Return from interrupt routine                               | 0 0 1 0     | 0 0 1 0                 | 1      | 1            | PC ← (STACK)<br>CF ZF ← CSF, ZSF  | A return from an interrupt service routine occurs.   | ZF CF   |   |
|  | BANK                                  | Change bank   | 1 1 1 1     | 1 1 0 1                 | 1      | 1            | PC11 ← (PC11)   | The bank is changed.   |         | Effective only when used immediately before the JMP instruction.  |
| Branch instructions                        | BAt addr                              | Branch on AC bit  | 0 1 1 1     | 0 0 1 1 t0              | 2      | 2            | PC7 ~ 0 ← P7 P6 P5 P4 P3 P2 P1 P0<br>if ACt = 1   | If a single bit of the AC specified with the immediate data t1 t0 is 1, a branch to the address specified with the immediate data P7 P6 P5 P4 P3 P2 P1 P0 within the same page occurs.     |         | Mnemonic is BA0 to BA3 according to the value of t.   |
|  | BNAt addr                             | Branch on no AC bit   | 0 0 1 1     | 0 0 1 1 t0              | 2      | 2            | PC7 ~ 0 ← P7 P6 P5 P4 P3 P2 P1 P0<br>if ACt = 0   | If a single bit of the AC specified with the immediate data t1 t0 is 0, a branch to the address specified with the immediate data P7 P6 P5 P4 P3 P2 P1 P0 within the same page occurs.     |         | Mnemonic is BNA0 to BNA3 according to the value of t.   |
|  | BMt addr                              | Branch on M bit   | 0 1 1 1     | 0 1 1 1 t0              | 2      | 2            | PC7 ~ 0 ← P7 P6 P5 P4 P3 P2 P1 P0<br>if (M[DP, t1 t0]) = 1  | If a single bit of the M(DP) specified with the immediate data t1 t0 is 1, a branch to the address specified with the immediate data P7 P6 P5 P4 P3 P2 P1 P0 within the same page occurs.  |         | Mnemonic is BM0 to BM3 according to the value of t.   |
|  | BNMt addr                             | Branch on no M bit  | 0 0 1 1     | 0 1 1 1 t0              | 2      | 2            | PC7 ~ 0 ← P7 P6 P5 P4 P3 P2 P1 P0<br>if (M[DP, t1 t0]) = 0  | If a single bit of the M(DP) specified with the immediate data t1 t0 is 0, a branch to the address specified with the immediate data P7 P6 P5 P4 P3 P2 P1 P0 within the same page occurs.  |         | Mnemonic is BNM0 to BNM3 according to the value of t.   |
|  | BPt addr                              | Branch on Port bit  | 0 1 1 1     | 1 0 1 1 t0              | 2      | 2            | PC7 ~ 0 ← P7 P6 P5 P4 P3 P2 P1 P0<br>if (P[DP, t1 t0]) = 1  | If a single bit of port P(DP) specified with the immediate data t1 t0 is 1, a branch to the address specified with the immediate data P7 P6 P5 P4 P3 P2 P1 P0 within the same page occurs. |         | Mnemonic is BP0 to BP3 according to the value of t.   |
|  | BNPt addr                             | Branch on no Port bit                                       | 0 0 1 1     | 1 0 1 1 t0              | 2      | 2            | PC7 ~ 0 ← P7 P6 P5 P4 P3 P2 P1 P0<br>if (P[DP, t1 t0]) = 0  | If a single bit of port P(DP) specified with the immediate data t1 t0 is 0, a branch to the address specified with the immediate data P7 P6 P5 P4 P3 P2 P1 P0 within the same page occurs. |         | Mnemonic is BNPD to BNPD3 according to the value of t.  |
|  | BTM addr                              | Branch on timer   | 0 1 1 1     | 1 1 0 0                 | 2      | 2            | PC7 ~ 0 ← P7 P6 P5 P4 P3 P2 P1 P0<br>if TMF = 1<br>then TMF ← 0   | If the TMF is 1, a branch to the address specified with the immediate data P7 P6 P5 P4 P3 P2 P1 P0 within the same page occurs. The TMF is reset.  | TMF     |   |

LC6520C, 6520H, 6522C, 6522H

| Instruction group         | Mnemonic              | Instruction code  |  | Bytes  | Cycles | Function  | Description <sup>1)</sup>  | Status flag affected   | Remarks  |  |
|---------------------------|-----------------------|---|--|--|--------|---|--|--|--|--|
|                           |                       | D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> | D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>            |  |        |   |  |  |  |  |
| Branch instructions       | BNTM addr             | Branch on no timer  | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 0 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>   | 2      | 2   | PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if TMF = 0<br>then TMF ← 0   | If the TMF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The TMF is reset.  | TMF  |  |
|                           | BI addr               | Branch on interrupt   | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 0 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>   | 2      | 2   | PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if EXTF = 1<br>then EXTF ← 0 | If the EXTF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The EXTF is reset.  | EXTF   |  |
|                           | BNI addr              | Branch on no interrupt                                      | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 0 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>   | 2      | 2   | PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if EXTF = 0<br>then EXTF ← 0 | If the EXTF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The EXTF is reset.  | EXTF   |  |
|                           | BC addr               | Branch on CF  | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>   | 2      | 2   | PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if CF = 1                    | If the CF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |  |  |
|                           | BNC addr              | Branch on no CF   | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>   | 2      | 2   | PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if CF = 0                    | If the CF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |  |  |
|                           | BZ addr               | Branch on ZF  | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>   | 2      | 2   | PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if ZF = 1                    | If the ZF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |  |  |
|                           | BNZ addr              | Branch on no ZF   | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>   | 2      | 2   | PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if ZF = 0                    | If the ZF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |  |  |
|                           | BF <sub>n</sub> addr  | Branch on flag bit  | 1 1 0 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2      | 2   | PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if F <sub>n</sub> = 1        | If the flag bit of the 16 flags specified with the immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. |  | Mnemonic is BF0 to BF15 according to the value of n.             |
|                           | BNF <sub>n</sub> addr | Branch on no flag bit                                       | 1 0 0 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2      | 2   | PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if F <sub>n</sub> = 0        | If the flag bit of the 16 flags specified with the immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. |  | Mnemonic is BN0 to BN15 according to the value of n.             |
| Input/Output instructions | IP                    | Input port to AC  | 0 0 0 0  | 1 1 0 0  | 1      | 1   | AC ← (P <sub>1</sub> DP <sub>1</sub> )   | Port P(DP <sub>1</sub> ) contents are loaded in the AC.  | ZF   |  |
|                           | OP                    | Output AC to port   | 0 1 1 0  | 0 0 0 1  | 1      | 1   | P(DP <sub>1</sub> ) ← (AC)   | The AC contents are outputted to port P(DP <sub>1</sub> ).   |  |  |
|                           | SPB bit               | Set port bit  | 0 0 0 0  | 0 1 B <sub>1</sub> B <sub>0</sub>  | 1      | 2   | P(DP <sub>1</sub> , B <sub>1</sub> B <sub>0</sub> ) ← 1  | A single bit in port P(DP <sub>1</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is set.   |  | When this instruction is executed, the E contents are destroyed. |
| RPB bit                   | Reset port bit        | 0 0 1 0   | 0 1 B <sub>1</sub> B <sub>0</sub>                                      | 1  | 2      | P(DP <sub>1</sub> , B <sub>1</sub> B <sub>0</sub> ) ← 0 | A single bit in port P(DP <sub>1</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is reset.   | ZF   | When this instruction is executed, the E contents are destroyed. |  |
| Other instructions        | SCTL bit              | Set control register bit(S)                                 | 0 0 1 0<br>1 0 0 0   | 1 1 0 0<br>B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>   | 2      | 2   | CTL ← (CTL) V<br>B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>   | The bits of the control register specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> are set.  |  |  |
|                           | RCTL bit              | Reset control register bit(S)                               | 0 0 1 0<br>1 0 0 1   | 1 1 0 0<br>B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>   | 2      | 2   | CTL ← (CTL) A<br>B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>   | The bits of the control register specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> are reset.  | ZF   |  |
|                           | WTTM                  | Write timer   | 1 1 1 1  | 1 0 0 1  | 1      | 1   | TM ← (E), (AC)<br>TMF ← 0  | The E and AC contents are loaded in the timer. The TMF is reset.   | TMF  |  |
|                           | HALT                  | Halt  | 1 1 1 1  | 0 1 1 0  | 1      | 1   | Halt   | All operations stop.   |  | Only when all pins of port PA are set at L, stop.                |
|                           | NOP                   | No operation  | 0 0 0 0  | 0 0 0 0  | 1      | 1   | No operation   | No operation is performed, but 1 machine cycle is consumed.  |  |  |

\*1 If the CLA instruction is used consecutively in such a manner as CLA, CLA, ———, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.

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