

SANYO

No.2577B

LC6538D

**SINGLE-CHIP 4-BIT MICROCOMPUTER FOR
LARGE-SCALE CONTROL-ORIENTED APPLICATIONS**
(with FLT Controller/Drivers, Comparator, PWM Output, 8K Byte-ROM)

The LC6538D is a single-chip 4-bit microcomputer placed in a 64-pin package. It contains a high-speed CPU (minimum cycle time: $0.92\mu\text{s}$) which is the heart of the LC6538D, an 8K-byte ROM, a 448-word RAM, an automatic FLT display controller/drivers, a dual 8-bit serial I/O port, an 8-bit timer, an interval timer capable of delivering 14-bit PWM output signal or 8-bit + 6-bit PWM output signal, a 14-bit time-keeping time base timer which can be also used as an event counter or watchdog timer, a 4-channel comparator input port, a horizontal sync detection counter, and provides 8 interrupt sources with 4 vector addresses. The LC6538D has 2 crystal oscillators (4.19MHz and 32.768kHz) which make it possible to select either clock signal for system clock or time-keeping as required and also make it possible to use either clock signal to continue time-keeping in the standby mode. The LC6538D is especially suited for use in VCR, CD, ECR applications. In particular, the LC6538D is so designed as to facilitate processing of the time-keeping/timer function, voltage/frequency synthesizer tuner control, remote control signal reception, tape counter, etc. on a single chip. Since the FLT display controller has the static output mode and structure capable of being also used as a general-purpose output port, the LC6538D is also especially suited for use in VCR, CD system/servo controller applications.

Features

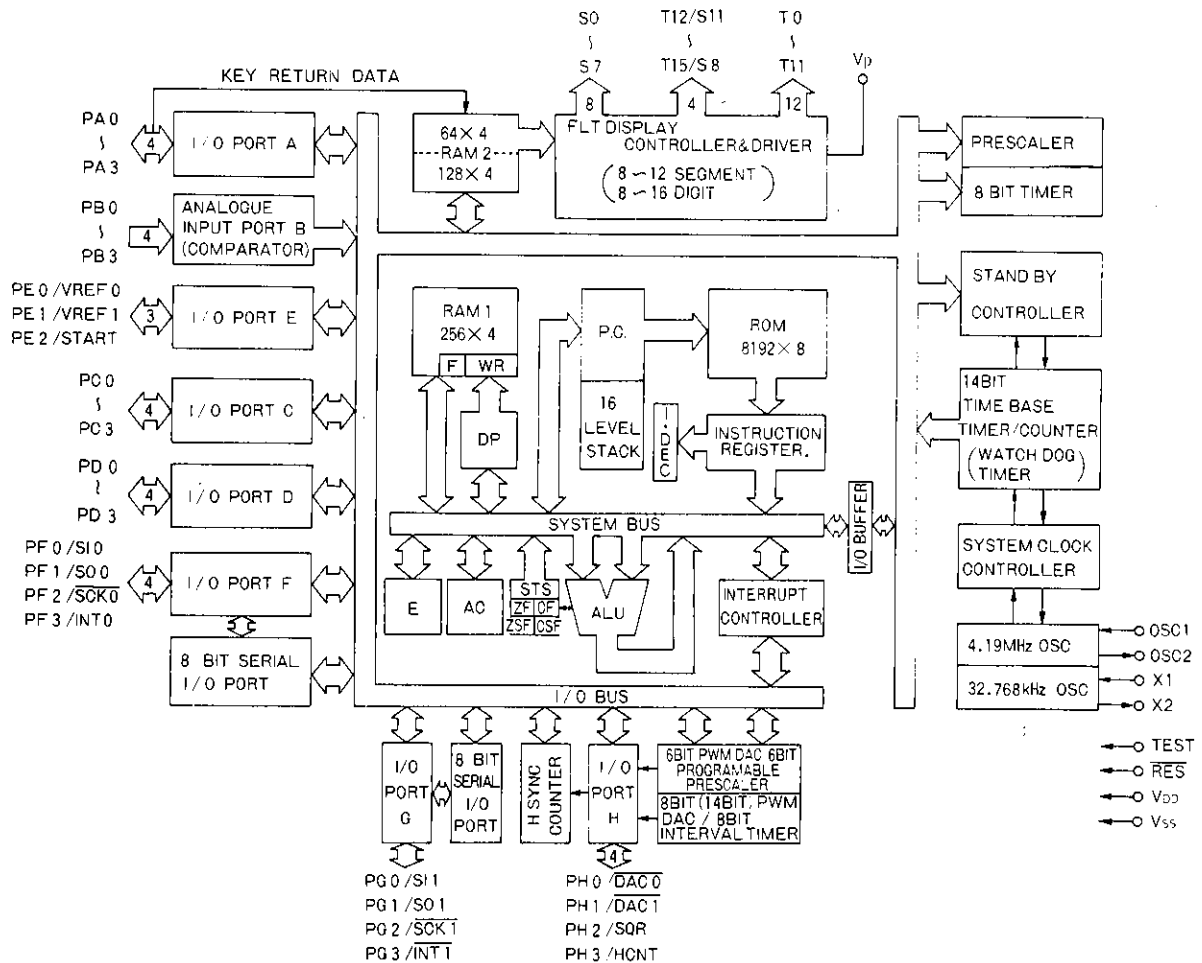
- 78 instructions
- On-chip 8192-byte ROM, 448x4-bit RAM (64x4 bits of the 448x4-bit RAM are used both for data memory and display, KEY Return Data memory.)
- Minimum instruction cycle time: $0.92\mu\text{s}$ (4.33MHz, $V_{DD} \geq 4.5\text{V}$)
 $61\mu\text{s}$ (32.768kHz, $V_{DD} \geq 2.7\text{V}$)
- Power-down function available when a system clock signal is selected (program-selectable)
 - When 4.19MHz clock signal is selected: $0.95\mu\text{s}$, $1.9\mu\text{s}$, $30.6\mu\text{s}$
 - When 32.768kHz clock signal is selected: $61\mu\text{s}$
- Working register/flag function
 - (16 flags + 8 working registers) x 4 banks
- Stack level: 16 levels
- I/O port: 55 pins in all
 - Input-only port 4 pins (common with comparator input)
 - Input/output common port 27 pins (high-current port for LED drive: 8 pins)
 - Output-only port 24 pins (FLT direct drive capability, high-current output for digits: 16 pins)
- On-chip FLT display controller
 - Number of segments: 8 to 12 Program-selectable
 - Number of digits: 16 to 8 Program-selectable
- On-chip automatic KEY Return Data input function
 - 4x15-bit
- Timer: 3 channels
 - 6-bit prescaler + 8-bit programmable timer
 - Interval timer: Common with PWM DAC, capable of frequency division for melody generation
 - Time-keeping time base timer: On-chip 14-stage frequency divider
- PWM DAC output: Common with Timer 1 (Interval Timer)
 - 6-bit PWM DAC + 8-bit PWM DAC or 14-bit PWM DAC
- Serial input/output interface (LSB first)
 - 8-bit input/output x 2 channels or 16-bit input/output x 1 channel
- Interrupt function: 8 sources, 4 vector addresses
 - External interrupt 2 lines
 - Timer interrupt 3 lines
 - Serial I/O interrupt 2 lines
 - Digit interrupt 1 line
- On-chip comparator for AFC signal detection (4 channels)

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LC6538D

- On-chip watchdog timer: Common with time-keeping time base timer (Option)
- On-chip 9-bit counter for horizontal sync detection
- On-chip OSC stabilizing time wait function in the reset mode
- OSC circuit: 2 channels
 - Main clock: 4.19MHz crystal OSC or 4.0MHz ceramic resonator OSC
 - Subclock: 32.768kHz crystal OSC
- Standby function: 2 modes of HALT and HOLD
- Supply voltage: 2.7 to 6.0V
- Package: DIP-64S
- Evaluation LSI: LC6593 (evaluation chip) + EVA800-TB6593 (evaluation chip board)
LC65PG38D (piggyback)

System Block Diagram

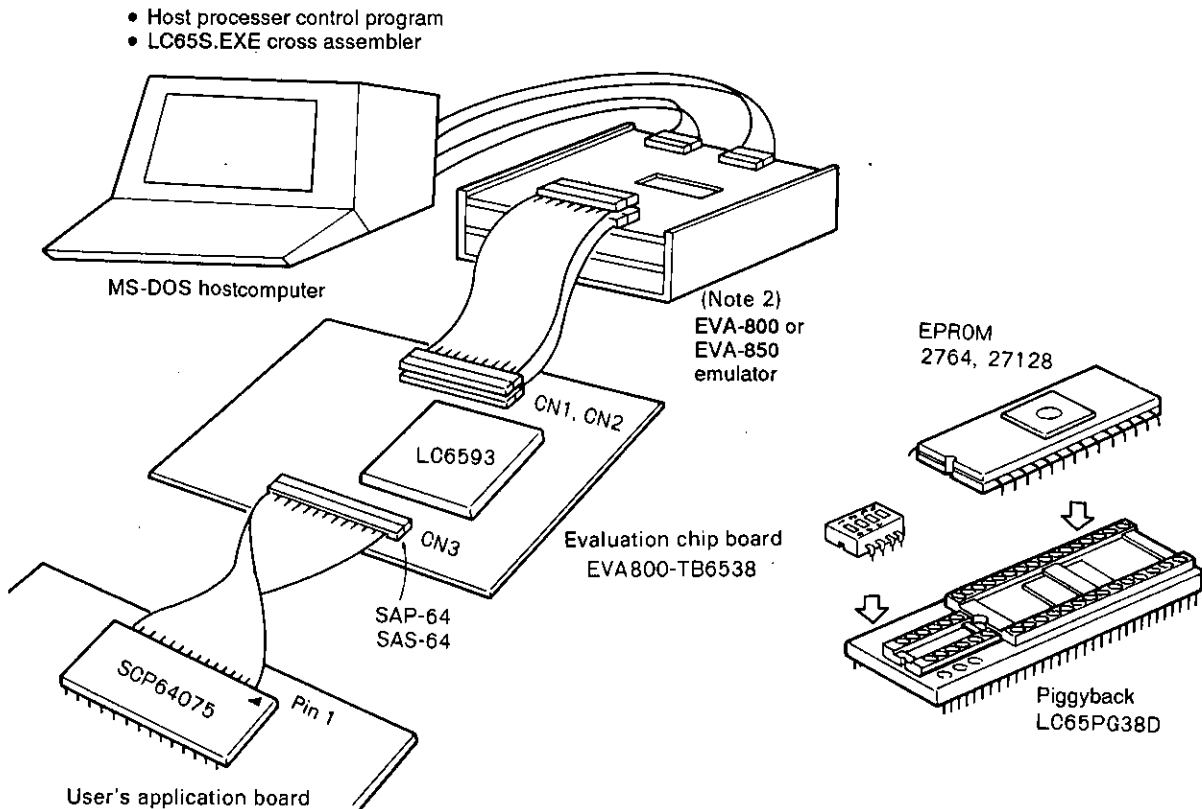


Development Support Tools

The following tools are provided to support the program development for the LC6538D microcomputer.

- (1) User's Manual
"LC6538D User's Manual" (Issued in February, 1988)
- (2) Development Tool Manual
This contains the basic information on the EVA-800. For more detailed information on the LC6538D, refer to the description of Development Support Tools in "LC6538D User's Manual".
- (3) Development Tools
 - ① For program development (Note 1)
 - i. MS-DOS-based host system and cross-assembler
 - ii. Cross assembler MS-DOS base cross assembler: (LC65S.EXE)
 - ② For program evaluation
 - i. Evaluation chip : LC6593
 - ii. Piggyback microcomputer: LC65PG38D
 - iii. Emulator : The EVA-800 controller board and evaluation chip board, or the EVA-850 emulator and evaluation chip board

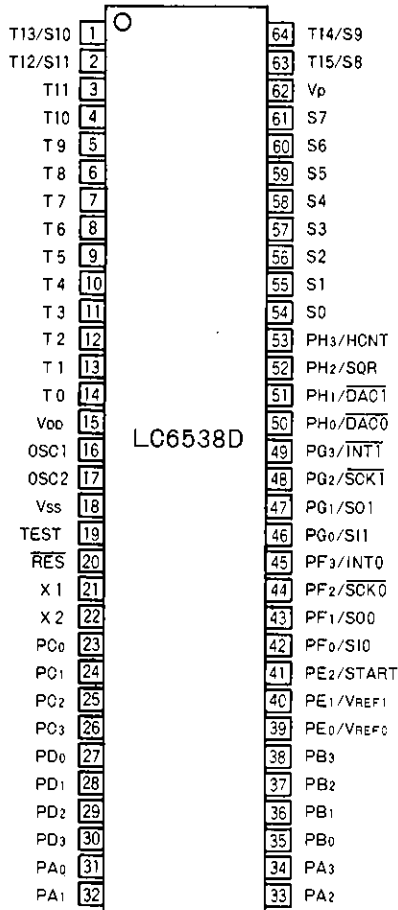
Appearance of Development Support System



(Note 1) MS-DOS: Trademark of MicroSoft Corporation

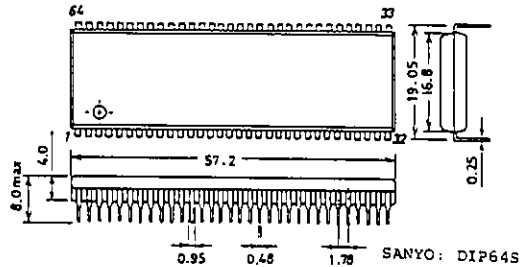
(Note 2) The EVA-800, EVA-850 is a general term for emulator. A suffix (A, B, ...) is added at the end of EVA-800, EVA-850 as the EVA-800, EVA-850 is improved to be a newer version. Do not use the EVA-800, EVA-850 with no suffix added.

Pin Assignment



- OSC1, OSC2 : Crystal or ceramic resonator OSC circuit for main OSC
- X1, X2 : Crystal OSC circuit for sub-OSC
- PA0-3 : Input/output common port A0-3, +15V breakdown voltage
- PB0-3 : Reference voltage variable input-only port B0-3
- PC0-3 : Input/output common port C0-3, +15V breakdown voltage
- PD0-3 : Input/output common port D0-3, +15V breakdown voltage
- PE0-2 : Input/output common port E0-2, PE2 only has +15V breakdown voltage.
- PF0-3 : Input/output common port F0-3, +15V breakdown voltage
- PG0-3 : Input/output common port G0-3, +15V breakdown voltage
- PH0-3 : Input/output common port H0-3, +15V breakdown voltage
- T0-T11 : Output port for digit only
- T12/S11-T15/S8 : Output port for both digit/segment } P-channel high-voltage output
- S0-S7 : Output port for segment only
- Vp : Power supply pin for P-channel high-voltage output port
- RES : Reset
- TEST : Test
- VDD, VSS : Power supply pin
- VREF0 : Comparator 0 reference voltage input pin
- VREF1 : Comparator 1 reference voltage input pin
- START : HALT control pin
- S10 : 8-bit/16-bit serial input port
- S00 : 8-bit/16-bit serial output port
- SCK0 : Input/output for serial clock 0
- INT0 : Interrupt 0 request input
- S11 : 8-bit serial input port
- SO1 : 8-bit serial output port
- SCK1 : Input/output for serial clock 1
- INT1 : Interrupt 1 request input
- DAC0 : 6-bit PWM output
- DAC1 : 6-bit/14-bit PWM output
- SQR : Burst pulse output
- HCNT : Horizontal sync detection input

Package Dimensions 3071-D64IC
(unit: mm)



Pin Description

PU: Output with pull-up MOS
OD: Open drain output

Pin Name	Pins	I/O	Functions	Output Driver	Option	During Reset
VDD	1	—	Power supply pin	—	—	—
VSS	1	—				
TEST	1	I	LSI test pin. Must be connected to VSS.	—	—	—
RES	1	I	System reset input Initial reset at RES=L	—	—	—
OSC1	1	I	Pin used for main system clock OSC For the external clock mode, the OSC2 is made open and the external clock is applied to the OSC1. With feedback resistance	—	—	—
OSC2	1	O				
X1	1	I	Pin used for sub-clock OSC For the external clock mode, the X2 is made open and the external clock is applied to the X1. With feedback resistance, damping resistance	—	—	—
X2	1	O				
T0 to T11	12	O	Output for FLT digit only Outputs a fixed address in the display RAM at the static mode.	Pch high breakdown voltage High-current type	Presence or absence of pull-down resistance (in bit units)	L
T12/S11 to T15/S8	4	O	Output for FLT digit/segment Outputs a fixed address in the display RAM at the static mode.	Pch high breakdown voltage High-current type	Presence or absence of pull-down resistance (in bit units)	L
S0 to S7	8	O	Output for FLT segment only Outputs a fixed address in the display RAM at the static mode.	Pch high breakdown voltage Medium-current type	Presence or absence of pull-down resistance (in bit units)	L
Vp	1		Power supply pin for FLT output pull-down resistance	—	—	—
PA0 to PA3	4	I/O	4-bit and single-bit input/output The input is of low threshold type for key scan and has the function to automatically fetch the key scan data into the RAM.	+15V breakdown voltage Medium-current type	PU or OD to be specified in bit units	H
PB0 to PB3	4	I	With 4-channel independent comparator Internal/external reference voltage selectable 4-bit/single-bit input The input function stops at the low-speed mode (1/32 mode, sub-clock mode).	—	—	Input function stop
PC0 to PC3	4	I/O	4-bit and single-bit input/output	+15V breakdown voltage High-current type	• PU or OD to be specified in bit units • Output at the reset mode	H/L (option)
PD0 to PD3	4	I/O	4-bit and single-bit input/output	+15V breakdown voltage High-current type	• PU or OD to be specified in bit units • Output at the reset mode	H/L (option)

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Pin Name	Pins	I/O	Functions	Output Driver	Option	During Reset
PE ₀ to PE ₂	3	I/O	3-bit and single-bit input/output PE ₀ /VREF ₀ Common with external reference voltage input of PB _{1..3} PE ₁ /VREF ₁ Common with external reference voltage input of PB ₀ PE ₂ /START Common with HALT mode control START	PE ₂ only: +15V breakdown voltage Other pins: Normal voltage Medium-current type	PU or OD to be specified in bit units	H
PF ₀ to PF ₃	4	I/O	4-bit and single-bit input/output PF ₀ /SIO Common with serial input SIO PF ₁ /SOO Common with serial output SOO PF ₂ /SCK ₀ Common with serial clock input/output SCK ₀ PF ₃ /INT ₀ Common with INT ₀ interrupt input	+15V breakdown voltage Medium-current type	PU or OD to be specified in bit units	H
PG ₀ to PG ₃	4	I/O	4-bit and single-bit input/output PG ₀ /SI ₁ Common with serial input SI ₁ PG ₁ /SO ₁ Common with serial output SO ₁ PG ₂ /SCK ₁ Common with serial clock input/output SCK ₁ PG ₃ /INT ₁ Common with INT ₁ interrupt input	+15V breakdown voltage Medium-current type	PU or OD to be specified in bit units	H
PH ₀ to PH ₃	4	I/O	4-bit and single-bit input/output PH ₀ /DAC ₀ Common with 6-bit PWM D/A output PH ₁ /DAC ₁ Common with 8/14-bit PWM D/A output PH ₂ /SQR Common with burst pulse output PH ₃ /HCNT Common with horizontal sync detection input	+15V breakdown voltage Medium-current type	PU or OD to be specified in bit units	H

User Options

1) Option of ports C, D Output Level at the Reset Mode.

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output at the reset mode: "H" level	All of 4 bits of ports C, D
2. Output at the reset mode: "L" level	All of 4 bits of ports C, D

2) Option of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option (in bit units).

Option Name	Circuit	Conditions, etc.
1. Open drain output		Ports A, C, D, E, F, G, H
		T0~T11, T12/S11~T15/S8, S0~S7
2. Output with pull-up resistance		Ports A, C, D, E, F, G, H
3. Output with pull-down resistance		T0~T11, T12/S11~T15/S8, S0~S7

3) Watchdog Reset Option

The presence or absence of the time base timer-used watchdog reset function may be selected by option.

Option Name	Conditions, etc.
1. With watchdog reset function	Programming must be made so that the time base interrupt request flag is reset within a certain period of time not to cause the watchdog reset to be performed as long as no runaway occurs.
2. Without watchdog reset function	—

LC6538D Electrical Characteristics

1. Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Applicable Pins, Remarks	Conditions	Limits	Unit
Maximum Supply Voltage	$V_{DD\text{ max}}$	V _{DD}		-0.3 to +7.0	V
Output Voltage	$V_{O(1)}$	X2, OSC2		Allowable up to voltage generated	V
	$V_{O(2)}$	T0 to T11, T12/S11 to T15/S8, S0 to S7		$V_{DD}-45$ to $V_{DD}+0.3$	V
Input Voltage	$V_{I(1)}$	X1, OSC1		Allowable up to voltage generated	V
	$V_{I(2)}$	TEST, RES, PBO to 3, OSC1, X1 at external clock mode		-0.3 to $V_{DD}+0.3$	V
	$V_{I(3)}$	Vp		$V_{DD}-45$ to $V_{DD}+0.3$	V
Input/Output Voltage	$V_{IO(1)}$	Ports A,C,D,E2,F,G,H	At open drain output option	-0.3 to +15	V
	$V_{IO(2)}$	Ports E0,E1		-0.3 to $V_{DD}+0.3$	V
Ports A,C,D,E2,F,G,H		At pull-up MOS-provided output option		-0.3 to $V_{DD}+0.3$	V
Peak Output Current	$I_{OP(1)}$	Ports A,E,F,G,H		-2 to 10	mA
	$I_{OP(2)}$	Ports C,D		-2 to 30	mA
	$I_{OP(3)}$	T0 to T11, T12/S11 to T15/S8		-30 to 0	mA
		S0 to S7		-10 to 0	mA
Average Output Current	$I_{OA(1)}$	Ports A,E,F,G,H	Per pin Average over the period of 100 msec.	-2 to 10	mA
	$I_{OA(2)}$	Ports C,D	Per pin Average over the period of 100 msec.	-2 to 30	mA
	$I_{OA(3)}$	T0 to T11, T12/S11 to T15/S8	Per pin Average over the period of 100 msec.	-30 to 0	mA
		S0 to S7	Per pin Average over the period of 100 msec.	-10 to 0	mA
	$\Sigma I_{OA(1)}$	Ports A,E	Total current of all applicable pins Average over the period of 100msec.	-14 to 20	mA
	$\Sigma I_{OA(2)}$	Ports F,G,H	Total current of all applicable pins Average over the period of 100msec.	-24 to 60	mA
	$\Sigma I_{OA(3)}$	Ports C,D	Total current of all applicable pins Average over the period of 100msec.	-16 to 80	mA
	$\Sigma I_{OA(4)}$	T0 to T11, T12/S11 to T15/S8, S0 to S7	Total current of all applicable pins Average over the period of 100msec.	-100 to 0	mA
Allowable Power Dissipation	$P_d\text{ max}$	DIP64S	$T_a = -30$ to $+70^\circ\text{C}$	600	mW
Operating Temperature	T_{opr}			-30 to +70	$^\circ\text{C}$
Storage Temperature	T_{stg}			-55 to +125	$^\circ\text{C}$

2. Allowable Operating Conditions at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Applicable Pins, Remarks	Conditions	Limits				Unit
				$V_{DD}[\text{V}]$	min	typ	max	
Operating Supply Voltage (Including supply voltage at standby mode)	$V_{DD}(1)$	VDD	$0.92\mu\text{s} \leq T_{\text{cyc}} < 1.9\mu\text{s}$	—	4.5		6.0	V
	$V_{DD}(2)$	VDD	$1.9\mu\text{s} \leq T_{\text{cyc}} \leq 6\mu\text{s}$	—	4.0		6.0	V
	$V_{DD}(3)$	VDD	$6\mu\text{s} < T_{\text{cyc}} \leq 67\mu\text{s}$	—	3.0		6.0	V
	$V_{DD}(4)$	VDD	4.19MHz OSC stop, 32kHz OSC operating	—	2.7		6.0	V
Memory Retention Supply Voltage	VST	VDD	At operation completely stopped mode (HOLD mode)	—	1.8		6.0	V
"H"-Level Input Voltage	$V_{IH}(1)$	Port A of OD type	Output Nch Tr OFF	3.0 to 6.0	1.90		13.5	V
	$V_{IH}(2)$	Port A of PU type	Output Nch Tr OFF	3.0 to 6.0	1.90		V_{DD}	V
	$V_{IH}(3)$	Ports C, D of OD type	Output Nch Tr OFF	4.5 to 6.0	$0.70V_{DD}$		13.5	V
				3.0 to 6.0	$0.75V_{DD}$		13.5	V
	$V_{IH}(4)$	Ports C, D of PU type	Output Nch Tr OFF	4.5 to 6.0	$0.70V_{DD}$		V_{DD}	V
				3.0 to 6.0	$0.75V_{DD}$		V_{DD}	V
	$V_{IH}(5)$	Ports E2, F to H of OD type	Output Nch Tr OFF	4.5 to 6.0	$0.75V_{DD}$		13.5	V
				3.0 to 6.0	$0.80V_{DD}$		13.5	V
	$V_{IH}(6)$	Ports E2, F to H of PU type	Output Nch Tr OFF	4.5 to 6.0	$0.75V_{DD}$		V_{DD}	V
				3.0 to 6.0	$0.80V_{DD}$		V_{DD}	V
$V_{IH}(7)$	Ports E0, E1	Output Nch Tr OFF	4.5 to 6.0	$0.75V_{DD}$		V_{DD}	V	
			3.0 to 6.0	$0.80V_{DD}$		V_{DD}	V	
$V_{IH}(8)$	Port B	At internal reference voltage mode	4.0 to 6.0	$0.65V_{DD}$		V_{DD}	V	
$V_{IH}(9)$	OSC1, X1	Fig. 5, Fig. 6	4.5 to 6.0	$0.70V_{DD}$		V_{DD}	V	
			3.0 to 6.0	$0.80V_{DD}$		V_{DD}	V	
$V_{IH}(10)$	RES	Fig. 7	4.5 to 6.0	$0.75V_{DD}$		V_{DD}	V	
			1.8 to 6.0	$0.80V_{DD}$		V_{DD}	V	
"L"-Level Input Voltage	$V_{IL}(1)$	Port A	Output Nch Tr OFF	4.5 to 6.0	V_{SS}		0.5	V
				3.0 to 6.0	V_{SS}		0.35	V
	$V_{IL}(2)$	Ports C, D	Output Nch Tr OFF	4.5 to 6.0	V_{SS}		$0.30V_{DD}$	V
				3.0 to 6.0	V_{SS}		$0.25V_{DD}$	V
	$V_{IL}(3)$	Ports E, F, G, H	Output Nch Tr OFF	4.5 to 6.0	V_{SS}		$0.25V_{DD}$	V
				3.0 to 6.0	V_{SS}		$0.20V_{DD}$	V
	$V_{IL}(4)$	Port B	At internal reference voltage mode	4.0 to 6.0	V_{SS}		$0.35V_{DD}$	V
$V_{IL}(5)$	RES	Fig. 7	4.5 to 6.0	V_{SS}		$0.25V_{DD}$	V	
			1.8 to 6.0	V_{SS}		$0.20V_{DD}$	V	
$V_{IL}(6)$	OSC1, X1	Fig. 5, Fig. 6	4.5 to 6.0	V_{SS}		$0.30V_{DD}$	V	
			3.0 to 6.0	V_{SS}		$0.20V_{DD}$	V	
$V_{IL}(7)$	TEST		4.5 to 6.0	V_{SS}		$0.30V_{DD}$	V	
			3.0 to 6.0	V_{SS}		$0.25V_{DD}$	V	
Common-Mode Input Voltage Range	V_{CMM}	Port B	Offset voltage $\leq V_{OFS}$	4.5 to 6.0	$V_{SS} + 1.0$		$V_{DD} - 1.5$	V
Instruction Cycle Time	T_{CYC}		(Note 1)	(Note 1)	0.92		67	μs
Main Clock OSC Frequency Range	f_{OSC}	OSC1, OSC2	Crystal, ceramic resonator OSC (Note 1) Fig. 1	3.0 to 6.0	3.5	4.19	4.2	MHz
Main Clock Input Frequency Range	f_{EOSC}	OSC1	External clock (Note 1) Fig. 5	3.0 to 6.0	2.0		4.33	MHz
Main Clock Input "H"-Level Pulse Width	t_{WOSCH}	OSC1	External clock Fig. 5	3.0 to 6.0	100			ns
Main Clock Input "L"-Level Pulse Width	t_{WOSCL}	OSC1	External clock Fig. 5	3.0 to 6.0	100			ns
Main Clock Rise Time	t_{OSCR}	OSC1	External clock Fig. 5	3.0 to 6.0			30	ns

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Parameter	Symbol	Applicable Pins, Remarks	Conditions	V _{DD} [V]	Limits			Unit
					min	typ	max	
Main Clock Fall Time	t _{O SCF}	OSC1	External clock Fig. 5	3.0 to 6.0			30	ns
Main Clock OSC Constant	CO1, CO2		Fig. 1	3.0 to 6.0	Refer to Table 1.			—
Sub-clock OSC Frequency Range	f _X	X1, X2	Crystal OSC Fig. 2	2.7 to 6.0	30	32.768	35	kHz
Sub-clock Input Frequency Range	f _{EX}	X1	External clock Fig. 6	2.7 to 6.0	30		35	kHz
Sub-clock Input "H"-Level Pulse Width	t _{WXH}	X1	External clock Fig. 6	2.7 to 6.0	6		34	μs
Sub-clock Input "L"-Level Pulse Width	t _{WXL}	X1	External clock Fig. 6	2.7 to 6.0	6		34	μs
Sub-clock Input Rise Time	t _{XR}	X1	External clock Fig. 6	2.7 to 6.0			0.2	μs
Sub-clock Input Fall Time	t _{XF}	X1	External clock Fig. 6	2.7 to 6.0			0.2	μs
Sub-clock OSC Constant	CX1, CX2		Fig. 2	2.7 to 6.0	Refer to Table 2.			—

(Note 1) Since the frequency also depends on the supply voltage and operating cycle time, both must be referred to.

3. Electrical Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Applicable Pins, Remarks	Conditions	$V_{DD}[\text{V}]$	Limits			Unit
					min	typ	max	
"H"-Level Input Current	$I_{IH}(1)$	Ports A, C, D, E2, F to H of OD type	Output Nch Tr OFF (Including Nch Tr OFF leakage current) $V_{IN}=+13.5\text{V}$	2.7 to 6.0			5.0	μA
	$I_{IH}(2)$	Ports E0, E1	Output Nch Tr OFF (Including Nch Tr OFF leakage current) $V_{IN}=V_{DD}$	2.7 to 6.0			1.0	μA
	$I_{IH}(3)$	Port B, RES OSC1, X1	$V_{IN}=V_{DD}$	2.7 to 6.0			10	μA
"L"-Level Input Current	$I_{IL}(1)$	Ports A, C to H of OD type Port B	Output Nch Tr OFF $V_{IN}=V_{SS}$	2.7 to 6.0	-1.0			μA
	$I_{IL}(2)$	Ports A, C to H of PU type	Output Nch Tr OFF $V_{IN}=V_{SS}$	2.7 to 6.0	-1.3	-0.35		mA
	$I_{IL}(3)$	OSC1, X1	$V_{IN}=V_{SS}$	2.7 to 6.0	-10			μA
	$I_{IL}(4)$	RES	$V_{IN}=V_{SS}$	2.7 to 6.0	-60	-25		μA
"H"-Level Output Voltage	$V_{OH}(1)$	Ports A, C to H of PU type	$I_{OH}=-50\mu\text{A}$	4.0 to 6.0	$V_{DD}-1.2$			V
	$V_{OH}(2)$	Ports A, C to H of PU type	$I_{OH}=-10\mu\text{A}$	3.0 to 6.0	$V_{DD}-0.5$			V
	$V_{OH}(3)$	T0 to T11, T12/S11 to T15/S8	$I_{OH}=-20\text{mA}$	4.0 to 6.0	$V_{DD}-1.8$			V
	$V_{OH}(4)$	T0 to T11, T12/S11 to T15/S8	$I_{OH}=-1\text{mA}$ I_{OH} in other ports is less than -1mA .	3.0 to 6.0	$V_{DD}-1.0$			V
	$V_{OH}(5)$	S0 to S7	$I_{OH}=-5\text{mA}$	4.0 to 6.0	$V_{DD}-1.8$			V
	$V_{OH}(6)$	S0 to S7	$I_{OH}=-1\text{mA}$ I_{OH} in other ports is less than -1mA .	3.0 to 6.0	$V_{DD}-1.0$			V
"L"-Level Output Voltage	$V_{OL}(1)$	Ports C, D	$I_{OL}=20\text{mA}$	4.0 to 6.0			1.5	V
	$V_{OL}(2)$	Ports C, D	$I_{OL}=2\text{mA}$ I_{OL} in other ports is less than 1mA .	3.0 to 6.0			0.5	V
	$V_{OL}(3)$	Ports A, E to H	$I_{OL}=5\text{mA}$	4.0 to 6.0			1.5	V
	$V_{OL}(4)$	Ports A, E to H	$I_{OL}=1\text{mA}$ I_{OL} in other ports is less than 1mA .	3.0 to 6.0			0.5	V
"L"-Level Output Current (Current flowing in pull-down resistor)	I_{OL}	T0 to T11, T12/S11 to T15/S8, S0 to S7 of PD type	Output Pch Tr OFF $V_{OUT}=3.0\text{V}$ $V_p=-35\text{V}$	5.0	190	362	760	μA
Output OFF-State Leakage Current	$I_{OFF}(1)$	T0 to T11, T12/S11 to T15/S8, S0 to S7 of OD type	Output Pch Tr OFF $V_{OUT}=V_{DD}$	3.0 to 6.0			30	μA
	$I_{OFF}(2)$	T0 to T11, T12/S11 to T15/S8, S0 to S7 of OD type	Output Pch Tr OFF $V_{OUT}=V_{DD}-40\text{V}$	3.0 to 6.0	-30			μA
Resistance of Pull-up MOS Transistor	R_{Tru}	Ports A, C to H of PU type		5.0	6	15	24	$\text{k}\Omega$
Pull-up Resistance	R_u	RES		5.0	100	220	400	$\text{k}\Omega$
Pull-down Resistance	R_d	T0 to T11, T12/S11 to T15/S8, S0 to S7 of PD type		5.0	50	105	200	$\text{k}\Omega$
Main Clock OSC Stabilizing Period	t_{MXS}	OSC1, OSC2	4.19MHz crystal OSC	3.0 to 6.0			30	ms
	t_{MCFS}	OSC1, OSC2	4.0MHz ceramic resonator OSC	3.0 to 6.0			10	ms

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Parameter	Symbol	Applicable Pins, Remarks	Conditions	VDD[V]	Limits			Unit
					min	typ	max	
Sub-clock OSC Stabilizing Period	tSXS	X1, X2	32.768kHz crystal OSC	2.7 to 6.0			10	s
Serial Clock								
Input Clock Cycle	tCKCY(1)	SCK0, SCK1	Fig. 8	4.5 to 6.0	1.6			μs
Output Clock Cycle	tCKCY(2)	SCK0, SCK1	Fig. 8	4.5 to 6.0	1.84			μs
Input Clock "L"-Level Pulse width (Note 2)	tCKL(1)	SCK0, SCK1	Fig. 8	4.5 to 6.0	0.7			μs
Output Clock "L"-Level Pulse Width	tCKL(2)	SCK0, SCK1	Fig. 8	4.5 to 6.0	0.92			μs
Input Clock "H"-Level Pulse Width (Note 2)	tCKH(1)	SCK0, SCK1	Fig. 8	4.5 to 6.0	0.7			μs
Output Clock "H"-Level Pulse Width	tCKH(2)	SCK0, SCK1	Fig. 8	4.5 to 6.0	0.92			μs
Input Clock Rise Time	tCKR(1)	SCK0, SCK1	Fig. 8	4.5 to 6.0			3.0	μs
Output Clock Rise Time	tCKR(2)	SCK0, SCK1	Fig. 8	4.5 to 6.0			0.1	μs
Input Clock Fall Time	tCKF(1)	SCK0, SCK1	Fig. 8	4.5 to 6.0			3.0	μs
Output Clock Fall Time	tCKF(2)	SCK0, SCK1	Fig. 8	4.5 to 6.0			0.1	μs
Serial Input								
Data Setup Time	tICK	SI0, SI1	Specified for f of SCK0, SCK1 Fig. 8	4.5 to 6.0	0.2			μs
Data Hold Time	tCKI	SI0, SI1		4.5 to 6.0	0.2			μs
Serial Output								
Output Delay Time	tCKO	SO0, SO1	Specified from λ of SCK0, SCK1 External 1kΩ External 50pF Fig. 8	4.5 to 6.0			0.5	μs
Hysteresis Voltage	VHYS	Ports E to H, RES		3.0 to 6.0		0.1VDD		V
Comparator Response Speed	TRs	Port B	At 100mV overdrive mode	4.5 to 6.0			50	μs
Comparator Input Offset Voltage	VOFS	Port B	VIN=1.0V to VDD-1.5V VREF=1.0V to VDD-1.5V	4.5 to 6.0		±20	±100	mV
Operating Current Dissipation (Note 3)	IDDOP(1)	VDD	4.19MHz x 1/1 high-speed operation mode (TCYC=0.95μs) 32.768kHz sub-clock oscillating	4.5 to 6.0		4.5	10	mA
	IDDOP(2)	VDD	4.19MHz x 1/2 high-speed operation mode (TCYC=1.9μs) 32.768kHz sub-clock oscillating	4.0 to 6.0		2.7	6	mA
	IDDOP(3)	VDD	4.19MHz x 1/32 low speed operation mode (TCYC=30.5μs) 32.768kHz sub-clock oscillating	3.0		0.35	0.7	mA
				6.0		1.5	3	mA
IDDOP(4)	VDD	32.768kHz low-speed operation mode (TCYC=61μs) 4.19MHz main clock stop	2.7		0.035	0.12	mA	
			6.0		0.4	1.2	mA	

(Note 2) When using the internal clock, T_{CKL(2)} and T_{CKH(2)} (pins SCK0 and SCK1) have a minimum pulsewidth of 0.92 μs. This value is, however, dependent on the pull-up resistor and may, in some cases, be less than the above rating. The value of the pull-up resistance should be selected to ensure a minimum pulsewidth for T_{CKL(1)} and T_{CKH(1)} that is greater than the rated 0.7 μs.

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Parameter	Symbol	Applicable Pins, Remarks	Conditions	Limits				
				VDD[V]	min	typ	max	Unit
Standby Current Dissipation (Note 3)	IDDST(1)	VDD	4.19MHz main clock stop 32.768kHz sub-clock oscillating (HALT mode)	2.7		4	18	μ A
				6.0		120	300	μ A
	IDDST(2)	VDD	Complete standby (HOLD mode)	1.8		0.02	4	μ A
				6.0		0.05	10	μ A

(Note 3) The current flowing in the I/O port transistors and pull-up/pull-down resistors is excluded.

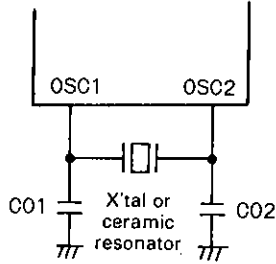


Fig. 1 Main Clock OSC Circuit

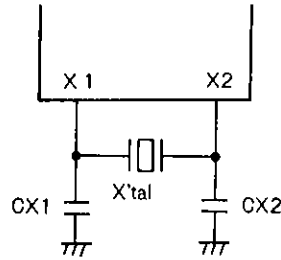


Fig. 2 Sub-clock Crystal OSC Circuit

Table 1 Main Clock OSC-Guaranteed Constants

OSC Mode	Maker	Resonator	CO1	CO2
4.194304MHz crystal OSC	Tokyo Denpa	HC-43/u CL=18pF Drive level =100mW	22pF	22pF
		Kinseki	15pF	15pF
	Kinseki	HC-49/u CL=24pF	27pF	27pF
4.0MHz ceramic resonator OSC	Murata	CSA-4.00MG	33pF	33pF
		CST-4.00MG*1	Unnecessary	Unnecessary
	Kyocera	KBR-4.0MS	33pF	33pF
		KBR-4.0MES*1	Unnecessary	Unnecessary

Table 2 Sub-clock Crystal OSC-Guaranteed Constants

OSC Mode	Maker	Resonator	CX1	CX2
32.768kHz crystal OSC	Kyocera	KF-38G-13200 CL=13pF	22pF	22pF
		KF-38G-10200 CL=10pF	20pF Trimmer	22pF

(Note) CL: Internal load capacitance of crystal resonator

The differential between CO1 and CO2 should be within $\pm 10\%$, including wiring capacitance.

*1: 3-pin ceramic resonator with on-chip capacitor

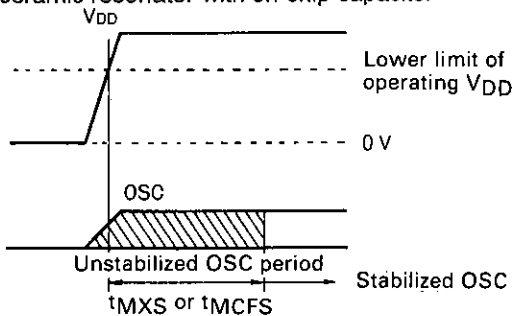


Fig. 3 Main Clock OSC Stabilizing Period

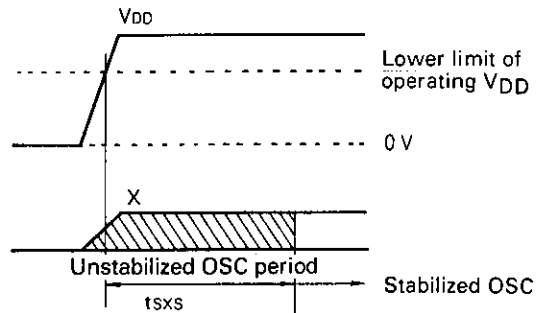


Fig. 4 Sub-clock OSC Stabilizing Period

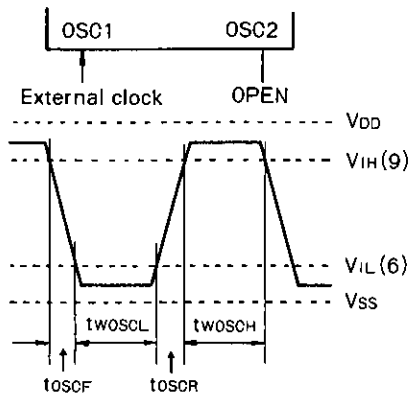


Fig. 5 Main Clock (External Clock) Input Waveform

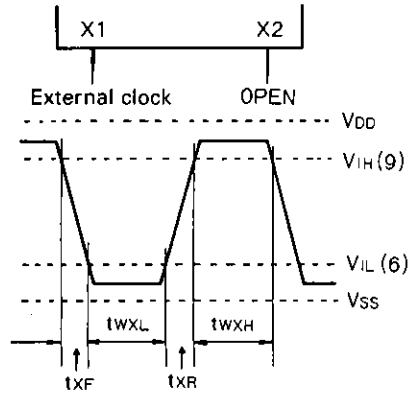
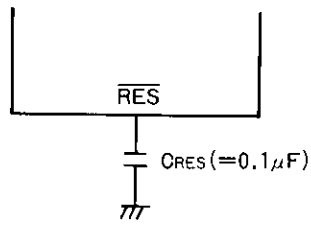


Fig. 6 Sub-clock (External Clock) Input Waveform

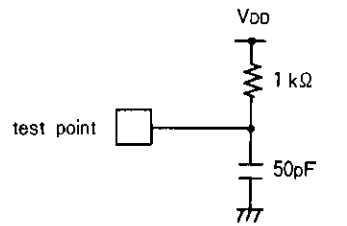


(Note)

When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at CRES = 0.1 μF.

If the rise time of the power supply is long, the value of CRES must be fixed so that the reset time becomes longer than the main clock OSC stabilizing period.

Fig. 7 Reset Circuit



Serial Output Load

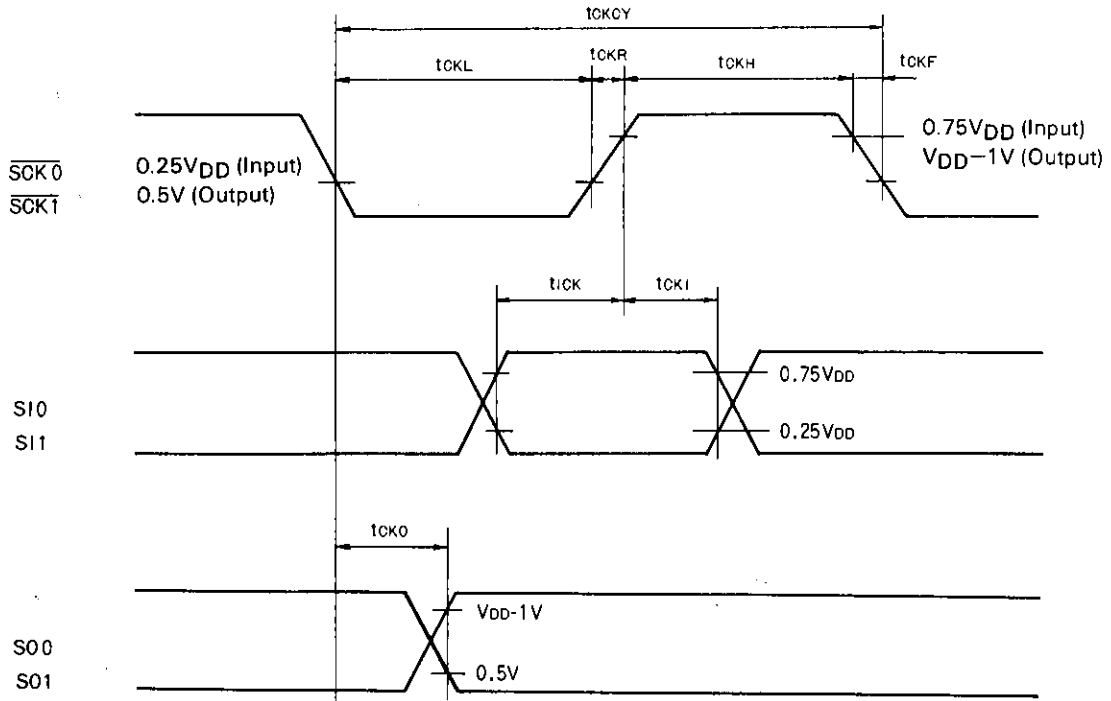


Fig. 8 Serial Clock Timing

Notes for Program Evaluation

- When evaluating the LC6538D with the evaluation chip (LC6593, LC65PG38D), the following must be observed.

Classification	Item	Function		Notes for evaluation
		Mass-production chip	Evaluation chip	
Notes for option	Ports C, D output level at reset mode	Ports C, D can be brought to "H" or "L" in a group of 4 bits.	Port C and port D can be brought to "H" or "L" by CHL pin and DHL pin, respectively.	CHL pin and DHL pin must be set according to option specified for mass-production chip.
	Watchdog reset function	The presence or absence of time base timer-used watchdog reset function can be selected.	Whether or not to perform watchdog reset function with WDC pin can be determined.	WDC pin must be set according to option specified for mass-production chip.
	Port output configuration PU/OD	PU or OD can be selected in bit units.	Only Nch OD configuration without pull-up resistance	(LC6593-applied evaluation) External resistor (10kohms) on evaluation chip board must be connected to necessary port. (LC65PG38D-applied evaluation) Resistor must be connected to necessary port on application board.
	PU resistor configuration	PU resistor brought to Hi-Z at "L" output mode (Pch Tr is turned OFF)	PU resistor, being external resistor, whose impedance remains unchanged at "L" output mode.	For mass-production chip, leakage current only flows in Pch Tr at "L" output mode; for evaluation chip, current continues flowing in PU resistor at "L" output mode.
	Port output configuration PD/OD	PD or OD can be selected in bit units.	Only Pch OD configuration without pull-down resistance.	(LC6593-applied evaluation) External resistor (100kohms) on evaluation chip board must be connected to necessary port. (LC65PG38D-applied evaluation) Resistor must be connected to necessary port on application board. Load power supply must be also supplied on application board side.
Notes for OSC	Constants for main clock	(Crystal OSC), (Ceramic resonator OSC) Catalog-guaranteed constants provide OSC at frequency specified in catalog.	(Crystal OSC), (Ceramic resonator OSC) Different from mass-production chip in circuit design and characteristic. OSC may be made unstable by wiring capacitance.	(Crystal OSC), (Ceramic resonator OSC) External constants must be fine-adjusted according to service conditions. Refer to note given below.
	Constants for sub-clock	(Crystal OSC) Catalog-guaranteed constants provide OSC at frequency specified in catalog.	(Crystal OSC) Different from mass-production chip in circuit design and characteristic. OSC may be made unstable by wiring capacitance.	(Crystal OSC) External constants must be fine-adjusted according to service conditions. Refer to note given below.
Notes for electrical characteristics	OSC frequency for main clock, sub-clock	OSC frequency characteristic as indicated in catalog	Different from mass-production chip in circuit design and characteristic.	ES, CS must be used to evaluate characteristic in detail.
	Operating current, standby current	Current characteristic as indicated in catalog	Different from mass-production chip in circuit design and characteristic.	Standby current cannot be evaluated in detail. However, standby current can be confirmed roughly in the manner shown below. Be sure to confirm standby current. ES, CS must be used to evaluate characteristic in detail.
	Operating voltage	Supply voltage range as indicated in catalog	Restricted to the operating range of EPROM, other LSI	Evaluation chip must be also used at $V_{DD} = 5V \pm 5\%$ at which EPROM, other LSI are used. Therefore, $V_{DD} = 5V \pm 5\%$ only can be used for evaluation of mass-production microcomputers.
	Operating temperature	Temperature range as indicated in catalog	Guaranteed temperature range: 10°C to 40°C	LC6593 and LC65PG38D must be used at 10°C to 40°C for evaluation.

< Confirmation methods for the standby function >

The standby current at the standby mode of the evaluation chip can be evaluated not exactly but approximately. Then, do the following steps.

(a) Confirmation of the standby state

Be sure to confirm whether or not the LSI enters the standby mode when the standby conditions are satisfied.

The following Table gives the current dissipation (typ.) at each mode as a guideline for confirmation of mode.

Mode	Main clock (4.19MHz)	Sub-clock (32kHz)	Current dissipation (typ.)
NORMAL, main clock 1/1 mode	OSC	OSC	Approx. 3.5mA to 3.7mA
NORMAL, main clock 1/2 mode	OSC	OSC	Approx. 2.3mA to 2.5mA
NORMAL, main clock 1/32 mode	OSC	OSC	Approx. 1mA to 1.2mA
NORMAL, sub-clock mode	OSC	OSC	
NORMAL, sub-clock mode	Stop	OSC	Approx. 100 μ A to 300 μ A
HALT, main clock 1/1 mode	OSC	OSC	Approx. 1mA
HALT, main clock 1/2 mode	OSC	OSC	
HALT, main clock 1/32 mode	OSC	OSC	
HALT, sub-clock mode	OSC	OSC	
HALT, sub-clock mode	Stop	OSC	Approx. 50 μ A
HOLD mode	Stop	Stop	Several nA to 300nA

- Note 1) The current dissipation values shown above are the values obtained when a separate power supply is used for the EPROM power supply.
- 2) The current dissipation values shown above are the values obtained when the WDC, CHL, DHL pins are brought to "L" level.
When brought to "H" level, the current dissipation value per pin increases by approximately 30 μ A.
- 3) The current dissipation at the NORMAL mode varies by the value of current dissipated in the pull-up resistor of IM0 to IM7.
IM0 to IM7: The current dissipation per bit at "L" level increases by approximately 25 μ A.
- 4) The current dissipation values at the HALT or HOLD mode are the values obtained when the EPROM is removed.
- 5) All other pins for the evaluation chip are left open.

(b) Confirmation by the load current

Your program must be designed so that the current is not transmitted to the input/output ports prior to the execution of the HALT instruction. This can reduce the useless dissipation of the load current at the standby mode and be confirmed on an oscilloscope.

- 1) Design your program so that the current is not transmitted to the output ports prior to the execution of the HALT instruction.
- 2) Design your program and peripherals so that the input/output ports are not brought to the floating state (Hi-Z) at the standby mode.
If brought to the floating state (Hi-Z), current flows in the microcomputer input circuit section, causing more current dissipation. Therefore, the backup enable time is shortened extremely in applications where the capacitor backup is used.

< OSC constants when the EVA800-TB6538 is used >

When developing your program using evaluation chip board EVA800-TB6538, adjust the capacitor value according to the stray capacitance of the circuit because the crystal/ceramic resonator OSC constants for main clock and the crystal OSC constants for sub-clock depend on the conditions for evaluation and the cable length, etc.

LC6538D INSTRUCTION SET (by function)

Symbol Description

AC	: Accumulator	M1(DP)	: Memory 1 addressed by DP	() []	: Contents
ACt	: Accumulator bit t	M2(DP)	: Memory 2 addressed by DP	-	: Transfer and direction
CF	: Carry flag	P(DPL)	: Input/output port addressed by DPL	+	: Addition
CTL	: Control register	GP(DP)	: Pseudo port specified by DP	-	: Subtraction
MSTEN	: Master interrupt enable flag	PC	: Program counter	^	: AND
DP	: Data pointer	STACK	: Stack register	v	: OR
E	: E register	TMO	: Timer 0	v	: Exclusive OR
bFn	: Flag bit n	TMOF	: Timer 0 interrupt request flag		
M1	: Memory 1	bAt,bHa,bLa	: Working register		
M2	: Memory 2	ZF	: Zero flag		

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	ZF	* 1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← \bar{AC}	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) - 1	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC ₀ ← (CF), AC _{n+1} ← AC _{n}, CF ← AC₃}	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)		
XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ↔ (E)			
Memory manipulation instructions	INM	Increment M1	0 0 1 0	1 1 1 0	1	1	M1(DP) ← M1(DP) + 1	ZF CF	
	DEM	Decrement M1	0 0 1 0	1 1 1 1	1	1	M1(DP) ← M1(DP) - 1	ZF CF	
	SMB bit	Set M1 data bit	0 0 0 0	1 0 B ₁ B ₀	1	1	M1(DP, B ₁ B ₀) ← 1		
	RMB bit	Reset M1 data bit	0 0 1 0	1 0 B ₁ B ₀	1	1	M1(DP, B ₁ B ₀) ← 0	ZF	
Arithmetic operation/comparison instructions	AD	Add M1 to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + M1(DP)	ZF CF	
	ADC	Add M1 to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + M1(DP) + (CF)	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	ZF	
	EXL	Exclusive OR M1 to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) v M1(DP)	ZF	
	AND	AND M1 to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ^ M1(DP)	ZF	
	OR	OR M1 to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) v M1(DP)	ZF	
	CM	Compare AC with M1	1 1 1 1	1 0 1 1	1	1	M1(DP) - (AC) + 1	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 1 3 1 2 1 1 0	2	2	1 ₃ 1 ₂ 1 ₁ 0 + (AC) + 1	ZF CF	
	CLI data	Compare DP _L with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 1 3 1 2 1 1 0	2	2	(DP _L) v 1 ₃ 1 ₂ 1 ₁ 0	ZF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	1 3 1 2 1 1 0	1	1	AC ← 1 ₃ 1 ₂ 1 ₁ 0	ZF	* 1
	S	Store AC to M1	0 0 0 0	0 0 1 0	1	1	M1(DP) ← (AC)		
	L	Load AC from M1	0 0 1 0	0 0 0 1	1	1	AC ← M1(DP)	ZF	
	XM data	Exchange AC with M1, then modify DP _H with immediate data	1 0 1 0	0 M ₂ M ₁ M ₀	1	2	(AC) ↔ M1(DP) DP _H ← (DP _H) v 0M ₂ M ₁ M ₀	ZF	The ZF is set/reset according to the result of (DP _H) v 0M ₂ M ₁ M ₀ .
	X	Exchange AC with M1	1 0 1 0	0 0 0 0	1	2	(AC) ↔ M1(DP)	ZF	The ZF is set/reset according to the time of instruction execution.
	XI	Exchange AC with M1, then increment DP _L	1 1 1 1	1 1 1 0	1	2	(AC) ↔ M1(DP) DP _L ← (DP _L) + 1	ZF	The ZF is set/reset according to the result of (DP _L) + 1.
XD	Exchange AC with M1, then decrement DP _L	1 1 1 1	1 1 1 1	1	2	(AC) ↔ M1(DP) DP _L ← (DP _L) - 1	ZF	The ZF is set/reset according to the result of (DP _L) - 1.	

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Instruction group	Mnemonic	Instruction code				Bytes	Cycles	Function	Description	Status flag affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀								
	RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC ← E ← ROM (PCh E, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.			
Data pointer manipulation instructions	LDZ data	Load DPH with Zero and DPL with immediate data respectively	1 0 0 0	1 3 1 2 1 1 1 0	1	1	DPH ← 0 DPL ← 1 3 1 2 1 1 1 0	The DPH and DPL are loaded with 0 and the immediate data 1 3 1 2 1 1 1 0 respectively.			
	LHI data	Load DPH with immediate data	0 1 0 0	1 3 1 2 1 1 1 0	1	1	DPH ← 1 3 1 2 1 1 1 0	The DPH is loaded with the immediate data 1 3 1 2 1 1 1 0.			
	IND	Increment DPL	1 1 1 0	1 1 1 1 0 1 1 1	1	1	DPL ← (DPL) + 1	The DPL contents are incremented +1.	ZF		
	DED	Decrement DPL	1 1 1 0	1 1 1 1 1 1 1 1	1	1	DPL ← (DPL) - 1	The DPL contents are decremented -1.	ZF		
	TAL	Transfer AC to DPL	1 1 1 1	0 1 1 1 1 1 1 1	1	1	DPL ← (AC)	The AC contents are transferred to the DPL.			
	TLA	Transfer DPL to AC	1 1 1 0	1 0 0 1 1 1 1 1	1	1	AC ← (DPL)	The DPL contents are transferred to the AC.	ZF		
	XAH	Exchange AC with DPH	0 0 1 0	0 0 1 1 1 1 1 1	1	1	(AC) ↔ (DPH)	The AC contents and the DPH contents are exchanged.			
Working register manipulation instructions	XA0	Exchange AC with working register Aa	1 1 1 0	1 1 1 0 0 0 0 0	1	1	(AC) ↔ (bA0)	The AC contents and the contents of working register Aa are exchanged. Aa is assigned one of bA0, bA1, bA2, bA3 according to 1 1 1 0 of specified register bank b.			
	XA1		1 1 1 0	0 1 1 0 0 0 0 0	1	1	(AC) ↔ (bA1)				
	XA2		1 1 1 0	1 0 1 0 0 0 0 0	1	1	(AC) ↔ (bA2)				
	XA3		1 1 1 0	1 1 1 0 0 0 0 0	1	1	(AC) ↔ (bA3)				
	XHa	Exchange DPH with working register Ha	1 1 1 1	1 1 0 0 0 0 0 0	1	1	(DPH) ↔ (bH0)	The DPH contents and the contents of working register Ha are exchanged. Ha is assigned either of bH0 or bH1 according to a of specified register bank b.			
	XH1		1 1 1 1	1 1 1 0 0 0 0 0	1	1	(DPH) ↔ (bH1)				
	XLa	Exchange DPL with working register La	1 1 1 1	0 1 0 0 0 0 0 0	1	1	(DPL) ↔ (bL0)	The DPL contents and the contents of working register La are exchanged. La is assigned either of bL0 to bL1 according to a of specified register bank b.			
XL1	1 1 1 1		0 1 1 0 0 0 0 0	1	1	(DPL) ↔ (bL1)					
SRBA	Set Register Bank Address	1 1 1 1	0 0 1 0 1 0 1 1	1	1	RBF ← 110 of SB	The bank value specified by the SB instruction is set in the register bank flag.				
Flag manipulation instructions	SFB flag	Set flag bit	0 1 0 1	B ₃ B ₂ B ₁ B ₀	1	1	bFn - 1	The flag specified with B ₃ B ₂ B ₁ B ₀ of specified register bank b is set.			
	RFB flag	Reset flag bit	0 0 0 1	B ₃ B ₂ B ₁ B ₀	1	1	bFn - 0	The flag specified with B ₃ B ₂ B ₁ B ₀ of specified register bank b is reset.	ZF	The flags are divided into 16 groups of OF0 to OF3, OF4 to OF7, ..., 3F8 to 3F11, 3F12 to 3F15. The ZF is set/reset according to the 4 bits including a single bit specified with immediate data B ₃ B ₂ B ₁ B ₀ .	
Jump/subroutine instructions	JMP addr	Jump in the current bank	0 1 1 0	1 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄	2	2	PC ← PC ₁₂ PC ₁₁ (or PC ₁₁) P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀	A jump to the address specified with the PC ₁₂ PC ₁₁ (or PC ₁₁) and immediate data P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ occurs.		If the BANK and SB instructions are executed consecutively, the bank is changed.	
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	PC _{7~0} ← (E, AC)	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.			
	CZP addr	Call subroutine in the zero page	1 0 1 1	P ₃ P ₂ P ₁ P ₀	1	1	STACK ← (PC) + 1 PC _{12~6} , PC _{11~0} ← 0 PC _{5~2} ← P ₃ P ₂ P ₁ P ₀	A subroutine in page 0 of bank 0 is called.			
	CAL addr	Call subroutine in the zero bank	1 0 1 0	1 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄	2	2	STACK ← (PC) + 2 PC _{12~0} ← 00P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀	A subroutine in bank 0 is called.			
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	PC ← (STACK)	A return from a subroutine occurs.			
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	PC ← (STACK) CF ZF ← CSF, ZSF	A return from an interrupt service routine occurs.	ZF CF		
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1	PC ₁₁ ← (PC ₁₁) GPRDP M2(DP)	The bank of ROM is specified. The pseudo port is specified. The RAM2 is specified.			
SB	Set bank	0 1 1 0	0 1 1 1 1 0	1	1	PC ₁₂ PC ₁₁ ← 11, 10 RBF ← 110	The bank of ROM is specified. The bank of working register, flag is specified.				

Continued on next page.

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Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks	
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀							
Branch instructions	BAI addr	Branch on AC bit	0 1 1 1 P ₇ P ₆ P ₅ P ₄	0 0 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC ₁ = 1	If a single bit of the AC specified with the immediate data t ₁ t ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAI addr	Branch on no AC bit	0 0 1 1 P ₇ P ₆ P ₅ P ₄	0 0 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC ₁ = 0	If a single bit of the AC specified with the immediate data t ₁ t ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMI addr	Branch on M1 bit	0 1 1 1 P ₇ P ₆ P ₅ P ₄	0 1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [M1(DP, t1t0)] = 1	If a single bit of the M1(DP) specified with the immediate data t ₁ t ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMI addr	Branch on no M1 bit	0 0 1 1 P ₇ P ₆ P ₅ P ₄	0 1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [M1(DP, t1t0)] = 0	If a single bit of the M1(DP) specified with the immediate data t ₁ t ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNMI0 to BNMI3 according to the value of t.
	BPI addr	Branch on Port bit	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 0 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (PIDPL, t1t0) = 1	If a single bit of port P(DP _L) specified with the immediate data t ₁ t ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BPI0 to BPI3 according to the value of t.
	BNPI addr	Branch on no Port bit	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 0 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (PIDPL, t1t0) = 0	If a single bit of port P(DP _L) specified with the immediate data t ₁ t ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNPI0 to BNPI3 according to the value of t.
	BC addr	Branch on CF	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		
	BFn addr	Branch on flag bit	1 1 0 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if bFn = 1	If the immediate data n ₃ n ₂ n ₁ n ₀ -specified flag bit of the 16 flags of specified register bank b is 1, a branch to the address specified with immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BFO to BF15 according to the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if bFn = 0	If the immediate data n ₃ n ₂ n ₁ n ₀ -specified flag bit of the 16 flags of specified register bank b is 0, a branch to the address specified with immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNFO to BNF15 according to the value of n.
Input/output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← [P(DP _L)] or [GP(DP)] or [M2(DP)]	The contents of port P(DP _L) or pseudo port GP(DP) or RAM2 are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DP _L) or GP(DP) or M2(DP) ← (AC)	The AC contents are output to port P(DP _L) or pseudo port GP(DP) or RAM2.		
	SPB bit	Set port bit	0 0 0 0	0 1 B ₁ B ₀	1	2	P(DP _L , B ₁ B ₀) or GP(DP, B ₁ B ₀) or M2(DP, B ₁ B ₀) ← 1	A single bit in port P(DP _L) or pseudo port GP(DP) or RAM2 specified with immediate data B ₁ B ₀ is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 B ₁ B ₀	1	2	P(DP _L , B ₁ B ₀) or GP(DP, B ₁ B ₀) or M2(DP, B ₁ B ₀) ← 0	A single bit in port P(DP _L) or pseudo port GP(DP) or RAM2 specified with immediate data B ₁ B ₀ is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	SCTL bit	Set control register bit	0 0 1 0 1 0 0 0	1 1 0 0 B ₃ B ₂ B ₁ B ₀	2	2	CTL, B ₃ B ₂ B ₁ B ₀ ← 1 or MSTEN ← 1	The immediate data B ₃ B ₂ B ₁ B ₀ -specified bits of the control register (individual interrupt enable flag) or the master interrupt enable flag is set.		*2
	RCTL bit	Reset control register bit	0 0 1 0 1 0 0 1	1 1 0 0 B ₃ B ₂ B ₁ B ₀	2	2	CTL, B ₃ B ₂ B ₁ B ₀ ← 0 or MSTEN ← 0	The immediate data B ₃ B ₂ B ₁ B ₀ -specified bits of the control register (individual interrupt enable flag) or the master interrupt enable flag is reset.	ZF	*2
	WTTM	Write timer ← 0	1 1 1 1	1 0 0 1	1	1	TM0 ← (E), (AC) TMOF ← 0	The E and AC contents are loaded in the timer 0. The TMF is reset.	TMOF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt, Hold	The standby mode is entered.		
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the CLA instruction is used consecutively in such a manner as CLA, CLA, ----, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.

*2 B₃B₂B₁B₀ = 0000B to 1000B

LC6538D Option Code Specifying Method

General Description

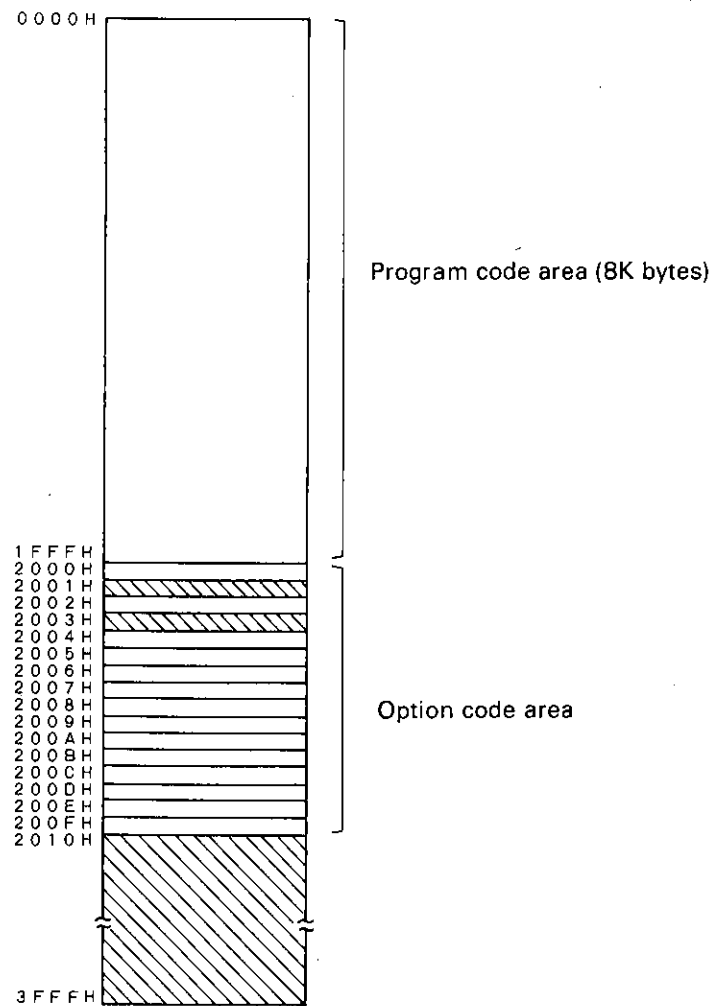
It is requested that you should submit to us various mask options of the LC6538D together with the program code which are stored in an EPROM.

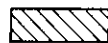
By using our cross assembler for the LC6538D, the option code can be specified interactively and stored in the EPROM.

If our cross assembler is not used, specify the option code as shown below. (This is the same as the method where the cross assembler is created.)

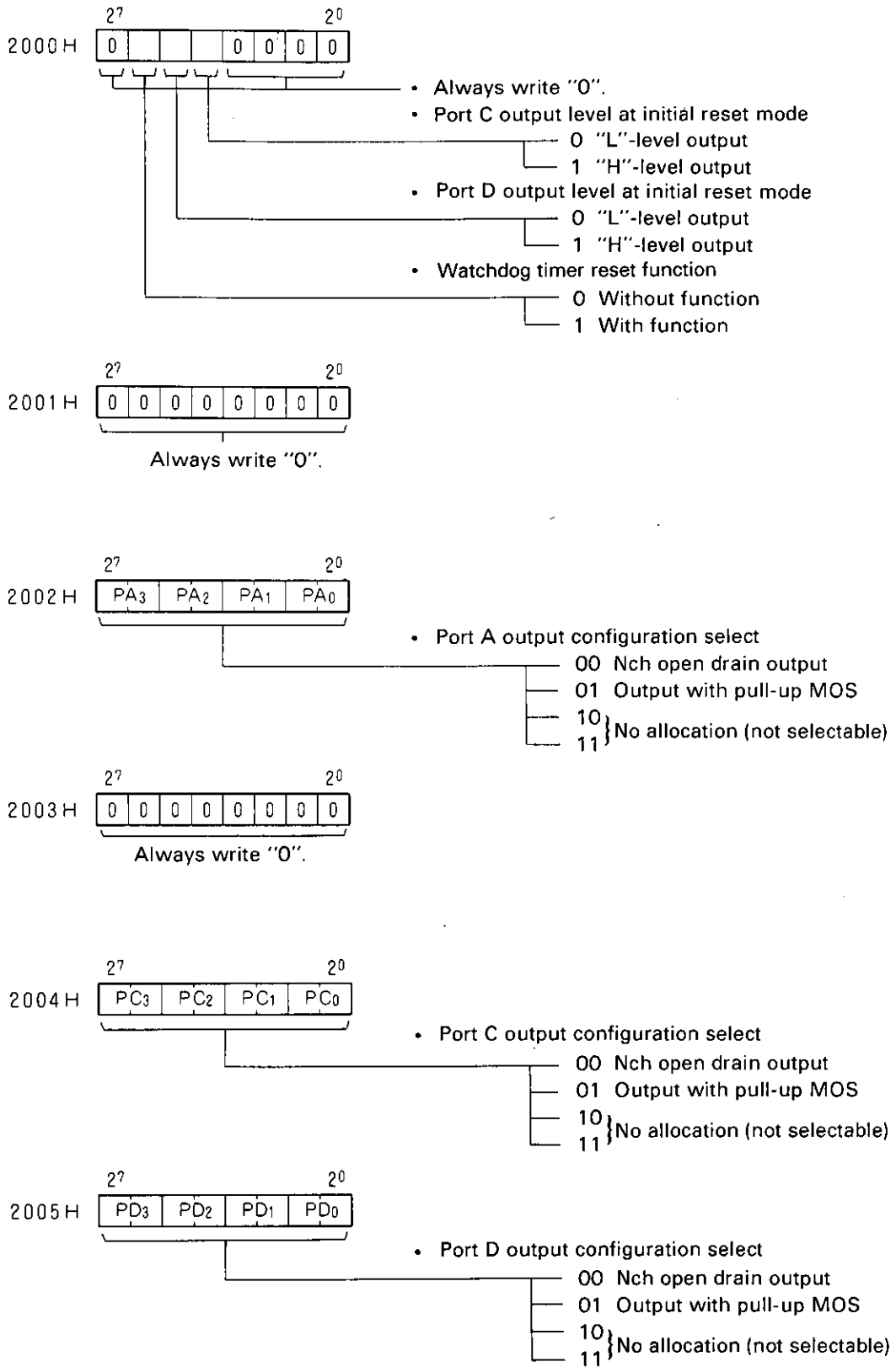
The Type No. of the EPROM to be submitted is 27128.

EPROM address map



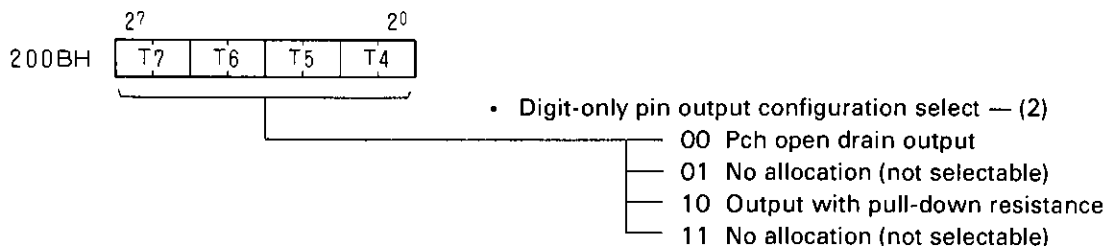
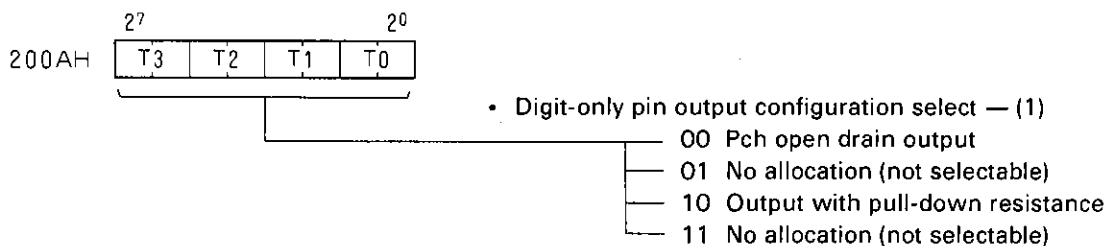
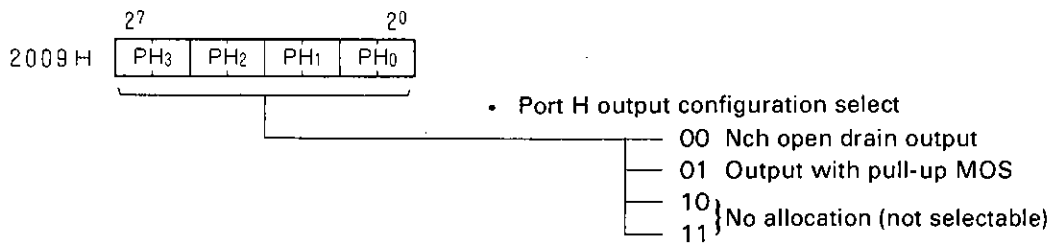
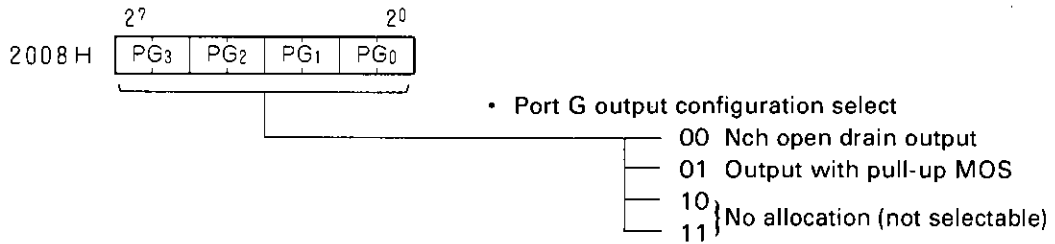
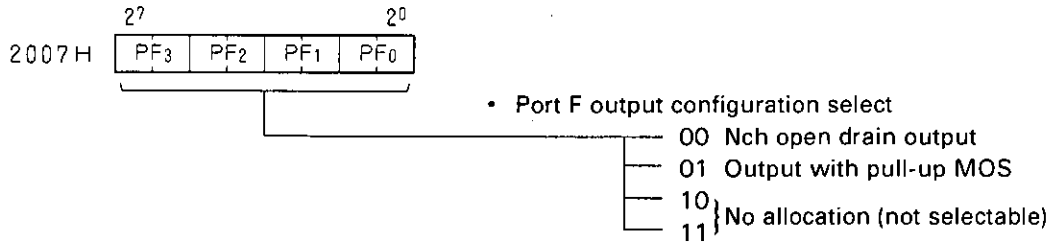
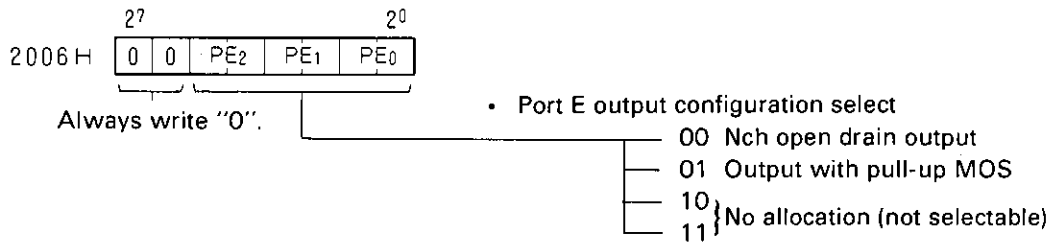
 Always write "00" in this shaded area.

Option Code Contents



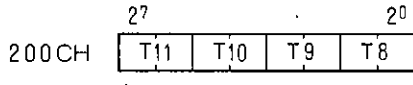
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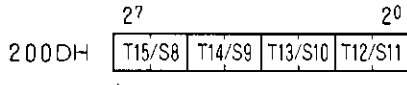


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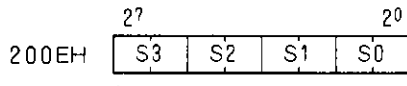
Continued from preceding page.



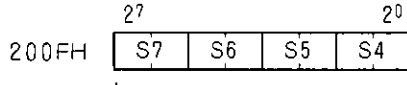
- Digit-only pin output configuration select — (3)
 - 00 Pch open drain output
 - 01 No allocation (not selectable)
 - 10 Output with pull-down resistance
 - 11 No allocation (not selectable)



- Digit/segment common pin output configuration select
 - 00 Pch open drain output
 - 01 No allocation (not selectable)
 - 10 Output with pull-down resistance
 - 11 No allocation (not selectable)



- Segment-only pin output configuration select — (1)
 - 00 Pch open drain output
 - 01 No allocation (not selectable)
 - 10 Output with pull-down resistance
 - 11 No allocation (not selectable)



- Segment-only pin output configuration select — (2)
 - 00 Pch open drain output
 - 01 No allocation (not selectable)
 - 10 Output with pull-down resistance
 - 11 No allocation (not selectable)

Notes on Programming

- In this section, we shall describe the notes on developing programs for the LC6538D microcomputer.

Item	Function	Notes										
System clock	<p>System clock mode</p> <p>One of the following clock sources can be selected on your program as the system clock source for the LC6538D microcomputer.</p> <p>① Main clock 1/1 mode ($T_{CYC}=0.95\mu s$) ② Main clock 1/2 mode ($T_{CYC}=1.9\mu s$) ③ Main clock 1/32 mode ($T_{CYC}=30.5\mu s$) ④ Sub-clock mode ($T_{CYC}=61\mu s$) (Note) Main clock: 4.194304MHz Sub-clock: 32.768kHz</p>	<ul style="list-style-type: none"> The main clock must be supplied at the system start-up. The sub-clock must be supplied when your application is designed to use the sub-clock mode. 										
	<p>System clock select</p> <p>The system clock source can be selected by setting data in the clock mode flag (CMF: 2 bits) of the system clock control register.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>CMF</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Main clock 1/32 mode (at the reset)</td> </tr> <tr> <td>1</td> <td>Main clock 1/1 mode</td> </tr> <tr> <td>2</td> <td>Main clock 1/2 mode</td> </tr> <tr> <td>3</td> <td>Sub-clock mode</td> </tr> </tbody> </table>	CMF	Mode	0	Main clock 1/32 mode (at the reset)	1	Main clock 1/1 mode	2	Main clock 1/2 mode	3	Sub-clock mode	<ul style="list-style-type: none"> System clock modes can be changed only when the main clock oscillation is stable or the clock signals are sent from external clock with the 4MSTPF flag set to "0". The clock mode newly selected by the CMF flag is actually activated up to $64/f_{OSC}$ cycles later after data is set in that flag. To change high-speed mode to low-speed mode and then start the standby mode, execute the HALT instruction after the buffer time elapses. Clock modes should be changed, with supplied voltage at 4.0V or greater.
	CMF	Mode										
	0	Main clock 1/32 mode (at the reset)										
1	Main clock 1/1 mode											
2	Main clock 1/2 mode											
3	Sub-clock mode											
<p>Main clock oscillation halt/start</p> <p>The main clock operation (halt/start) can be controlled by setting data in the 4MSTPF flag of the system clock control register.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>4MSTPF</th> <th>Main clock</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Start (at the reset)</td> </tr> <tr> <td>1</td> <td>Halt</td> </tr> </tbody> </table>	4MSTPF	Main clock	0	Start (at the reset)	1	Halt	<ul style="list-style-type: none"> If one of the main clock modes is selected as the system clock source, you must not set the 4MSTPF flag to "1". Set the 4MSTPF flag to "1" after the sub-clock mode becomes actually activated. That is, you have to set the flag to "1" after the sub-clock mode is specified by the flag data and then becomes activated after the buffer time elapses. To change the main clock halt state at the sub-clock mode to one of the main clock modes, set the 4MSTPF flag to "0" and wait at least until the main clock oscillation becomes stable. Wait for t_{MXS} or M_{CFS} cycles. 					
4MSTPF	Main clock											
0	Start (at the reset)											
1	Halt											
<p>Low-speed operation mode</p> <p>The following blocks are forced to stop their functions when the low-speed operation mode (main clock 1/32 mode or sub-clock mode) is selected.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Item</th> <th>Contents</th> </tr> </thead> <tbody> <tr> <td>Port B (comparator input)</td> <td>If data is input to the accumulator (AC) from port B, 0 (zero) is input to the AC.</td> </tr> <tr> <td>H counter</td> <td>The contents of the H counter are cleared.</td> </tr> <tr> <td>Display controller</td> <td>Not to support dynamic display mode operation</td> </tr> </tbody> </table>	Item	Contents	Port B (comparator input)	If data is input to the accumulator (AC) from port B, 0 (zero) is input to the AC.	H counter	The contents of the H counter are cleared.	Display controller	Not to support dynamic display mode operation	<ul style="list-style-type: none"> Do not use the blocks at the left column during the low-speed operation mode. Note that the low-speed operation is selected at the system reset. 			
Item	Contents											
Port B (comparator input)	If data is input to the accumulator (AC) from port B, 0 (zero) is input to the AC.											
H counter	The contents of the H counter are cleared.											
Display controller	Not to support dynamic display mode operation											

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	Item	Function	Notes
Standby mode	HALT mode activation/release	<p>(Activation) The HALT mode can be activated by executing the HALT instruction when the SLPF flag of the standby control register has been already set to "0". However, the HALT instruction will be processed equally as the NOP instruction when the following HALT mode release conditions are satisfied.</p> <p>(Release) ① Reset ② The PE2/START pin signal level is "H" with the WG2=1. ③ The interrupt release signal is delivered with the WG3=1. ④ The overflow signal is generated by the time base timer circuit.</p>	<ul style="list-style-type: none"> ● If you want to release the HALT mode by using the PE₂/START pin "H" level signal or interrupt release signal, set the WG2 or WG3 flag prior to the execution of the HALT instruction.
	HOLD mode activation/release	<p>(Activation) The HOLD mode can be selected by executing the HALT instruction with the SLPF="1".</p> <p>(Release) Reset</p>	<ul style="list-style-type: none"> ● The HOLD mode can be released only by the reset signal. ● Execute a single NOP instruction prior to the execution of the HALT instruction for activating the HOLD mode. ● Never output logic "1" to bit 1 of the standby control register (STBC).
	Watchdog timer reset (effective only if the watchdog timer function has been selected by option)	The time base timer can be used to detect runaway and cause watchdog reset to occur.	<ul style="list-style-type: none"> ● You have to create a routine which allows the TBF flag to be reset every program-defined time cycle (0.5sec. max.). ● The clock which has been already in operation must be selected as the time base timer source. ● If the time base interrupt request flag (TBF) is set to "1" prior to HALT activation, the HALT mode release signal triggered by time base overflow signal and watchdog reset signal are to be generated at the same time. To avoid the generation of watchdog reset signal in the above case, there are two methods as follows: ① Reset the TBF flag immediately before the HALT instruction is executed. or ② Set the time base interrupt enable flag (TBEN) and HALT release enable flag (WG3) before the HALT instruction is executed.
Interrupt	Interrupt enable flag (Control register: 8 bits)	<ul style="list-style-type: none"> ● There are 8 interrupt enable flags, which are assigned to 8 interrupt sources. These flags are set to enable interrupt requests by SCTL0 to SCTL7 instructions. Note that two or more flags cannot be set at a time. ● All the interrupt enable flags are set to disable interrupt at the reset mode. 	<ul style="list-style-type: none"> ● The interrupt enable flags are not reset after interrupt processing is carried out. If you want to reset interrupt enable flag, you have to use the RCTL instruction. ● All the interrupt enable flags are reset when the HOLD mode is started up. You have to set necessary flags after the HOLD mode is released.

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Item		Function	Notes
Interrupt	Interrupt request flag	<ul style="list-style-type: none"> There are 8 interrupt request flags, which are assigned to 8 interrupt sources. Four interrupt request flags are assigned as an interrupt extended register. That is, 8 interrupt request flags are assigned as two internal extended registers. Therefore, these registers can be accessed by executing the BANK and IP/OP instructions consecutively. If you input data to the accumulator (AC) from one of these registers, you can use the BANK and IP instructions consecutively. If you output data to one of these registers, you can use the BANK and OP instructions consecutively. However, you cannot set any bit of the internal extended register. If you are to reset some bits of the register, set data of 0 for them but 1 for other bits in the accumulator and output the data to interrupt request register by executing the BANK and OP instructions consecutively. Flags other than timer 1 interrupt request flag (TM1F) are set to "0" at the reset mode. The TMOF, SIOOF, SIO1F flags are reset at the time of WTTM instruction execution, SIOO, SIO1 data transfer start, respectively. 	<ul style="list-style-type: none"> These flags are not reset even after interrupt processing is carried out. Reset the interrupt source flag of a corresponding interrupt source factor when interrupt processing is performed. All the flags are reset when the HOLD mode is started up. The interrupt request register cannot be manipulated by the BANK + SPB/RPB instructions.
Notes on use of common ports	Port E	PE ₀ /VREF ₀ PE ₁ /VREF ₁	Port E ₀ and E ₁ can be also used as the external reference voltage input pins VREF ₀ and VREF ₁ for comparator input (port B).
		PE ₂ /START	Port E ₂ can be also used as the HALT mode control pin START.
	Port F	PF ₀ /SI ₀ PF ₁ /SO ₀ PF ₂ /SCK ₀	Port F ₀ and F ₁ , and F ₂ can be also used as the SI ₀ , SO ₀ , and SCK ₀ pins for serial data transfer 0.
		PF ₃ /INT ₀	Port F ₃ can be also used as the INT ₀ pin for external interrupt 0 input.
	Port G	PG ₀ /SI ₁ PG ₁ /SO ₁ PG ₂ /SCK ₁	Port G ₀ , G ₁ , and G ₂ can be also used as the SI ₁ , SO ₁ , and SCK ₁ pins for serial data transfer 1.
		PG ₃ /INT ₁	Port G ₃ can be also used as the INT ₁ pin for external interrupt 1 input.
	Port H	PH ₀ /DAC ₀ PH ₁ /DAC ₁	Port H ₀ and H ₁ can be also used as the DAC ₀ and DAC ₁ pins for PWM type DAC output.
		PH ₂ /SQR	Port H ₂ can be also used as the SQR pin for burst pulse signal output.
		PH ₃ /HCNT	Port H ₃ can be also used as the HCNT pin for horizontal sync signal input.

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Item		Function		Notes
Display controller	Operational status at system clock selection	When the CPU has entered low-speed operation mode (main clock 1/32 mode or sub-clock mode), dynamic display mode operation is not successfully carried out.		<ul style="list-style-type: none"> When low-speed operation mode is employed, do not select the dynamic display mode.
	Operational status at standby mode	Dynamic display mode	<ul style="list-style-type: none"> Segment output pin----"H"-level output at all the pins Digit output pin----Unpredictable Fixed address output pin-----Keeps old contents. 	<ul style="list-style-type: none"> Select display OFF mode prior to the standby mode activation so that no current is dissipated by FLT pin.
		Static display mode	<ul style="list-style-type: none"> S0 to S7 pins---"H"-level output at all the pins T0 to T11 T12/S11 to T15/S8 pins-----Keeps old contents. 	
		Display OFF mode	<ul style="list-style-type: none"> All FLT pins---"L"-level output at the all pins 	

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