Ordering number : EN5997

CMOS IC

LC662508A, 662512A, 662516A

Four-Bit Single-Chip Microcontrollers with 8, 12, and 16 KB of On-Chip ROM

Overview

The LC662516A, LC662512A, and LC662508A are 4-bit CMOS microcontrollers that integrate on a single chip all the functions required in a special-purpose telephone controller, including ROM, RAM, I/O ports, a serial interface, a DTMF generator, timers, and interrupt functions. These microcontrollers are available in a 64-pin package.

Features and Functions

- On-chip ROM capacities of 8, 12, and 16 kilobytes, and an on-chip RAM capacity of 512 × 4 bits.
- Fully supports the LC66000 Series common instruction set (128 instructions).
- I/O ports: 58 pins
- DTMF generator
  This microcontroller incorporates a circuit that can generate two sine wave outputs, DTMF output, or a melody output for software applications.
- 8-bit serial interface: Two-wire interface (16-bit data length. Supports cascade connection.)
- Instruction cycle time: 0.95 to 10 µs (at 3.0 to 5.5 V)
- Powerful timer functions and prescalers
  — Time limit timer, event counter, pulse width measurement, and square wave output using a 12-bit timer.
  — Time limit timer, event counter, PWM output, and square wave output using an 8-bit timer.
  — Time base function using a 12-bit prescaler.
- Powerful interrupt system with 11 interrupt factors and 8 interrupt vector locations.
  — External interrupts: 3 factors/3 vector locations
  — Internal interrupts: 8 factors/5 vector locations
  (Waveform output internal interrupts: 3 factors and 1 vector; shared with external expansion interrupts)
- Flexible I/O functions
  Selectable options include 20mA drive outputs, inverter circuits, pull-up and open drain circuits.
- Optional runaway detection function (watchdog timer)
- 8-bit I/O functions
- Power saving functions using halt and hold modes.
- Packages: DIP64S, QIP64E (QFP64E)
- Evaluation ICs: LC665099 (evaluation chip) + EVA86K-ECB662500
  LC66E2516(on-chip EPROM microcontroller)

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

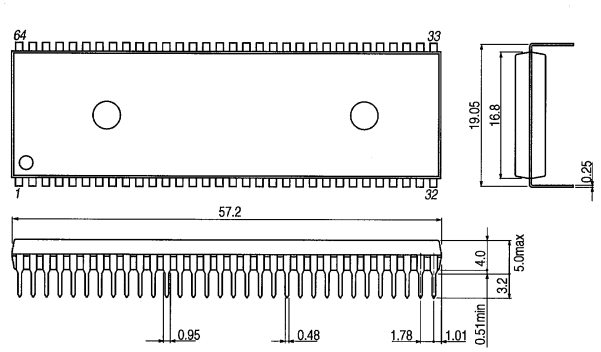
O1698RM (OT) No. 5997-1/17

Package Dimensions

unit: mm

3071-DIP64S

[LC662508A,12A,16A]

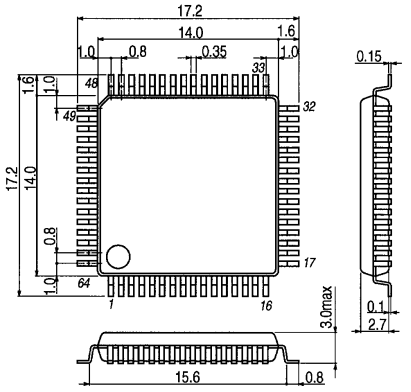


SANYO: DIP64S

unit: mm

3159-QFP64E

[LC662508A,12A,16A]



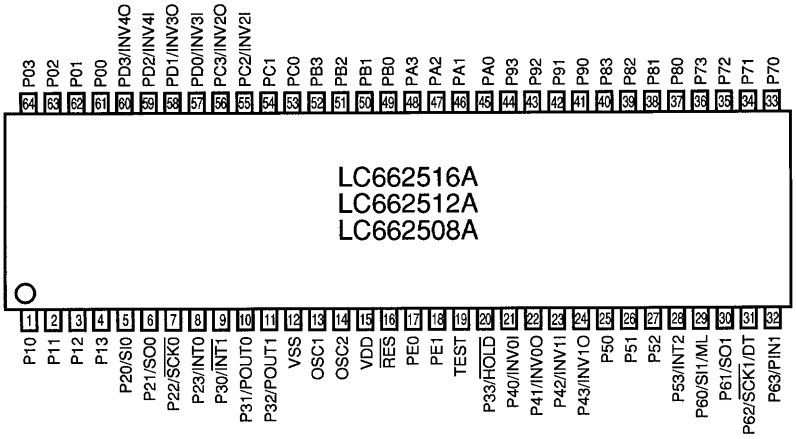
SANYO: QFP64E

Series Organization

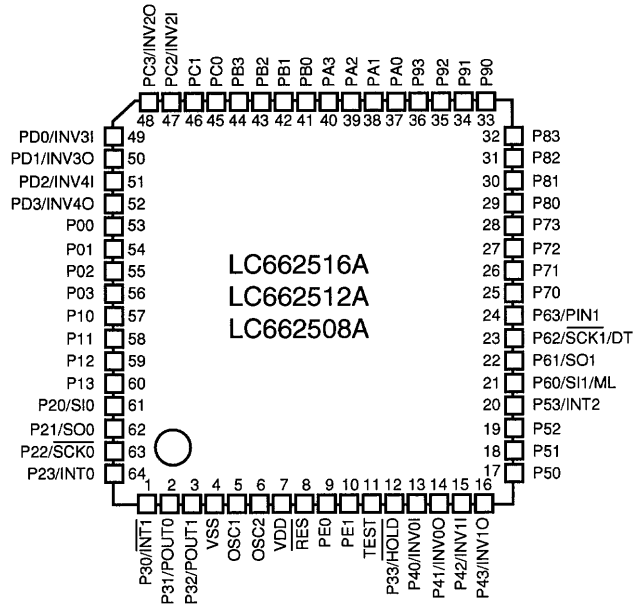
Type No.	No. of pins	ROM capacity	RAM capacity	Package		Features
LC66304A/306A/308A	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	Normal versions 4.0 to 6.0 V/0.92 µs
LC66404A/406A/408A	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	
LC66506B/508B/512B/516B	64	6 K/8 K/12 K/16 KB	512 W	DIP64S	QFP64A	
LC66354A/356A/358A	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	Low-voltage versions 2.2 to 5.5 V/3.92 µs
LC66354S/356S/358S	42	4 K/6 K/8 KB	512 W		QFP44M	
LC66556A/558A/562A/566A	64	6 K/8 K/12 K/16 KB	512 W	DIP64S	QFP64E	
LC66354B/356B/358B	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	Low-voltage high-speed versions 3.0 to 5.5 V/0.92 µs
LC66556B/558B/562B/566B	64	6 K/8 K/12 K/16 KB	512 W	DIP64S	QFP64E	
LC66354C/356C/358C	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	2.5 to 5.5 V/0.92 µs
LC662104A/06A/08A	30	4 K/6 K/8 KB	384 W	DIP30SD	MFP30S	On-chip DTMF generator versions 3.0 to 5.5 V/0.95 µs
LC662304A/06A/08A/12A/16A	42	4 K/6 K/8 K/12 K/16 KB	512 W	DIP42S	QFP48E	
LC662508A/12A/16A	64	8 K/12 K/16 KB	512 W	DIP64S	QFP64E	
LC665304A/06A/08A/12A/16A	48	4 K/6 K/8 K/12 K/16 KB	512 W	DIP48S	QFP48E	Dual oscillator support 3.0 to 5.5 V/0.95 µs
LC66E308	42	EPROM 8 KB	512 W	DIC42S with window	QFC48 with window	Window and OTP evaluation versions 4.5 to 5.5 V/0.92 µs
LC66P308	42	OTPROM 8 KB	512 W	DIP42S	QFP48E	
LC66E408	42	EPROM 8 KB	512 W	DIC42S with window	QFC48 with window	
LC66P408	42	OTPROM 8 KB	512 W	DIP42S	QFP48E	
LC66E516	64	EPROM 16 KB	512 W	DIC64S with window	QFC64 with window	
LC66P516	64	OTPROM 16 KB	512 W	DIP64S	QFP64E	
LC66E2108	30	EPROM 8 KB	384 W			Window evaluation versions 4.5 to 5.5 V/0.92 µs
LC66E2316	42	EPROM 16 KB	512 W	DIC42S with window	QFC48 with window	
LC66E2516	64	EPROM 16 KB	512 W	DIC64S with window	QFC64 with window	
LC66E5316	52/48	EPROM 16 KB	512 W	DIC52S with window	QFC48 with window	
LC66P2108	30	OTPROM 8 KB	384 W	DIP30SD	MFP30S	OTP 4.0 to 5.5 V/0.95 µs
LC66P2316	42	OTPROM 16 KB	512 W	DIP42S	QFP48E	
LC66P2516	64	OTPROM 16 KB	512 W	DIP64S	QFP64E	
LC66P5316	48	OTPROM 16 KB	512 W	DIP48S	QFP48E	

Pin Assignments

DIP64S



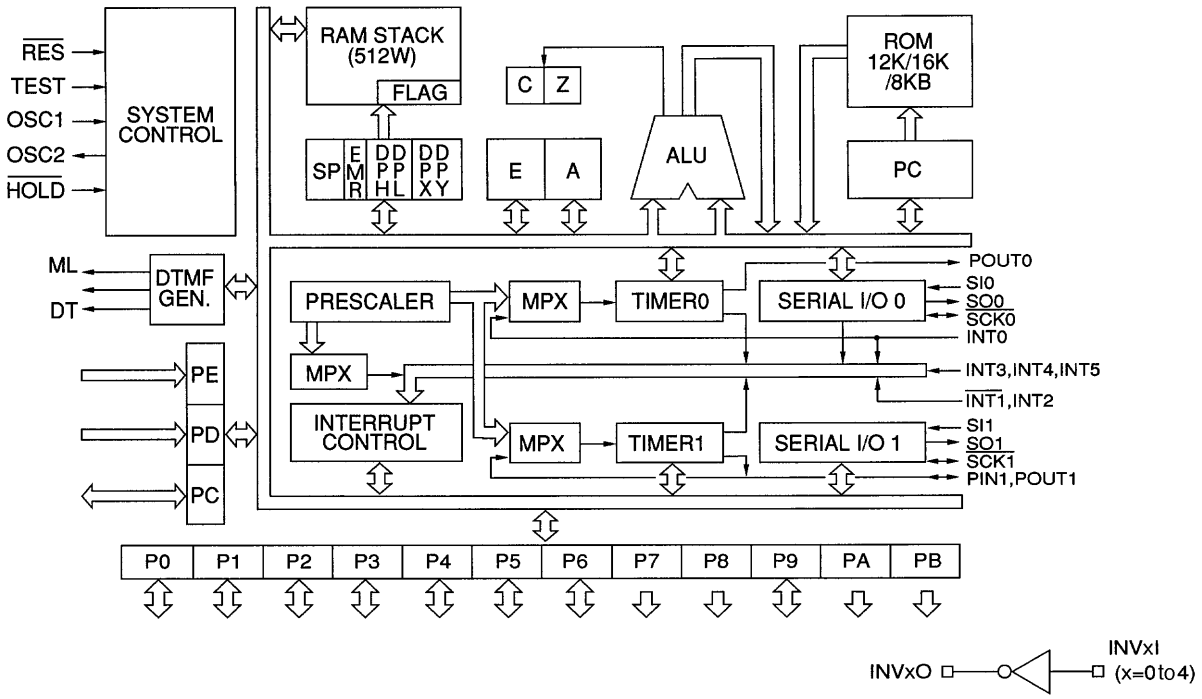
QFP64E



Top view

We recommend the use of reflow-soldering techniques to solder-mount QFP packages.
Please consult with your Sanyo representative for details on process conditions if the package itself is to be directly immersed in a dip-soldering bath (dip-soldering techniques).

System Block Diagram



- When DT, ML, and DP are used, only the SIO channel can be used for serial I/O.
- The INT3, INT4, and INT5 pins can be used with internal functions.

Differences between the LC665XX Series and the LC6625XX Series

Item	LC6650XB Series (Including the LC66599 evaluation chip)	LC6655XB Series	LC6625XX Series
System differences • Hardware wait time (number of cycles) when hold mode is cleared	65536 cycles About 64 ms at 4 MHz (Tcyc = 1 µs)	16384 cycles About 16 ms at 4 MHz (Tcyc = 1 µs)	16384 cycles About 16 ms at 4 MHz (Tcyc = 1 µs)
• Value of timer 0 after a reset (Including the value after hold mode is cleared)	Set to FF0.	Set to FFC.	Set to FFC.
• DTMF generator	None (Tools are handled with external devices.)	None	Yes
• Inverter array	None (Tools are handled with external devices.)	None	Yes
• Three-value inputs/comparator inputs	Yes	Yes	None
• Three-state output from P31 and P32	None	None	Yes
• Using P0 to clear halt mode	In 4-bit groups	In 4-bit groups	Can be specified for each bit.
• External extended interrupts	For INT3, INT4, and INT5. (Tools are handled with external devices.)	For INT3, INT4, and INT5.	INT3, INT4, and INT5 can be used with the internal functions.
• INT2 functions	Shared with P90 ($\overline{\text{INT2}}$) (Tools are handled with external devices.)	Shared with P90 ($\overline{\text{INT2}}$)	Shared with P53 (INT2)
Differences in main characteristics • Operating power-supply voltage and operating speed (cycle time)	• LC66506B/08B/12B/16B 4.0 to 6.0 V/0.92 to 10 µs • LC66E516/P516 4.5 to 5.5 V/0.92 to 10 µs	• 3.0 to 5.5 V/0.92 to 10 µs • LC6655XA, 56XA 2.2 to 5.5 V/3.92 to 10 µs 3.0 to 5.5 V/1.96 to 10 µs	3.0 to 5.5 V/0.95 to 10 µs
• Pull-up resistors	P0, P1, P4, and P5: about 3 to 10 kΩ	P0, P1, P4, and P5: about 3 to 10 kΩ	P0, P1, P4, and P5: about 100 kΩ
• Port voltage handling	• P2, P3, P6, P7, and PA: 15V handling • Others: Normal voltage	• P2, P3, P6, P7, and PA: 15V handling • Others: Normal voltage	P2, P3, P61, P63, and PA: 15V voltage handling Others: normal voltage

Pin Function Overview

Pin	I/O	Overview	Output driver type	Options	State after a reset	Standby mode operation
P00 P01 P02 P03	I/O	I/O ports P00 to P03 • Input or output in 4-bit or 1-bit units • P00 to P03 support the halt mode control function (This function can be specified in bit units.)	• Pch: Pull-up MOS type • Nch: Intermediate sink current type	• Pull-up MOS or Nch OD output • Output level on reset	High or low (option)	Hold mode: Output off Halt mode: Output retained
P10 P11 P12 P13	I/O	I/O ports P10 to P13 Input or output in 4-bit or 1-bit units	• Pch: Pull-up MOS type • Nch: Intermediate sink current type	• Pull-up MOS or Nch OD output • Output level on reset	High or low (option)	Hold mode: Output off Halt mode: Output retained
P20/SI0 P21/$\overline{SO0}$ P22/$\overline{SCK0}$ P23/INT0	I/O	I/O ports P20 to P23 • Input or output in 4-bit or 1-bit units • P20 is also used as the serial input SI0 pin. • P21 is also used as the serial output $\overline{SO0}$ pin. • P22 is also used as the serial clock $\overline{SCK0}$ pin. • P23 is also used as the INT0 interrupt request pin, and also as the timer 0 event counting and pulse width measurement input.	• Pch: CMOS type • Nch: Intermediate sink current type • Nch: +15V handling when OD option selected	CMOS or Nch OD output	H	Hold mode: Output off Halt mode: Output retained
P30/$\overline{INT1}$ P31/POUT0 P32/POUT1	I/O	I/O ports P30 to P32 • Input or output in 3-bit or 1-bit units • P30 is also used as the $\overline{INT1}$ interrupt request. • P31 is also used for the square wave output from timer 0. • P32 is also used for the square wave and PWM output from timer 1. • P31 and P32 also support 3-state outputs.	• Pch: CMOS type • Nch: Intermediate sink current type • Nch: +15V handling when OD option selected	CMOS or Nch OD output	H	Hold mode: Output off Halt mode: Output retained
P33/$\overline{HOLD}$	I	Hold mode control input • Hold mode is set up by the $\overline{HOLD}$ instruction when $\overline{HOLD}$ is low. • In hold mode, the CPU is restarted by setting $\overline{HOLD}$ to the high level. • This pin can be used as input port P33 along with P30 to P32. • When the P33/$\overline{HOLD}$ pin is at the low level, the CPU will not be reset by a low level on the $\overline{RES}$ pin. Therefore, applications must not set P33/$\overline{HOLD}$ low when power is first applied.				
P40/INV0I P41/INV0O P42/INV1I P43/INV1O	I/O	I/O ports P40 to P43 • Input or output in 4-bit or 1-bit units • Input or output in 8-bit units when used in conjunction with P50 to P53. • Can be used for output of 8-bit ROM data when used in conjunction with P50 to P53. • Dedicated inverter circuit (option)	• Pch: Pull-up MOS type • CMOS type when the inverter circuit option is selected • Nch: Intermediate sink current type	• Pull-up MOS or Nch OD output • Output level on reset • Inverter circuit	High or low or inverter I/O (option)	Hold mode: Port output off, inverter output off Halt mode: Port output retained, inverter output continues

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Pin	I/O	Overview	Output driver type	Options	State after a reset	Standby mode operation
P50 P51 P52 P53/INT2	I/O	I/O ports P50 to P53 • Input or output in 4-bit or 1-bit units • Input or output in 8-bit units when used in conjunction with P40 to P43. • Can be used for output of 8-bit ROM data when used in conjunction with P40 to P43. • P53 is also used as the INT2 interrupt request.	• Pch: Pull-up MOS type • Nch: Intermediate sink current type	• Pull-up MOS or Nch OD output • Output level on reset	High or low (option)	Hold mode: Output off Halt mode: Output retained
P60/SI1/ML P61/S01/ P62/ SCK1/DT/ P63/PIN1	I/O	I/O ports P60 to P63 • Input or output in 4-bit or 1-bit units • P60 is also used as the SI1 serial input pin and as the ML melody output pin. • P61 is also used as the SO1 serial output pin. • P62 is also used as the $\overline{\text{SCK1}}$ serial clock pin and the DT dial tone output pin. • P63 is also used for the event count input to timer 1.	• Pch: CMOS type • Nch: Intermediate sink current type • Nch: +15V handling when OD option selected (P61 and P63 only)	CMOS or Nch OD output (When the ML or DT output is used, select open-drain output and provide an external pull-up resistor.)	H	Hold mode: Output off Halt mode: Output retained
P70 P71 P72 P73	O	Output ports P70 to P73 • Output in either 1-bit or 4-bit units. • The contents of the output latch are input by input instruction.	• Pch: Pu MOS • Nch: Intermediate sink current type	Pull-up MOS or Nch OD output	H	Hold mode: Output off Halt mode: Output retained
P80 P81 P82 P83	O	Output ports P80 to P83 • Output in either 1-bit or 4-bit units. • The contents of the output latch are input by input instruction.	• Pch: Pu MOS • Nch: Intermediate sink current type	• CMOS or Pch OD output • Output level on reset	High or low (option)	Hold mode: Output off Halt mode: Output retained
P90 P91 P92 P93	I/O	I/O ports P90 to 93. • Input or output in either 1-bit or 4-bit units.	• Pch: CMOS • Nch: Intermediate sink current type	CMOS or Nch OD output	H	Hold mode: Output off Halt mode: Output retained
PA0 PA1 PA2 PA3	O	Output ports PA0 to PA3 • Output in either 1-bit or 4-bit units. • The contents of the output latch are input by input instruction.	• Pch: Pu MOS • Nch: +15-V handling when OD option selected	Pull-up MOS or Nch OD output	H	Hold mode: Output off Halt mode: Output retained
PB0 PB1 PB2 PB3	O	Output ports PB0 to PB3 • Output in either 1-bit or 4-bit units. • The contents of the output latch are input by input instruction.	• Pch: Pull-up MOS • Nch: Intermediate sink current type	Pull-up MOS or Nch OD output	H	Hold mode: Output off Halt mode: Output retained
PC0 PC1 PC2/INV2I PC3/INV2O	I/O	I/O ports PC0 to PC3 • Output in either 1-bit or 4-bit units. • Dedicated input ports PC2 to PC3 • Dedicated inverter circuits (option)	• Pch: CMOS • Nch: Intermediate sink current type	• CMOS or Nch OD output • Inverter circuit	High or inverter I/O (option)	Hold mode: Port output off Inverter output off Halt mode: Port output retained Inverter output retained

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Pin	I/O	Overview	Output driver type	Options	State after a reset	Standby mode operation
PD0/INV3I PD1/INV3O PD2/INV4I PD3/INV4O	I	Dedicated input ports PD0 to PD3 Dedicated inverter circuits (option)	• When the inverter circuit option is selected. • Pch: CMOS type • Nch: Intermediate sink current type	Inverter circuits	Normal input or inverter I/O (option)	Inverter • Hold mode: output off • Halt mode: output continues
PE0 PE1	I	Dedicated input ports				Hold mode: input disabled Halt mode: input enabled
OSC1 OSC2	I O	System clock oscillator connections When an external clock is used, leave OSC2 open and connect the clock signal to OSC1.		Ceramic oscillator or external clock selection	Option selection	Hold mode: Oscillator stops Halt mode: Oscillator continues
$\overline{\text{RES}}$	I	System reset input When the P33/$\overline{\text{HOLD}}$ pin is at the high level, a low level input to the $\overline{\text{RES}}$ pin will initialize the CPU.				
TEST	I	CPU test pin This pin must be connected to V_{SS} during normal operation.				
V_{DD} V_{SS}		Power supply pins				

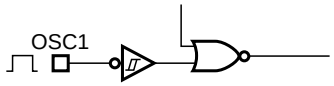
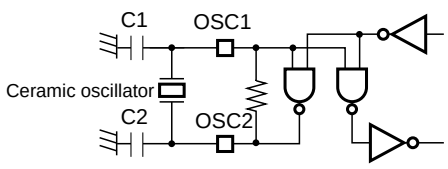
Note: Pull-up MOS type: The output circuit includes a MOS transistor that pulls the pin up to V_{DD}.
CMOS output: Complementary output.
OD output: Open-drain output

User Options

1. Ports 0, 1, 4, 5, and 8 output level at reset option
   The output levels at reset for I/O ports 0, 1, 4, 5, and 8 in independent 4-bit groups, can be selected from the following two options.

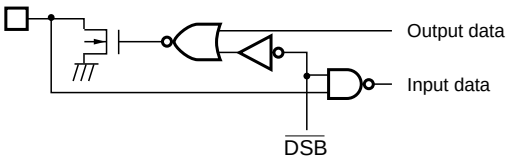
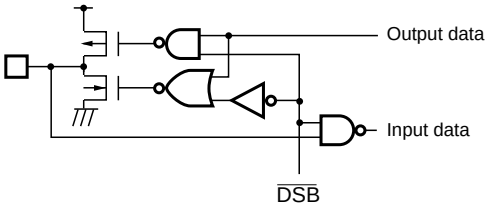
Option	Conditions and notes
Output high at reset	The four bits of ports 0, 1, 4, 5, or 8 are set in a group
Output low at reset	The four bits of ports 0, 1, 4, 5, or 8 are set in a group

2. Oscillator circuit options
   • Main clock

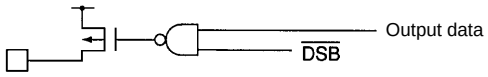
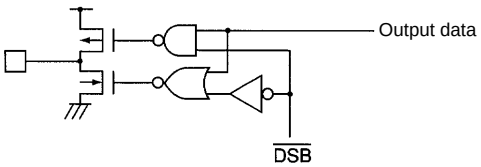
Option	Circuit	Conditions and notes
External clock		The input has Schmitt characteristics
Ceramic oscillator		

Note: There is no RC oscillator option.

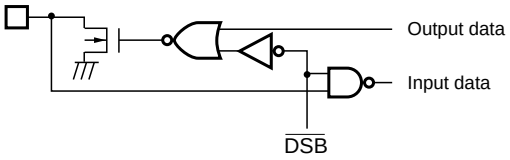
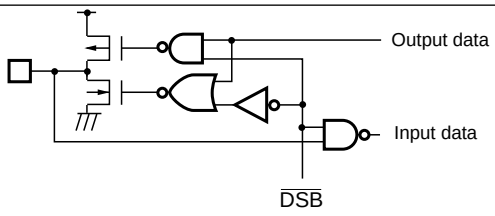
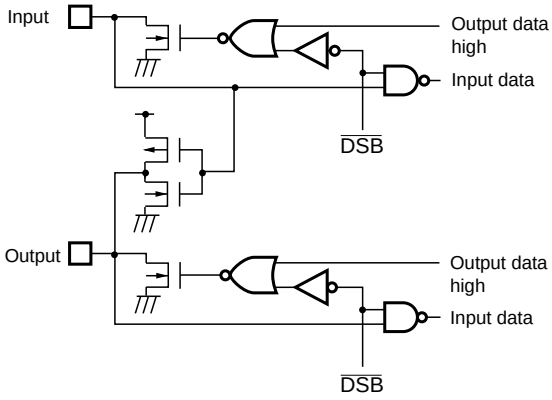
3. Watchdog timer option
   A runaway detection function (watchdog timer) can be selected as an option.
4. Port output type options
   • The output type of each bit (pin) in ports P0, P1, P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P4, P5, P6, P7, P9, PA, PB, and PC can be selected individually from the following two options. (in1-bit units)

Option	Circuit	Conditions and notes
Open-drain output		The ports P2, P3, P5, P6, and P9 inputs have Schmitt characteristics. P7, PA, and PB are output-only ports.
Output with built-in pull-up resistor		The ports P2, P3, P5, P6, and P9 inputs have Schmitt characteristics. The CMOS outputs (ports P2, P3, P6, P9, and PC) and the pull-up MOS outputs (P0, P1, P4, P5, P7, PA, and PB) are distinguished by the drive capacity of the p-channel transistor.

   • The two options can be specified for P8 (in 1-bit units)

Option	Circuit	Conditions and notes
Open-drain output		
Output with built-in pull-up resistor (CMOS output)		

5. Inverter array circuit option
   One of the following options can be selected for each of the following port sets: P40/P41, P42/P43, PC2/PC3, PD0/PD1, and PD2/PD3. (PDs do not use option 1 because they are dedicated to input.)

Option	Circuit	Conditions and notes
Normal port I/O circuit		When the open-drain output type is selected
		When the built-in pull-up resistor output type is selected. The CMOS outputs (PC) and the pull-up MOS outputs (P4) are distinguished by the drive capacity of the P-channel transistor.
Inverter I/O circuit		If this option is selected, The I/O circuit is disabled by the DSB signal. Also note that the open-drain port output type option and the high level at reset option must be selected.

LC662516 Series Option Data Area and Definitions

ROM area	Bit	Option specified		Option/data relationship
3FF0H	7	P5	Output level at reset	0 = high level, 1 = low level
	6	P4		
	5	Unused		This bit must be set to 0.
	4	Oscillator option		0 = external clock, 1 = ceramic oscillator
	3	P8	Output level at reset	0 = low level, 1 = high level
	2	P1		
	1	P0		
	0	Watchdog timer option		0 = none, 1 = yes
3FF1H	7	P13	Output type	0 = OD, 1 = PU
	6	P12		
	5	P11		
	4	P10		
	3	P03	Output type	0 = OD, 1 = PU
	2	P02		
	1	P01		
	0	P00		
3FF2H	7	Unused		This bit must be set to 0.
	6	P32	Output type	0 = OD, 1 = PU
	5	P31		
	4	P30		
	3	P23	Output type	0 = OD, 1 = PU
	2	P22		
	1	P21		
	0	P20		
3FF3H	7	P53	Output type	0 = OD, 1 = PU
	6	P52		
	5	P51		
	4	P50		
	3	P43	Output type	0 = OD, 1 = PU
	2	P42		
	1	P41		
	0	P40		
3FF4H	7	P73	Output type	0 = OD, 1 = PU
	6	P72		
	5	P71		
	4	P70		
	3	P63	Output type	0 = OD, 1 = PU
	2	P62		
	1	P61		
	0	P60		
3FF5H	7	P93	Output type	0 = OD, 1 = PU
	6	P92		
	5	P91		
	4	P90		
	3	P83	Output type	0 = OD, 1 = PU
	2	P82		
	1	P81		
	0	P80		
3FF6H	7	PB3	Output type	0 = OD, 1 = PU
	6	PB2		
	5	PB1		
	4	PB0		
	3	PA3	Output type	0 = OD, 1 = PU
	2	PA2		
	1	PA1		
	0	PA0		

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ROM area	Bit	Option specified		Option/data relationship
3FF7H	7	Unused		This bit must be set to 0.
	6			
	5			
	4			
	3	PC3	Output type	0 = OD, 1 = PU
	2	PC2		
	1	PC1		
	0	PC2		
3FF8H	7	ML disabled option		0 = disabled, 1 = enabled
	6	Unused		This bit must be set to 1.
	5	Unused		This bit must be set to 1.
	4	PD3	Inverter output	0 = inverter output, 1 = none
	3	PD1		
	2	PC3		
	1	P43		
	0	P41		
3FF9H	7	Unused		This bit must be set to 0.
	6			
	5			
	4			
	3	Unused		This bit must be set to 0.
	2			
	1			
	0			
3FFAH	7	Unused		This bit must be set to 0.
	6			
	5			
	4			
	3	Unused		This bit must be set to 0.
	2			
	1			
	0			
3FFBH	7	Unused		This bit must be set to 0.
	6			
	5			
	4			
	3	Unused		This bit must be set to 0.
	2			
	1			
	0			
3FFCH	7	Unused		This bit must be set to 0.
	6			
	5			
	4			
	3	Unused		This bit must be set to 0.
	2			
	1			
	0			
3FFDH	7	Reserved. Must be set to predefined data values.		This data is generated by the assembler. If the assembler is not used, set this data to 00.
	6			
	5			
	4			
	3			
	2			
	1			
	0			

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ROM area	Bit	Option specified	Option/data relationship
3FFEH	7	Reserved. Must be set to predefined data values.	This data is generated by the assembler. If the assembler is not used, set this data to 00.
	6		
	5		
	4		
	3		
	2		
	1		
	0		
3FFFH	7	Reserved. Must be set to predefined data values.	This data is generated by the assembler. If the assembler is not used, set this data to 00.
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit	Note
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V	
Input voltage	$V_{IN}1$	P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P61, and P63	–0.3 to +15.0	V	1
	$V_{IN}2$	All other inputs	–0.3 to V_{DD} + 0.3	V	2
Output voltage	$V_{OUT}1$	P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P61, P63, and PA	–0.3 to +15.0	V	1
	$V_{OUT}2$	All other inputs	–0.3 to V_{DD} + 0.3	V	2
Output current per pin	$I_{ON}1$	P0, P1, P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P4, P5, P6, P7, P8, P9, PA, PB, PC, PD1, PD3	20	mA	3
	$I_{ON}2$	P41, P43, PC3, PD1, PD3	20	mA	3
	$-I_{OP}1$	P0, P1, P4, P5, P7, PA, PB	2	mA	4
	$-I_{OP}2$	P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P6, P8, P9, and PC	4	mA	4
	$-I_{OP}3$	P41, P43, PC3, PD1, PD3	10	mA	4
Total pin current	$\Sigma I_{ON}1$	P0, P1, P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), PB, PC, and PD	75	mA	3
	$\Sigma I_{ON}2$	P4, P5, P6, P7, P8, P9, and PA	75	mA	3
	$\Sigma I_{OP}1$	P0, P1, P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), PB, PC, and PD	25	mA	4
	$\Sigma I_{OP}2$	P4, P5, P6, P7, P8, P9, and PA	25	mA	4
Allowable power dissipation	Pd max	Ta = –30 to +70°C: DIP64S (QFP64E)	600 (430)	mW	5
Operating temperature	Topr		–30 to +70	°C	
Storage temperature	Tstg		–55 to +125	°C	

Note: 1. Applies to pins with open-drain output specifications. For pins with other than open-drain output specifications, the ratings in the pin column for that pin apply.
2. For the oscillator input and output pins, levels up to the free-running oscillation level are allowed.
3. Sink current (Applies to P8 when the CMOS output specifications and applies to PD when the inverter array specifications are selected.)
4. Source current (Applies to all pins except P8 for which the pull-up output specifications, the CMOS output specifications, or the inverter array specifications have been selected. Applies to PD pins for which the inverter array specifications have been selected.)
Contact your Sanyo representative for details on the electrical characteristics when the inverter array specifications option is selected.
5. We recommend the use of reflow soldering techniques to solder mount QFP packages.
Please consult with your Sanyo representative for details on process conditions if the package itself is to be directly immersed in a dip-soldering bath (dip-soldering techniques).

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V, unless otherwise specified.

Parameter	Symbol	Conditions	min	typ	max	Unit	Note
Operating supply voltage	V_{DD}	V_{DD}	3.0		5.5	V	
Memory retention supply voltage	$V_{DD}H$	V_{DD}: During hold mode	1.8		5.5	V	
Input high-level voltage	$V_{IH}1$	P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P61, and P63: N-channel output transistor off	0.8 V_{DD}		13.5	V	1
	$V_{IH}2$	P33/$\overline{\text{HOLD}}$, P5, P60, P62, P9, $\overline{\text{RES}}$, OSC1: N-channel output transistor off	0.8 V_{DD}		V_{DD}	V	2
	$V_{IH}3$	P0, P1, P4, P5, PC, PD, PE: N-channel output transistor off	0.8 V_{DD}		V_{DD}	V	3
Input low-level voltage	$V_{IL}1$	P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P5, P6, P9, $\overline{\text{RES}}$, and OSC1: N-channel output transistor off	V_{SS}		0.2 V_{DD}	V	2
	$V_{IL}2$	P33/$\overline{\text{HOLD}}$: V_{DD} = 1.8 to 5.5 V	V_{SS}		0.2 V_{DD}	V	
	$V_{IL}3$	P0, P1, P4, P5, PC, PD, PE, TEST: N-channel output transistor off	V_{SS}		0.2 V_{DD}	V	3
Operating frequency (instruction cycle time)	fop (Tcyc)		0.4 (10)		4.2 (0.95)	MHz (µs)	
[External clock input conditions]							
Frequency	f_{ext}	OSC1: Defined by Figure 1. Input the clock signal to OSC1 and leave OSC2 open. (External clock input must be selected as the oscillator circuit option.)	0.4		4.2	MHz	
Pulse width	t_{extH}, t_{extL}	OSC1: Defined by Figure 1. Input the clock signal to OSC1 and leave OSC2 open. (External clock input must be selected as the oscillator circuit option.)	100			ns	
Rise and fall times	t_{extR}, t_{extF}	OSC1: Defined by Figure 1. Input the clock signal to OSC1 and leave OSC2 open. (External clock input must be selected as the oscillator circuit option.)			30	ns	

Note: 1. Applies to pins with open-drain specifications. However, $V_{IH}2$ applies to the P33/$\overline{\text{HOLD}}$ pin.
When ports P2, P3, and P6 have CMOS output specifications they cannot be used as input pins.
2. Applies to pins with open-drain specifications. P9 port pins with CMOS output specifications cannot be used as input pins.
3. PC port pins with CMOS output specifications cannot be used as input pins.
Contact Sanyo for details on the allowable operating ranges for P4,PC, and PD pins with inverter array specifications.

Electrical Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V unless otherwise specified.

Parameter		Symbol	Conditions	min	typ	max	Unit	Note
Input high-level current		$I_{IH}1$	P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P61, and P63: V_{IN} = 13.5 V, with the output Nch transistor off			5.0	µA	1
		$I_{IH}2$	P0, P1, P4, P5, P6, P9, PC, TEST, $\overline{\text{RES}}$, and P33/$\overline{\text{HOLD}}$ (Does not apply to P61 and P63.): V_{IN} = V_{DD}, with the output Nch transistor off			1.0	µA	1
		$I_{IH}3$	PD, PE: V_{IN} = V_{DD}, with the output Nch transistor off			1.0	µA	1
Input low-level current		$I_{IL}1$	Input ports other than PD and PE3: V_{IN} = V_{SS}, with the output Nch transistor off	–1.0			µA	2
		$I_{IL}2$	PD, PE: V_{IN} = V_{SS}, with the output Nch transistor off	–1.0			µA	2
Output high-level voltage		$V_{OH}1$	P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P6, P8, P9, and PC: I_{OH} = –1 mA	V_{DD} – 1.0			V	3
			P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P6, P8, P9, and PC: I_{OH} = –0.1 mA	V_{DD} – 0.5				
Value of the output pull-up resistor		R_{PO}	P0, P1, P4, P5, P7, PA, and PB	30	100	300	kΩ	
Output low-level voltage		$V_{OL}1$	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, and PC (except for the P33/$\overline{\text{HOLD}}$ pin): I_{OL} = 1.6 mA			0.4	V	5
		$V_{OL}2$	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, and PC (except for the P33/$\overline{\text{HOLD}}$ pin): I_{OL} = 8 mA			1.5	V	5
Output off leakage current		$I_{OFF}1$	P2, P3, P61, P63, and PA: V_{IN} = 13.5 V			5.0	µA	6
		$I_{OFF}2$	Does not apply to P2, P3, P61, P63, P8, and PA: V_{IN} = V_{DD}			1.0	µA	6
		$I_{OFF}3$	P8: V_{IN} = V_{SS}	–1.0			µA	7
[Schmitt characteristics]								
Hysteresis voltage		V_{HYS}	P2, P3, P5, P6, P61, P9, $\overline{\text{RES}}$, OSC1 (EXT)		0.1 V_{DD}		V	
High-level threshold voltage		Vt_H		0.5 V_{DD}		0.8 V_{DD}	V	
Low-level threshold voltage		Vt_L		0.2 V_{DD}		0.5 V_{DD}	V	
[Ceramic oscillator]								
Oscillator frequency		f_{CF}	OSC1, OSC2: See Figure 2. 4 MHz		4.0		MHz	
Oscillator stabilization time		f_{CFS}	See Figure 3. 4 MHz			10.0	ms	
[Serial clock]								
Cycle time	Input	t_{CKCY}	$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$: With the timing of Figure 4 and the test load of Figure 5.	0.9			µs	
	Output			2.0			Tcyc	
Low-level and high-level pulse widths	Input	t_{CKL}		0.4			µs	
	Output	t_{CKH}		1.0			Tcyc	
Rise an fall times	Output	t_{CKR}, t_{CKF}				0.1	µs	
[Serial input]								
Data setup time		t_{ICK}	SI0, SI1: With the timing of Figure 4. Stipulated with respect to the rising edge (↑) of $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$.	0.3			µs	
Data hold time		t_{CKI}		0.3			µs	
[Serial output]								
Output delay time		t_{CKO}	SO0, SO1: With the timing of Figure 5 and the test load of Figure 5. Stipulated with respect to the falling edge (↓) of $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$.			0.3	µs	

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Parameter	Symbol	Conditions	min	typ	max	Unit	Note
[Pulse conditions]							
INT0 high and low-level pulse widths	t_{IOH}, t_{IOL}	INT0: Figure 6, conditions under which the INT0 interrupt can be accepted, conditions under which the timer 0 event counter or pulse width measurement input can be accepted	2			Tcyc	
High and low-level pulse widths for interrupt inputs other than INT0	t_{IIH}, t_{IIL}	$\overline{INT1}$, $\overline{INT2}$: Figure 6, conditions under which the corresponding interrupt can be accepted	2			Tcyc	
PIN1 high and low-level pulse widths	t_{PINH}, t_{PINL}	PIN1: Figure 6, conditions under which the timer 1 event counter input can be accepted	2			Tcyc	
$\overline{RES}$ high and low-level pulse widths	t_{RSH}, t_{RSL}	$\overline{RES}$: Figure 6, conditions under which reset can be applied.	3			Tcyc	
Operating current drain	$I_{DD\ OP}$	V_{DD}: 4MHz ceramic oscillator		4.5	8.0	mA	8
		V_{DD}: 4MHz external clock		4.5	8.0	mA	
Halt mode current drain	I_{DDHALT}	V_{DD}: 4MHz ceramic oscillator		2.5	5.5	mA	
		V_{DD}: 4MHz external clock		2.5	5.5	mA	
Hold mode current drain	I_{DDHOLD}	V_{DD}: V_{DD} = 1.8 to 5.5 V		0.01	10	µA	

Note: 1. With the output Nch transistor off in shared I/O ports with the open-drain output specifications. These pins cannot be used as input pins if the CMOS output specifications are selected.
2. With the output Nch transistor off in shared I/O ports with the open-drain output specifications. The rating for the pull-up output specification pins is stipulated in terms of the output pull-up current IPO. These pins cannot be used as input pins if the CMOS output specifications are selected.
3. With the output Nch transistor off for CMOS output specification pins. (Also applicable when the p-channel open-drain option is specified for P8.)
4. With the output Nch transistor off for pull-up output specification pins.
5. Applies to P8 when the CMOS output specifications are selected.
6. With the output Nch transistor off for open-drain output specification pins.
7. With the output Pch transistor off for open-drain output specification pins.
8. Reset state

Tone (DTMF) Output Characteristics

DC Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V

1. When the MLOUT enable option is selected (the ML output function can be used)

Parameter	Symbol	Conditions	min	typ	max	Unit
Tone output voltage (p-p)	V_{T1}	DT: Dual tone, V_{DD} = 3.5 to 5.5 V*	0.9	1.3	2.0	V
Row/column tone output voltage ratio	D_{BCR1}	DT: Dual tone, V_{DD} = 3.5 to 5.5 V*	1.0	2.0	3.0	dB
Tone distortion	THD1	DT: Single tone, V_{DD} = 3.5 to 5.5 V*		2	7	%

Note: * See item 2. below if the MLOUT disable mask option is selected.

2. When the MLOUT disable option is selected (the ML output function cannot be used)

Parameter	Symbol	Conditions	min	typ	max	Unit
Tone output voltage (p-p)	V_{T1}	DT: Dual tone, V_{DD} = 3.0 to 5.5 V*	0.9	1.3	2.0	V
Row/column tone output voltage ratio	D_{BCR1}	DT: Dual tone, V_{DD} = 3.0 to 5.5 V*	1.0	2.0	3.0	dB
Tone distortion	THD1	DT: Single tone, V_{DD} = 3.0 to 5.5 V*		2	7	%

Note: * See item 1. above if the MLOUT enable mask option is selected.

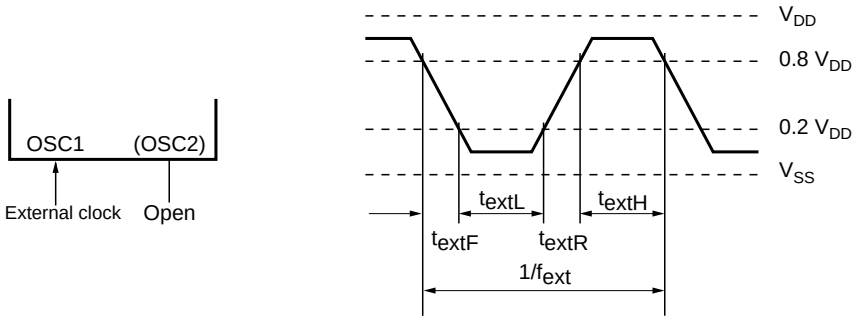

Figure 1 External Clock Input Waveform

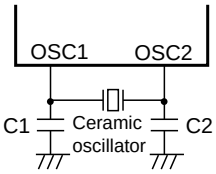

Figure 2 Ceramic Oscillator Circuit

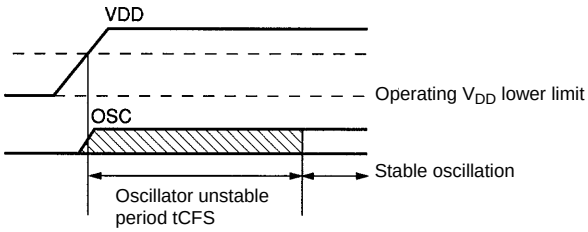

Figure 3 Oscillator Stabilization Period

Table 1 Recommended Ceramic Oscillator Constants

External capacitor type		Built-in capacitor type
4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MG	C1 = 33 pF C2 = 33 pF	4 MHz (Murata Mfg. Co., Ltd.) CST4.00MG
4 MHz (Kyocera Corporation) KBR4.0MSB	C1 = 33 pF C2 = 33 pF	4 MHz (Kyocera Corporation) KBR4.0MKC

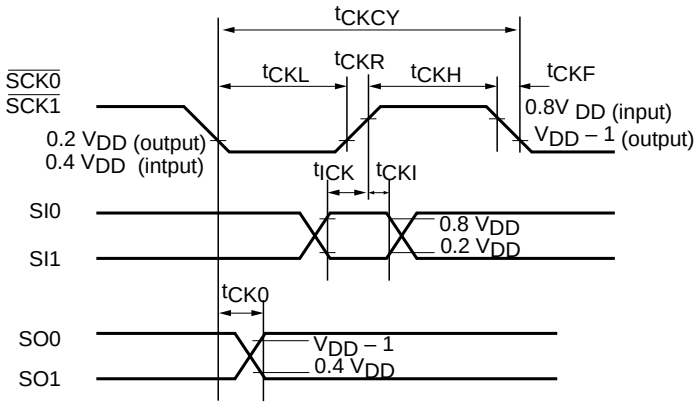

Figure 4 Serial I/O Timing

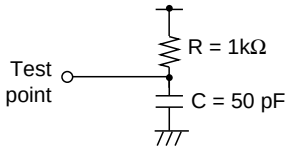

Figure 5 Timing Load

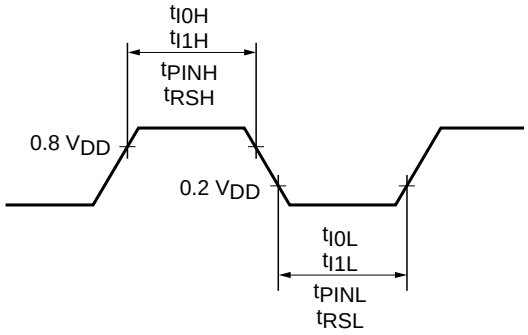

Figure 6 Input Timing for the INT0, $\overline{\text{INT1}}$, INT2, PIN1, and $\overline{\text{RES}}$ pins

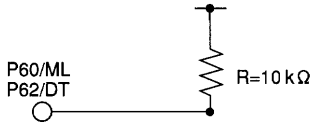

Figure 7 Tone Output Pin Load