



Four-Bit Single-Chip Microcontrollers with 4, 6, 8, 12, and 16 KB of On-Chip ROM

Preliminary

Overview

The LC665304A, LC665306A, LC665308A, LC665312A, and LC665316A are 4-bit CMOS microcontrollers that integrate on a single chip all the functions required in a system controller, including ROM, RAM, I/O ports, a serial interface, 16-value comparator inputs, timers, interrupt functions, and an optional sub-oscillator circuit. These microcontrollers are available in a 48-pin package.

Features and Functions

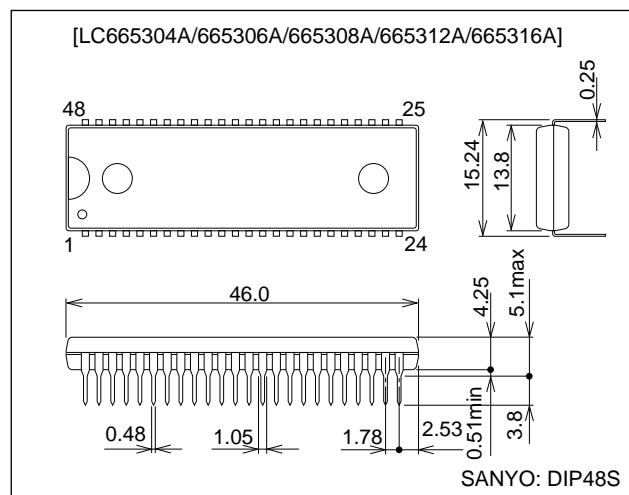
- On-chip ROM capacity of 4, 6, 8, 12, and 16 kilobytes, and an on-chip RAM capacity of 512×4 bits.
- Fully supports the LC66000 Series common instruction set (128 instructions).
- I/O ports: 42 pins
- A sub-oscillator circuit can be used (option)
This circuit allows power dissipation to be reduced by operating at lower speeds.
- 8-bit serial interface: two circuits (can be connected in cascade to form a 16-bit interface)
- Instruction cycle time: 0.95 to 10 μ s (at 3 to 5.5 V)
- Powerful timer functions and prescalers
 - Time limit timer, event counter, pulse width measurement, and square wave output using a 12-bit timer.
 - Time limit timer, event counter, PWM output, and square wave output using an 8-bit timer.
 - Time base function using a 12-bit prescaler.
- Powerful interrupt system with 8 interrupt factors and 8 interrupt vector locations.
 - External interrupts: 3 factors/3 vector locations
 - Internal interrupts: 5 factors/5 vector locations
- Flexible I/O functions
16-value comparator inputs, 20-mA drive outputs, inverter circuits, pull-up and open-drain circuits selectable as options.
- Optional runaway detection function (watchdog timer)
- 8-bit I/O functions
- Power saving functions using halt and hold modes.
- Packages: DIP48S, QIP48E (QFP48E)

- Evaluation LSIs: LC66599 (evaluation chip) + EVA800/850-TB662YXX2
LC66E5316(on-chip EPROM microcontroller)

Package Dimensions

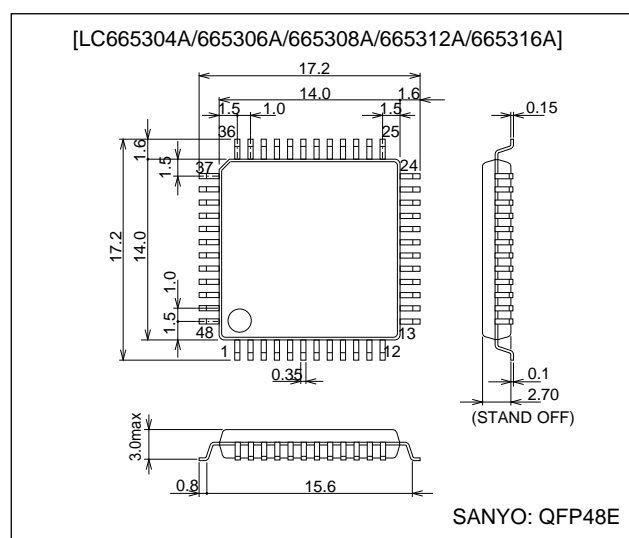
unit: mm

3149-DIP48S



unit: mm

3156-QFP48E

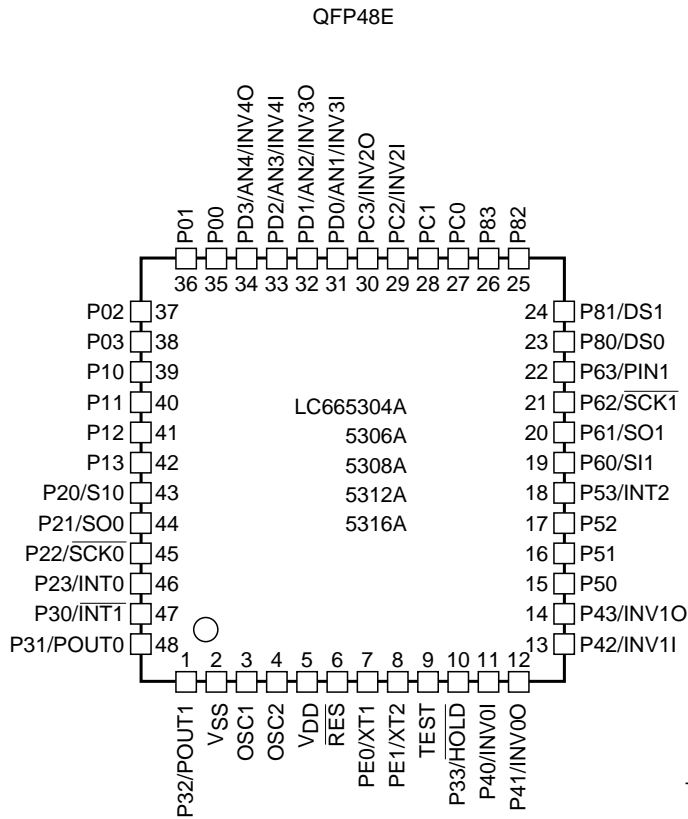
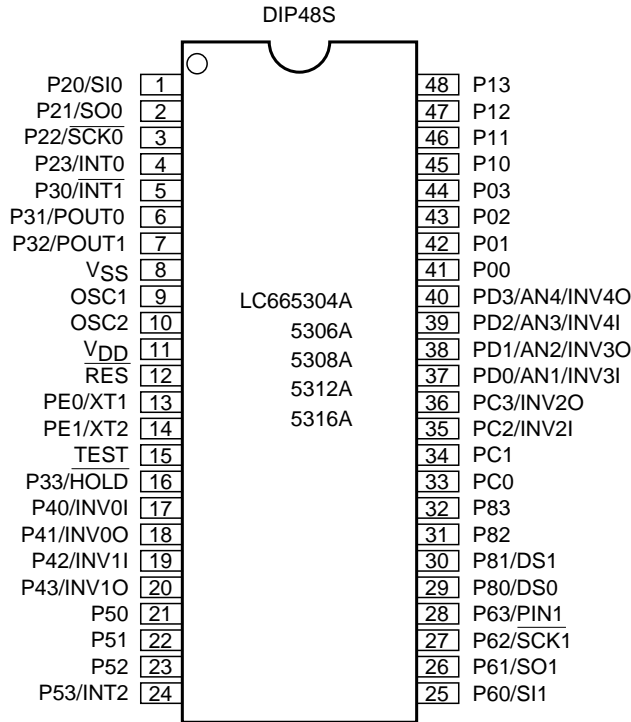


Series Organization

| Type No. | No. of pins | ROM capacity | RAM capacity | Package | | Features |
|---------------------------|-------------|------------------------|--------------|-----------------------|----------------------|--|
| LC66304A/306A/308A | 42 | 4 K/6 K/8 KB | 512 W | DIP42S | QFP48E | Normal versions 4.0 to 6.0 V/0.92 μs |
| LC66404A/406A/408A | 42 | 4 K/6 K/8 KB | 512 W | DIP42S | QFP48E | |
| LC66506B/508B/512B/516B | 64 | 6 K/8 K/12 K/16 KB | 512 W | DIP64S | QFP64A | |
| LC66354A/356A/358A | 42 | 4 K/6 K/8 KB | 512 W | DIP42S | QFP48E | Low-voltage versions 2.2 to 5.5 V/3.92 μs |
| LC66354S/356S/358S | 42 | 4 K/6 K/8 KB | 512 W | | QFP44M | |
| LC66556A/558A/562A/566A | 64 | 6 K/8 K/12 K/16 KB | 512 W | DIP64S | QFP64E | Low-voltage high-speed versions 3.0 to 5.5 V/0.92 μs |
| LC66354B/356B/358B | 42 | 4 K/6 K/8 KB | 512 W | DIP42S | QFP48E | |
| LC66556B/558B/562B/566B | 64 | 6 K/8 K/12 K/16 KB | 512 W | DIP64S | QFP64E | |
| LC66354C/356C/358C | 42 | 4 K/6 K/8 KB | 512 W | DIP42S | QFP48E | 2.5 to 5.5 V/0.92 μs |
| LC662104A/06A/08A | 30 | 4 K/6 K/8 KB | 384 W | DIP30SD | MFP30S | On-chip DTMF generator versions 3.0 to 5.5 V/0.95 μs |
| LC662304A/06A/08A/12A/16A | 42 | 4 K/6 K/8 K/12 K/16 KB | 512 W | DIP42S | QFP48E | |
| LC662508A/12A/16A | 64 | 8 K/12 K/16 KB | 512 W | DIP64S | QFP64E | |
| LC665304A/06A/08A/12A/16A | 48 | 4 K/6 K/8 K/12 K/16 KB | 512 W | DIP48S | QFP48E | Dual oscillator support 3.0 to 5.5 V/0.95 μs |
| LC66E308 | 42 | EPROM 8 KB | 512 W | DIC42S with window | QFC48 with window | Window and OTP evaluation versions 4.5 to 5.5 V/0.92 μs |
| LC66P308 | 42 | OTPROM 8 KB | 512 W | DIP42S | QFP48E | |
| LC66E408 | 42 | EPROM 8 KB | 512 W | DIC42S with window | QFC48 with window | |
| LC66P408 | 42 | OTPROM 8 KB | 512 W | DIP42S | QFP48E | |
| LC66E516 | 64 | EPROM 16 KB | 512 W | DIC64S with window | QFC64 with window | |
| LC66P516 | 64 | OTPROM 16 KB | 512 W | DIP64S | QFP64E | |
| LC66E2108* | 30 | EPROM 8 KB | 384 W | | | |
| LC66E2316 | 42 | EPROM 16 KB | 512 W | DIC42S with window | QFC48 with window | Window evaluation versions 4.5 to 5.5 V/0.92 μs |
| LC66E2516 | 64 | EPROM 16 KB | 512 W | DIC64S with window | QFC64 with window | |
| LC66E5316 | 52/48 | EPROM 16 KB | 512 W | DIC52S with window | QFC48 with window | |
| LC66P2108* | 30 | OTPROM 8 KB | 384 W | DIP30SD | MFP30S | OTP 4.0 to 5.5 V/0.95 μs |
| LC66P2316* | 42 | OTPROM 16 KB | 512 W | DIP42S | QFP48E | |
| LC66P2516 | 64 | OTPROM 16 KB | 512 W | DIP64S | QFP64E | |
| LC66P5316 | 48 | OTPROM 16 KB | 512 W | DIP48S | QFP48E | |

Note: * Under development

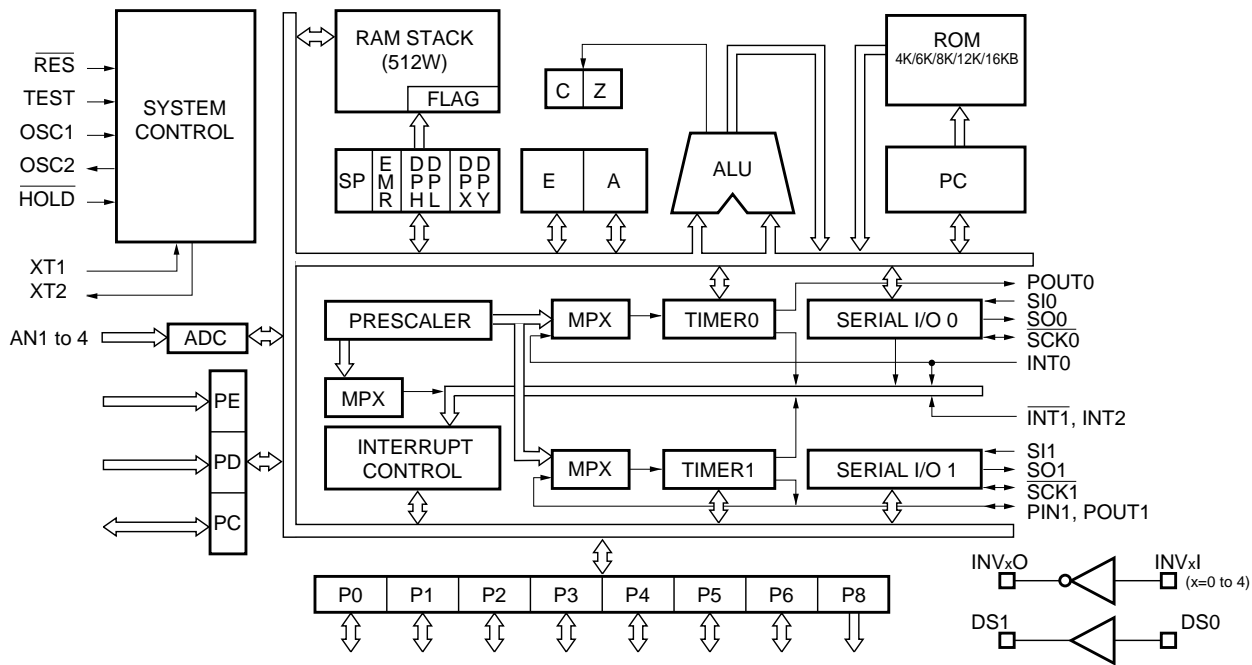
Pin Assignments



We recommend the use of reflow soldering techniques to solder-mount QFP packages.

Please consult with your Sanyo representative for details on process conditions if the package itself is to be directly immersed in a dip-soldering bath (dip-soldering techniques).

System Block Diagram



Differences between the LC6653XX Series and the LC663XX Series

| Item | LC6630X Series (Including the LC66599 evaluation chip) | LC6635XB Series | LC6653XX Series |
|---|---|---|--|
| System differences | 65536 cycles | 16384 cycles | 16384 cycles |
| • Hardware wait time (number of cycles) when hold mode is cleared | About 64 ms at 4 MHz (T _{cyc} = 1 μs) | About 16 ms at 4 MHz (T _{cyc} = 1 μs) | About 16 ms at 4 MHz (T _{cyc} = 1 μs) |
| • Value of timer 0 after a reset (Including the value after hold mode is cleared) | Set to FF0. | Set to FFC. | Set to FFC. |
| • Inverter array | None (Tools are handled with external devices.) | None | Yes |
| • Buffer array (data shaper circuit) | None (Tools are handled with external devices.) | None | Yes |
| • Sub-oscillator | None | None | Yes (option) |
| • Three-value inputs/comparator inputs | Yes | Yes | Only a 16-value comparator |
| • Three-state output from P31 and P32 | None | None | Yes |
| • Using P0 to clear halt mode | In 4-bit groups | In 4-bit groups | Can be specified for each bit. |
| • External extended interrupts | None for INT3, INT4, and INT5. (Tools are handled with external devices.) | None for INT3, INT4, and INT5. | None for INT3, INT4, and INT5. |
| • Other P53 functions | Shared with INT2 (Tools are handled with external devices.) | Shared with INT2 | Shared with INT2 (The logic is inverted.) |
| Differences in main characteristics | • LC66304A/306A/308A 4.0 to 6.0 V/0.92 to 10 μs | • 3.0 to 5.5 V/0.92 to 10 μs | • 3.0 to 5.5 V/0.95 to 10 μs (When the main oscillator is operating) |
| • Operating power-supply voltage and operating speed (cycle time) | • LC66E308/P308 4.5 to 5.5 V/0.92 to 10 μs | • LC6635XA 2.2 to 5.5 V/3.92 to 10 μs 3.0 to 5.5 V/1.96 to 10 μs | • 3.0 to 5.5 V/25 to 127 μs (When the sub-oscillator is operating) |
| • Pull-up resistors | P0, P1, P4, and P5: about 3 to 10 k | P0, P1, P4, and P5: about 3 to 10 k | P0, P1, P4, and P5: about 100 k |
| • Port voltage handling | • P2 to P6 and PC: 15-V handling • P0, P1, PD, PE: Normal voltage handling | • P2 to P6 and PC: 15-V handling • P0, P1, PD, PE: Normal voltage handling | All ports: normal voltage handling (7-V handling provided) |

For other differences and details, see the data sheets for the individual products.

Pin Function Overview

| Pin | I/O | Overview | Output driver type | Options | State after a reset | Standby mode operation |
|--|-----|--|--|---|--------------------------------------|--|
| P00 P01 P02 P03 | I/O | I/O ports P00 to P03 <ul style="list-style-type: none"> Input or output in 4-bit or 1-bit units P00 to P03 support the halt mode control function (This function can be specified in bit units.) | <ul style="list-style-type: none"> Pch: Pull-up MOS type Nch: Intermediate sink current type | <ul style="list-style-type: none"> Pull-up MOS or Nch OD output Output level on reset | High or low (option) | Hold mode: Output off ----- Halt mode: Output retained |
| P10 P11 P12 P13 | I/O | I/O ports P10 to P13 Input or output in 4-bit or 1-bit units | <ul style="list-style-type: none"> Pch: Pull-up MOS type Nch: Intermediate sink current type | <ul style="list-style-type: none"> Pull-up MOS or Nch OD output Output level on reset | High or low (option) | Hold mode: Output off ----- Halt mode: Output retained |
| P20/SI0 P21/SO0 P22/SCK0 P23/INT0 | I/O | I/O ports P20 to P23 <ul style="list-style-type: none"> Input or output in 4-bit or 1-bit units P20 is also used as the serial input SI0 pin. P21 is also used as the serial output SO0 pin. P22 is also used as the serial clock SCK0 pin. P23 is also used as the INT0 interrupt request pin, and also as the timer 0 event counting and pulse width measurement input. | <ul style="list-style-type: none"> Pch: CMOS type Nch: Intermediate sink current type Nch: +7-V handling when OD option selected | CMOS or Nch OD output | H | Hold mode: Output off ----- Halt mode: Output retained |
| P30/INT1 P31/POUT0 P32/POUT1 | I/O | I/O ports P30 to P32 <ul style="list-style-type: none"> Input or output in 3-bit or 1-bit units P30 is also used as the INT1 interrupt request. P31 is also used for the square wave output from timer 0. P32 is also used for the square wave and PWM output from timer 1. P31 and P32 also support 3-state outputs. | <ul style="list-style-type: none"> Pch: CMOS type Nch: Intermediate sink current type Nch: +7-V handling when OD option selected | CMOS or Nch OD output | H | Hold mode: Output off ----- Halt mode: Output retained |
| P33/HOLD | I | Hold mode control input <ul style="list-style-type: none"> Hold mode is set up by the HOLD instruction when HOLD is low. In hold mode, the CPU is restarted by setting HOLD to the high level. This pin can be used as input port P33 along with P30 to P32. When the P33/HOLD pin is at the low level, the CPU will not be reset by a low level on the RES pin. Therefore, applications must not set P33/HOLD low when power is first applied. | | | | |
| P40/INV0I P41/INV0O P42/INV1I P43/INV1O | I/O | I/O ports P40 to P43 <ul style="list-style-type: none"> Input or output in 4-bit or 1-bit units Input or output in 8-bit units when used in conjunction with P50 to P53. Can be used for output of 8-bit ROM data when used in conjunction with P50 to P53. Dedicated inverter circuit (option) | <ul style="list-style-type: none"> Pch: Pull-up MOS type CMOS type when the inverter circuit option is selected Nch: Intermediate sink current type | <ul style="list-style-type: none"> Pull-up MOS or Nch OD output Output level on reset Inverter circuit | High or low or inverter I/O (option) | Hold mode: Port output off, inverter output off ----- Halt mode: Port output retained, inverter output continues |

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| Pin | I/O | Overview | Output driver type | Options | State after a reset | Standby mode operation |
|---|-----|---|---|--|---------------------------------------|--|
| P50 P51 P52 P53/INT2 | I/O | I/O ports P50 to P53 <ul style="list-style-type: none"> Input or output in 4-bit or 1-bit units Input or output in 8-bit units when used in conjunction with P40 to P43. Can be used for output of 8-bit ROM data when used in conjunction with P40 to P43. P53 is also used as the INT2 interrupt request. | <ul style="list-style-type: none"> Pch: Pull-up MOS type Nch: Intermediate sink current type | <ul style="list-style-type: none"> Pull-up MOS or Nch OD output Output level on reset | High or low (option) | Hold mode: Output off ----- Halt mode: Output retained |
| P60/SI1 P61/SO1 P62/SCK1 P63/PIN1 | I/O | I/O ports P60 to P63 <ul style="list-style-type: none"> Input or output in 4-bit or 1-bit units P60 is also used as the serial input SI1 pin. P61 is also used as the serial output SO1 pin. P62 is also used as the serial clock SCK1 pin. P63 is also used for the event count input to timer 1. | <ul style="list-style-type: none"> Pch: MOS type Nch: Intermediate sink current type Nch: +7-V handling when OD option selected (P61 and P63 only) | <ul style="list-style-type: none"> CMOS or Nch OD output | H | Hold mode: Output off ----- Halt mode: Output retained |
| P80/DS0 P81/DS1 P82 P83 | O | Dedicated output ports P80 to P83 <ul style="list-style-type: none"> Output in 4-bit or 1-bit units The contents of the output latch are input using input instructions. P80 is a buffer input or a zero-cross buffer input and P81 is a buffer input (options). | <ul style="list-style-type: none"> Pch: CMOS type Nch: Intermediate sink current type | <ul style="list-style-type: none"> CMOS or Pch OD output Output level at reset Buffer circuit Zero-cross detector buffer circuit | High or low Buffered I/O (option) | Hold mode: Port output off, buffer output off ----- Halt mode: Port output retained, buffer output continues with the buffer resistor off. |
| PC0 PC1 PC2/INV2I PC3/INV2O | I/O | I/O ports PC0 to PC3 <ul style="list-style-type: none"> Output in 4-bit or 1-bit units Dedicated inverter circuits (option) | <ul style="list-style-type: none"> Pch: CMOS type Nch: Intermediate sink current type | <ul style="list-style-type: none"> CMOS or Nch OD output Inverter circuit | H | Hold mode: Port output off, inverter output off ----- Halt mode: Port output retained, inverter output continues. |
| PD0/AN1/ INV3I PD1/AN2/ INV3O PD2/AN3 INV4I PD3/AN4/ INV4O | I | Dedicated input ports PD0 to PD3 <ul style="list-style-type: none"> Can be switched in software to function as 16-value analog inputs. Dedicated inverter circuits (option) | <ul style="list-style-type: none"> Inverter circuits can be selected as options. Pch: CMOS type Nch: Intermediate sink current type | Inverter circuit | Normal input or inverter I/O (option) | Inverter: <ul style="list-style-type: none"> Hold mode: Output off Halt mode: Output continues |
| PE0/XT1 PE1/XT2 | I | Dedicated input ports and sub-oscillator connections | | Sub-oscillator/port PE selection | Selected as an option | Sub-oscillator: Hold mode: Oscillator stopped ----- Halt mode: Oscillator operates |

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| Pin | I/O | Overview | Output driver type | Options | State after a reset | Standby mode operation |
|-------------------------|--------|--|--------------------|--|-----------------------|---|
| OSC1 OSC2 | I O | System clock oscillator connections When an external clock is used, leave OSC2 open and connect the clock signal to OSC1. | | Ceramic oscillator or external clock selection | Selected as an option | Hold mode: Oscillator stopped Halt mode: Oscillator operates |
| $\overline{\text{RES}}$ | I | System reset input When the P33/HOLD pin is at the high level, a low level input to the RES pin will initialize the CPU. | | | | |
| TEST | I | CPU test pin This pin must be connected to V_{SS} during normal operation. | | | | |
| V_{DD} V_{SS} | | Power supply pins | | | | |

Note: Pull-up MOS type: The output circuit includes a MOS transistor that pulls the pin up to V_{DD} .
CMOS output: Complementary output.
OD output: Open-drain output.

User Options

1. Port 0, 1, 4, 5, and 8 output level at reset option

The output levels at reset for I/O ports 0, 1, 4, 5, and 8, in independent 4-bit groups, can be selected from the following two options.

| Option | Conditions and notes |
|-------------------------|--|
| 1. Output high at reset | The four bits of ports 0, 1, 4, 5, or 8 are set in a group |
| 2. Output low at reset | The four bits of ports 0, 1, 4, 5, or 8 are set in a group |

2. Oscillator circuit options

• Main clock

| Option | Circuit | Conditions and notes |
|-----------------------|---------|---------------------------------------|
| 1. External clock | | The input has Schmitt characteristics |
| 2. Ceramic oscillator | | |

Note: There is no RC oscillator option.

• Sub-clock

| Option | Circuit | Conditions and notes |
|---------------------------------------|---------|----------------------|
| 1. Ports PE0 and PE1 | | |
| 2 Sub-oscillator (crystal oscillator) | | |

3. Watchdog timer option

A runaway detection function (watchdog timer) can be selected as an option.

4. Port output type options

- The output type of each bit (pin) in ports P0, P1, P2, P3 (except for the P33/ $\overline{\text{HOLD}}$ pin), P4, P5, P6, and PC can be selected individually from the following two options.

| Option | Circuit | Conditions and notes |
|--|---------|--|
| 1. Open-drain output | | The port P2, P3, P5, and P6 inputs have Schmitt characteristics. |
| 2. Output with built-in pull-up resistor | | <p>The port P2, P3, P5, and P6 inputs have Schmitt characteristics.</p> <p>The CMOS outputs (ports P2, P3, P6, and PC) and the pull-up MOS outputs (P0, P1, P4, and P5) are distinguished by the drive capacity of the p-channel transistor.</p> |

- One of the following two options can be selected for P8, in bit units.

| Option | Circuit | Conditions and notes |
|--|---------|----------------------|
| 1. Open-drain output | | |
| 2. Output with built-in pull-down resistor (CMOS output) | | |

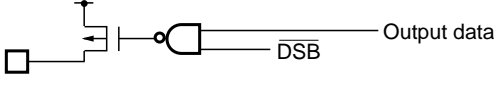
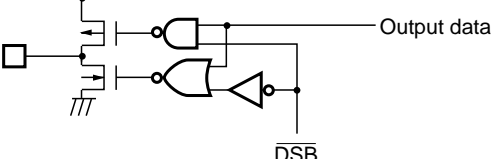
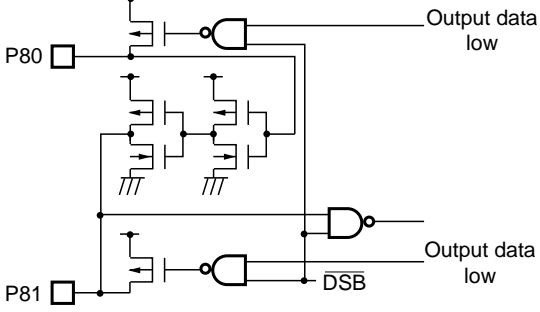
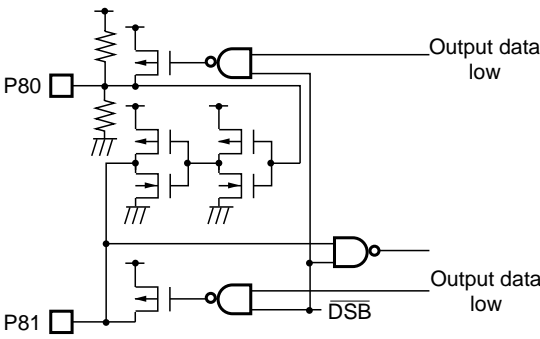
5. Inverter array circuit option

One of the following options can be selected for each of the following port sets: P40/P41, P42/P43, PC2/PC3, PD0/PD1, and PD2/PD3. (PDs do not use option 1 because they are dedicated to inputs)

| Option | Circuit | Conditions and notes |
|----------------------------|---------|--|
| 1. Normal port I/O circuit | | <p>When the open-drain output type is selected</p> |
| | | <p>When the built-in pull-up resistor output type is selected The CMOS outputs (PC) and the pull-up MOS outputs (P4) are distinguished by the drive capacity of the p-channel transistor.</p> |
| 2. Inverter I/O circuit | | <p>If this option is selected, The I/O circuit is disabled by the \overline{DSB} signal. Also note that the open-drain port output type option and the high level at reset option must be selected.</p> |

6. Buffer array circuit option

In addition to normal port output, one of the following two options may also be selected for P80 and P81.

| Option | Circuit | Conditions and notes |
|---|---|--|
| <p>1. Normal port output</p> |  | <p>When the open-drain output type is selected</p> |
| |  | <p>When the built-in pull-down resistor output type is selected (CMOS output)</p> |
| <p>2. Buffer input (P80) and buffer output (P81) circuits</p> |  | <p>If this option is selected, the I/O circuit is disabled by the \overline{DSB} signal. Also note that the open-drain port output type option and the high level at reset option must be selected.</p> |
| <p>3. Buffer input (P80) and buffer output (P81) circuits with built-in zero-cross detection circuits</p> |  | <p>If this option is selected, the I/O circuit is disabled by the \overline{DSB} signal. Also note that the open-drain port output type option and the high level at reset option must be selected.</p> |

LC665316 Series Option Data Area and Definitions

| ROM area | Bit | Option specified | | Option/data relationship | |
|----------|-----|-----------------------|-----------------------|-------------------------------|--|
| 3FF0H | 7 | P5 | Output level at reset | 0 = high level, 1 = low level | |
| | 6 | P4 | | | |
| | 5 | Sub-oscillator option | | | 0 = port PE, 1 = crystal oscillator |
| | 4 | Oscillator option | | | 0 = external clock, 1 = ceramic oscillator |
| | 3 | P8 | Output level at reset | | 0 = low level, 1 = high level |
| | 2 | P1 | | | |
| | 1 | P0 | | | |
| | 0 | Watchdog timer option | | | |
| 3FF1H | 7 | P13 | Output type | 0 = OD, 1 = PU | |
| | 6 | P12 | | | |
| | 5 | P11 | | | |
| | 4 | P10 | | | |
| | 3 | P03 | Output type | | 0 = OD, 1 = PU |
| | 2 | P02 | | | |
| | 1 | P01 | | | |
| | 0 | P00 | | | |
| 3FF2H | 7 | Unused | | This bit must be set to 0. | |
| | 6 | P32 | Output type | 0 = OD, 1 = PU | |
| | 5 | P31 | | | |
| | 4 | P30 | | | |
| | 3 | P23 | | | |
| | 2 | P22 | Output type | | 0 = OD, 1 = PU |
| | 1 | P21 | | | |
| | 0 | P20 | | | |
| 3FF3H | 7 | P53 | | | |
| | 6 | P52 | | | |
| | 5 | P51 | | | |
| | 4 | P50 | | | |
| | 3 | P43 | Output type | 0 = OD, 1 = PU | |
| | 2 | P42 | | | |
| | 1 | P41 | | | |
| | 0 | P40 | | | |
| 3FF4H | 7 | Unused | | This bit must be set to 0. | |
| | 6 | Unused | | 0 = OD, 1 = PU | |
| | 5 | Unused | | | |
| | 4 | Unused | | | |
| | 3 | P63 | Output type | | |
| | 2 | P62 | | | |
| | 1 | P61 | | | |
| | 0 | P60 | | | |
| 3FF5H | 7 | Unused | | | This bit must be set to 0. |
| | 6 | Unused | | 0 = OD, 1 = PD | |
| | 5 | Unused | | | |
| | 4 | Unused | | | |
| | 3 | P83 | Output type | | |
| | 2 | P82 | | | |
| | 1 | P81 | | | |
| | 0 | P80 | | | |
| 3FF6H | 7 | Unused | | | This bit must be set to 0. |
| | 6 | Unused | | This bit must be set to 0. | |
| | 5 | Unused | | | |
| | 4 | Unused | | | |
| | 3 | Unused | | | |
| | 2 | Unused | | | |
| | 1 | Unused | | | |
| | 0 | Unused | | | |

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| ROM area | Bit | Option specified | | Option/data relationship |
|----------|-----|--|-----------------|--|
| 3FF7H | 7 | Unused | | This bit must be set to 0. |
| | 6 | | | |
| | 5 | | | |
| | 4 | | | |
| | 3 | PC3 | Output type | 0 = OD, 1 = PU |
| | 2 | PC2 | | |
| | 1 | PC1 | | |
| | 0 | PC0 | | |
| 3FF8H | 7 | Unused | | This bit must be set to 1. |
| | 6 | Buffer output | | 0 = used, 1 = none |
| | 5 | Buffer output with zero-cross bias input | | 0 = used, 1 = none |
| | 4 | PD3 | Inverter output | 0 = inverter output, 1 = none |
| | 3 | PD1 | | |
| | 2 | PC3 | | |
| | 1 | P43 | | |
| | 0 | P41 | | |
| 3FF9H | 7 | Unused | | This bit must be set to 0. |
| | 6 | | | |
| | 5 | | | |
| | 4 | | | |
| | 3 | Unused | | This bit must be set to 0. |
| | 2 | | | |
| | 1 | | | |
| | 0 | | | |
| 3FFAH | 7 | Unused | | This bit must be set to 0. |
| | 6 | | | |
| | 5 | | | |
| | 4 | | | |
| | 3 | Unused | | This bit must be set to 0. |
| | 2 | | | |
| | 1 | | | |
| | 0 | | | |
| 3FFBH | 7 | Unused | | This bit must be set to 0. |
| | 6 | | | |
| | 5 | | | |
| | 4 | | | |
| | 3 | Unused | | This bit must be set to 0. |
| | 2 | | | |
| | 1 | | | |
| | 0 | | | |
| 3FFCH | 7 | Unused | | This bit must be set to 0. |
| | 6 | | | |
| | 5 | | | |
| | 4 | | | |
| | 3 | Unused | | This bit must be set to 0. |
| | 2 | | | |
| | 1 | | | |
| | 0 | | | |
| 3FFDH | 7 | Reserved. Must be set to predefined data values. | | This data is generated by the assembler. If the assembler is not used, set this data to '00'. |
| | 6 | | | |
| | 5 | | | |
| | 4 | | | |
| | 3 | | | |
| | 2 | | | |
| | 1 | | | |
| | 0 | | | |

Continued on next page.

Continued from preceding page.

| ROM area | Bit | Option specified | Option/data relationship |
|-------------------|-----|--|--|
| 3FFE _H | 7 | Reserved. Must be set to predefined data values. | This data is generated by the assembler. If the assembler is not used, set this data to '00'. |
| | 6 | | |
| | 5 | | |
| | 4 | | |
| | 3 | | |
| | 2 | | |
| | 1 | | |
| | 0 | | |
| 3FFF _H | 7 | Reserved. Must be set to predefined data values. | This data is generated by the assembler. If the assembler is not used, set this data to '00'. |
| | 6 | | |
| | 5 | | |
| | 4 | | |
| | 3 | | |
| | 2 | | |
| | 1 | | |
| | 0 | | |

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit | Note |
|-----------------------------|---------------------|--|-------------------------------|------|------|
| Maximum supply voltage | V _{DD max} | V _{DD} | -0.3 to +7.0 | V | |
| Input voltage | V _{IN1} | P2, P3 (except for the P33/HOLD pin), P61, and P63 | -0.3 to +7.0 | V | 1 |
| | V _{IN2} | All other inputs | -0.3 to V _{DD} + 0.3 | V | 2 |
| Output voltage | V _{OUT1} | P2, P3 (except for the P33/HOLD pin), P61, and P63 | -0.3 to +7.0 | V | 1 |
| | V _{OUT2} | All other inputs | -0.3 to V _{DD} + 0.3 | V | 2 |
| Output current per pin | I _{ON1} | P0, P1, P2, P3 (except for the P33/HOLD pin), P4, P5, P6, P8, PC, PD1, PD3 | 20 | mA | 3 |
| | -I _{OP1} | P0, P1, P4, P5 | 2 | mA | 4 |
| | -I _{OP2} | P2, P3 (except for the P33/HOLD pin), P6, P8, and PC | 4 | mA | 4 |
| | -I _{OP3} | P41, P43, PC3, PD1, PD3, P81 | 10 | mA | 4 |
| Total pin current | Σ I _{ON1} | P4, P5, P6, P8, PC | 75 | mA | 3 |
| | Σ I _{ON2} | P0, P1, P2, P3 (except for the P33/HOLD pin), PD1, PD3 | 75 | mA | 3 |
| | Σ I _{OP1} | P4, P5, P6, P8, PC | 25 | mA | 4 |
| | Σ I _{OP2} | P0, P1, P2, P3 (except for the P33/HOLD pin), PD1, PD3 | 25 | mA | 4 |
| Allowable power dissipation | Pd max | Ta = -30 to +70°C: DIP48S (QFP48E) | 600 (430) | mW | 5 |
| Operating temperature | Topr | | -30 to +70 | °C | |
| Storage temperature | Tstg | | -55 to +125 | °C | |

- Note: 1. Applies to pins with open-drain output specifications. For pins with other than open-drain output specifications, the ratings in the pin column for that pin apply.
2. For the oscillator input and output pins, levels up to the free-running oscillation level are allowed.
3. Sink current (Applies to P8 and PD when either the CMOS output specifications or the inverter array specifications have been selected.)
4. Source current (Applies to all pins except P8 and PD for which the pull-up output specifications, the CMOS output specifications, or the inverter array specifications have been selected. Applies to PD pins for which the inverter array specifications have been selected.) Contact your Sanyo representative for the electrical characteristics when the inverter array or buffer array options are specified.
5. We recommend the use of reflow-soldering techniques to solder-mount QFP packages.
Please consult with your Sanyo representative for details on process conditions if the package itself is to be directly immersed in a dip-soldering bath (dip-soldering spray techniques).

Allowable Operating Ranges at Ta = -30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V, unless otherwise specified.

| Parameter | Symbol | Conditions | min | typ | max | Unit | Note |
|---|--|--|---------------------|-----------------|---------------------|-------------------|------|
| Operating supply voltage | V _{DD} | V _{DD} | 3.0 | | 5.5 | V | |
| Memory retention supply voltage | V _{DDH} | V _{DD} : During hold mode | 1.8 | | 5.5 | V | |
| Input high-level voltage | V _{IH1} | P2, P3 (except for the P33/ $\overline{\text{HOLD}}$ pin), P61, and P63: N-channel output transistor off | 0.8 V _{DD} | | +7.0 | V | 1 |
| | V _{IH2} | P33/ $\overline{\text{HOLD}}$, P60, P62, $\overline{\text{RES}}$, OSC1: N-channel output transistor off | 0.8 V _{DD} | | V _{DD} | V | 1 |
| | V _{IH3} | P0, P1, P4, P5, PC, PD, PE: N-channel output transistor off | 0.8 V _{DD} | | V _{DD} | V | 2 |
| Input low-level voltage | V _{IL1} | P2, P3 (except for the P33/ $\overline{\text{HOLD}}$ pin), P6, $\overline{\text{RES}}$, and OSC1: N-channel output transistor off | V _{SS} | | 0.2 V _{DD} | V | 3 |
| | V _{IL2} | P0, P1, P4, P5, PC, PD, PE, TEST: N-channel output transistor off | V _{SS} | | 0.2 V _{DD} | V | 2 |
| | V _{IL3} | P33/ $\overline{\text{HOLD}}$: V _{DD} = 1.8 to 5.5 V | V _{SS} | | 0.2 V _{DD} | V | |
| Operating frequency (instruction cycle time) | f _{op} (T _{Cyc}) | When the main oscillator is operating | 0.4 (10) | | 4.20 (0.95) | MHz (μ s) | |
| | | When the sub-oscillator is operating | 30 (133) | 32.768 (122) | 100 (25) | kHz (μ s) | |
| [External clock input conditions] | | | | | | | |
| Frequency | f _{ext} | OSC1: Defined by Figure 1. Input the clock signal to OSC1 and leave OSC2 open. (External clock input must be selected as the oscillator circuit option.) | 0.4 | | 4.20 | MHz | |
| Pulse width | t _{extH} , t _{extL} | OSC1: Defined by Figure 1. Input the clock signal to OSC1 and leave OSC2 open. (External clock input must be selected as the oscillator circuit option.) | 100 | | | ns | |
| Rise and fall times | t _{extR} , t _{extF} | OSC1: Defined by Figure 1. Input the clock signal to OSC1 and leave OSC2 open. (External clock input must be selected as the oscillator circuit option.) | | | 30 | ns | |

- Note: 1. Applies to pins with open-drain specifications. However, V_{IH2} applies to the P33/ $\overline{\text{HOLD}}$ pin. When ports P2, P3, and P6 have CMOS output specifications they cannot be used as input pins.
2. PC port pins with CMOS output specifications cannot be used as input pins. Contact your Sanyo representative for the allowable operating ranges for P4, PC, and PD when the inverter array is used, and for P8 when the buffer array is used.
3. Applies to pins with open-drain specifications. However, V_{IL3} applies to the P33/ $\overline{\text{HOLD}}$ pin. P2, P3, and P6 port pins with CMOS output specifications cannot be used as input pins.

Electrical Characteristics at Ta = -30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V unless otherwise specified.

| Parameter | Symbol | Conditions | min | typ | max | Unit | Note |
|---------------------------------------|-------------------|--|-------------------------------------|---------------------|---------------------|------|------|
| Input high-level current | I _{IH1} | P2, P3 (except for the P33/HOLD pin), P61, and P63: V _{IN} = +7 V, with the output Nch transistor off | | | 5.0 | μA | 1 |
| | I _{IH2} | P0, P1, P4, P5, P6, PC, OSC1, $\overline{\text{RES}}$, and P33/HOLD (Does not apply to PD, PE, PC2, PC3, P61, and P63.): V _{IN} = V _{DD} , with the output Nch transistor off | | | 1.0 | μA | 1 |
| | I _{IH3} | PD, PE, PC2, PC3: V _{IN} = V _{DD} , with the output Nch transistor off | | | 1.0 | μA | 1 |
| Input low-level current | I _{IL1} | Input ports other than PD, PE, PC2, and PC3: V _{IN} = V _{SS} , with the output Nch transistor off | -1.0 | | | μA | 2 |
| | I _{IL2} | PC2, PC3, PD, PE0: V _{IN} = V _{SS} , with the output Nch transistor off | -1.0 | | | μA | 2 |
| | I _{IL4} | PE1 (When used as a port; does not apply when the sub-oscillator option is selected.): V _{IN} = V _{SS} | | 20 | | μA | 1 |
| Output high-level voltage | V _{OH1} | P2, P3 (except for the P33/HOLD pin), P6, P8, and PC: I _{OH} = -1 mA | V _{DD} - 1.0 | | | V | 3 |
| | | P2, P3 (except for the P33/HOLD pin), P6, P8, and PC: I _{OH} = -0.1 mA | V _{DD} - 0.5 | | | | |
| Value of the output pull-up resistor | R _{PO} | P0, P1, P4, P5 | 30 | 100 | 150 | k | 4 |
| Output low-level voltage | V _{OL1} | P0, P1, P2, P3, P4, P5, P6, P8, and PC (except for the P33/HOLD pin): I _{OL} = 1.6 mA | | | 0.4 | V | 5 |
| | V _{OL2} | P0, P1, P2, P3, P4, P5, P6, P8, and PC (except for the P33/HOLD pin): I _{OL} = 8 mA | | | 1.5 | V | |
| Output off leakage current | I _{OFF1} | P2, P3, P61, P63: V _{IN} = +7 V | | | 5.0 | μA | 6 |
| | I _{OFF2} | Does not apply to P2, P3, P61, P63, and P8.: V _{IN} = V _{DD} | | | 1.0 | μA | 6 |
| | I _{OFF3} | P8: V _{IN} = V _{SS} | -1.0 | | | μA | 7 |
| [Schmitt characteristics] | | | | | | | |
| Hysteresis voltage | V _{HYS} | | | 0.1 V _{DD} | | V | |
| High-level threshold voltage | V _{tH} | P2, P3, P5, P6, OSC1 (EXT), $\overline{\text{RES}}$ | 0.5 V _{DD} | | 0.8 V _{DD} | V | |
| Low-level threshold voltage | V _{tL} | | 0.2 V _{DD} | | 0.5 V _{DD} | V | |
| [Ceramic oscillator] | | | | | | | |
| Oscillator frequency | f _{CF} | OSC1, OSC2: Figure 2, 4 MHz | | 4.0 | | MHz | |
| Oscillator stabilization time | f _{CFS} | Figure 3, 4 MHz | | | 10.0 | ms | |
| [Crystal oscillator] | | | | | | | |
| Oscillator frequency | f _{XT} | XT1, XT2: Figure 2, when the sub-oscillator option is selected, 32 kHz | | 32.768 | | kHz | |
| Oscillator stabilization time | f _{XTS} | Figure 3, when the sub-oscillator option is selected, 32 kHz | | 1.0 | 5.0 | s | |
| [Serial clock] | | | | | | | |
| Cycle time | Input | SCK0, SCK1: With the timing of Figure 4 and the test load of Figure 5. | t _{CKCY} | 0.9 | | | μs |
| | Output | | | 2.0 | | | Tcyc |
| Low-level and high-level pulse widths | Input | | t _{CKL} | 0.4 | | | μs |
| | Output | | t _{CKH} | 1.0 | | | Tcyc |
| Rise and fall times | Output | | t _{CKR} , t _{CKF} | | | 0.1 | μs |
| [Serial input] | | | | | | | |
| Data setup time | t _{ICK} | S10, S11: With the timing of Figure 4. Stipulated with respect to the rising edge (↑) of SCK0 or SCK1. | 0.3 | | | μs | |
| Data hold time | t _{CKI} | | 0.3 | | | μs | |
| [Serial output] | | | | | | | |
| Output delay time | t _{CKO} | SO0, SO1: With the timing of Figure 5 and the test load of Figure 5. Stipulated with respect to the falling edge (↓) of SCK0 or SCK1. | | | 0.3 | μs | |

Continued on next page.

Continued from preceding page.

| Parameter | Symbol | Conditions | min | typ | max | Unit | Note |
|--|----------------------|--|-----|------|-----|---------|------|
| [Pulse conditions] | | | | | | | |
| INT0 high and low-level | t_{IOH}, t_{IOL} | INT0: Figure 6, conditions under which the INT0 interrupt can be accepted, conditions under which the timer 0 event counter or pulse width measurement input can be accepted | 2 | | | Tcyc | |
| High and low-level pulse widths for interrupt inputs other than INT0 | t_{IIH}, t_{IIL} | INT1: Figure 6, conditions under which the corresponding interrupt can be accepted | 2 | | | Tcyc | |
| PIN1 high and low-level pulse widths | t_{PINH}, t_{PINL} | PIN1: Figure 6, conditions under which the timer 1 event counter input can be accepted | 2 | | | Tcyc | |
| RES high and low-level pulse widths | t_{RSH}, t_{RSL} | RES: Figure 6, conditions under which reset can be applied. | 3 | | | Tcyc | |
| Operating current drain | I_{DDOP} | V_{DD} : 4-MHz ceramic oscillator | | 4.0 | 8.0 | mA | 8 |
| | | V_{DD} : 4-MHz ceramic oscillator, $V_{DD} = 3.0$ to 4.0 V | | 3.0 | 5.0 | | |
| | | V_{DD} : 4-MHz external clock | | 4.0 | 8.0 | mA | |
| Halt mode current drain | I_{DDHALT} | V_{DD} : 4-MHz ceramic oscillator | | 2.0 | 3.5 | mA | |
| | | V_{DD} : 4-MHz ceramic oscillator, $V_{DD} = 3.0$ to 4.0 V | | 1.0 | 2.0 | | |
| | | V_{DD} : 4-MHz external clock | | 2.0 | 3.5 | | |
| | | V_{DD} : 32 kHz (main oscillator stopped), sub-oscillator: crystal | | 10 | 100 | μ A | |
| | | V_{DD} : 32 kHz (main oscillator stopped), sub-oscillator: crystal, $V_{DD} = 3.0$ to 4.0 V | | 10 | 50 | | |
| Hold mode current drain | I_{DDHOLD} | V_{DD} : $V_{DD} = 1.8$ to 5.5 V | | 0.01 | 10 | μ A | |

- Note: 1. With the output Nch transistor off in shared I/O ports with the open-drain output specifications. These pins cannot be used as input pins if the CMOS output specifications are selected. When the port option is selected for PE.
 2. With the output Nch transistor off in shared I/O ports with the open-drain output specifications. The rating for the pull-up output specification pins is stipulated in terms of the output pull-up current IPO. These pins cannot be used as input pins if the CMOS output specifications are selected.
 3. With the output Nch transistor off for CMOS output specification pins. (Also applies when the Pch open-drain option is selected for P8.)
 4. With the output Nch transistor off for pull-up output specification pins.
 5. When CMOS output specifications are selected for P8.
 6. With the output Nch transistor off for open-drain output specification pins.
 7. With the output Pch transistor off for open-drain output specification pins.
 8. Reset state

Comparator Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0$ V

| Parameter | Symbol | Conditions | min | typ | max | Unit | Note |
|--------------------|------------|---------------------------------------|----------|-----------|----------|---------|------|
| Absolute precision | V_{CECM} | AN1 to AN4: $V_{DD} = 3.0$ to 5.5 V | | $\pm 1/2$ | ± 1 | LSB | 1 |
| Threshold voltage | V_{THCM} | $V_{DD} = 3.0$ to 5.5 V | V_{SS} | | V_{DD} | V | |
| Input voltage | V_{INCM} | AN1 to AN4: $V_{DD} = 3.0$ to 5.5 V | V_{SS} | | V_{DD} | V | |
| Conversion time | T_{CCM} | $V_{DD} = 3.0$ to 5.5 V | | | 20 | ms | |
| | | $V_{DD} = 4.0$ to 5.5 V | | | 30 | μ s | |

Note: 1. Does not include the quantization error.

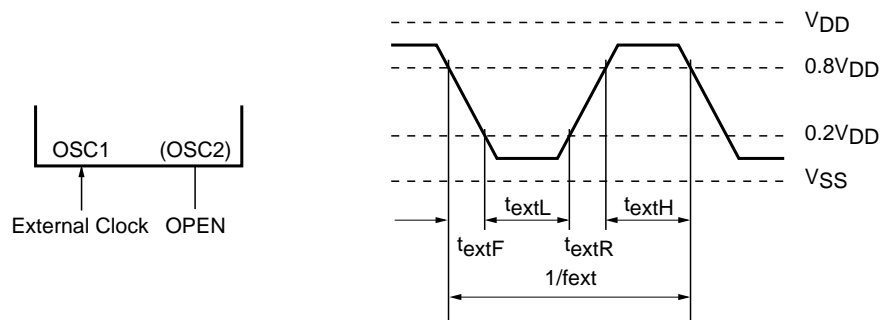


Figure 1 External Clock Input Waveform

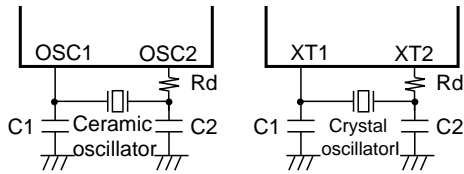


Figure 2 Ceramic Oscillator Circuit

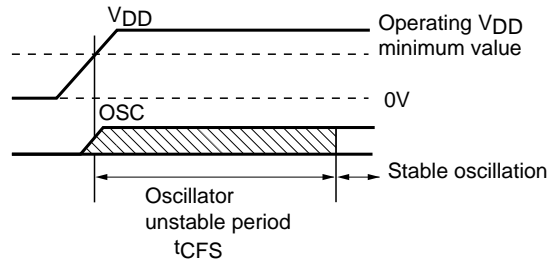


Figure 3 Oscillator Stabilization Period

Table 1 Guaranteed Ceramic Oscillator Constants External capacitor type

| External capacitor type | | Built-in capacitor type | |
|---|------------------|---|---------------|
| 4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MG | C1 = 33 pF ± 10% | 4 MHz (Murata Mfg Co., Ltd) CST4.00MG | Rd = 220 ± 5% |
| | C2 = 33 pF ± 10% | | |
| | Rd = 220 ± 5% | | |
| 4 MHz (Kyocera Corporation) KBR4.0MS | C1 = 33 pF ± 10% | 4 MHz (Kyocera Corporation) KBR4.0MES | Rd = 0 |
| | C2 = 33 pF ± 10% | | |
| | Rd = 0 | | |

Table 2 Guaranteed Crystal Oscillator Constants

| | |
|------------------------------------|------------------|
| 32 kHz (Seiko Epson) C-002RX | C1 = 18 pF ± 10% |
| | C2 = 18 pF ± 10% |
| | Rd = 470 k ± 5% |

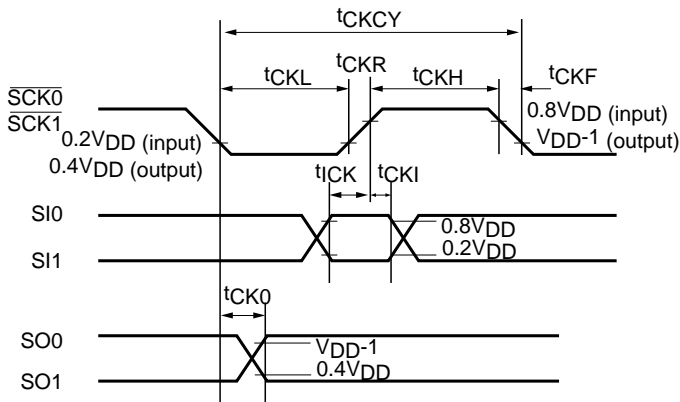


Figure 4 Serial I/O Timing

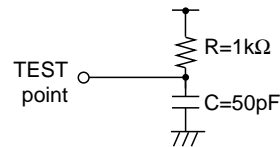


Figure 5 Timing Load

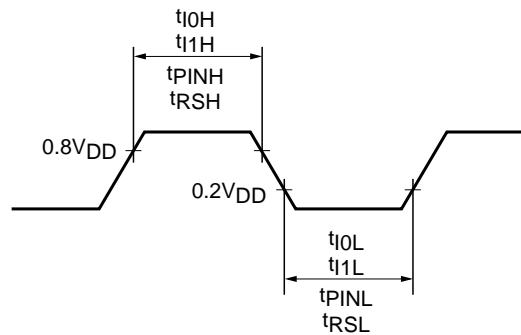


Figure 6 Input Timing for the INT0, INT1, INT2, PIN1, and RES pins

LC66XXXX Series Instruction Table (by function)

Abbreviations:

| | |
|----------|--|
| AC: | Accumulator |
| E: | E register |
| CF: | Carry flag |
| ZF: | Zero flag |
| HL: | Data pointer DPH, DPL |
| XY: | Data pointer DPX, DPY |
| M: | Data memory |
| M (HL): | Data memory pointed to by the DPH, DPL data pointer |
| M (XY): | Data memory pointed to by the DPX, DPY auxiliary data pointer |
| M2 (HL): | Two words of data memory (starting on an even address) pointed to by the DPH, DPL data pointer |
| SP: | Stack pointer |
| M2 (SP): | Two words of data memory pointed to by the stack pointer |
| M4 (SP): | Four words of data memory pointed to by the stack pointer |
| in: | n bits of immediate data |
| t2: | Bit specification |

| | | | | |
|-----|----------------|----------------|----------------|----------------|
| t2 | 11 | 10 | 01 | 00 |
| Bit | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ |

| | |
|-----------|--|
| PCh: | Bits 8 to 11 in the PC |
| PCm: | Bits 4 to 7 in the PC |
| PCl: | Bits 0 to 3 in the PC |
| Fn: | User flag, n = 0 to 15 |
| TIMER0: | Timer 0 |
| TIMER1: | Timer 1 |
| SIO: | Serial register |
| P: | Port |
| P (i4): | Port indicated by 4 bits of immediate data |
| INT: | Interrupt enable flag |
| (), []: | Indicates the contents of a location |
| ←: | Transfer direction, result |
| ∨: | Exclusive or |
| ∧: | Logical and |
| ∨: | Logical or |
| +: | Addition |
| -: | Subtraction |
| —: | Taking the one's complement |

| Mnemonic | Instruction code | | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note | |
|---|---|--|--|------------------|-----------|---|---|--------|--|
| | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | | | | | | | |
| [Accumulator manipulation instructions] | | | | | | | | | |
| CLA | Clear AC | 1 0 0 0 | 0 0 0 0 | 1 | 1 | AC ← 0 (Equivalent to LAI 0.) | Clear AC to 0. | ZF | Has a vertical skip function. |
| DAA | Decimal adjust AC in addition | 1 1 0 0 0 0 1 0 | 1 1 1 1 0 1 1 0 | 2 | 2 | AC ← (AC) + 6 (Equivalent to ADI 6.) | Add six to AC. | ZF | |
| DAS | Decimal adjust AC in subtraction | 1 1 0 0 0 0 1 0 | 1 1 1 1 1 0 1 0 | 2 | 2 | AC ← (AC) + 10 (Equivalent to ADI 0AH.) | Add 10 to AC. | ZF | |
| CLC | Clear CF | 0 0 0 1 | 1 1 1 0 | 1 | 1 | CF ← 0 | Clear CF to 0. | CF | |
| STC | Set CF | 0 0 0 1 | 1 1 1 1 | 1 | 1 | CF ← 1 | Set CF to 1. | CF | |
| CMA | Complement AC | 0 0 0 1 | 1 0 0 0 | 1 | 1 | AC ← $\overline{(AC)}$ | Take the one's complement of AC. | ZF | |
| IA | Increment AC | 0 0 0 1 | 0 1 0 0 | 1 | 1 | AC ← (AC) + 1 | Increment AC. | ZF, CF | |
| DA | Decrement AC | 0 0 1 0 | 0 1 0 0 | 1 | 1 | AC ← (AC) - 1 | Decrement AC. | ZF, CF | |
| RAR | Rotate AC right through CF | 0 0 0 1 | 0 0 0 0 | 1 | 1 | AC ₃ ← (CF), AC _n ← (AC _n + 1), CF ← (AC ₀) | Shift AC (including CF) right. | CF | |
| RAL | Rotate AC left through CF | 0 0 0 0 | 0 0 0 1 | 1 | 1 | AC ₀ ← (CF), AC _n + 1 ← (AC _n), CF ← (AC ₃) | Shift AC (including CF) left. | CF, ZF | |
| TAE | Transfer AC to E | 0 1 0 0 | 0 1 0 1 | 1 | 1 | E ← (AC) | Transfer the contents of AC to E. | | |
| TEA | Transfer E to AC | 0 1 0 0 | 0 1 1 0 | 1 | 1 | AC ← (E) | Transfer the contents of E to AC. | ZF | |
| XAE | Exchange AC with E | 0 1 0 0 | 0 1 0 0 | 1 | 1 | (AC) ↔ (E) | Exchange the contents of AC and E. | | |
| [Memory manipulation instructions] | | | | | | | | | |
| IM | Increment M | 0 0 0 1 | 0 0 1 0 | 1 | 1 | M (HL) ← [M (HL)] + 1 | Increment M (HL). | ZF, CF | |
| DM | Decrement M | 0 0 1 0 | 0 0 1 0 | 1 | 1 | M (HL) ← [M (HL)] - 1 | Decrement M (HL). | ZF, CF | |
| IMDR i8 | Increment M direct | 1 1 0 0 I ₇ I ₆ I ₅ I ₄ | 0 1 1 1 I ₃ I ₂ I ₁ I ₀ | 2 | 2 | M (i8) ← [M (i8)] + 1 | Increment M (i8). | ZF, CF | |
| DMDR i8 | Decrement M direct | 1 1 0 0 I ₇ I ₆ I ₅ I ₄ | 0 0 1 1 I ₃ I ₂ I ₁ I ₀ | 2 | 2 | M (i8) ← [M (i8)] - 1 | Decrement M (i8). | ZF, CF | |
| SMB t2 | Set M data bit | 0 0 0 0 | 1 1 t ₁ t ₀ | 1 | 1 | [M (HL), t2] ← 1 | Set the bit in M (HL) specified by t0 and t1 to 1. | | |
| RMB t2 | Reset M data bit | 0 0 1 0 | 1 1 t ₁ t ₀ | 1 | 1 | [M (HL), t2] ← 0 | Clear the bit in M (HL) specified by t0 and t1 to 0. | ZF | |
| [Arithmetic, logic and comparison instructions] | | | | | | | | | |
| AD | Add M to AC | 0 0 0 0 | 0 1 1 0 | 1 | 1 | AC ← (AC) + [M (HL)] | Add the contents of AC and M (HL) as two's complement values and store the result in AC. | ZF, CF | |
| ADDR i8 | Add M direct to AC | 1 1 0 0 I ₇ I ₆ I ₅ I ₄ | 1 0 0 1 I ₃ I ₂ I ₁ I ₀ | 2 | 2 | AC ← (AC) + [M (i8)] | Add the contents of AC and M (i8) as two's complement values and store the result in AC. | ZF, CF | |
| ADC | Add M to AC with CF | 0 0 0 0 | 0 0 1 0 | 1 | 1 | AC ← (AC) + [M (HL)] + (CF) | Add the contents of AC, M (HL) and C as two's complement values and store the result in AC. | ZF, CF | |
| ADI i4 | Add immediate data to AC | 1 1 0 0 0 0 1 0 | 1 1 1 1 I ₃ I ₂ I ₁ I ₀ | 2 | 2 | AC ← (AC) + I ₃ , I ₂ , I ₁ , I ₀ | Add the contents of AC and the immediate data as two's complement values and store the result in AC. | ZF | |
| SUBC | Subtract AC from M with CF | 0 0 0 1 | 0 1 1 1 | 1 | 1 | AC ← [M (HL)] - (AC) - (CF) | Subtract the contents of AC and CF from M (HL) as two's complement values and store the result in AC. | ZF, CF | CF will be zero if there was a borrow and one otherwise. |
| ANDA | And M with AC then store AC | 0 0 0 0 | 0 1 1 1 | 1 | 1 | AC ← (AC) ∧ [M (HL)] | Take the logical and of AC and M (HL) and store the result in AC. | ZF | |
| ORA | Or M with AC then store AC | 0 0 0 0 | 0 1 0 1 | 1 | 1 | AC ← (AC) ∨ [M (HL)] | Take the logical or of AC and M (HL) and store the result in AC. | ZF | |

Continued from preceding page.

| Mnemonic | Instruction code | | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note | | | | | | | | | | | | | |
|--|---|--|--|------------------|-----------|--|---|----------------------|------------------------------|----|--|----|---|--|---|---|--|---|---|--------|--|
| | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | | | | | | | | | | | | | | | | | | | |
| [Arithmetic, logic and comparison instructions] | | | | | | | | | | | | | | | | | | | | | |
| EXL | Exclusive or M with AC then store AC | 0 0 0 1 | 0 1 0 1 | 1 | 1 | $AC \leftarrow (AC) \nabla [M (HL)]$ | Take the logical exclusive or of AC and M (HL) and store the result in AC. | ZF | | | | | | | | | | | | | |
| ANDM | And M with AC then store M | 0 0 0 0 | 0 0 1 1 | 1 | 1 | $M (HL) \leftarrow (AC) \wedge [M (HL)]$ | Take the logical and of AC and M (HL) and store the result in M (HL). | ZF | | | | | | | | | | | | | |
| ORM | Or M with AC then store M | 0 0 0 0 | 0 1 0 0 | 1 | 1 | $M (HL) \leftarrow (AC) \vee [M (HL)]$ | Take the logical or of AC and M (HL) and store the result in M (HL). | ZF | | | | | | | | | | | | | |
| CM | Compare AC with M | 0 0 0 1 | 0 1 1 0 | 1 | 1 | $\overline{[M (HL)]} + (AC) + 1$ | Compare the contents of AC and M (HL) and set or clear CF and ZF according to the result. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>Magnitude comparison</td> <td>CF</td> <td>ZF</td> </tr> <tr> <td>$[M (HL)] > (AC)$</td> <td>0</td> <td>0</td> </tr> <tr> <td>$[M (HL)] = (AC)$</td> <td>1</td> <td>1</td> </tr> <tr> <td>$[M (HL)] < (AC)$</td> <td>1</td> <td>0</td> </tr> </table> | Magnitude comparison | CF | ZF | $[M (HL)] > (AC)$ | 0 | 0 | $[M (HL)] = (AC)$ | 1 | 1 | $[M (HL)] < (AC)$ | 1 | 0 | ZF, CF | |
| Magnitude comparison | CF | ZF | | | | | | | | | | | | | | | | | | | |
| $[M (HL)] > (AC)$ | 0 | 0 | | | | | | | | | | | | | | | | | | | |
| $[M (HL)] = (AC)$ | 1 | 1 | | | | | | | | | | | | | | | | | | | |
| $[M (HL)] < (AC)$ | 1 | 0 | | | | | | | | | | | | | | | | | | | |
| CI i4 | Compare AC with immediate data | 1 1 0 0 1 0 1 0 | 1 1 1 1 i ₃ i ₂ i ₁ i ₀ | 2 | 2 | $\overline{i_3 i_2 i_1 i_0} + (AC) + 1$ | Compare the contents of AC and the immediate data i ₃ i ₂ i ₁ i ₀ and set or clear CF and ZF according to the result. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>Magnitude comparison</td> <td>CF</td> <td>ZF</td> </tr> <tr> <td>i₃ i₂ i₁ i₀ > AC</td> <td>0</td> <td>0</td> </tr> <tr> <td>i₃ i₂ i₁ i₀ = AC</td> <td>1</td> <td>1</td> </tr> <tr> <td>i₃ i₂ i₁ i₀ < AC</td> <td>1</td> <td>0</td> </tr> </table> | Magnitude comparison | CF | ZF | i ₃ i ₂ i ₁ i ₀ > AC | 0 | 0 | i ₃ i ₂ i ₁ i ₀ = AC | 1 | 1 | i ₃ i ₂ i ₁ i ₀ < AC | 1 | 0 | ZF, CF | |
| Magnitude comparison | CF | ZF | | | | | | | | | | | | | | | | | | | |
| i ₃ i ₂ i ₁ i ₀ > AC | 0 | 0 | | | | | | | | | | | | | | | | | | | |
| i ₃ i ₂ i ₁ i ₀ = AC | 1 | 1 | | | | | | | | | | | | | | | | | | | |
| i ₃ i ₂ i ₁ i ₀ < AC | 1 | 0 | | | | | | | | | | | | | | | | | | | |
| CLI i4 | Compare DP _L with immediate data | 1 1 0 0 1 0 1 1 | 1 1 1 1 i ₃ i ₂ i ₁ i ₀ | 2 | 2 | ZF ← 1 if (DP _L) = i ₃ i ₂ i ₁ i ₀ ZF ← 0 if (DP _L) ≠ i ₃ i ₂ i ₁ i ₀ | Compare the contents of DP _L with the immediate data. Set ZF if identical and clear ZF if not. | ZF | | | | | | | | | | | | | |
| CMB t2 | Compare AC bit with M data bit | 1 1 0 0 1 1 0 1 | 1 1 1 1 0 0 t ₁ t ₀ | 2 | 2 | ZF ← 1 if (AC, t ₂) = [M (HL), t ₂] ZF ← 0 if (AC, t ₂) ≠ [M (HL), t ₂] | Compare the corresponding bits specified by t ₀ and t ₁ in AC and M (HL). Set ZF if identical and clear ZF if not. | ZF | | | | | | | | | | | | | |
| [Load and store instructions] | | | | | | | | | | | | | | | | | | | | | |
| LAE | Load AC and E from M2 (HL) | 0 1 0 1 | 1 1 0 0 | 1 | 1 | $AC \leftarrow M (HL), E \leftarrow M (HL + 1)$ | Load the contents of M2 (HL) into AC, E. | | | | | | | | | | | | | | |
| LAI i4 | Load AC with immediate data | 1 0 0 0 | i ₃ i ₂ i ₁ i ₀ | 1 | 1 | $AC \leftarrow i_3 i_2 i_1 i_0$ | Load the immediate data into AC. | ZF | Has a vertical skip function | | | | | | | | | | | | |
| LADR i8 | Load AC from M direct | 1 1 0 0 i ₇ i ₆ i ₅ i ₄ | 0 0 0 1 i ₃ i ₂ i ₁ i ₀ | 2 | 2 | $AC \leftarrow [M (i8)]$ | Load the contents of M (i8) into AC. | ZF | | | | | | | | | | | | | |
| S | Store AC to M | 0 1 0 0 | 0 1 1 1 | 1 | 1 | $M (HL) \leftarrow (AC)$ | Store the contents of AC into M (HL). | | | | | | | | | | | | | | |
| SAE | Store AC and E to M2 (HL) | 0 1 0 1 | 1 1 1 0 | 1 | 1 | $M (HL) \leftarrow (AC), M (HL + 1) \leftarrow (E)$ | Store the contents of AC, E into M2 (HL). | | | | | | | | | | | | | | |
| LA reg | Load AC from M (reg) | 0 1 0 0 | 1 0 t ₀ 0 | 1 | 1 | $AC \leftarrow [M (reg)]$ | Load the contents of M (reg) into AC. The reg is either HL or XY depending on t ₀ . <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>reg</td> <td>T₀</td> </tr> <tr> <td>HL</td> <td>0</td> </tr> <tr> <td>XY</td> <td>1</td> </tr> </table> | reg | T ₀ | HL | 0 | XY | 1 | ZF | | | | | | | |
| reg | T ₀ | | | | | | | | | | | | | | | | | | | | |
| HL | 0 | | | | | | | | | | | | | | | | | | | | |
| XY | 1 | | | | | | | | | | | | | | | | | | | | |

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Continued from preceding page.

| Mnemonic | | Instruction code | | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note | | | | | | |
|--|---|--|--|-----------------|------------------|--|--|----------------------|--|----|---|----|---|--|--|
| | | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | | | | | | | | | | | | |
| [Load and store instructions] | | | | | | | | | | | | | | | |
| LA reg, I | Load AC from M (reg) then increment reg | 0 1 0 0 | 1 0 t ₀ 1 | 1 | 2 | AC ← [M (reg)] DP _L ← (DP _L) + 1 or DP _Y ← (DP _Y) + 1 | Load the contents of M (reg) into AC. (The reg is either HL or XY.) Then increment the contents of either DP _L or DP _Y . The relationship between t ₀ and reg is the same as that for the LA reg instruction. | ZF | ZF is set according to the result of incrementing DP _L or DP _Y . | | | | | | |
| LA reg, D | Load AC from M (reg) then decrement reg | 0 1 0 1 | 1 0 t ₀ 1 | 1 | 2 | AC ← [M (reg)] DP _L ← (DP _L) - 1 or DP _Y ← (DP _Y) - 1 | Load the contents of M (reg) into AC. (The reg is either HL or XY.) Then decrement the contents of either DP _L or DP _Y . The relationship between t ₀ and reg is the same as that for the LA reg instruction. | ZF | ZF is set according to the result of decrementing DP _L or DP _Y . | | | | | | |
| XA reg | Exchange AC with M (reg) | 0 1 0 0 | 1 1 t ₀ 0 | 1 | 1 | (AC) ↔ [M (reg)] | Exchange the contents of M (reg) and AC. The reg is either HL or XY depending on t ₀ . <table border="1" style="margin-left: 20px;"> <tr> <td>reg</td> <td>T₀</td> </tr> <tr> <td>HL</td> <td>0</td> </tr> <tr> <td>XY</td> <td>1</td> </tr> </table> | reg | T ₀ | HL | 0 | XY | 1 | | |
| reg | T ₀ | | | | | | | | | | | | | | |
| HL | 0 | | | | | | | | | | | | | | |
| XY | 1 | | | | | | | | | | | | | | |
| XA reg, I | Exchange AC with M (reg) then increment reg | 0 1 0 0 | 1 1 t ₀ 1 | 1 | 2 | (AC) ↔ [M (reg)] DP _L ← (DP _L) + 1 or DP _Y ← (DP _Y) + 1 | Exchange the contents of M (reg) and AC. (The reg is either HL or XY.) Then increment the contents of either DP _L or DP _Y . The relationship between t ₀ and reg is the same as that for the XA reg instruction. | ZF | ZF is set according to the result of incrementing DP _L or DP _Y . | | | | | | |
| XA reg, D | Exchange AC with M (reg) then decrement reg | 0 1 0 1 | 1 1 t ₀ 1 | 1 | 2 | (AC) ↔ [M (reg)] DP _L ← (DP _L) - 1 or DP _Y ← (DP _Y) - 1 | Exchange the contents of M (reg) and AC. (The reg is either HL or XY.) Then decrement the contents of either DP _L or DP _Y . The relationship between t ₀ and reg is the same as that for the XA reg instruction. | ZF | ZF is set according to the result of decrementing DP _L or DP _Y . | | | | | | |
| XADR i8 | Exchange AC with M direct | 1 1 0 0 l ₇ l ₆ l ₅ l ₄ | 1 0 0 0 l ₃ l ₂ l ₁ l ₀ | 2 | 2 | (AC) ↔ [M (i8)] | Exchange the contents of AC and M (i8). | | | | | | | | |
| LEAI i8 | Load E & AC with immediate data | 1 1 0 0 l ₇ l ₆ l ₅ l ₄ | 0 1 1 0 l ₃ l ₂ l ₁ l ₀ | 2 | 2 | E ← l ₇ l ₆ l ₅ l ₄ AC ← l ₃ l ₂ l ₁ l ₀ | Load the immediate data i8 into E, AC. | | | | | | | | |
| RTBL | Read table data from program ROM | 0 1 0 1 | 1 0 1 0 | 1 | 2 | E, AC ← [ROM (PCh, E, AC)] | Load into E, AC the ROM data at the location determined by replacing the lower 8 bits of the PC with E, AC. | | | | | | | | |
| RTBLP | Read table data from program ROM then output to P4, 5 | 0 1 0 1 | 1 0 0 0 | 1 | 2 | Port 4, 5 ← [ROM (PCh, E, AC)] | Output from ports 4 and 5 the ROM data at the location determined by replacing the lower 8 bits of the PC with E, AC. | | | | | | | | |
| [Data pointer manipulation instructions] | | | | | | | | | | | | | | | |
| LDZ i4 | Load DP _H with zero and DP _L with immediate data respectively | 0 1 1 0 | l ₃ l ₂ l ₁ l ₀ | 1 | 1 | DP _H ← 0 DPL ← l ₃ l ₂ l ₁ l ₀ | Load zero into DP _H and the immediate data i4 into DP _L . | | | | | | | | |
| LHI i4 | Load DP _H with immediate data | 1 1 0 0 0 0 0 0 | l ₃ l ₂ l ₁ l ₀ | 2 | 2 | DP _H ← l ₃ l ₂ l ₁ l ₀ | Load the immediate data i4 into DP _H . | | | | | | | | |
| LLI i4 | Load DP _L with immediate data | 1 1 0 0 0 0 0 1 | l ₃ l ₂ l ₁ l ₀ | 2 | 2 | DP _L ← l ₃ l ₂ l ₁ l ₀ | Load the immediate data i4 into DP _L . | | | | | | | | |
| LHLI i8 | Load DP _H , DP _L with immediate data | 1 1 0 0 l ₇ l ₆ l ₅ l ₄ | 0 0 0 0 l ₃ l ₂ l ₁ l ₀ | 2 | 2 | DP _H ← l ₇ l ₆ l ₅ l ₄ DP _L ← l ₃ l ₂ l ₁ l ₀ | Load the immediate data into DL _H , DP _L . | | | | | | | | |
| LXYI i8 | Load DP _X , DP _Y with immediate data | 1 1 0 0 l ₇ l ₆ l ₅ l ₄ | 0 0 0 0 l ₃ l ₂ l ₁ l ₀ | 2 | 2 | DP _X ← l ₇ l ₆ l ₅ l ₄ DP _Y ← l ₃ l ₂ l ₁ l ₀ | Load the immediate data into DL _X , DP _Y . | | | | | | | | |

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| Mnemonic | Instruction code | | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note |
|--|---|--|--|------------------|-----------|---|---|--|
| | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | | | | | | |
| [Data pointer manipulation instructions] | | | | | | | | |
| IL | Increment DP _L | 0 0 0 1 | 0 0 0 1 | 1 | 1 | DP _L ← (DP _L) + 1 | Increment the contents of DP _L . | ZF |
| DL | Decrement DP _L | 0 0 1 0 | 0 0 0 1 | 1 | 1 | DP _L ← (DP _L) - 1 | Decrement the contents of DP _L . | ZF |
| IY | Increment DP _Y | 0 0 0 1 | 0 0 1 1 | 1 | 1 | DP _Y ← (DP _Y) + 1 | Increment the contents of DP _Y . | ZF |
| DY | Decrement DP _Y | 0 0 1 0 | 0 0 1 1 | 1 | 1 | DP _Y ← (DP _Y) - 1 | Decrement the contents of DP _Y . | ZF |
| TAH | Transfer AC to DP _H | 1 1 0 0 1 1 1 1 | 1 1 1 1 0 0 0 0 | 2 | 2 | DP _H ← (AC) | Transfer the contents of AC to DP _H . | |
| THA | Transfer DP _H to AC | 1 1 0 0 1 1 1 0 | 1 1 1 1 0 0 0 0 | 2 | 2 | AC ← (DP _H) | Transfer the contents of DP _H to AC. | ZF |
| XAH | Exchange AC with DP _H | 0 1 0 0 | 0 0 0 0 | 1 | 1 | (AC) ↔ (DP _H) | Exchange the contents of AC and DP _H . | |
| TAL | Transfer AC to DP _L | 1 1 0 0 1 1 1 1 | 1 1 1 1 0 0 0 1 | 2 | 2 | DP _L ← (AC) | Transfer the contents of AC to DP _L . | |
| TLA | Transfer DP _L to AC | 1 1 0 0 1 1 1 0 | 1 1 1 1 0 0 0 1 | 2 | 2 | AC ← (DP _L) | Transfer the contents of DP _L to AC. | ZF |
| XAL | Exchange AC with DP _L | 0 1 0 0 | 0 0 0 1 | 1 | 1 | (AC) ↔ (DP _L) | Exchange the contents of AC and DP _L . | |
| TAX | Transfer AC to DP _X | 1 1 0 0 1 1 1 1 | 1 1 1 1 0 0 1 0 | 2 | 2 | DP _X ← (AC) | Transfer the contents of AC to DP _X . | |
| TXA | Transfer DP _X to AC | 1 1 0 0 1 1 1 0 | 1 1 1 1 0 0 1 0 | 2 | 2 | AC ← (DP _X) | Transfer the contents of DP _X to AC. | ZF |
| XAX | Exchange AC with DP _X | 0 1 0 0 | 0 0 1 0 | 1 | 1 | (AC) ↔ (DP _X) | Exchange the contents of AC and DP _X . | |
| TAY | Transfer AC to DP _Y | 1 1 0 0 1 1 1 1 | 1 1 1 1 0 0 1 1 | 2 | 2 | DP _Y ← (AC) | Transfer the contents of AC to DP _Y . | |
| TYA | Transfer DP _Y to AC | 1 1 0 0 1 1 1 0 | 1 1 1 1 0 0 1 1 | 2 | 2 | AC ← (DP _Y) | Transfer the contents of DP _Y to AC. | ZF |
| XAY | Exchange AC with DP _Y | 0 1 0 0 | 0 0 1 1 | 1 | 1 | (AC) ↔ (DP _Y) | Exchange the contents of AC and DP _Y . | |
| [Flag manipulation instructions] | | | | | | | | |
| SFB n ₄ | Set flag bit | 0 1 1 1 | n ₃ n ₂ n ₁ n ₀ | 1 | 1 | F _n ← 1 | Set the flag specified by n ₄ to 1. | |
| RFB n ₄ | Reset flag bit | 0 0 1 1 | n ₃ n ₂ n ₁ n ₀ | 1 | 1 | F _n ← 0 | Reset the flag specified by n ₄ to 0. | ZF |
| [Jump and subroutine instructions] | | | | | | | | |
| JMP addr | Jump in the current bank | 1 1 1 0 P ₇ P ₆ P ₅ P ₄ | P ₁₁ P ₁₀ P ₉ P ₈ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC13, 12 ← PC13, 12 PC11 to 0 ← P ₁₁ to P ₈ | Jump to the location in the same bank specified by the immediate data P12. | This becomes PC12 + (PC12) immediately following a BANK instruction. |
| JPEA | Jump to the address stored at E and AC in the current page | 0 0 1 0 | 0 1 1 1 | 1 | 1 | PC13 to 8 ← PC13 to 8, PC7 to 4 ← (E), PC3 to 0 ← (AC) | Jump to the location determined by replacing the lower 8 bits of the PC by E, AC. | |
| CAL addr | Call subroutine | 0 1 0 1 P ₇ P ₆ P ₅ P ₄ | 0 P ₁₀ P ₉ P ₈ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC13 to 11 ← 0, PC10 to 0 ← P ₁₀ to P ₀ , M4 (SP) ← (CF, ZF, PC13 to 0), SP ← (SP)-4 | Call a subroutine. | |
| CZP addr | Call subroutine in the zero page | 1 0 1 0 | P ₃ P ₂ P ₁ P ₀ | 1 | 2 | PC13 to 6, PC10 ← 0, PC5 to 2 ← P ₃ to P ₀ , M4 (SP) ← (CF, ZF, PC12 to 0), SP ← SP-4 | Call a subroutine on page 0 in bank 0. | |
| BANK | Change bank | 0 0 0 1 | 1 0 1 1 | 1 | 1 | | Change the memory bank and register bank. | |

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| Mnemonic | Instruction code | | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note | | | | | | | | | | | | | | | | |
|------------------------------------|---|--|--|------------------|-----------|--|--|---|----------------|----------------|----|---|---|----|---|---|----|---|---|---------------|---|---|--|--|
| | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | | | | | | | | | | | | | | | | | | | | | | |
| [Jump and subroutine instructions] | | | | | | | | | | | | | | | | | | | | | | | | |
| PUSH reg | Push reg on M2 (SP) | 1 1 0 0 1 1 1 1 | 1 1 1 1 1 i ₁ i ₀ 0 | 2 | 2 | M2 (SP) ← (reg) SP ← (SP) - 2 | Store the contents of reg in M2 (SP). Subtract 2 from SP after the store. <table border="1" style="margin-left: 20px;"> <tr> <td>reg</td> <td>i₁</td> <td>i₀</td> </tr> <tr> <td>HL</td> <td>0</td> <td>0</td> </tr> <tr> <td>XY</td> <td>0</td> <td>1</td> </tr> <tr> <td>AE</td> <td>1</td> <td>0</td> </tr> <tr> <td>Illegal value</td> <td>1</td> <td>1</td> </tr> </table> | reg | i ₁ | i ₀ | HL | 0 | 0 | XY | 0 | 1 | AE | 1 | 0 | Illegal value | 1 | 1 | | |
| reg | i ₁ | i ₀ | | | | | | | | | | | | | | | | | | | | | | |
| HL | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | |
| XY | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | |
| AE | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | |
| Illegal value | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | |
| POP reg | Pop reg off M2 (SP) | 1 1 0 0 1 1 1 0 | 1 1 1 1 1 i ₁ i ₀ 0 | 2 | 2 | SP ← (SP) + 2 reg ← [M2 (SP)] | Add 2 to SP and then load the contents of M2(SP) into reg. The relation between i1i0 and reg is the same as that for the PUSH reg instruction. | | | | | | | | | | | | | | | | | |
| RT | Return from subroutine | 0 0 0 1 | 1 1 0 0 | 1 | 2 | SP ← (SP) + 4 PC ← [M4 (SP)] | Return from a subroutine or interrupt handling routine. ZF and CF are not restored. | | | | | | | | | | | | | | | | | |
| RTI | Return from interrupt routine | 0 0 0 1 | 1 1 0 1 | 1 | 2 | SP ← (SP) + 4 PC ← [M4 (SP)] CF, ZF ← [M4 (SP)] | Return from a subroutine or interrupt handling routine. ZF and CF are restored. | ZF, CF | | | | | | | | | | | | | | | | |
| [Branch instructions] | | | | | | | | | | | | | | | | | | | | | | | | |
| BAt2 addr | Branch on AC bit | 1 1 0 1 P ₇ P ₆ P ₅ P ₄ | 0 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (AC, t ₂) = 1 | Branch to the location in the same page specified by P ₇ to P ₀ if the bit in AC specified by the immediate data t ₁ t ₀ is one. | | | | | | | | | | | | | | | | | |
| BNAt2 addr | Branch on no AC bit | 1 0 0 1 P ₇ P ₆ P ₅ P ₄ | 0 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (AC, t ₂) = 0 | Branch to the location in the same page specified by P ₇ to P ₀ if the bit in AC specified by the immediate data t ₁ t ₀ is zero. | | | | | | | | | | | | | | | | | |
| BMt2 addr | Branch on M bit | 1 1 0 1 P ₇ P ₆ P ₅ P ₄ | 0 1 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [M (HL), t ₂] = 1 | Branch to the location in the same page specified by P ₇ to P ₀ if the bit in M (HL) specified by the immediate data t ₁ t ₀ is one. | | | | | | | | | | | | | | | | | |
| BNMt2 addr | Branch on no M bit | 1 0 0 1 P ₇ P ₆ P ₅ P ₄ | 0 1 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [M (HL), t ₂] = 0 | Branch to the location in the same page specified by P ₇ to P ₀ if the bit in M (HL) specified by the immediate data t ₁ t ₀ is zero. | | | | | | | | | | | | | | | | | |
| BPt2 addr | Branch on Port bit | 1 1 0 1 P ₇ P ₆ P ₅ P ₄ | 1 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [P (DP _L), t ₂] = 1 | Branch to the location in the same page specified by P ₇ to P ₀ if the bit in port (DP _L) specified by the immediate data t ₁ t ₀ is one. | Internal control registers can also be tested by executing this instruction immediately after a BANK instruction. However, this is limited to registers that can be read out. | | | | | | | | | | | | | | | | |
| BNPt2 addr | Branch on no Port bit | 1 0 0 1 P ₇ P ₆ P ₅ P ₄ | 1 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [P (DP _L), t ₂] = 0 | Branch to the location in the same page specified by P ₇ to P ₀ if the bit in port (DP _L) specified by the immediate data t ₁ t ₀ is zero. | Internal control registers can also be tested by executing this instruction immediately after a BANK instruction. However, this is limited to registers that can be read out. | | | | | | | | | | | | | | | | |

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| Mnemonic | Instruction code | | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note |
|-----------------------|---|--|--|------------------|-----------|---|--|------|
| | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | | | | | | |
| [Branch instructions] | | | | | | | | |
| BC addr | Branch on CF | 1 1 0 1 P ₇ P ₆ P ₅ P ₄ | 1 1 0 0 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (CF) = 1 | Branch to the location in the same page specified by P ₇ to P ₀ if CF is one. | |
| BNC addr | Branch on no CF | 1 0 0 1 P ₇ P ₆ P ₅ P ₄ | 1 1 0 0 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (CF) = 0 | Branch to the location in the same page specified by P ₇ to P ₀ if CF is zero. | |
| BZ addr | Branch on ZF | 1 1 0 1 P ₇ P ₆ P ₅ P ₄ | 1 1 0 1 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (ZF) = 1 | Branch to the location in the same page specified by P ₇ to P ₀ if ZF is one. | |
| BNZ addr | Branch on no ZF | 1 0 0 1 P ₇ P ₆ P ₅ P ₄ | 1 1 0 0 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (ZF) = 0 | Branch to the location in the same page specified by P ₇ to P ₀ if ZF is zero. | |
| BFn4 addr | Branch on flag bit | 1 1 1 1 P ₇ P ₆ P ₅ P ₄ | n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (Fn) = 1 | Branch to the location in the same page specified by P ₀ to P ₇ if the flag (of the 16 user flags) specified by n ₃ n ₂ n ₁ n ₀ is one. | |
| BNFn4 addr | Branch on no flag bit | 1 0 1 1 P ₇ P ₆ P ₅ P ₄ | n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀ | 2 | 2 | PC7 to 0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (Fn) = 0 | Branch to the location in the same page specified by P ₀ to P ₇ if the flag (of the 16 user flags) specified by n ₃ n ₂ n ₁ n ₀ is zero. | |
| [I/O instructions] | | | | | | | | |
| IP0 | Input port 0 to AC | 0 0 1 0 | 0 0 0 0 | 1 | 1 | AC ← (P0) | Input the contents of port 0 to AC. | ZF |
| IP | Input port to AC | 0 0 1 0 | 0 1 1 0 | 1 | 1 | AC ← [P (DP _L)] | Input the contents of port P (DP _L) to AC. | ZF |
| IPM | Input port to M | 0 0 0 1 | 1 0 0 1 | 1 | 1 | M (HL) ← [P (DP _L)] | Input the contents of port P (DP _L) to M (HL). | |
| IPDR i4 | Input port to AC direct | 1 1 0 0 0 1 1 0 | 1 1 1 1 i ₃ i ₂ i ₁ i ₀ | 2 | 2 | AC ← [P (i4)] | Input the contents of P (i4) to AC. | ZF |
| IP45 | Input port 4, 5 to E, AC respectively | 1 1 0 0 1 1 0 1 | 1 1 1 1 0 1 0 0 | 2 | 2 | E ← [P (4)] AC ← [P (5)] | Input the contents of ports P (4) and P (5) to E and AC respectively. | |
| OP | Output AC to port | 0 0 1 0 | 0 1 0 1 | 1 | 1 | P (DP _L) ← (AC) | Output the contents of AC to port P (DP _L). | |
| OPM | Output M to port | 0 0 0 1 | 1 0 1 0 | 1 | 1 | P (DP _L) ← [M (HL)] | Output the contents of M (HL) to port P (DP _L). | |
| OPDR i4 | Output AC to port direct | 1 1 0 0 0 1 1 1 | 1 1 1 1 i ₃ i ₂ i ₁ i ₀ | 2 | 2 | P (i4) ← (AC) | Output the contents of AC to P (i4). | |
| OP45 | Output E, AC to port 4, 5 respectively | 1 1 0 0 1 1 0 1 | 1 1 1 1 0 1 0 1 | 2 | 2 | P (4) ← (E) P (5) ← (AC) | Output the contents of E and AC to ports P (4) and P (5) respectively. | |
| SPB t2 | Set port bit | 0 0 0 0 | 1 0 t ₁ t ₀ | 1 | 1 | [P (DP _L), t2] ← 1 | Set to one the bit in port P (DP _L) specified by the immediate data t ₁ t ₀ . | |
| RPB t2 | Reset port bit | 0 0 1 0 | 1 0 t ₁ t ₀ | 1 | 1 | [P (DP _L), t2] ← 0 | Clear to zero the bit in port P (DP _L) specified by the immediate data t ₁ t ₀ . | ZF |
| ANDPDR i4, p4 | And port with immediate data then output | 1 1 0 0 i ₃ i ₂ i ₁ i ₀ | 0 1 0 1 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | P (P ₃ to P ₀) ← [P (P ₃ to P ₀)] ∨ i ₃ to i ₀ | Take the logical AND of P (P ₃ to P ₀) and the immediate data i ₃ i ₂ i ₁ i ₀ and output the result to P (P ₃ to P ₀). | ZF |
| ORPDR i4, p4 | Or port with immediate data then output | 1 1 0 0 i ₃ i ₂ i ₁ i ₀ | 0 1 0 0 P ₃ P ₂ P ₁ P ₀ | 2 | 2 | P (P ₃ to P ₀) ← [P (P ₃ to P ₀)] ∨ i ₃ to i ₀ | Take the logical OR of P (P ₃ to P ₀) and the immediate data i ₃ i ₂ i ₁ i ₀ and output the result to P (P ₃ to P ₀). | ZF |

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| Mnemonic | Instruction code | D ₇ D ₆ D ₅ D ₄ | D ₃ D ₂ D ₁ D ₀ | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note |
|-----------------------------------|------------------------------------|---|--|-----------------|------------------|--|---|----------------------|------|
| | | | | | | | | | |
| [Timer control instructions] | | | | | | | | | |
| WTTM0 | Write timer 0 | 1 1 0 0 | 1 0 1 0 | 1 | 2 | TIMER0 ← [M2 (HL)], (AC) | Write the contents of M2 (HL), AC into the timer 0 reload register. | | |
| WTTM1 | Write timer 1 | 1 1 0 0 1 1 1 1 | 1 1 1 1 0 1 0 0 | 2 | 2 | TIMER1 ← (E), (AC) | Write the contents of E, AC into the timer 1 reload register A. | | |
| RTIM0 | Read timer 0 | 1 1 0 0 | 1 0 1 1 | 1 | 2 | M2 (HL), AC ← (TIMER0) | Read out the contents of the timer 0 counter into M2 (HL), AC. | | |
| RTIM1 | Read timer 1 | 1 1 0 0 1 1 1 1 | 1 1 1 1 0 1 0 1 | 2 | 2 | E, AC ← (TIMER1) | Read out the contents of the timer 1 counter into E, AC. | | |
| START0 | Start timer 0 | 1 1 0 0 1 1 1 0 | 1 1 1 1 0 1 1 0 | 2 | 2 | Start timer 0 counter | Start the timer 0 counter. | | |
| START1 | Start timer 1 | 1 1 0 0 1 1 1 0 | 1 1 1 1 0 1 1 1 | 2 | 2 | Start timer 1 counter | Start the timer 1 counter. | | |
| STOP0 | Stop timer 0 | 1 1 0 0 1 1 1 1 | 1 1 1 1 0 1 1 0 | 2 | 2 | Stop timer 0 counter | Stop the timer 0 counter. | | |
| STOP1 | Stop timer 1 | 1 1 0 0 1 1 1 1 | 1 1 1 1 0 1 1 1 | 2 | 2 | Stop timer 1 counter | Stop the timer 1 counter. | | |
| [Interrupt control instructions] | | | | | | | | | |
| MSET | Set interrupt master enable flag | 1 1 0 0 0 1 0 1 | 1 1 0 1 0 0 0 0 | 2 | 2 | MSE ← 1 | Set the interrupt master enable flag to one. | | |
| MRESET | Reset interrupt master enable flag | 1 1 0 0 1 0 0 1 | 1 1 0 1 0 0 0 0 | 2 | 2 | MSE ← 0 | Clear the interrupt master enable flag to zero. | | |
| EIH i4 | Enable interrupt high | 1 1 0 0 0 1 0 1 | 1 1 0 1 i ₃ i ₂ i ₁ i ₀ | 2 | 2 | EDIH ← (EDIH) ∨ i4 | Set the interrupt enable flag to one. | | |
| EIL i4 | Enable interrupt low | 1 1 0 0 0 1 0 0 | 1 1 0 1 i ₃ i ₂ i ₁ i ₀ | 2 | 2 | EDIL ← (EDIL) ∨ i4 | Set the interrupt enable flag to one. | | |
| DIH i4 | Disable interrupt high | 1 1 0 0 1 0 0 1 | 1 1 0 1 i ₃ i ₂ i ₁ i ₀ | 2 | 2 | EDIH ← (EDIH) ∧ $\bar{i}4$ | Clear the interrupt enable flag to zero. | ZF | |
| DIL i4 | Disable interrupt low | 1 1 0 0 1 0 0 0 | 1 1 0 1 i ₃ i ₂ i ₁ i ₀ | 2 | 2 | EDIL ← (EDIL) ∧ $\bar{i}4$ | Clear the interrupt enable flag to zero. | ZF | |
| WTSP | Write SP | 1 1 0 0 1 1 0 1 | 1 1 1 1 1 0 1 0 | 2 | 2 | SP ← (E), (AC) | Transfer the contents of E, AC to SP. | | |
| RSP | Read SP | 1 1 0 0 1 1 0 1 | 1 1 1 1 1 0 1 1 | 2 | 2 | E, AC ← (SP) | Transfer the contents of SP to E, AC. | | |
| [Standby control instructions] | | | | | | | | | |
| HALT | HALT | 1 1 0 0 1 1 0 1 | 1 1 1 1 1 1 1 0 | 2 | 2 | HALT | Enter halt mode. | | |
| HOLD | HOLD | 1 1 0 0 1 1 0 1 | 1 1 1 1 1 1 1 1 | 2 | 2 | HOLD | Enter hold mode. | | |
| [Serial I/O control instructions] | | | | | | | | | |
| STARTS | Start serial I O | 1 1 0 0 1 1 1 0 | 1 1 1 1 1 1 1 0 | 2 | 2 | START SIO | Start SIO operation. | | |
| WTSIO | Write serial I O | 1 1 0 0 1 1 1 0 | 1 1 1 1 1 1 1 1 | 2 | 2 | SIO ← (E), (AC) | Write the contents of E, AC to SIO. | | |
| RSIO | Read serial I O | 1 1 0 0 1 1 1 1 | 1 1 1 1 1 1 1 1 | 2 | 2 | E, AC ← (SIO) | Read out the contents of SIO into E, AC. | | |
| [Other instructions] | | | | | | | | | |
| NOP | No operation | 0 0 0 0 | 0 0 0 0 | 1 | 1 | No operation | Consume one machine cycle without performing any operation. | | |
| SB i2 | Select bank | 1 1 0 0 1 1 0 0 | 1 1 1 1 0 0 i ₁ i ₀ | 2 | 2 | PC13, PC12 ← i ₁ i ₀ | Specify the memory bank. | | |

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