Ordering number : ENA1539A

LC70310KBG

CMOS LSI

Noise Canseller IC

ON Semiconductor®

http://onsemi.com

Overview

The LC70310KBG is a noise-cancellation IC that uses an original digital signal processor (DSP) designed for audio applications as the core and integrates the serial PCM interface and host CPU interface on a single chip. In addition, by incorporating an audio signal processing program using our company's unique noise-cancelling algorithm, it features a significantly improved noise-cancelling accuracy.

While reducing the noise components to one-tenth or less, the IC is still capable of maintaining the quality of the sound with no loss of its naturalness.

The LC70310KBG also makes it possible to provide filter processing and other such operations alongside the noisecancelling function.

The PCM interface supports the I^2S mode and enables stereo sound processing.

Features

(1) DSP block
- 16-bit DSP core
- Noise-cancellation processing, filter processing
- Power-save mode (oscillation stop, PLL stop, switching between high-speed operation and low-speed operation)

(2) Host CPU interface (4-line system or I^2C bus* format): Slave (also used as GPIO0 to 3, GPIO13 to 14)

(3) Serial PCM interface (4-line system) : 2 systems of master and slave (also used as GPIO4 to 7, GPIO10 and 11)
- I^2S, left justified, long frame synchronization, short frame synchronization: Fs=8 kHz supported in master mode

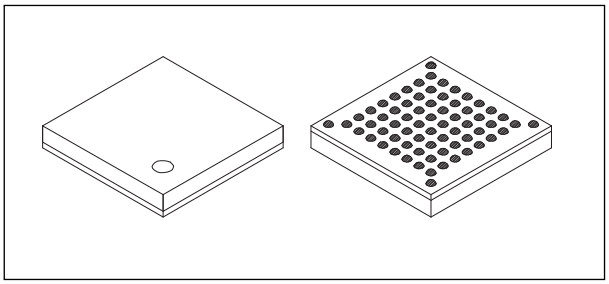
(4) GPIO: 16 ports (also used as host CPU interface and serial PCM interface)

(5) Package: FBGA64K (5mm × 5mm)

(6) Power supplies (supply voltages) : 2 power sources. 2.85V: 2.7V to 3.6V (IO, XVDD), 1.2V±10% (internal logic)

Package

FBGA64K(5mm × 5mm)



FBGA64K

Figure 1

ORDERING INFORMATION

See detailed ordering and shipping information on page 48 of this data sheet.

Internal Block Diagram

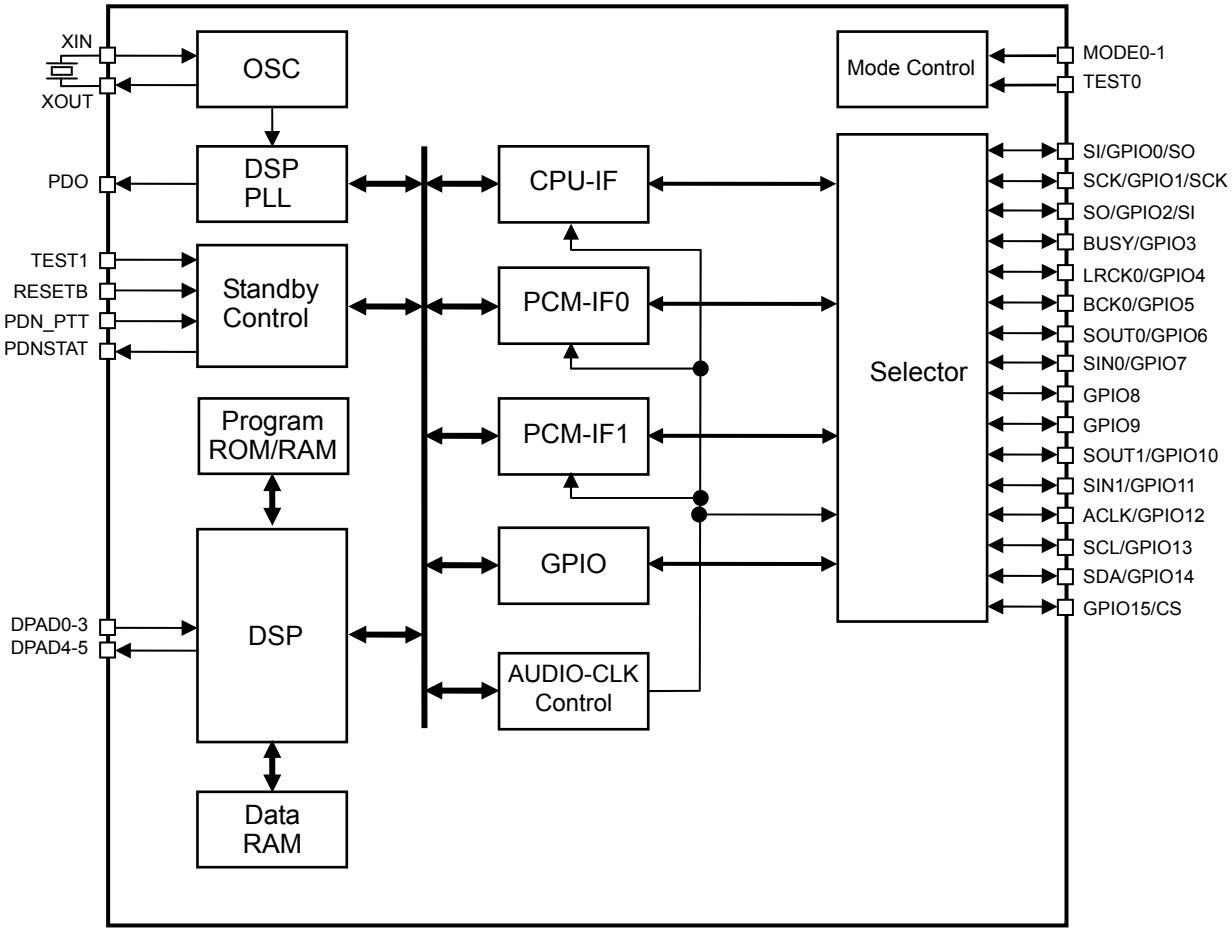


Figure 2 LC70310 Internal Block Diagram

Pin Assignment and Pin Functions (FBGA64K)

(1) Pin Assignment

	A	B	C	D	E	F	G	H	
1	MODE0	**PLLVDD**	XIN	XOUT	**XVSS**	GPIO8	DPAD4	DPAD5	1
2	**CVDD4**	PDO	**PLLVSS**	**XVDD**	**CVSS1**	**CVDD1**	**DVDD1**	DPAD3	2
3	GPIO9	MODE1	(NC)	(NC)	(NC)	(NC)	**DVSS1**	DPAD1	3
4	SOUT1 /GPIO10	**CVSS4**	(NC)	(NC)	(NC)	(NC)	DPAD2	DPAD0	4
5	SIN1 /GPIO11	**DVDD3**	(NC)	(NC)	(NC)	(NC)	**CVDD2**	BUSY /GPIO3	5
6	TEST0	TEST1	**DVSS3**	(NC)	**DVSS2**	(NC)	**CVSS2**	SO /GPIO2 /SI	6
7	BCK0 /GPIO5	LRCK0 /GPIO4	**CVSS3**	**CVDD3**	PDNSTAT	**DVDD2**	SDA /GPIO14	SI /GPIO0 /SO	7
8	ACLK /GPIO12	SOUT0 /GPIO6	SIN0 /GPIO7	RESETB	PDN_PTT	GPIO15 /CS	SCL /GPIO13	SCK /GPIO1 /SCK	8
	A	B	C	D	E	F	G	H	

*Bottom view

Figure 3 Pin Assignment (FBGA64K)

(2) Pin Description

Table 1 (a) Pin Functions

Pin No	Pin Name	IO Attribute	Power Supply System	Function
A1	MODE0	DIS		Mode setting pin 0
A2	CVDD4	Power supply	2.85V	Digital power supply (for IO, 2.7V to 3.6V)
A3	GPIO9	DB		GPIO9 (general-purpose I/O) pin
A4	SOUT1	DB		PCM-IF1 serial data output / GPIO10
A5	SIN1	DB		PCM-IF1 serial data input / GPIO11
A6	TEST0	DIS		Test pin
A7	BCK0	DB		PCM-IF0 bit clock input/output / GPIO5
A8	ACLK	DBS		Audio clock output / GPIO12
B1	PLLVDD	Power supply	1.2V	PLL power supply (1.2V±10%)
B2	PDO	AO		PLL loop filter pin
B3	MODE1	DIS		Mode setting pin 1
B4	CVSS4	Power supply	GND	Digital ground
B5	DVDD3	Power supply	1.2V	Digital power supply (for internal logic, 1.2V±10%)
B6	TEST1	DIS		Test pin
B7	LRCK0	DB		PCM-IF0 serial synchronous input/output / GPIO4
B8	SOUT0	DB		PCM-IF0 serial data output / GPIO6
C1	XIN	AI		Connected to crystal/CERALOCK (ceramic) resonator (8.192MHz)
C2	PLLVSS	Power supply	GND	PLL GND
C3	(NC)	NC		NC
C4	(NC)	NC		NC
C5	(NC)	NC		NC
C6	DVSS3	Power supply	GND	Digital ground
C7	CVSS3	Power supply	GND	Digital ground
C8	SIN0	DB		PCM-IF0 serial data input / GPIO7
D1	XOUT	AO		Connected to crystal / CERALOCK (ceramic) resonator
D2	XVDD	Power supply	2.85V	OSC power source (2.7V to 3.6V)
D3	(NC)	NC		NC
D4	(NC)	NC		NC
D5	(NC)	NC		NC
D6	(NC)	NC		NC
D7	CVDD3	Power supply	2.85V	Digital power supply (for IO, 2.7V to 3.6V)
D8	RESETB	DIS		Reset input pin
E1	XVSS	Power supply	GND	OSC GND
E2	CVSS1	Power supply	GND	Digital ground
E3	(NC)	NC		NC
E4	(NC)	NC		NC
E5	(NC)	NC		NC
E6	DVSS2	Power supply	GND	Digital ground
E7	PDNSTAT	DO		Standby state output pin
E8	PDN_PTT	DIS		Standby control pin/PTT pin
F1	GPIO8	DB		GPIO8 (general-purpose I/O) pin
F2	CVDD1	Power supply	2.85V	Digital power supply (for IO, 2.7V to 3.6V)
F3	(NC)	NC		NC
F4	(NC)	NC		NC
F5	(NC)	NC		NC
F6	(NC)	NC		NC
F7	DVDD2	Power supply	1.2V	Digital power supply (for internal logic, 1.2V±10%)
F8	CS	DB		GPIO15 / FLASH memory chip select output: CS
G1	DPAD4	DO		Output pin for evaluation (normally open)
G2	DVDD1	Power supply	1.2V	Digital power supply (for internal logic, 1.2V±10%)
G3	DVSS1	Power supply	GND	Digital ground
G4	DPAD2	DI		Input pin for evaluation (normally GND)
G5	CVDD2	Power supply	2.85V	Digital power supply (for IO, 2.7V to 3.6V)
G6	CVSS2	Power supply	GND	Digital ground
G7	SDA	DBS		I2C bus interface data input/output / GPIO14
G8	SCL	DBS		I2C bus interface clock / GPIO13
H1	DPAD5	DO		Output pin for evaluation (normally open)
H2	DPAD3	DI		Input pin for evaluation (normally GND)
H3	DPAD1	DI		Input pin for evaluation (normally GND)
H4	DPAD0	DI		Input pin for evaluation (normally GND)
H5	BUSY	DB		CPU interface BUSY/GPIO3
H6	SO	DB		CPU interface data output / GPIO2 / FLASH memory data input: SI
H7	SI	DB		CPU interface data input / GPIO0 / FLASH memory data output: SO
H8	SCK	DB		CPU interface clock / GPIO1 / FLASH memory clock output

* TEST0 and TEST1 pins must be fixed low.

* The voltages applied to the power pins must satisfy the following conditions:

XVDD ≥ CVDD1 to 4 > DVDD1 to 3 = PLLVDD

Table 1 (b) IO Attribute Symbols

IO Attribute	Description
DI	Digital input
DIS	Digital input (Schmidt input)
DO	Digital output
DB	Digital input / output
DBS	Digital input / output (Schmidt input)
AI	Analog input
AO	Analog output
Power supply	Power supply / GND
NC	No connection

Electrical Characteristics

(1) Absolute Maximum Ratings at VSS=0V

Parameter	Symbol	Pin Name		Ratings	Unit
Maximum supply voltage	VDD28max	CVDD1 to 4		−0.3 to +3.96	V
	VDD12max	DVDD1 to 3		−0.3 to +1.8	
	XVDD28max	XVDD		−0.3 to +3.96	
	AVDD12max	PLLVDD		−0.3 to +1.8	
Input voltage	VI28	2.85V system digital I/O pin		−0.3 to VDD28+0.3	
Output voltage	VO1	2.85V system digital I/O pin		−0.3 to VDD28+0.3	
Allowable power dissipation	Pdmax	FBGA64K (5x5)	Ta=−30 to 70°C	124	mW
Operating ambient temperature	Topr			−30 to +70	°C
Storage ambient temperature	Tstg			−55 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

(2) Allowable Operating Ranges at Ta= −30°C to +70°C, VSS=0V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	VDD28	CVDD1 to 4		2.7	2.85	3.6	V
	VDD12	DVDD1 to 3		1.08	1.2	1.32	
	XVDD28	XVDD		2.7	2.85	3.6	
	AVDD12	PLLVDD		1.08	1.2	1.32	
Input voltage range	VI28	DPAD0 to 3,TEST0 to 1,MODE0 to 1, RESETB,PDN_PTT, BUSY,SCK,SO,SI,CS, SOUT0,SIN0,LRCK0,BCK0, SOUT1,SIN1,ACLK, SCL,SDA,GPIO8 to 9		0	-	VDD28	
	VIX28	XIN		0	-	XVDD28	
Oscillator frequency	Fopr	XIN,XOUT			8.192		MHz

* Power supply conditions: XVDD ≥ CVDD1 to 4 > DVDD1 to 3 = PLLVDD

(3) DC Characteristic at Ta=-30°C to +70°C, VDD28=2.7V to 3.6V, VDD12=1.08V to 1.32V, VSS=0V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
High level input voltage	VIH	DPAD0 to 3,TEST0 to 1, MODE0 to 1, RESETB,PDN_PTT, BUSY,SCK,SO,SI,CS, SOUT0,SIN0,LRCK0,BCK0, SOUT1,SIN1,ACLK, SCL,SDA,GPIO8 to 9		0.7VDD28	-	-	V
Low level input voltage	VIL	DPAD0 to 3,TEST0 to 1, MODE0 to 1, RESETB,PDN_PTT, BUSY,SCK,SO,SI,CS, SOUT0,SIN0,LRCK0,BCK0, SOUT1,SIN1,ACLK, SCL,SDA,GPIO8 to 9		-	-	0.3VDD28	
High level input current	IIH	DPAD0 to 3,TEST0 to 1, MODE0 to 1, RESETB,PDN_PTT, BUSY,SCK,SO,SI,CS, SOUT0,SIN0,LRCK0,BCK0, SOUT1,SIN1,ACLK, SCL,SDA,GPIO8 to 9	VI=VDD28	−10	-	+10	µA
Low level input current	IIL		VI=VSS	−10	-	+10	
High level output voltage	VOH	DPAD4,PDNSTAT, SCK,SO,SI,CS, SOUT0,SIN0,LRCK0,BCK0, SOUT1,SIN1, GPIO8 to 9	IOH=−2mA	VDD28−0.4	-	-	V
Low level output voltage	VOL		IOL=2mA	-	-	0.4	
High level output voltage	VOH	ACLK, BUSY,SCL,SDA, DPAD5	IOH=−4mA	VDD28−0.4	-	-	
Output low level voltage	VOL		IOL=4mA	-	-	0.4	
Output leakage current	IOZ	BUSY,SCK,SO,SI,CS, SOUT0,SIN0,LRCK0,BCK0, SOUT1,SIN1,SCL,SDA, ACLK,GPIO8 to 9	VO=Hi_z	−10	-	+10	µA
Quiescent current dissipation	IDDS		Output open VI=VSS or VDD28	-	10	-	

(4) Current Drain at Ta=25°C, VDD28=2.85V, XVDD28=2.85V, VDD12=1.2V, VSS=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain (with DSP core running at 32MHz)	IDD12D	Digital 1.2V system (core)		8.5		mA
	IDD12A	Analog 1.2V system (PLL)		0.5		mA
	IDD28	2.85V system (IO, XVDD)		1		mA
	IDD	Total		10		mA

(5) Clock Reset at Ta=-30 to +70°C, VDD28=2.7 to 3.6V, XVDD28=2.7 to 3.6V, VSS=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Oscillator frequency	fop			8.192		MHz
Reset hold time	tres		500			µs

*) "CERALOCK®" made by Murata Manufacturing Co., Ltd.: Use of the CSTCE8M19G55-R0 is recommended.

Operation Modes

The operation mode of the LC70310 can be switched depending on the state of the MODE0 pin at startup. (TEST0 and TEST1 must be fixed to "L.") There are two operation modes, namely, the CPU mode and standalone mode. The CPU mode is the mode in which the LC70310 operates under the control exercised by host CPU. In the standalone mode, this IC operates independently. In both operation modes, programs are downloaded from the external source at startup. In the CPU mode, it is possible to select the 4-line interface or the I^2C bus format.

Operation Modes Chart

Operation Mode	CPU Mode		Standalone Mode
	4-line System	I^2C Bus Format	
MODE0 pin	L	L	H
MODE1 pin	L	H	L

Pin	Signal Name	I/O Attribute	Signal Name	I/O Attribute	Signal Name	I/O Attribute
SI / GPIO0 / SO	SI	I	GPIO0	I/O	SO	O
SCK / GPIO1 / SCK	SCK	I	GPIO1	I/O	SCK	O
SO / GPIO2 / SI	SO	O	GPIO2	I/O	SI	I
BUSY / GPIO3	BUSY	I/O	BUSY	O	GPIO3	I/O
LRCK0 / GPIO4	LRCK0 / GPIO4	I/O I/O	LRCK0 / GPIO4	I/O I/O	LRCK0 / GPIO4	I/O I/O
BCK0 / GPIO5	BCK0 / GPIO5	I/O I/O	BCK0 / GPIO5	I/O I/O	BCK0 / GPIO5	I/O I/O
SOUT0 / GPIO6	SOUT0 / GPIO6	O I/O	SOUT0 / GPIO6	O I/O	SOUT0 / GPIO6	O I/O
SIN0 / GPIO7	SIN0 / GPIO7	I I/O	SIN0 / GPIO7	I I/O	SIN0 / GPIO7	I I/O
GPIO8	GPIO8	I/O	GPIO8	I/O	GPIO8	I/O
GPIO9	GPIO9	I/O	GPIO9	I/O	GPIO9	I/O
SOUT1 / GPIO10	SOUT1 / GPIO10	O I/O	SOUT1 / GPIO10	O I/O	SOUT1 / GPIO10	O I/O
SIN1 / GPIO11	SIN1 / GPIO11	I I/O	SIN1 / GPIO11	I I/O	SIN1 / GPIO11	I I/O
ACLK / GPIO12	ACLK / GPIO12	O I/O	ACLK / GPIO12	O I/O	ACLK / GPIO12	O I/O
SCL / GPIO13	GPIO13	I/O	SCL	I/O	GPIO13	I/O
SDA / GPIO14	GPIO14	I/O	SDA	I/O	GPIO14	I/O
GPIO15 / CS	GPIO15	I/O	GPIO15	I/O	CS	O

(1) CPU Mode

In the CPU mode, the external CPU is the master, and the LC70310 is controlled through the host CPU interface. The CPU mode startup sequence is described below.

(1-1) CPU mode startup sequence (example: when the 4-line interface is used)

When the LC70310 is to be used in the CPU mode, the host CPU is started up by system reset after power-on, and the host CPU resets the LC70310 (by setting the RESETB pin and PDN_PTT pin to "L") and sets up the CPU interface ports. Next, after waiting for the time taken (several ms) for the LC70310 oscillation to stabilize, the host CPU sets the RESETB pin and PDN_PTT pin of the IC to "H" to release the reset. It then waits about 8 ms (*) before starting the transfer of the program data. (Transfer can start if the BUSY signal is "H.") After the program uploading is completed, the host CPU transfers to the control mode of the LC70310. The program data of the LC70310 must be stored ahead of time in the memory (internal flash memory or external non-volatile memory) of the host CPU.

After power-on, the LC70310 starts oscillation, but the reset state is maintained by the reset control exercised from the host CPU. In approximately 8 ms (*) after the host CPU releases the reset, the LC70310 starts the boot program and responds to the transfer of the program data from the host CPU. When the program data downloading is completed, it automatically returns to address 0 and executes the downloaded program. (Noise-cancelling processing now starts.)

(*) This is the time taken when the frequency of the resonator is 8.192MHz.

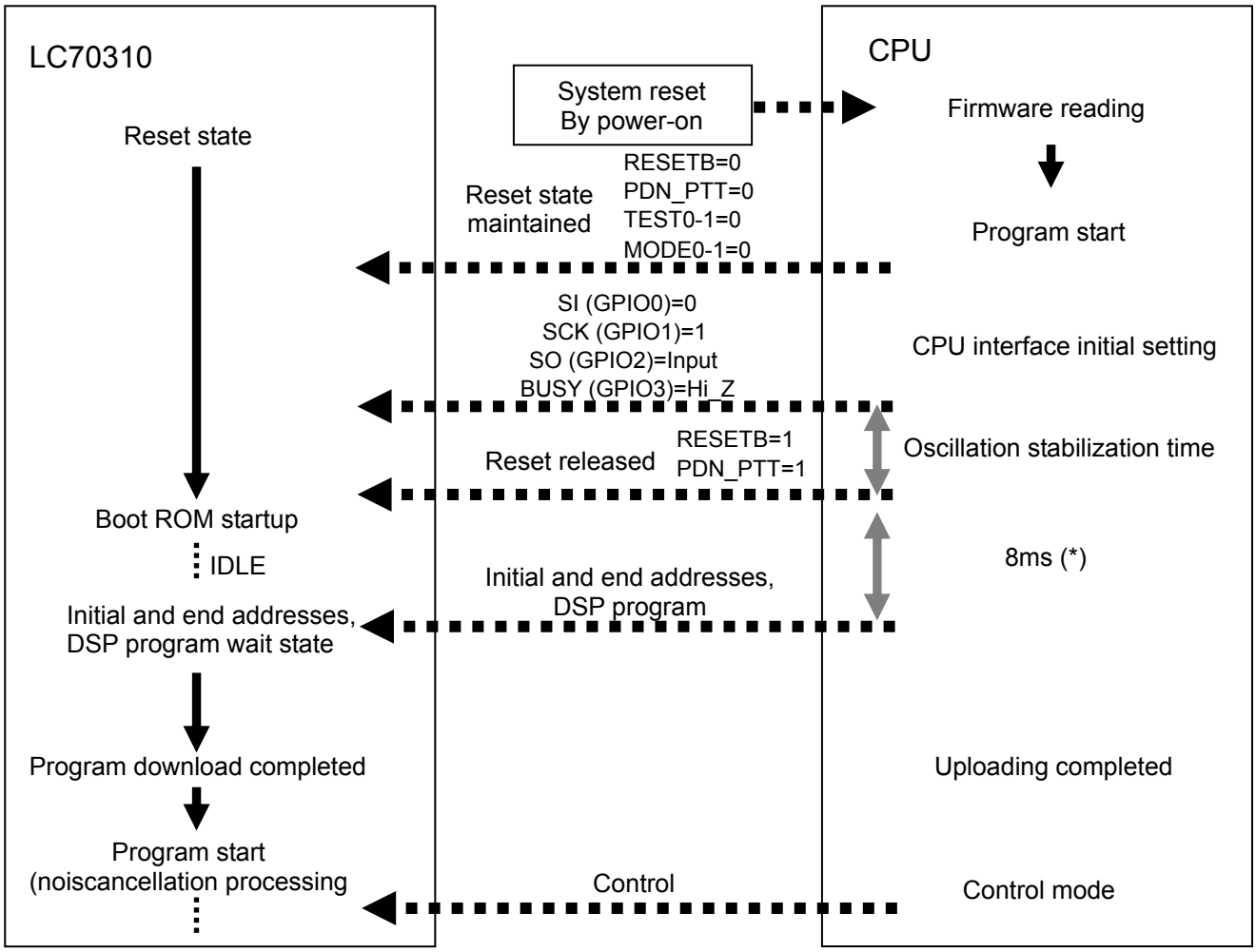


Figure 4

The program data of the LC70310 must be stored ahead of time in the memory (internal flash memory or external nonvolatilememory) of the host CPU. Figures 5 and 6 show examples of where the program data is stored.

<<CPU mode configuration 1: Configuration when using a CPU with internal flash memory>>

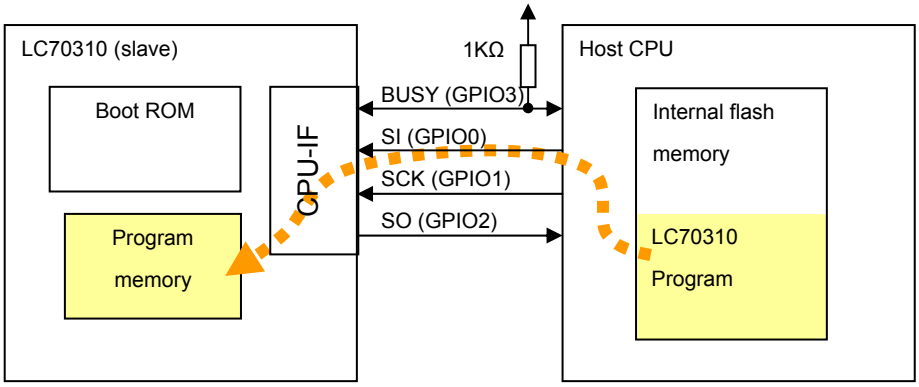


Figure 5

<<CPU mode configuration 2: Configuration when using a CPU and external non-volatile memory>>

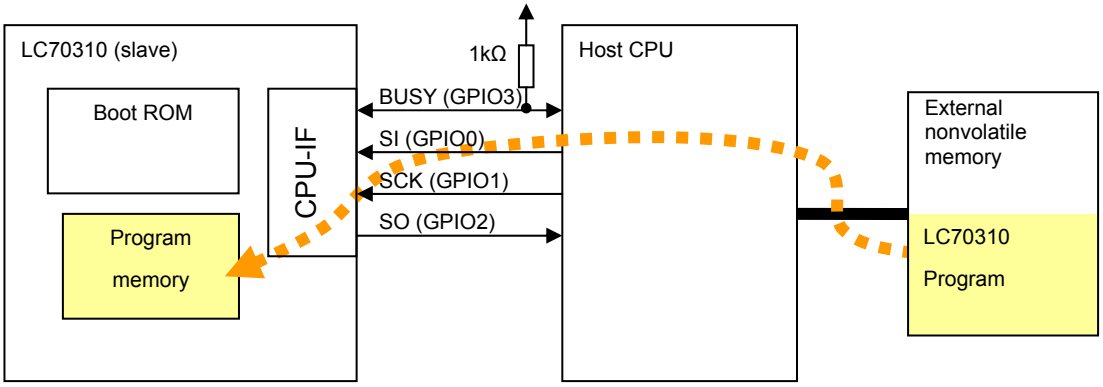


Figure 6

(1-2) Procedure for program data transfer using 4-line interface

The host CPU confirms that the BUSY signal is “H,” outputs “L” to the BUSY pin (open drain pin), and then starts transferring the program data to the LC70310. The program data is transferred in 6-word units (18 bytes) with the MSB first.

After transferring the first 6 words, the host CPU returns the BUSY pin to “H.” In response, the LC70310 executes the internal processing. At this time, the LC70310 sets the BUSY pin to “L,” and informs the host CPU that processing is in progress. The host CPU confirms that the BUSY pin has been set to “H,” and starts transferring the next 6 words. It repeats this transfer up to the end address of the program. (Refer to Figure. 7(a).)

When the host CPU completes the transfer of the last 6 words and sets the BUSY pin to “H,” the LC70310 executes the internal processing, and then it automatically executes the program from address 0. (Refer to Figure 7(b).)

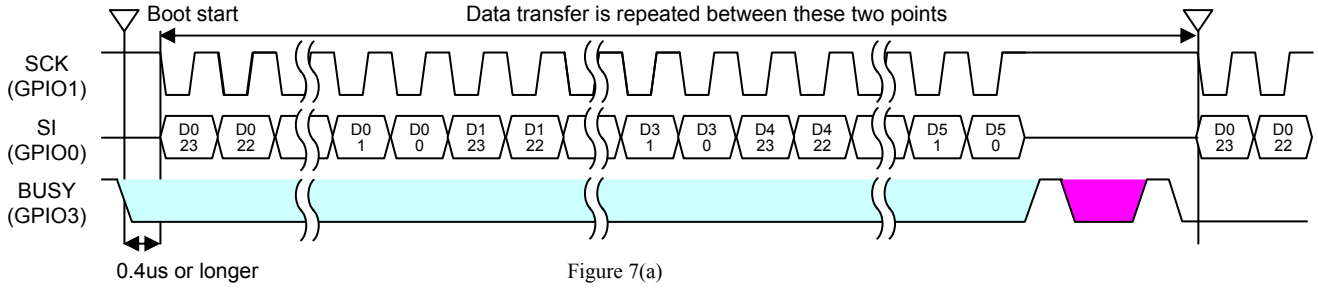


Figure 7(a)

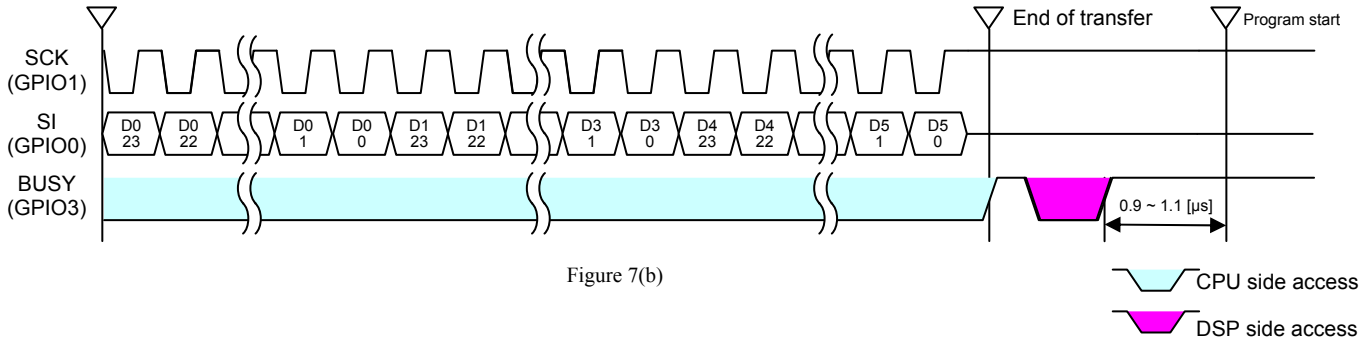


Figure 7(b)

(1-3) Program transfer using I2C bus

Figure 8 shows the procedure for the program data transfer when the I2C bus is used. The LC70310 has a slave function, and a 7-bit slave address is supported. The data can be transferred in the standard mode (up to 100kbps) or fast mode (up to 400kbps).

The host CPU confirms that the SCL signal and SDA signal (both pins are open drain pins) are “H,” outputs “L” to the SDA pin (this constitutes the START condition), and then starts transferring the program data to the LC70310. The program data is transferred in 6-word units (18 bytes) with the MSB first.

After transferring the first 6 words, the host CPU changes the SDA signal from “L” to “H” while the SCL signal is “H” (this constitutes the STOP condition). In response, the LC70310 executes the internal processing. After the busfree time (see Table 15) between the STOP and START conditions has passed, the host CPU starts transferring the next 6 words. It repeats this transfer up to the end address of the program.

When the host CPU completes the transfer of the last 6 words and issues the STOP condition, the LC70310 executes the internal processing, and then automatically executes the program from address 0.

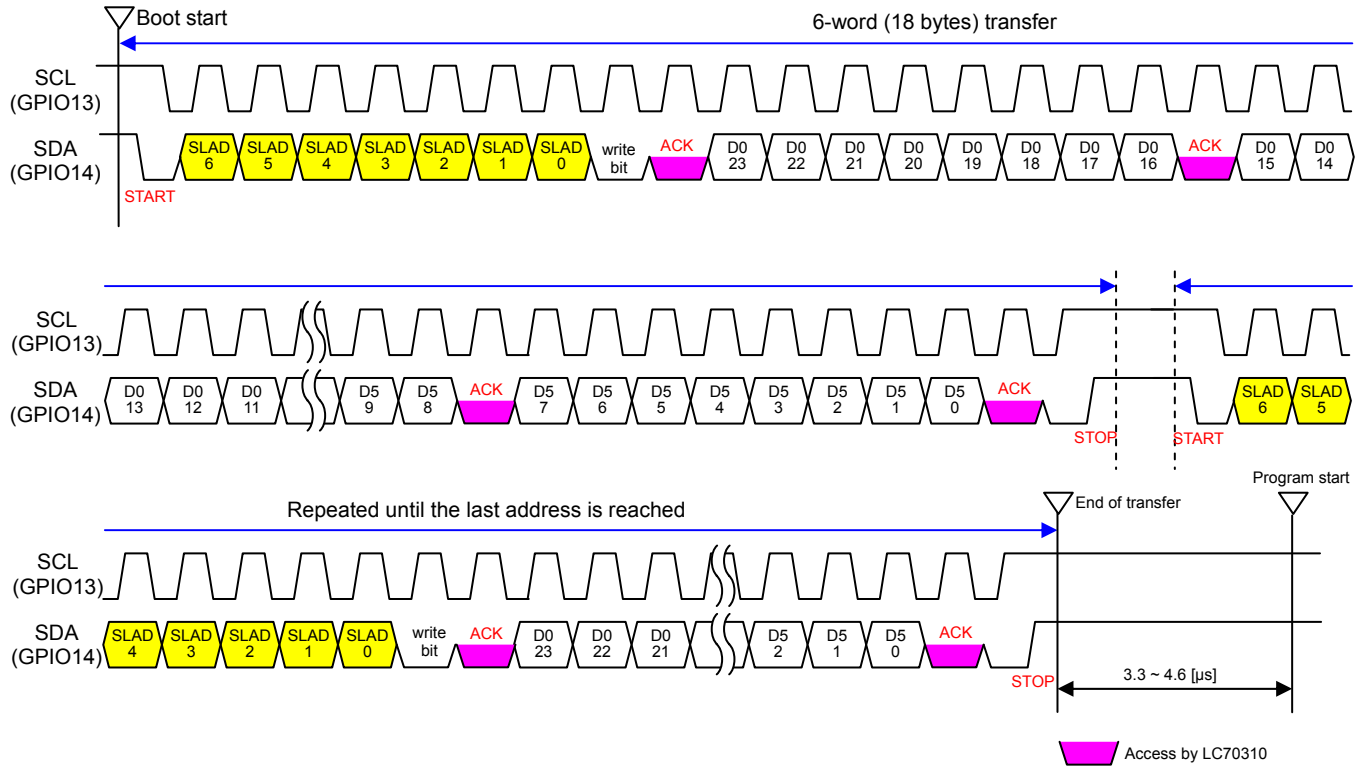


Figure 8

(2) Standalone Mode

In the standalone mode, the LC70310, as a result of system reset initiated by power-on, starts the program loader stored in the boot ROM, and downloads the program data provided ahead of time in the external serial EEPROM through the GPIO0 to GPIO3 pins to the internal program memory. Up to 6144 words (18432bytes) can be loaded. After the downloading is completed, it automatically returns to address 0, and executes the downloaded program. (Noisecancelling starts.) The program to be downloaded must be stored ahead of time in the serial EEPROM from address 0.

*) A serial EEPROM with the SPI system and at least 256Kbits must be provided.

Figure 9 shows the loading sequence (SPI system).

<<Standalone mode configuration>>

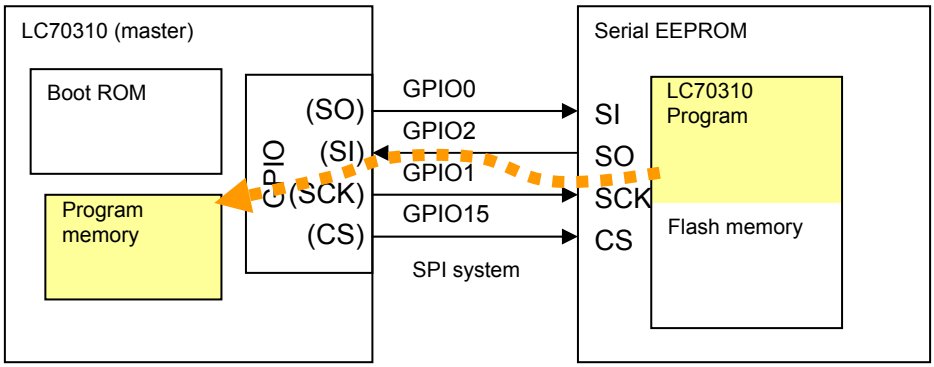


Figure 9

Program loading sequence

Figure 10 shows the transfer format using the SPI system.

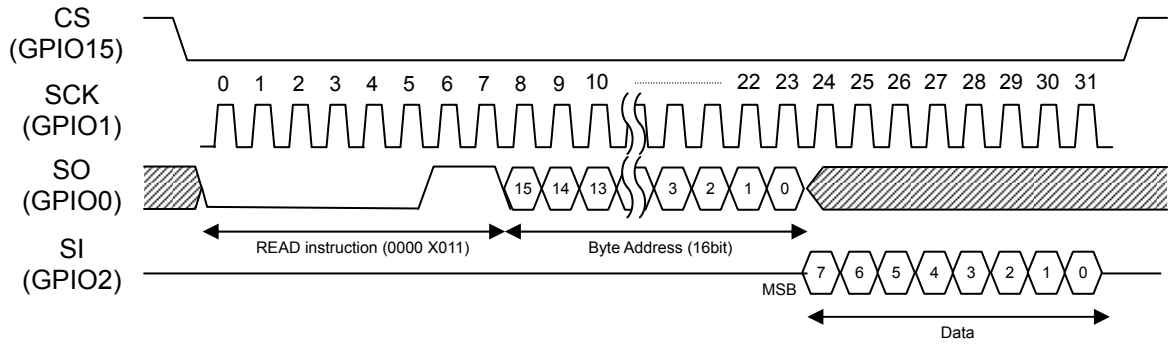


Figure 10

Host CPU Interface

The host CPU interface is a serial interface which supports the 4-line system (SCK, SIN, SOUT and BUSY) and I2C bus format (SDA and SCL). It operates as a slave device for the external host CPU, and either the 4-line system or I2C bus format is selected when it is used. Control over the various operations of the LC70310 and setting or changing its parameters can be performed from the external host CPU through this interface.

The host CPU interface consists of a command register (16-bit width) and 16 parameter registers (16-bit width: 8 write buffers and 8 read buffers) and, based on the commands sent to the command register, the data is transferred to the parameter registers and processed.

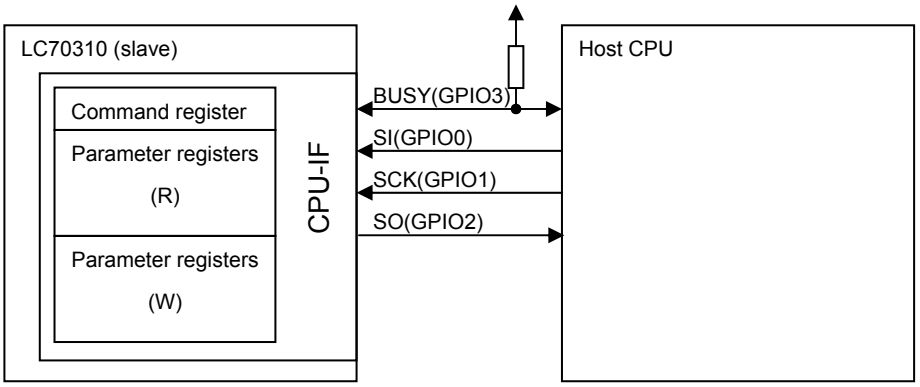


Figure 11 (a) 4-line Interface

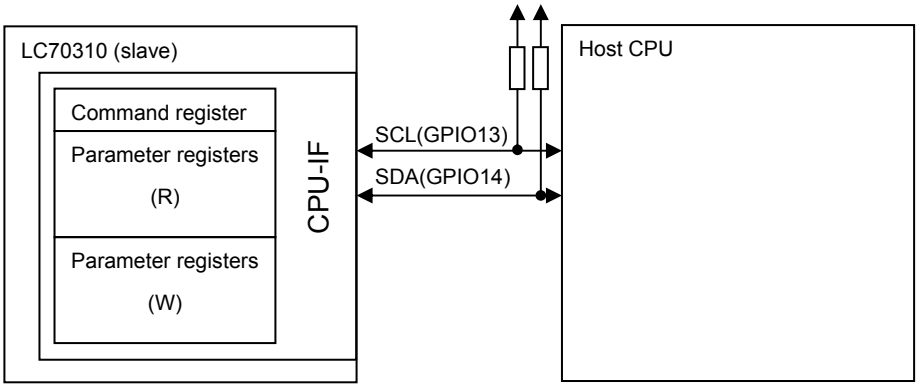


Figure 11 (b) I^2C Bus Interface

(1) Description of 4-line Interface Sequences

(1-1) CPU → LC70310: Write sequence

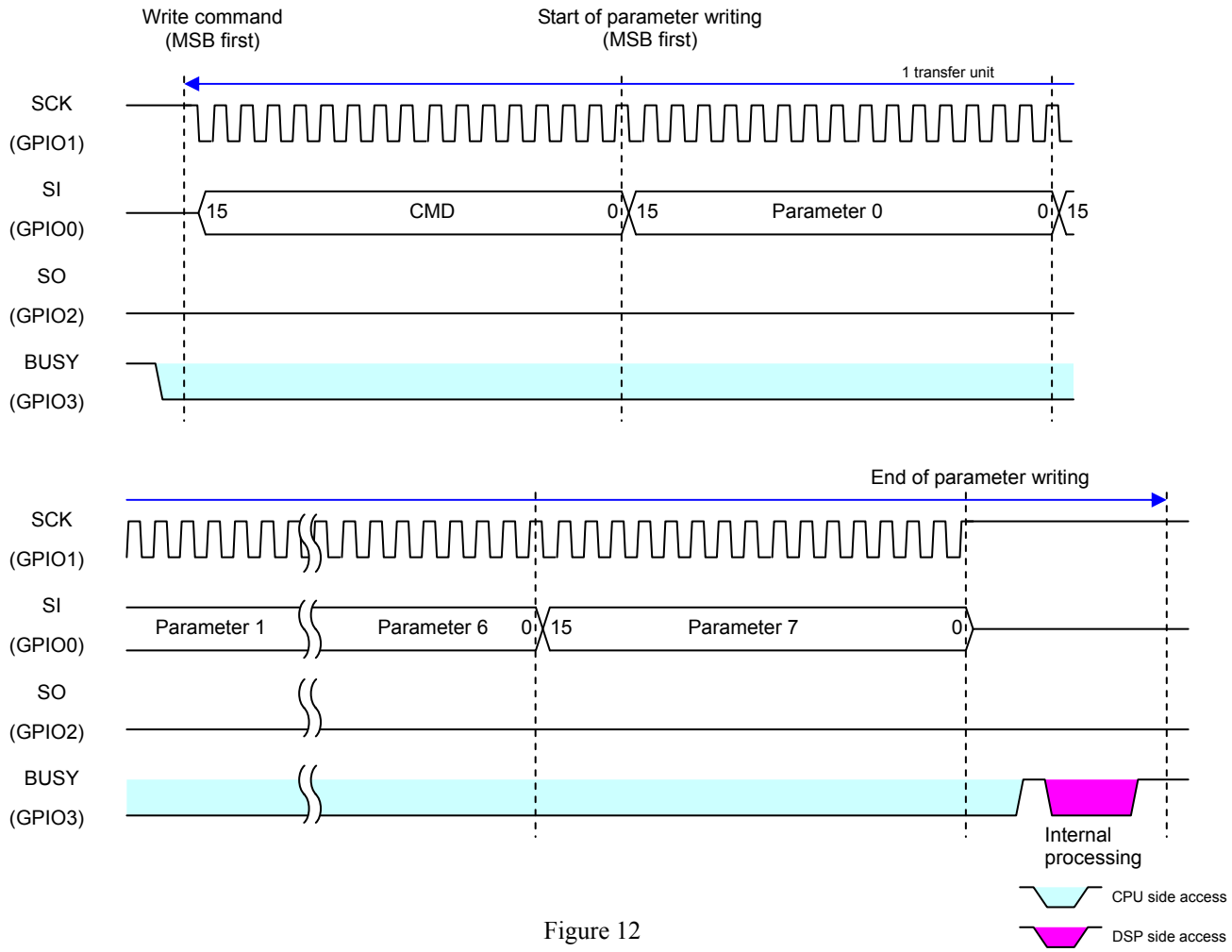


Figure 12

Procedure for writing the control data (commands and parameters) from the host CPU

First, the host CPU confirms that the BUSY signal is “H.” If it is “H,” it outputs “L” to the BUSY signal, and starts the serial transfer (CPU → LC70310). Here, the serial transfer data is sent with the MSB first after the write command (CMD15 to CMD0: 16 bits) in the sequence of parameter 0, parameter 1 and so on to parameter 7. After the data has been transferred, Hi_z is output to the BUSY signal.

*) The port of the host CPU which controls the BUSY signal needs to be the open drain (L / Hi_z) type.

(1-2) LC70310 → CPU: Read sequence

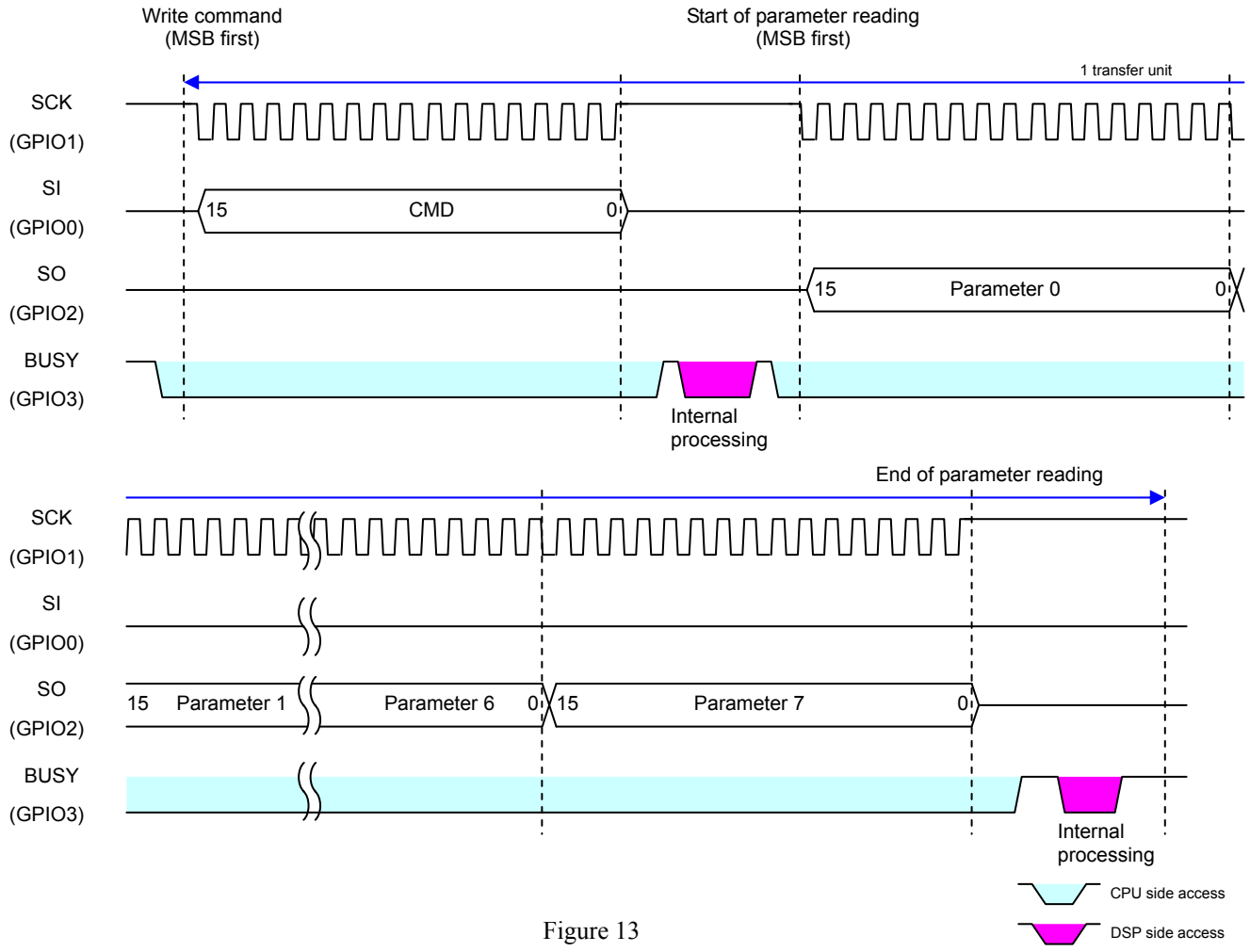


Figure 13

Procedure for reading the control data (commands and parameters) into the host CPU

First, the host CPU confirms that the BUSY signal is “H.” If it is “H,” it outputs “L” to the BUSY signal, and starts the serial transfer (CPU → LC70310). First, it sends the read command (CMD15 to CMD0: 16 bits), and outputs Hi_z to the BUSY signal. *) (The BUSY signal is now set to “H.”) As a result, the LC70310 prepares the data corresponding to the read command in the transfer buffers. While the LC70310 is executing the internal processing, the BUSY signal is set to “L,” and when the data preparation is completed, the BUSY signal is again set to “H.” After confirming this, the host CPU again outputs “L” to the BUSY signal, and data is sent in the sequence of parameter 0, parameter 1 and so on to parameter 7 in each case with the MSB first. After the data has been transferred, Hi_z is output to the BUSY signal. Upon completion of the internal processing, the next serial transfer can be performed.

*) The port of the host CPU which controls the BUSY signal needs to be the open drain (L / Hi_z) type.

(2) Description of I2C Bus Interface Sequences

(2-1) CPU → LC70310: Write sequence

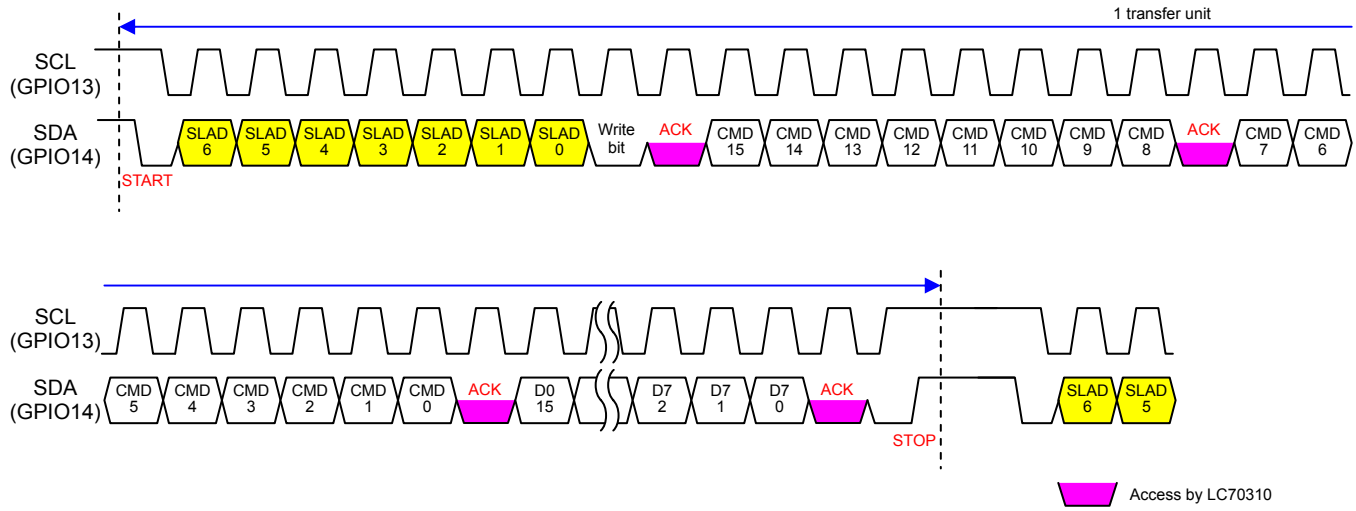


Figure 14

<1> The host CPU confirms that the SCL signal and SDA signal are both “H.” If they are both “H,” the host CPU outputs “L” to the SDA signal (this constitutes the START condition).

<2> The host CPU outputs the 7-bit slave address and write bit (“L”) in synchronization with the SCL signal. (The SDA signal changes when the SCL signal is “L.”). The LC70310 sends ACK (“L”) to the CPU if the receive address matches its own slave address. If it does not match, it sends NACK (“H”) to the CPU. (Note 1)

<3> After confirming ACK from the LC70310, it starts serial transfer (CPU → LC70310). The serial transfer data is sent in 8-bit units after the write command (CMD15 to CMD0: 16 bits) in the sequence of parameter 0, parameter 1 and so on to parameter 7 in each case with the MSB first. Each time LC70310 receives 8 bits, it sends ACK. (Note 2)

<4> After the data has been transferred, the SDA signal is changed from “L” to “H” while the SCL signal is “H” (this constitutes the STOP condition). In response, the internal processing inside the LC70310 starts.

<5> After the bus-free time (see Table 15) between the STOP and START conditions has passed, the next serial transfer can be performed.

*) The port of the host CPU which controls the SCL and SDA signals needs to be the open drain type.

Note 1: If NACK has been confirmed, the STOP condition must be issued, and then the sequence must be repeated from <1>.

Note 2: If NACK has been confirmed during the course of the transfer, the STOP condition must be issued, and then the sequence must be repeated from <1>.

(2-2) LC70310 → CPU: Read Sequence

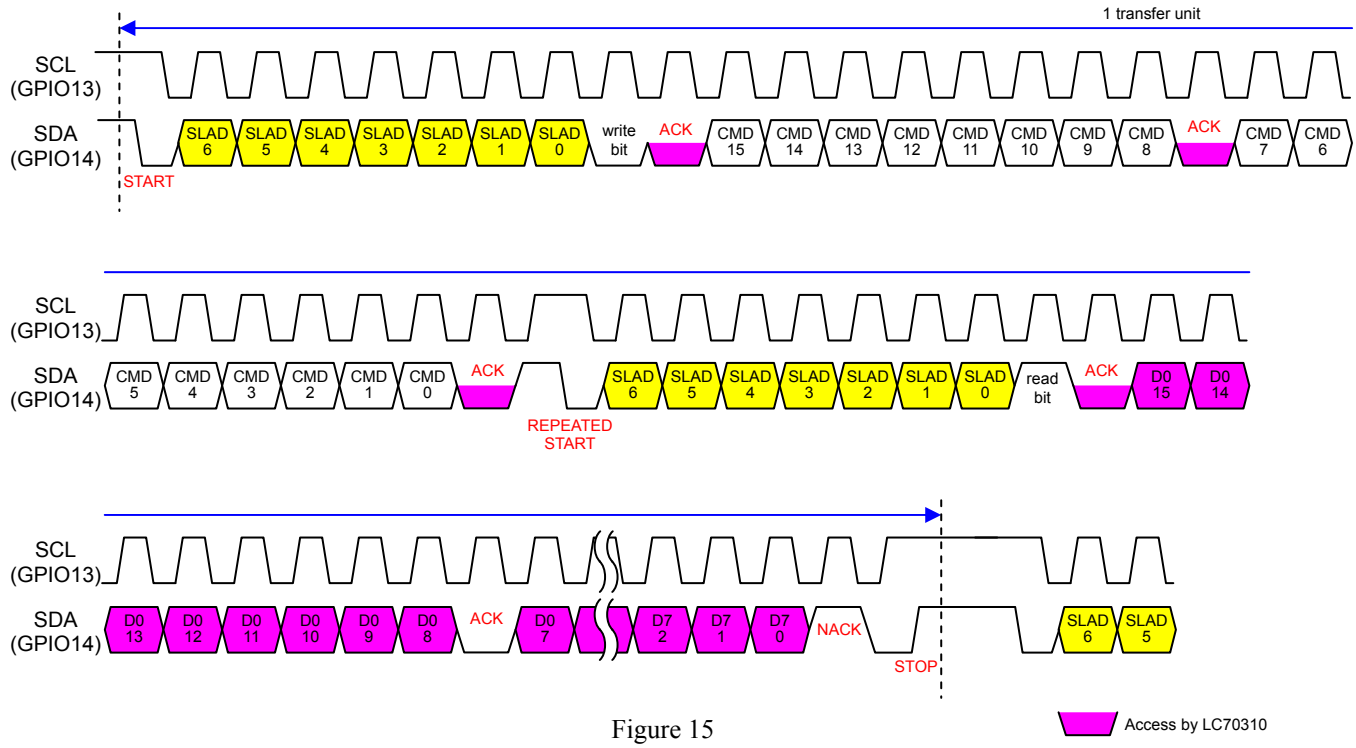


Figure 15

<1> The host CPU confirms that the SCL signal and SDA signal are both “H.” If they are both “H,” the host CPU outputs “L” to the SDA signal (this constitutes the START condition).

<2> The host CPU outputs the 7-bit slave address and write bit (“L”) in synchronization with the SCL signal. (The SDA signal changes when the SCL signal is “L.”). The LC70310 sends ACK (“L”) to the CPU if the receive address matches its own slave address. If it does not match, it sends NACK (“H”) to the CPU. (Note 1)

<3> After confirming ACK from the LC70310, the read command (CMD15 to CMD0: 16 bits) is sent in 8-bit units with the MSB first. Each time the LC70310 receives 8 bits, it sends ACK.

<4> After the read command has been sent, the SDA signal is changed from “H” to “L” while the SCL signal is “H” (this constitutes the repeat START condition). As a result, the LC70310 prepares the data corresponding to the read command in the transfer buffers.

<5> The LC70310 outputs the 7-bit slave address and read bit (“H”) in synchronization with the SCL signal. It sends ACK to the CPU if the receive address matches its own slave address. If it does not match, it sends NACK to the CPU. (Note 1)

<6> After confirming ACK from the LC70310, the data is sent in the sequence of parameter 0, parameter 1 and so on to parameter 7 in each case with the MSB first. The host CPU sends ACK each time 8 bits are received. However, NACK is sent only when all the data has been received. (Note 2)

<7> After NACK has been sent, the SDA signal is changed from “L” to “H” while the SCL signal is “H” (this constitutes the STOP condition).

<8> After the bus-free time (see Table 15) between the STOP and START conditions has passed, the next serial transfer can be performed.

*) The port of the host CPU which controls the SCL and SDA signals needs to be the open drain type.

Note 1: If NACK has been confirmed, the STOP condition must be issued, and then the sequence must be repeated from <1>.

Note 2: If the host CPU is to suspend the receiving of the data while it is being transferred, NACK must be sent to the LC70310 without fail, and the STOP condition must be issued. To resume the transfer, the sequence must be repeated from <1>.

(2-3) Notes when using the I2C interface

(2-3-a) Extension of “L” period of SCL signal

If the internal processing is still being executed when ACK is sent to the host CPU, the LC70310 sets and holds the status of the SCL signal to “L” and delays the ACK response until the internal processing is completed. This means that the host CPU needs to monitor the SCL signal state and control the SCL signal in such a way that the data transfer after the completion of the internal processing is undertaken correctly. Attention must be paid to the duration of the “H” period of the SCL signal after the internal processing is completed. Given below is an example of when the “L” period of the SCL signal is to be extended.

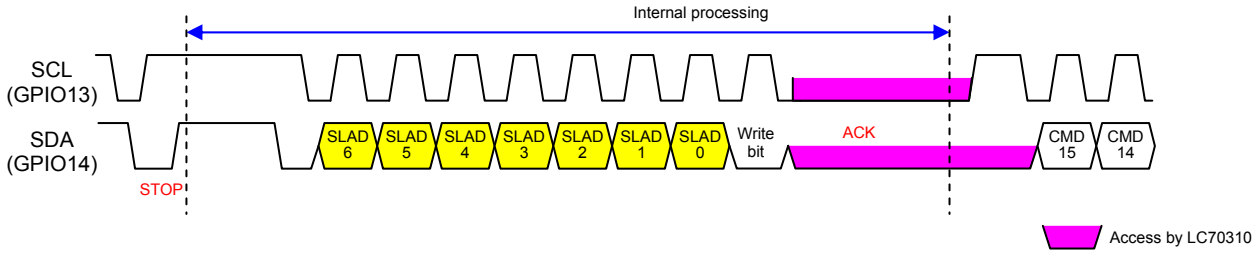


Figure 16

(2-3-b) Pull-up resistor

The resistance of the external pull-up resistor (RP) is determined by the supply voltage, clock speed and static capacitance of the bus. The appropriate RP value must be selected so that the stipulations for the rise and fall times of the SDA and SCL signals are satisfied (see Table 15) while taking into account the electrical characteristics of the host CPU which controls the LC70310 and the VOL-IOL characteristics of the LC70310. If this value is too high, the SCL frequency will be limited; conversely, if it is too low, the operating current consumption will increase.

In the case of a 2.85V power supply, a resistance of at least 1k∧ or so is required for RP. (A resistance in the range of several kΩ to 10kΩ is recommended.)

(2-3-c) General call

The LC70310 does not support the general call address.

Connected Device-side Interfaces (Serial PCM interfaces)

The LC70310 comes with two serial PCM interfaces supporting a master and slave as the connected device-side digital interfaces. These interfaces support four transfer modes: I2S, left justified, long frame synchronization and short frame synchronization, and enable data to be transferred at a sampling frequency of 8 kHz. Either the transfer clock polarity (rise synchronization or fall synchronization) or transfer sequence (MSB first or LSB first) can be specified as the transfer data format.

In the master mode, the LC70310 generates the serial transfer clock (BCK) with a frequency equivalent to Fs*32 and the sync pulse (LRCK) to execute serial transfer. It also outputs from the ACLK pin a clock with a frequency equivalent to Fs*256 to the connection destination (slave device). In the slave mode, serial transfer is accomplished using the serial transfer clock (whose frequency is equivalent to Fs*32) which is input to the BCK pin and the sync pulse which is input to the LRCK pin.

In both the master mode and slave mode, it is possible to input and output two channels of data (SIN0 / SOUT0 and SIN1 / SOUT1) at the same time. At times like this, the serial transfer clock (BCK) and sync pulse (LRCK) are commonly used for the two channels of data (at the same timing).

These serial PCM interfaces use the same pins as those used by the seven GPIO4 to GPIO7 and GPIO10 to GPIO12 general-purpose ports. When they are not used, these pins can be used as general-purpose ports. Table 8 shows the correspondence between the GPIO4 to GPIO7 and GPIO10 to GPIO12 general-purpose ports and serial PCM interfaces.

Table 8 Correspondence between general-purpose ports and serial PCM interfaces

When the Pins are Not Used		Serial PCM Interface	
GPIO4	I/O	LRCK0	I/O
GPIO5	I/O	BCK0	I/O
GPIO6	I/O	SOUT0	O
GPIO7	I/O	SIN0	I
GPIO10	I/O	SOUT1	O
GPIO11	I/O	SIN1	I
GPIO12	I/O	ACLK	O

The serial interface is selected by the host CPU with the setting command via the host CPU interface.

(1) Serial PCM Interface Master/Slave

(1-1) Master mode

When the serial PCM interfaces are in the master mode, the LC70310 generates the transfer clock (BCK0) and sync pulse (LRCK0). Output from the BCK0 pin as the transfer clock is a clock whose frequency is 32 times the sampling frequency (synchronization clock frequency). Output from the ACLK pin to the connection destination (slave device) is the master clock (whose frequency is equivalent to Fs*256).

Fig. 17 shows the connections in the master mode.

<<Diagram of connections in master mode>>

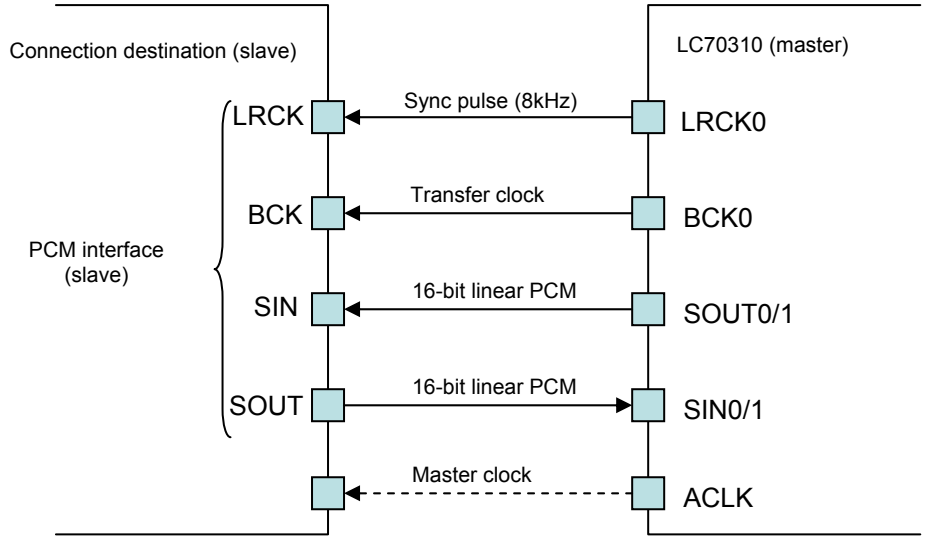


Figure 17

(1-2) Slave mode

When the serial PCM interfaces are in the slave mode, the LC70310 executes data transfer using the transfer clock (Fs*32) and sync pulse (Fs) from the connection destination (master device). Since the internal processing is executed using the DSP clock, it is not necessary to input ACLK from an external source.

Fig. 18 shows the connections in the slave mode.

<<Diagram of connection in slave mode connection diagram>>

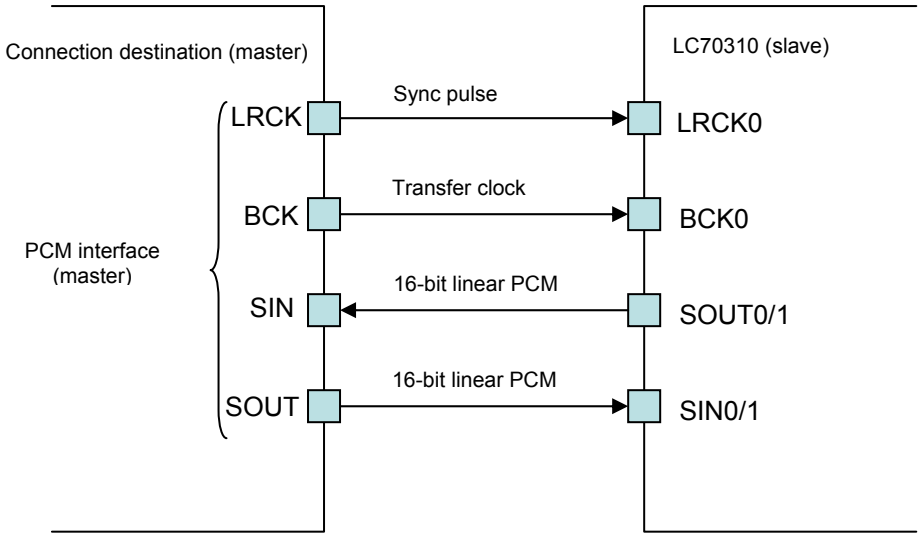


Figure 18

(2) Long Frame Synchronization Mode

In the long frame synchronization mode, the rising edge of the LRCK signal is the start of the serial PCM data. The transfer clock (BCK) polarity (rise synchronization or fall synchronization) can be selected. The transfer sequence (MSB first or LSB first) can also be selected.

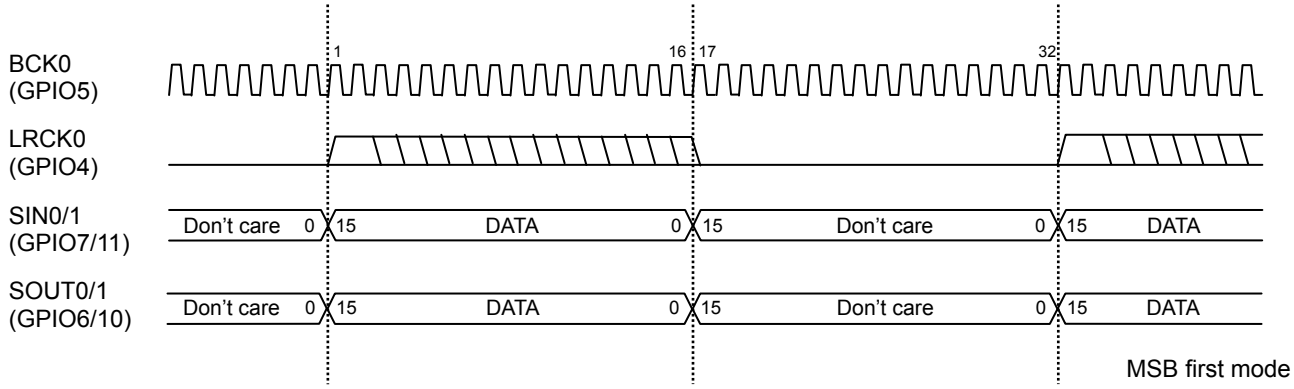


Figure 19

(3) Short Frame Synchronization Mode

In the short frame synchronization mode, the falling edge of the LRCK signal is the start of the serial PCM data. The pulse width of the LRCK signals must be equivalent to one period of the transfer clock (BCK). As in the long frame synchronization mode, the transfer clock (BCK) polarity (rise synchronization or fall synchronization) can be selected.

The transfer sequence (MSB first or LSB first) can also be selected.

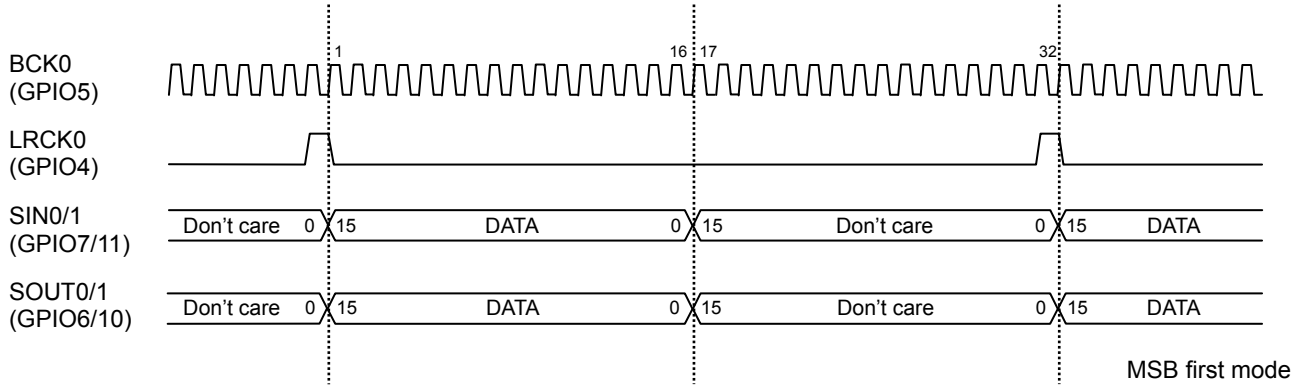


Figure 20

(4) I^2S Mode

In the I^2S mode, Lch (16 bits) and Rch (16 bits) transfer is possible during the sampling period. Serial PCM data transfer is synchronized with the falling edge of BCK. The start of the Lch and Rch data is one BCK period after the falling edge and rising edge of the LRCK signal, respectively. The data format is fixed at MSB first.

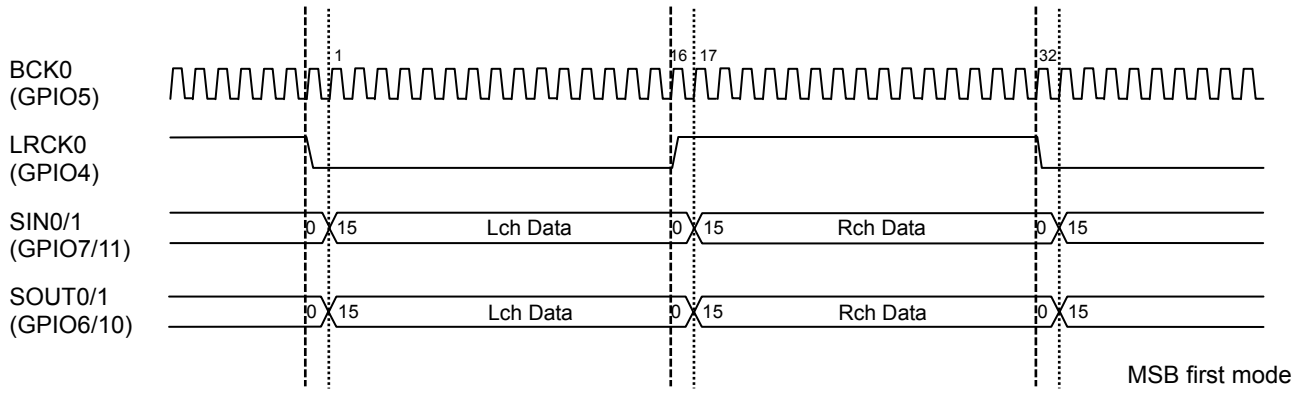


Figure 21

(5) Left Justified Mode

In the left justified mode, the Lch data starts at the rising edge of the LRCK signal, and the Rch data starts at the falling edge of the LRCK signal. The transfer clock (BCK) polarity (rise synchronization or fall synchronization) can be selected. The transfer sequence (MSB first or LSB first) can also be selected.

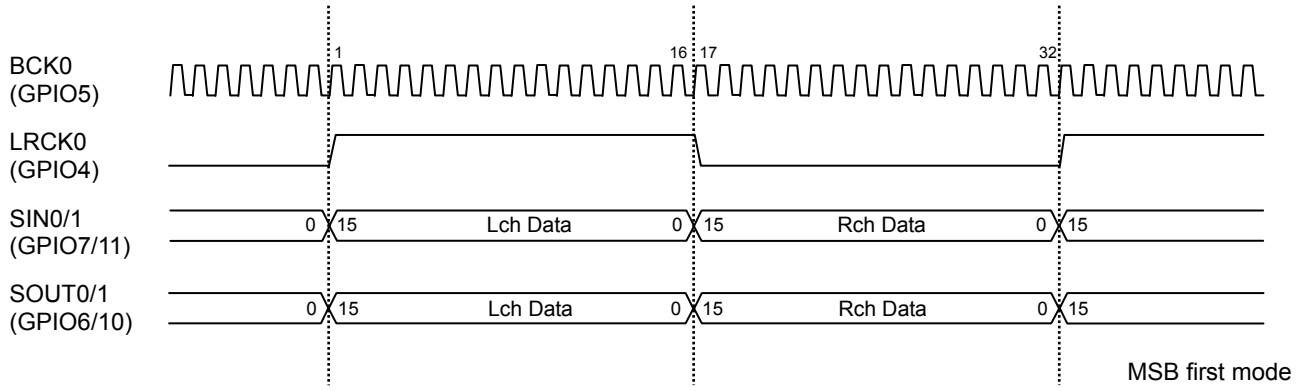


Figure 22

Standby and System Control

(1) Startup Sequence

When the power is turned on, the RESETB pin and PDN_PTT pin must be set to “L.” Oscillation starts immediately after power-on. After waiting for the oscillation to stabilize, the RESETB pin and PDN_PTT pin must be set to “H” to release the LC70310 reset. In approximately 8ms (*) after reset has been released, the boot program starts, and the downloading of the noise-cancelling program is started.

(*) This is the time taken when the frequency of the master clock is 8.192MHz.

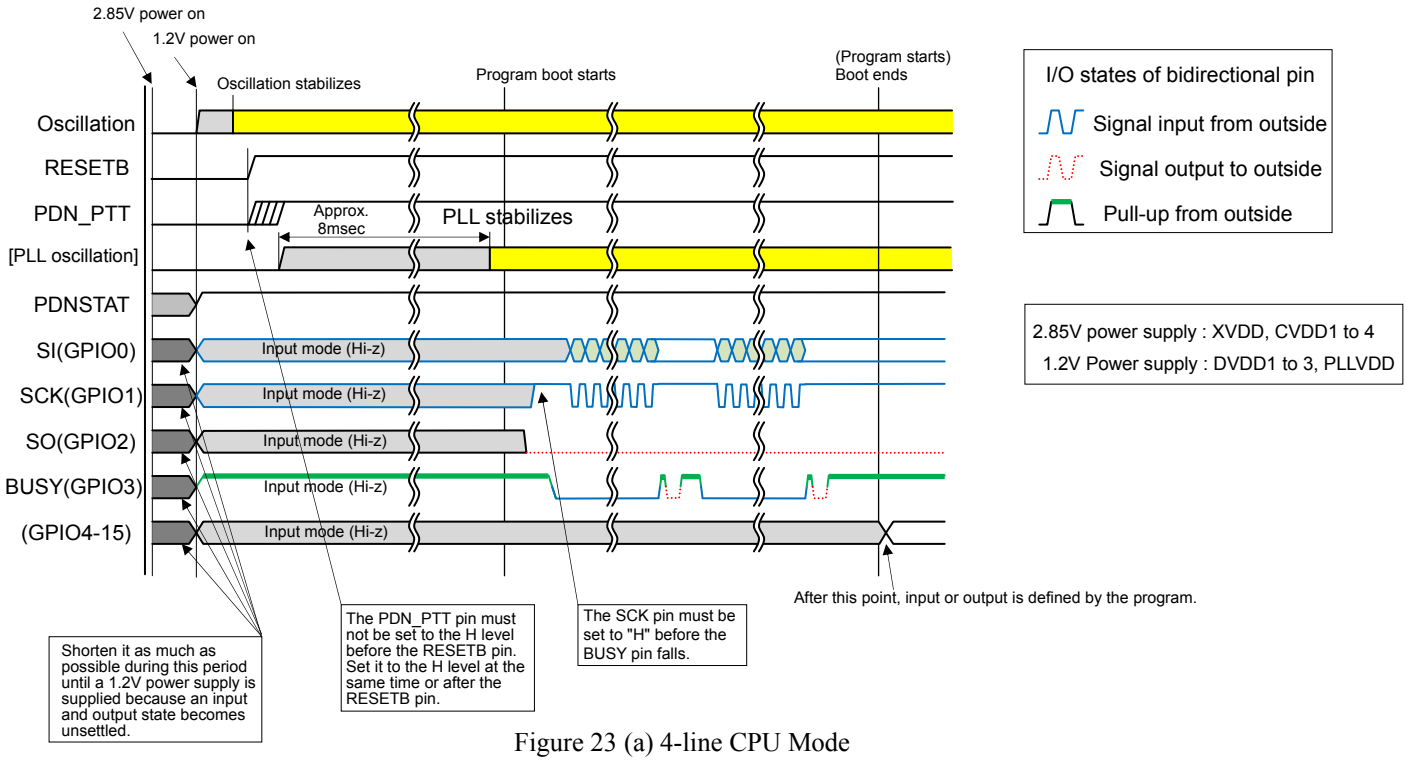


Figure 23 (a) 4-line CPU Mode

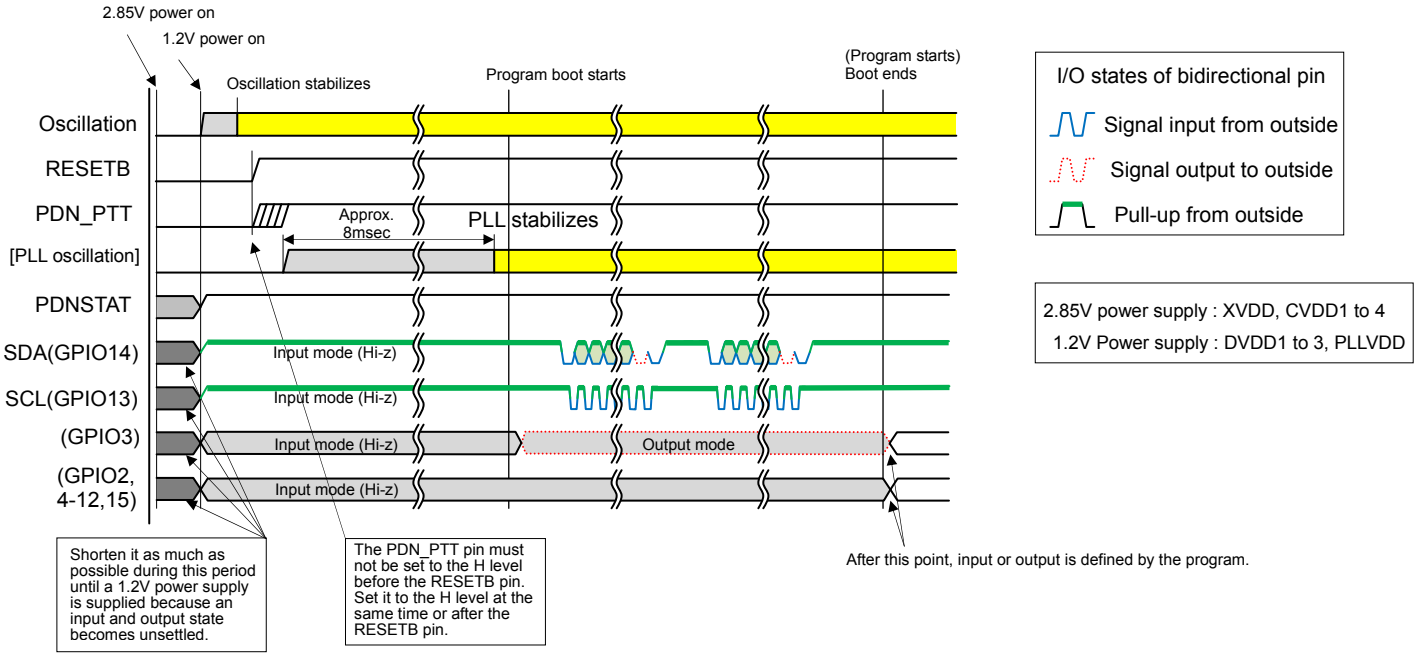


Figure 23 (b) I^2C Mode

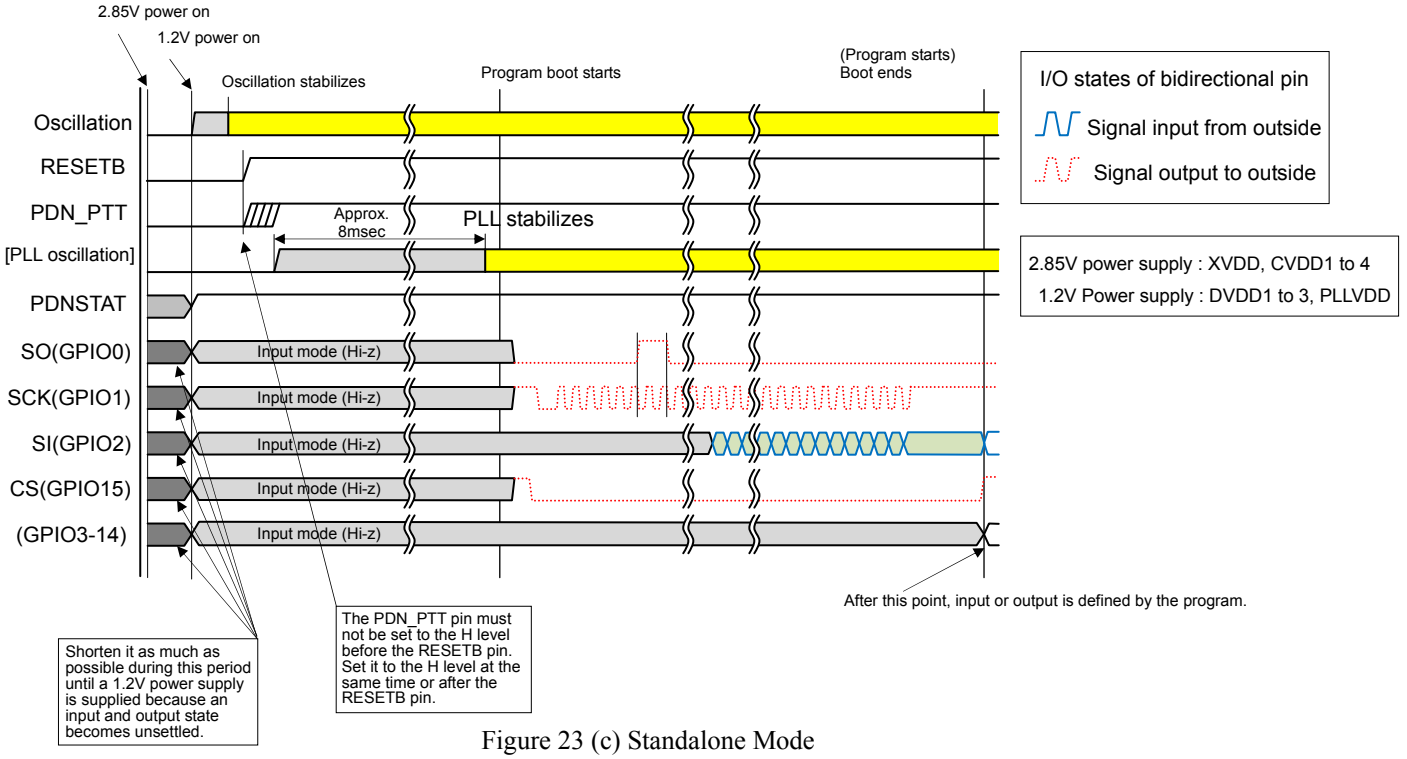


Figure 23 (c) Standalone Mode

(2) Standby Control

The LC70310 enables standby control using the PDN_PTT pin. When this pin is set to “L” during a noise-cancelling operation, the standby interrupt is generated in the internal DSP, and operation transfers to the standby set or release routine. This routine starts the processing for transfer to the standby mode, and after the internal statuses and pin settings have been set to the statuses (such as Hi_z) to be established during standby, all the clocks are stopped.

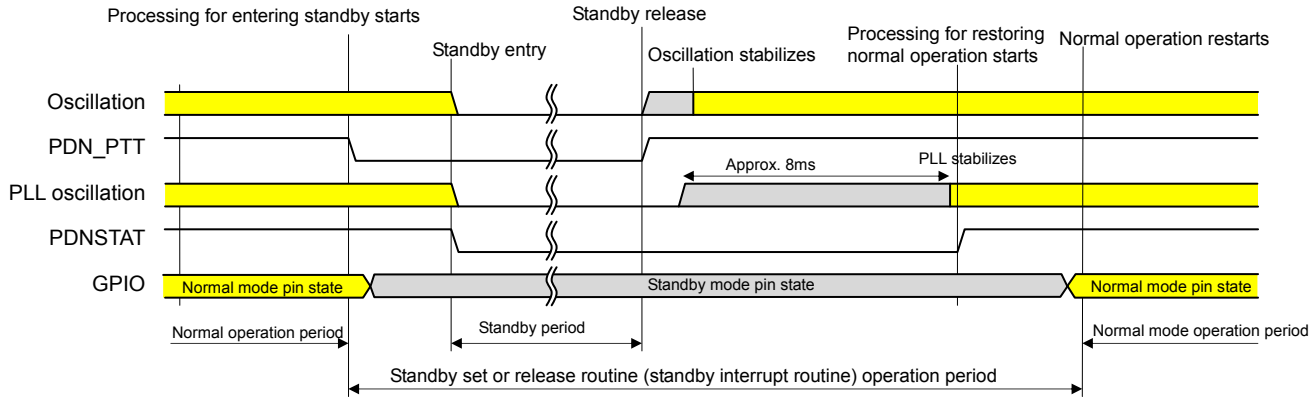
While the LC70310 is in the standby mode, the PDNSTAT pin is set to “L,” notifying the external devices that the LC70310 is in the standby mode.

Standby is released by setting the PDN_PTT pin to “H.” When this pin is set to “H,” the oscillation and PLL oscillation start, and after they have stabilized (in approx. 8ms (*)), the normal internal statuses and pin settings are restored by the standby set or release routine.

Normal operation is resumed when the standby set or release routine ends.

(*) This is the time taken when the frequency of the resonator is 8.192MHz.

(*) During a standby period, the terminal state of GPIO (input and output mode, level at the time of the listing) does not change.



Transfer to standby

1. Set the PDN_PTT pin to “L.”
2. Oscillation and PLL stop.

Standby release

1. Set the PDN_PTT pin to “H.”
2. Oscillation starts, and PLL starts.
3. About 8 ms later, the standby mode is released.

Figure 24

(3) Standby Control Immediately Before Program Downloading at Startup

In the CPU mode (4-line CPU boot or I^2C boot), the LC70310 can wait in the standby mode with oscillation stopped immediately before the program downloading operation after power-on.

When, after power-on, the PDN_PTT pin and RESETB pin are set to "H" and reset is released, about 8ms later the PLL oscillation stabilizes, and the program boot operation is started. Since, after the program boot operation has started, program downloading is started at the fall of the BUSY pin in the case of 4-line CPU boot and at the fall of the SDA pin in the case of I^2C boot, the standby mode is established by setting the PDN_PTT pin to "L" before the above operation.

The standby mode is released in approximately 8ms after the PDN_PTT pin has been set to "H" and the PLL oscillation is stabilized. (The PDNSTAT pin is set to "H.")

After standby release, program downloading is performed immediately, and the start operation ends.

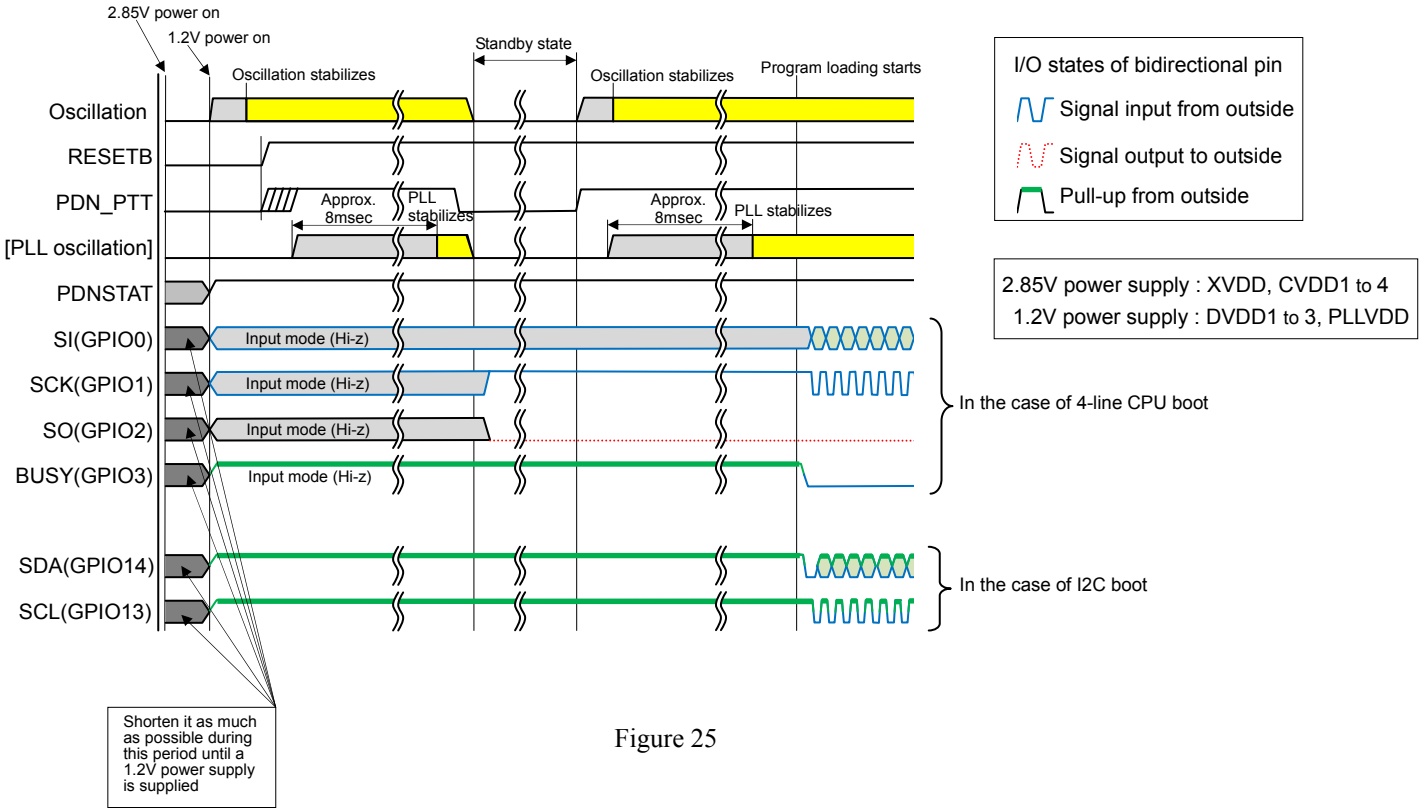


Figure 25

PLL for DSP

The LC70310 generates a high-speed clock for the DSP from the oscillation clock (8.192MHz) using the internal DSP PLL.

Figure 26 and Table 9 show the filter circuit for the PLL and its recommended values.

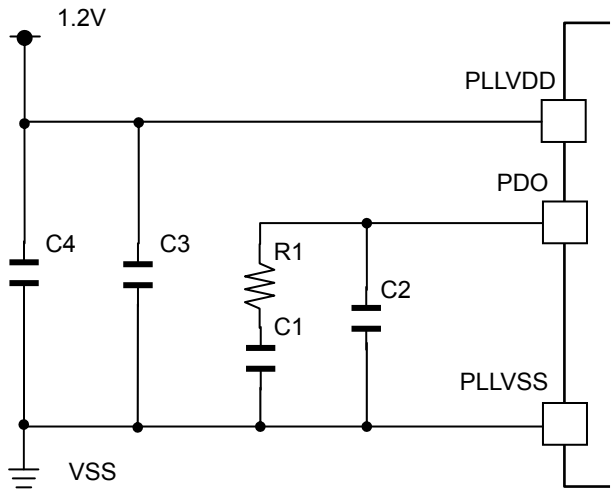


Figure 26 Example of DSP

Table 9 Recommended Filter Values for PLL

Symbol	Recommended Value	Remarks
R1	680Ω	±5%
C1	0.033μF	capacitance error: ±10% Temperature characteristics ±10%
C2	0.0033μF (C1*(1/10 to1/100))	
C3	0.1μF	
C4	10μF	

Notes

Bypass capacitors (recommended values: 0.1μF for C3 and 10μF for C4 connected in parallel) must be inserted in close proximity to the IC between the PLLVDD and PLLVSS power supplies.

The capacitances of C1 and C2 must stand in the following relationship: C2=C1*(1/10 to 1/100).

C2 is an additional capacitor which does not affect the intrinsic characteristics of the loop filter but which contributes to the PLL stability.

Oscillator Circuit

The system clock for the LC70310 is generated by connecting a resonator between the XIN and XOUT pins.
Figure 27 and Table 10 show the recommended circuit and its recommended values.

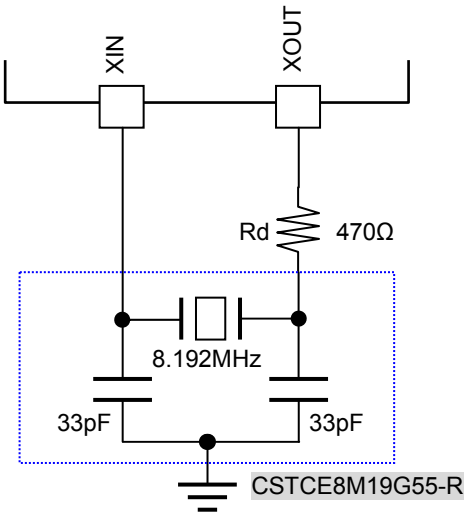


Figure 27 Recommended Circuit

Table 10 Recommended Circuit Constant Values

Oscillator Name	Vendor Name	Frequency (MHz)	Rd(Ω)
CSTCE8M19G55-R0	Murata	8.192MHz	470Ω

*) “CERALOCK®” made by Murata Manufacturing Co., Ltd.: Use of the CSTCE8M19G55-R0 is recommended.

Examples of Reference Circuits

(1) LC70310KBG reference circuit diagram (standalone mode)

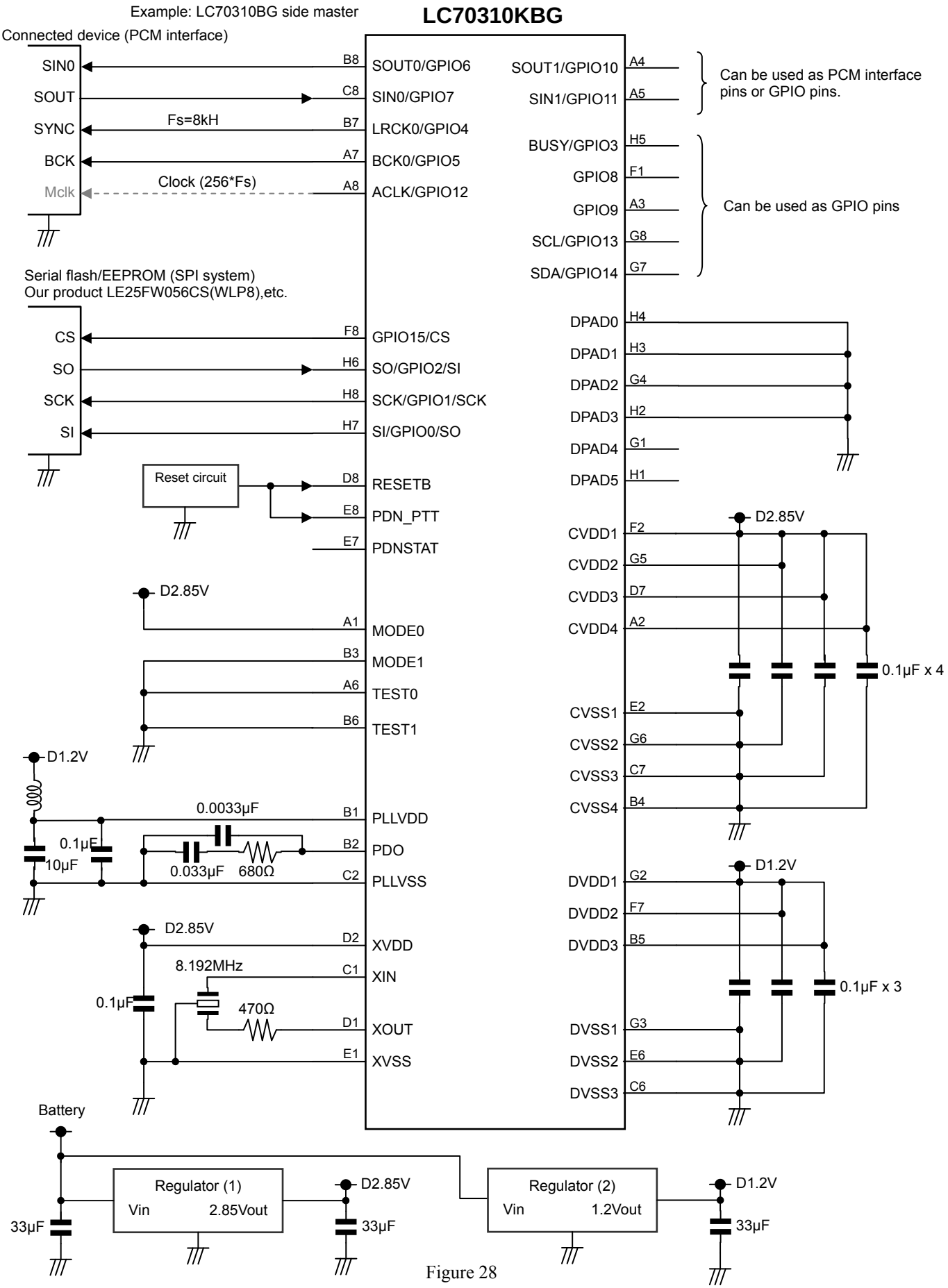


Figure 28

(2) LC70310KBG reference circuit diagram (CPU mode, 4-line system)

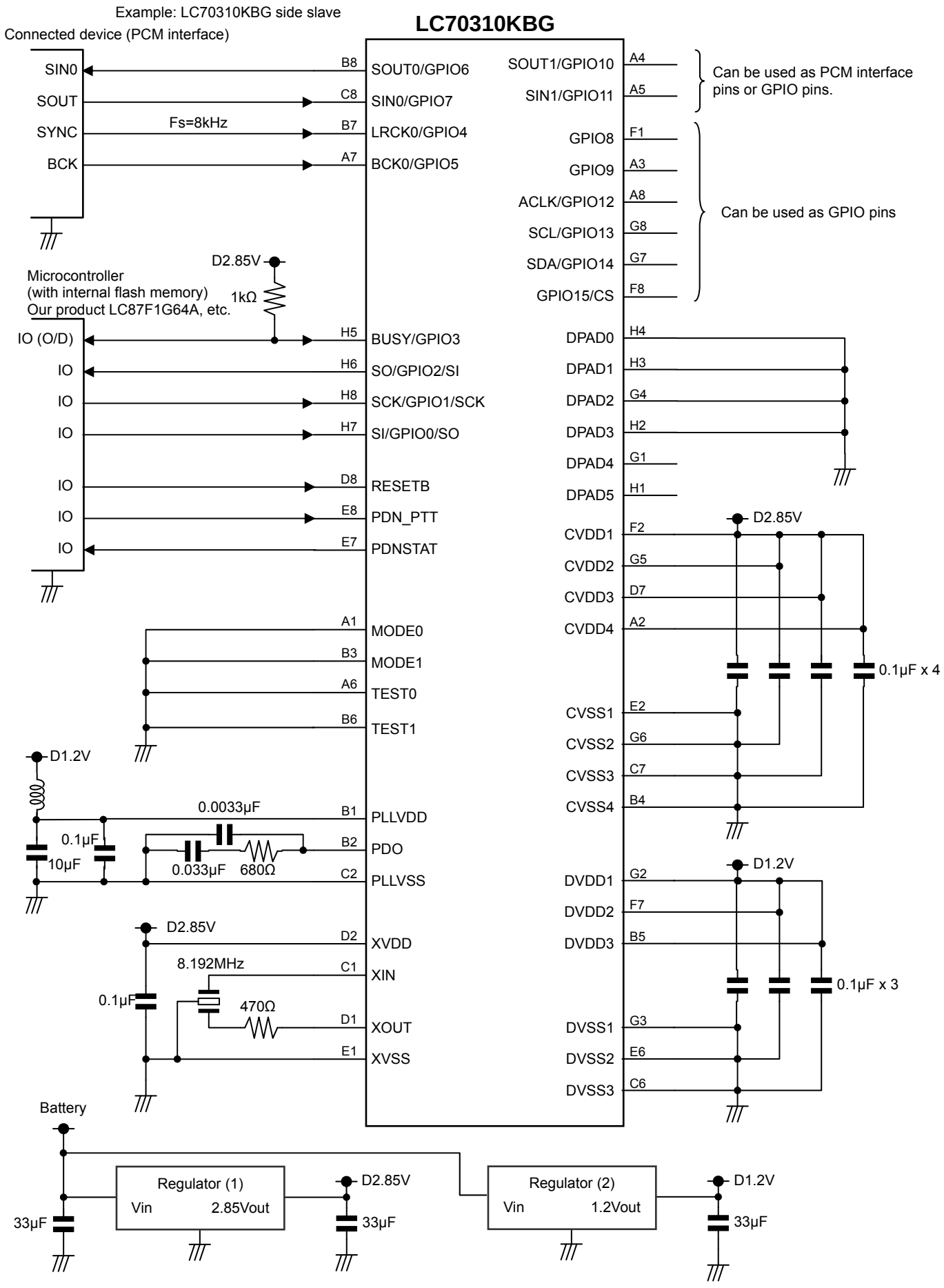


Figure 29

(3) LC70310BG reference circuit diagram (CPU mode, I^2C bus format)

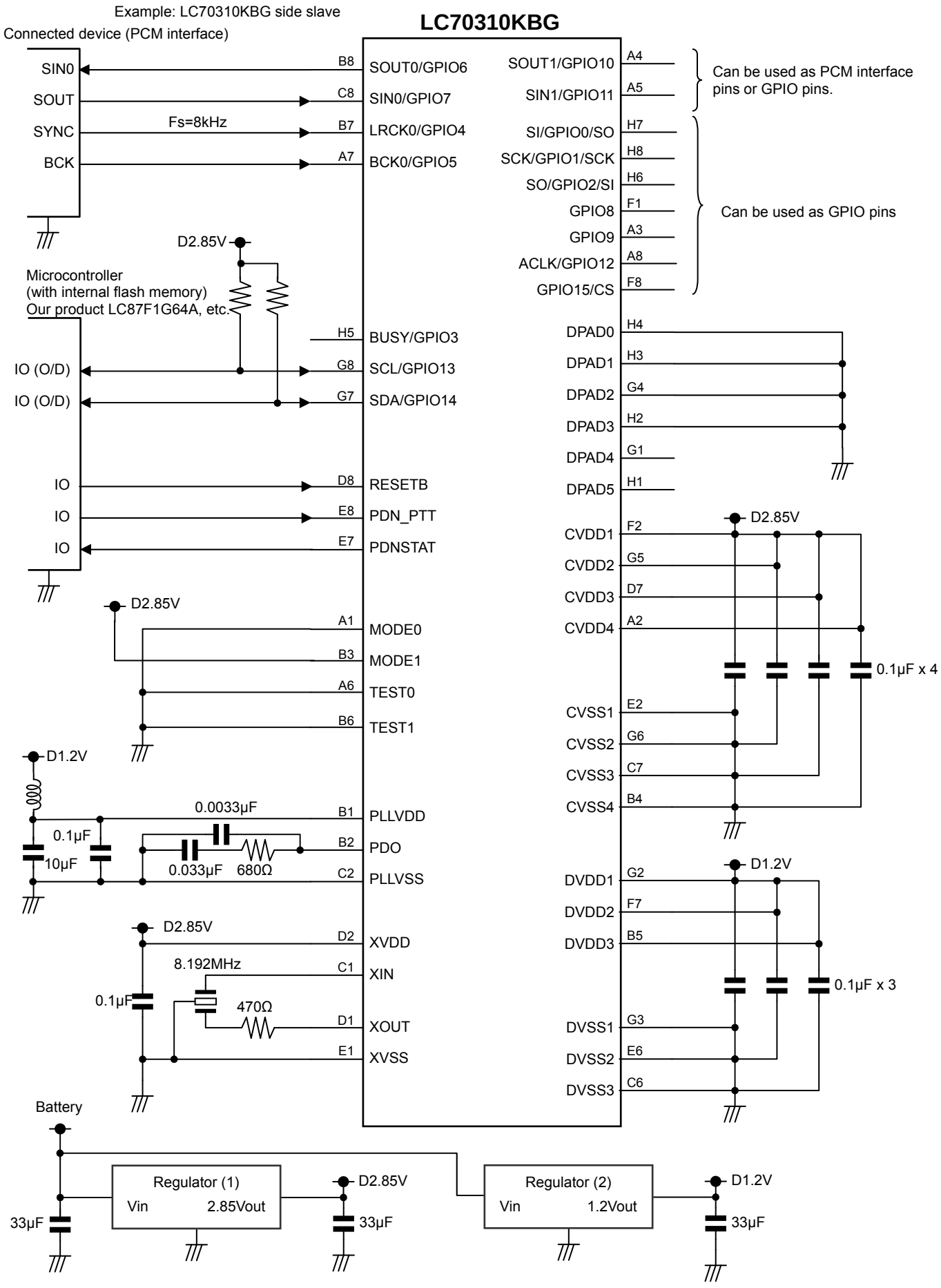


Figure 30

(4) Parts Lists

Table 11 Parts List for Standalone Mode

Block Name	Parts Name	Type	Quantity	Remarks
LC70310	LC70310	IC	1	Noise canceller IC
Memory (SPI type)	Flash	IC	1	SPI serial flash (LE25FW056CS)
Oscillator circuit	Resonator	OSC	1	8.192MHz (Ceralock or X'tal)
	Resistor	R	1	Resonator damping resistor
PLL filter	Resistor	R	1	Filter resistor
	Capacitor	C	2	Filter capacitor
Reset circuit	Reset IC or discrete parts	IC or R/C/diode	1	For power-on reset
Power supply circuit	Regulator	IC	2	Generates 2.85V and 1.2V.
	Capacitor	C	9	Decoupling capacitor (0.1μF)
	Capacitor	C	4	Smoothing capacitor (33μF, 10μF)
	Coil	L	1	Filter inductor (22μH)

Table 12 Parts List for CPU Mode

Block Name	Parts Name	Type	Quantity	Remarks
LC70310	LC70310	IC	1	Noise canceller IC
Microcontroller	Microcontroller	IC	1	Control microcomputer (LC87F1G64A)
Oscillator circuit	Resonator	OSC	1	8.192MHz (Ceralock or X'tal)
	Resistor	R	1	Resonator damping resistor
PLL filter	Resistor	R	1	Filter resistor
	Capacitor	C	2	Filter capacitor
Pull-up resistor	Resistor	R	1 or 2	Pull-up resistor
Power supply circuit	Regulator	IC	2	Generates 2.85V and 1.2V.
	Capacitor	C	9	Decoupling capacitor (0.1μF)
	Capacitor	C	4	Smoothing capacitor (33μF, 10μF)
	Coil	L	1	Filter inductor (22μH)

Timing

(1) CPU interface timing

(1-1) 4-line system CPU interface timing

The timing diagram and ratings for program loading using the 4-line system CPU interface are shown in Figure 31 and Table 13.

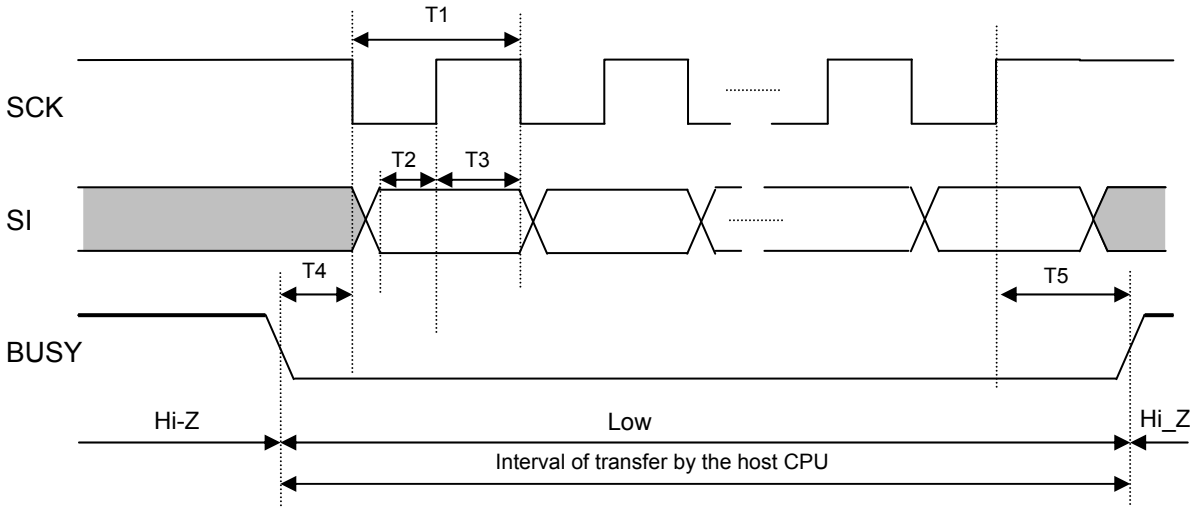


Figure 31

Table 13 4-line system CPU Interface Timing

Parameter	Symbol	min	typ	max	unit
SCK period	T1	1	–	–	μs
SI setup time	T2	0.1	–	–	μs
SI hold time	T3	0.1	–	–	μs
BUSY setup time	T4	0.4	–	–	μs
BUSY hold time	T5	1	–	–	μs

The program data is taken into the LC70310 on the rising edges of SCK.

(1-2) BUSY output timing

The output timing diagram and ratings for the BUSY signal are shown in Figure 32 and Table 14.

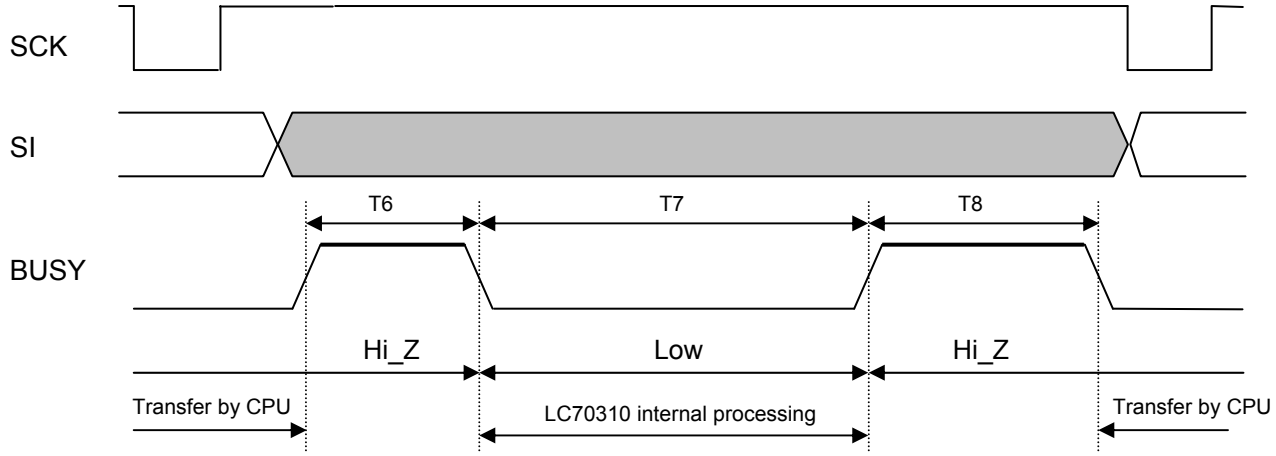


Figure 32

Table 14 BUSY Signal Output Timing

Parameter	Symbol	min	typ	max	unit
LC70310 internal processing setup time	T6	0.36	–	0.49	μs
LC70310 internal processing time	T7	2.4	–	3.5	μs
Host CPU access setup time	T8	0.49	–	–	μs

(1-3) I^2C bus interface timing

The timing diagram and ratings for the I2C bus interface are shown in Figure 33 and Table 15.

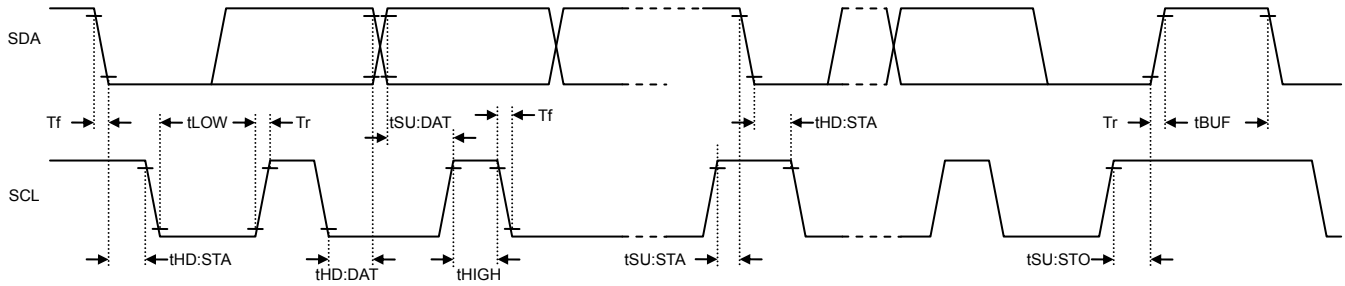


Figure 33

Table 15 I^2C Bus Interface Timing

Parameter	Symbol	Standard mode		Fast Mode		unit
		min	max.	min.	max.	
SCL frequency	fSCL	0	100	0	400	kHz
Hold time (repeat) START condition (The first clock pulse is generated after this time)	tHD:STA	4.0	–	0.6	–	μs
SCL “L” period	tLOW	4.7	–	1.3	–	μs
SCL “H” period	tHIGH	4.0	–	0.6	–	μs
Repeat START condition setup time	tSU:STA	4.7	–	0.6	–	μs
Data hold time	tHD:DAT	0	3.45	0	0.9	μs
Data setup time	tSU:DAT	250	–	100	–	ns
SDA and SCL signal rise time	Tr	–	1000	–	300	ns
SDA and SCL signal fall time	Tf	–	300	–	300	ns
STOP condition setup time	tSU:STO	4.0	–	0.6	–	μs
Bus free time between the STOP and START conditions	tBUF	4.7	–	1.3	–	μs

(1-4) Serial flash access timing (SPI mode)

The timing diagram and ratings for accessing serial flash memory in the standalone mode are shown in Figure 34 and Table 16.

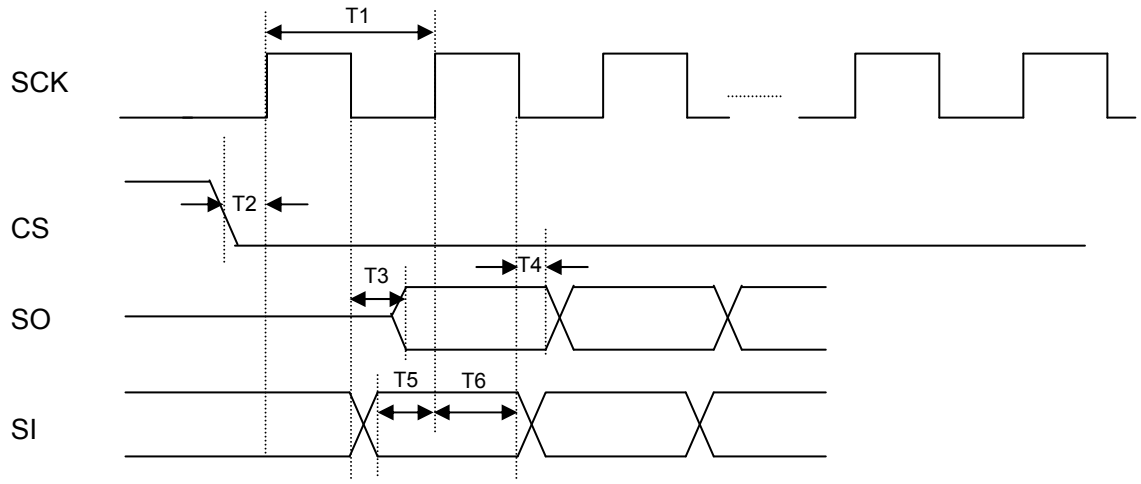


Figure 34

Table 16 Serial Flash Memory Access Timing

Parameter	Symbol	min	typ	max	unit
SCK period	T1	1	–	–	μs
CS setup time	T2	0.4	–	–	μs
SO delay time	T3	–	–	0.4	μs
SO hold time	T4	0	–	0.4	μs
SI setup time	T5	0.1	–	–	μs
SI hold time	T6	0.1	–	–	μs

(2) PCM interface timing

(2-1) Long frame/short frame synchronization mode (master) timing

(2-1-a) Long frame synchronization mode

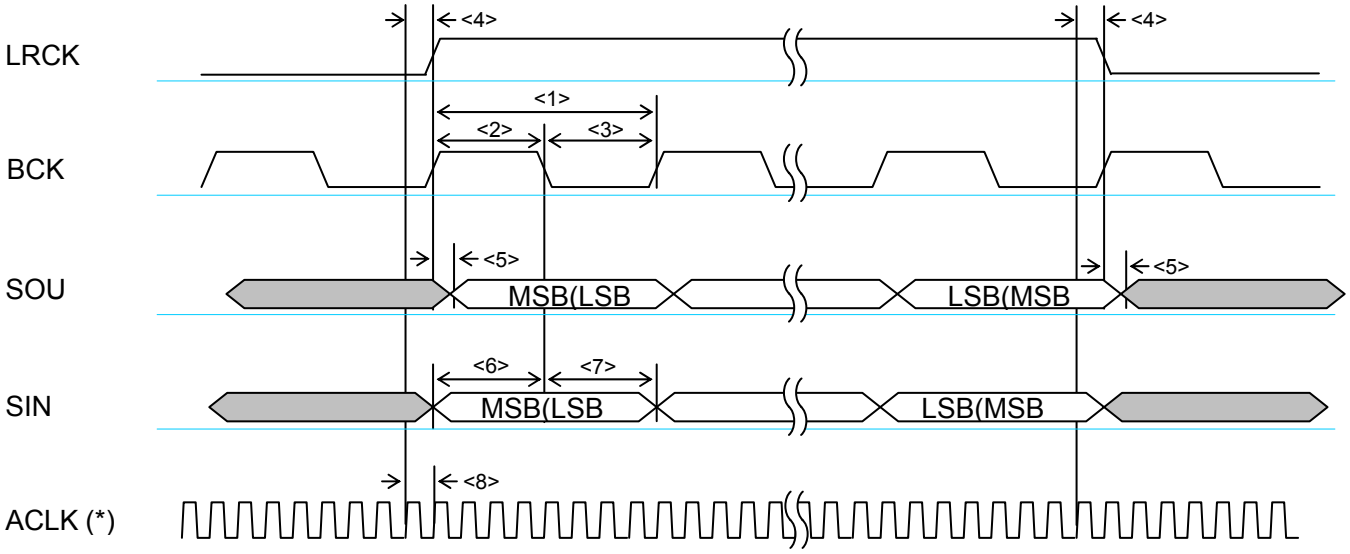


Figure 35

(2-1-b) Short frame synchronization mode

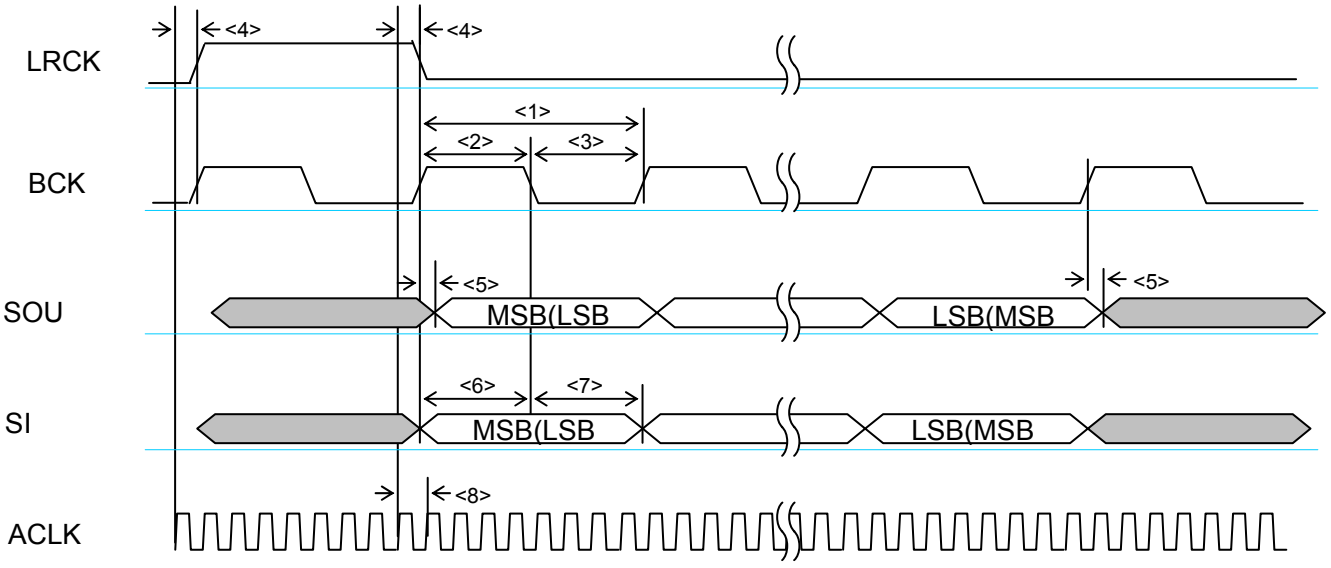


Figure 36

*) The master clock (with a frequency equivalent to Fs · 256 times) is output from the ACLK pin to the connection destination.

Table 17 Long Frame/Short Frame Synchronization Mode (Master) Timing

Symbol	Parameter	min	typ	max	unit
–	LRCK frequency (Fs)		8		kHz
<1>	PCM clock : BCK frequency (32Fs)		256		kHz
<2>	PCM clock: BCK “H” time		1/64Fs		s
<3>	PCM clock: BCK “L” time		1/64Fs		s
<4>	LRCK/BCL output delay time			40	ns
<5>	SOUT output delay time			250	ns
<6>	SIN input setup time	250			ns
<7>	SIN input hold time	250			ns
<8>	Master clock: ACLK output frequency (256Fs)		2048		kHz

This is the timing when the DSP clock operates at 20MHz or higher.

(2-2) Long frame/short frame synchronization mode (slave) timing

(2-2-a) Long frame synchronization mode

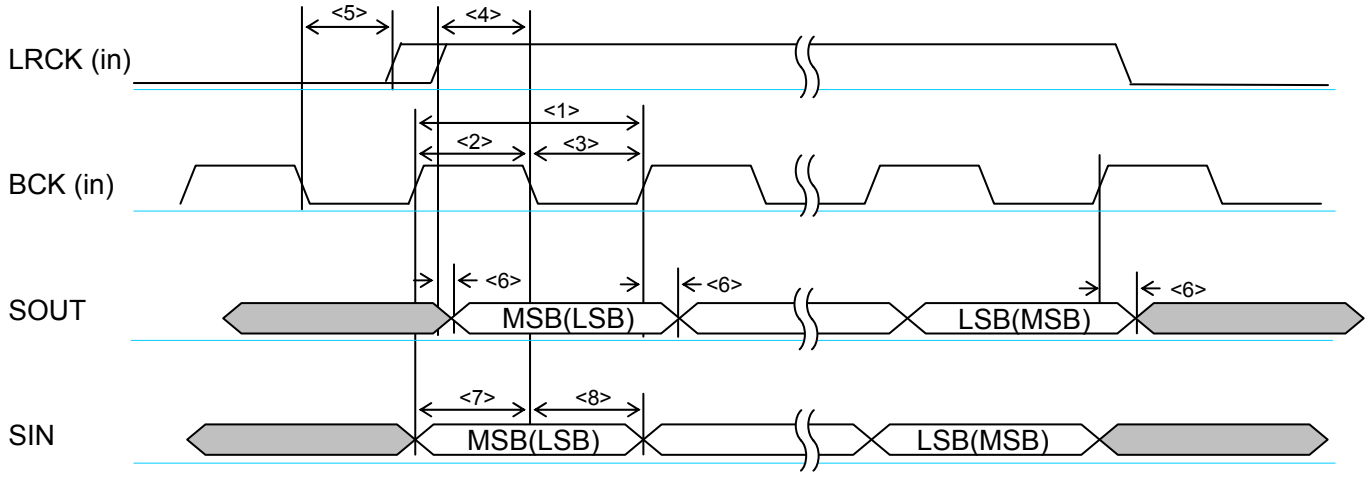


Figure 37

(2-2-b) Short frame synchronization mode

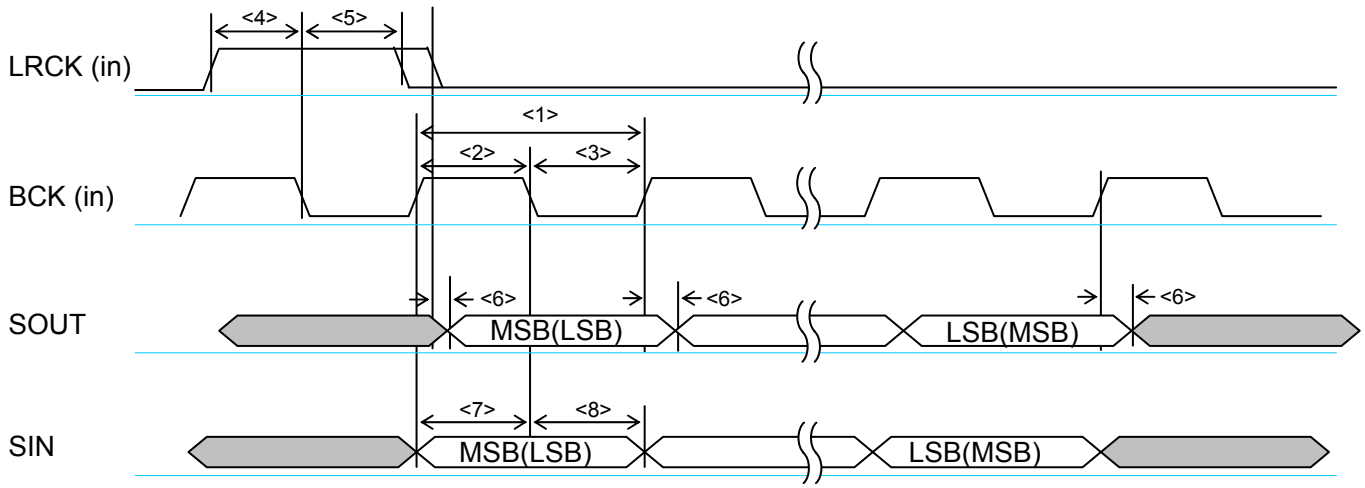


Figure 38

Table 18 Long Frame/Short Frame Synchronization Mode (Slave) Timing

Symbol	Parameter	min	typ	Max	unit
–	LRCK frequency (Fs)		8		kHz
<1>	PCM clock: BCK frequency (32Fs)		256		kHz
<2>	PCM clock: BCK “H” time		1/64Fs		s
<3>	PCM clock: BCK “L” time		1/64Fs		s
<4>	LRCK setup time	250			ns
<5>	LRCK hold time	250			ns
<6>	SOUT output delay time			250	ns
<7>	SIN input setup time	250			ns
<8>	SIN input hold time	250			ns

This is the timing when the DSP clock operates at 20MHz or higher.

(2-3) I^2S mode (master) timing

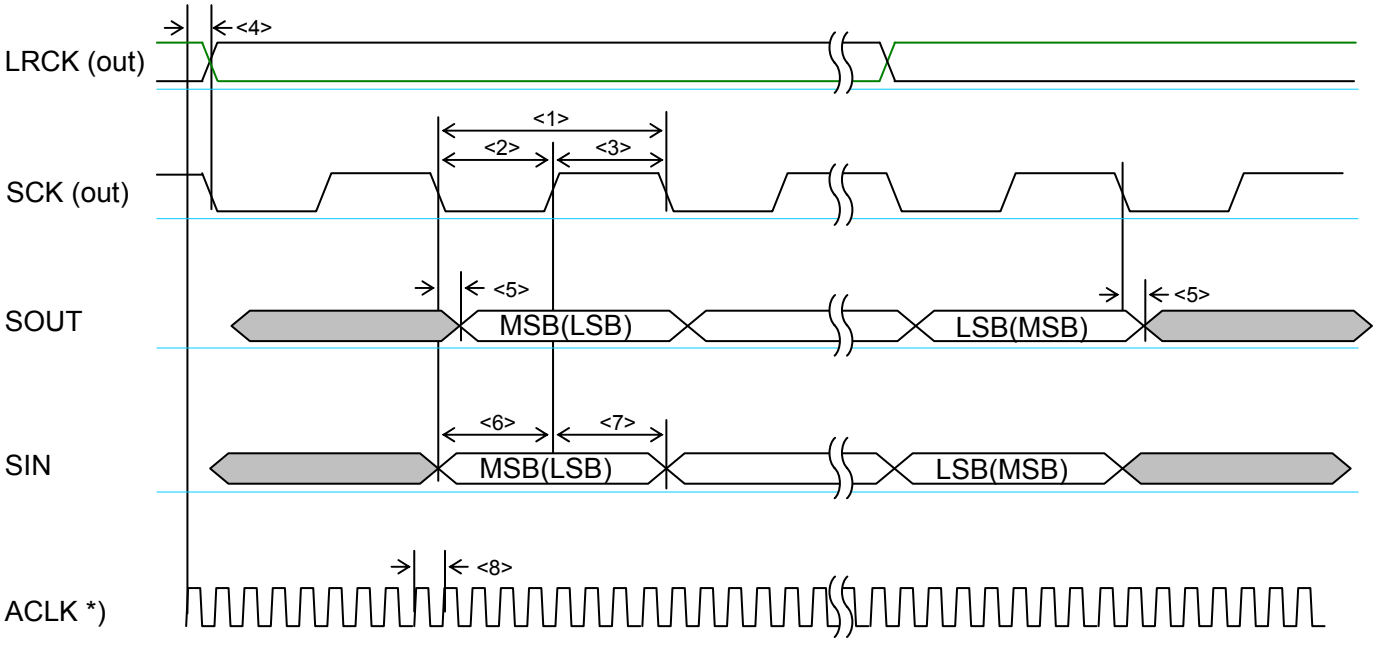


Figure 39

*) The master clock (with a frequency equivalent to Fs · 256 times) is output from the ACLK pin to the connection destination.

Table 19 I^2S Mode (Master) Timing

Symbol	Parameter	min	typ	max	unit
–	LRCK frequency (Fs)		8		kHz
<1>	PCM clock: BCK frequency (32Fs)		256		kHz
<2>	PCM clock: BCK “H” time		1/64Fs		s
<3>	PCM clock: BCK “L” time		1/64Fs		s
<4>	LRCK output delay time			40	ns
<5>	SOUT output delay time			250	ns
<6>	SIN input setup time	250			ns
<7>	SIN input hold time	250			ns
<8>	Master clock: ACLK output frequency (256Fs)		2048		kHz

(2-4) I^2S mode (slave) timing

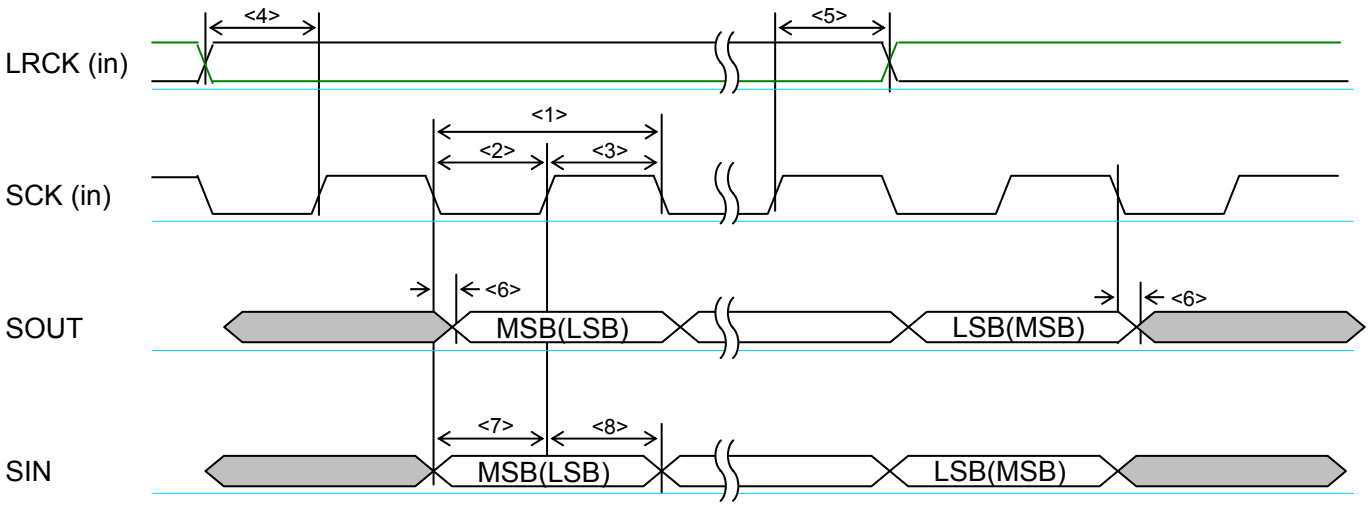


Figure 40

Table 20 I^2S Mode (Slave) Timing

Symbol	Parameter	min	typ	max	unit
–	LRCK frequency (Fs)		8		kHz
<1>	PCM clock: BCK frequency (32Fs)		256		kHz
<2>	PCM clock: BCK “H” time		1/64Fs		s
<3>	PCM clock: BCK “L” time		1/64Fs		s
<4>	LRCK setup time	250			ns
<5>	LRCK hold time	250			ns
<6>	SOUT output delay time			250	ns
<7>	SIN input setup time	250			ns
<8>	SIN input hold time	250			ns

(2-5) Left justified mode (master) timing

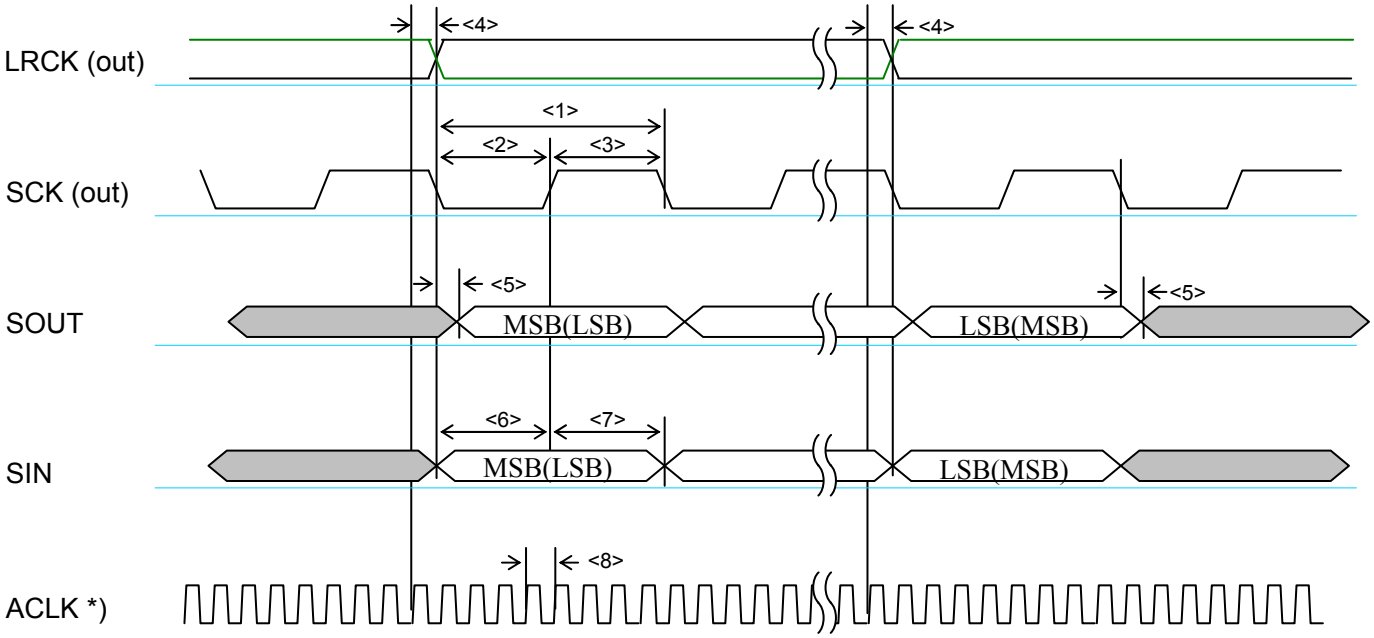


Figure 41

*) The master clock (with a frequency equivalent to Fs · 256 times) is output from the ACLK pin to the connection destination.

Table 21 Left justified Mode (Master) Timing

Symbol	Parameter	min	typ	max	unit
–	LRCK frequency (Fs)		8		kHz
<1>	PCM clock: BCK frequency (32Fs)		256		kHz
<2>	PCM clock: BCK ”H” time		1/64Fs		s
<3>	PCM clock: BCK ”L” time		1/64Fs		s
<4>	LRCK output delay time			40	ns
<5>	SOUT output delay time			250	ns
<6>	SIN input setup time	250			ns
<7>	SIN input hold time	250			ns
<8>	Master clock: ACLK output frequency (256Fs)		2048		kHz

(2-6) Left justified mode (slave) timing

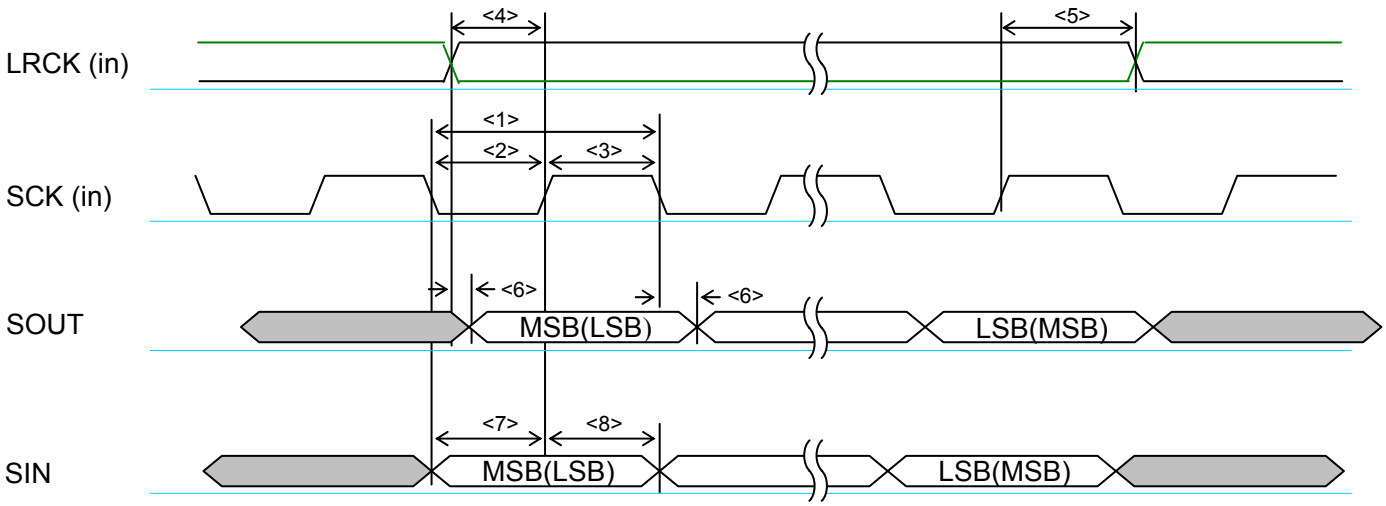


Figure 42

Table 22 Left Justified Mode (Slave) Timing

Symbol	Parameter	min	typ	max	unit
–	LRCK frequency (Fs)		8		kHz
<1>	PCM clock: BCK frequency (32Fs)		256		kHz
<2>	PCM clock: BCK “H” time		1/64Fs		s
<3>	PCM clock: BCK “L” time		1/64Fs		s
<4>	LRCK setup time	250			ns
<5>	LRCK hold time	250			ns
<6>	SOUT output delay time			250	ns
<7>	SIN input setup time	250			ns
<8>	SIN input hold time	250			ns

Notes on Designing

In order to achieve reliability as a total system , it goes without saying that not only must the absolute maximum ratings and allowable operation ranges (recommended operating conditions) of this IC be strictly observed, but that also the ambient temperature, static and other prevailing conditions in the operating environment as well as the mounting conditions be taken into consideration. This section describes some notes to be observed on design and IC mounting.

(1) Handling of Unused Pins

<1> Input pins which are not being used must be connected to GND (0V) without fail.

<2> Output pins which are not being used must be left open (unconnected).

<3> Input/output pins which are not being used must be set to input and connected to GND (0V) or they must be connected to the I/O power supply pins or set to output and left open.

(2) Latch-up Prevention

<1> The voltages supplied to the power supply pins of this IC must stand in the following relationship:

XVDD ≥ CVDD1-4, DVDD1-3 ≥ PLLVDD.

<2> Since latch-up may occur if the power supply rise timing of the power supply pins is off, ensure that there is no time difference in this timing.

<3> Ensure that the voltage levels of the pins are in compliance with the absolute maximum ratings and allowable operation ranges at power-on as well.

<4> Ensure that no excessive voltages or abnormal noise is applied to the IC.

<5> The outputs must not be shorted.

(3) Interface Notes

When the inputs and outputs of different devices are connected, malfunctions may occur if the input VIL/VIH levels do not match the corresponding output VOL / VOH levels. Level shifters must be inserted to prevent destruction of the devices if devices with differing supply voltages are connected.

(4) Load Capacitance and Output Current

<1> When connected to high capacitance loads, lines may be melted since the effect of such loads is the same as the load being shorted for an extended period. Also, high charge/discharge currents may result in noise that may degrade equipment performance and cause malfunctions. The recommended load capacitance ratings must be observed.

<2> Excessive output sink or source currents can cause similar problems. Observe the maximum allowable power dissipation ratings and use this IC within the recommended current value range.

(5) Notes on Power Application and Reset

<1> There are cases where special care is required at power-on, during a reset, and after a reset is released. Implement design taking these concerns into account.

<2> This IC's output pin states, I/O settings, register values, etc., are undefined when power is first applied. The operation of items that are defined by a reset operation or mode settings is only guaranteed only after the corresponding reset or setting operation. A reset must be applied to the IC after power is first applied. Also the state of the undefined pin or register values may change from the initial design statuses and, as such, caution is required.

<3> At power-on, the RESETB pin and PDN_PTT pin must be set to "L" for a period of time longer than the time taken for the oscillation of the resonator used to stabilize. The PDN_PTT pin must be set to "H" after the RESETB pin has been set to "H."

<4> The general-purpose input/output pins function as input pins when the IC is reset. If necessary, perform pull-up or pull-down processing to ensure that the pins are not undefined (Hi_z).

<5> Because it does not arrive at the inside, after 2.85V power supply activation, as for the reset input, the state of the terminal becomes unsettled during until the injection of the 1.2V power supply. Because input / output mode is not decided, during this period particularly the interactive terminal (GPIO) consider influence on outside circuitry. In addition, after 2.85V power supply activation, shorten it as much as possible for the time to injection of the 1.2V power supply.

(6) Notes on Thermal Design

The failure rate of semiconductor devices is accelerated significantly by increase in ambient temperature and power consumption. To assure high reliability, design the application heat dissipation system to provide adequate margin for variations in ambient conditions.

(7) Notes on PCB Pattern Design

<1> Ideally, there should be separate VDD and ground lines for each system to reduce the influence of common impedance.

<2> The VDD and ground lines should be as thick and as short as possible, and the impedance to high frequencies should be as small as possible. Ideally, decoupling capacitors (0.01 to 1μF) should be inserted between each VDD and ground line. Capacitors must be located as close to the power supply pins as possible.

It is also appropriate to insert a capacitor with a capacitance level of 10 to 47μF or so between each VDD and GND line to serve as low-frequency filters.

<3> Errors in operation are caused when noise is generated in the CPU interface and PCM interface. Generally , short connections are used for the interface lines to reduce the inductance and capacitance. However, attention must be paid to crosstalk.

When interface lines are long and when there are high levels of extraneous noise, inserting damping resistors or other noise-cancelling circuits is effective. Design filters that take the timing of the interfaces into consideration.

<4> Surround the resonator with GND patterns.

(8) Notes on Software Design

<1> If the documentation contains any prohibitions or recommendations applied when software is designed, they must be strictly observed.

(9) Other checkpoints

If there are any points that are unclear or if you have any questions, contact our sales representative during the design phase.

This IC is an application specific integrated circuit (IC) for noise cancellation applications, and has specifications that differ from those of general-purpose logic devices.

Package Dimensions

unit : mm

[LC70310KBG]

LFBGA64 5x5 / FBGA64K
CASE 566DE
ISSUE O

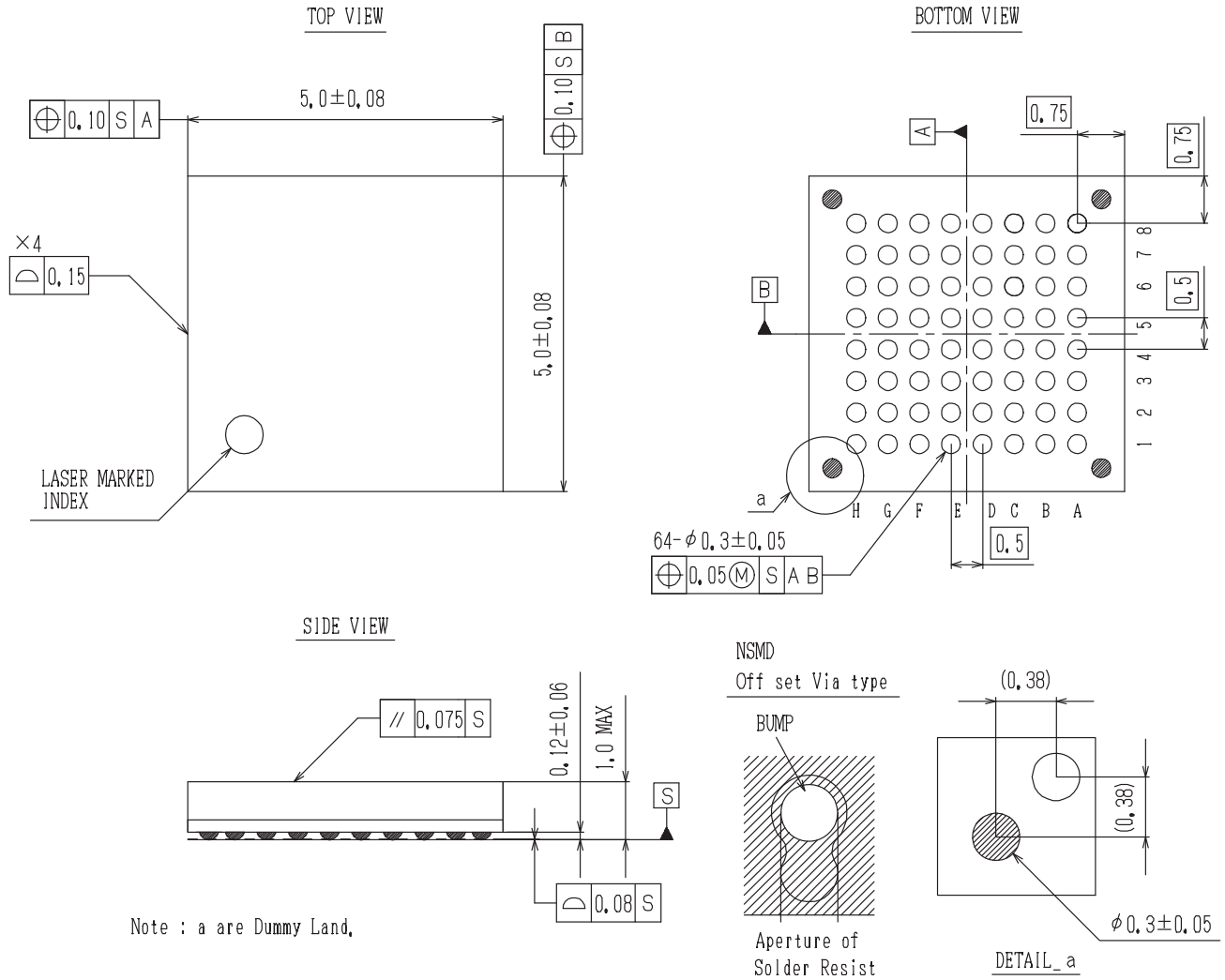


Figure 43 LC70310KBG [FBGA64K (5mm × 5mm)]

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC70310KBG-TLM-H	FBGA64K (Pb-Free / Halogen Free)	2000 / Tape & Reel