Ordering number : ENN7236

CMOS LSI

LC708728V

High-Performance 24-Bit 192 kHz D/A Converter Features Built-in Electronic Volume Control and DSD Support

www.DataSheet4U.com

Overview

The LC708728V is a high-performance stereo D/A converter developed for high-end audio applications such as DVD systems, home theater systems, and digital TV sets. It supports 16 to 32-bit word length PCM data as its digital input format, and supports sampling rates up to 192 kHz. It can also be used in a DSD (Direct Stream Digital) compatible mode by supplying a 64-bit stream for each input channel.

This IC is formed from serial interface port, digital interpolation filter, multi-bit ∑Δ converter, and stereo D/A converter functions. It includes muting and attenuator circuits that can be controlled individually for each channel.

The operating mode can be selected to be either software control mode or hardware control mode. In software control mode, the IC can be controlled by a microcontroller over a 2-wire or 3-wire serial port. In this mode, a wide range of functions, including muting, attenuation, and phase inversion can be controlled.

DSD mode can only be used in hardware control mode.

This IC is optimal for use as an interface for AC-3, DTS, and MPEG audio decoders for surround control, and for use in DVD players that support DVD-A.

Features

- Stereo D/A converter that supports both 24-bit PCM and 1-bit DSD
- Signal-to-noise ratio: 106 dB (48 kHz, A weighted)
- Total harmonic distortion: –97 dB
- D/A converter sampling frequency: 8 kHz to 192 kHz
- Control modes: Either software or hardware mode can be selected.
- Built-in microprocessor interface (either 2-wire or 3-wire)
- Input data formats
  I²S, left/right justified, DSP
  16, 20, 24, and 32 bits
- Built-in electronic volume control with independent left and right channel controls
  0 to 127.5 dB in 0.5 dB steps
- Operating voltage range: 3.0 to 5.5 V
- Package: 20-pin SSOP

Applications

- DVD audio and DVD “universal” players
- Home theater systems
- Digital TVs
- Digital broadcast receivers

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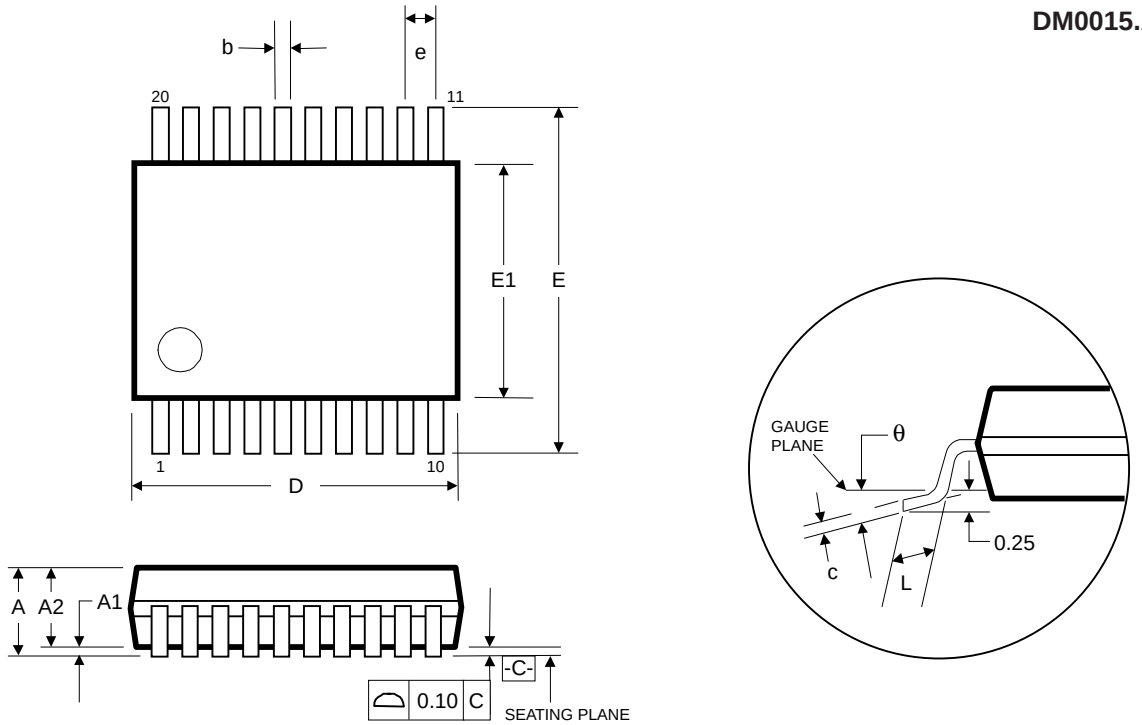
Package Dimensions

unit: mm

20-pin SSOP

[LC708728V]

DM0015.A

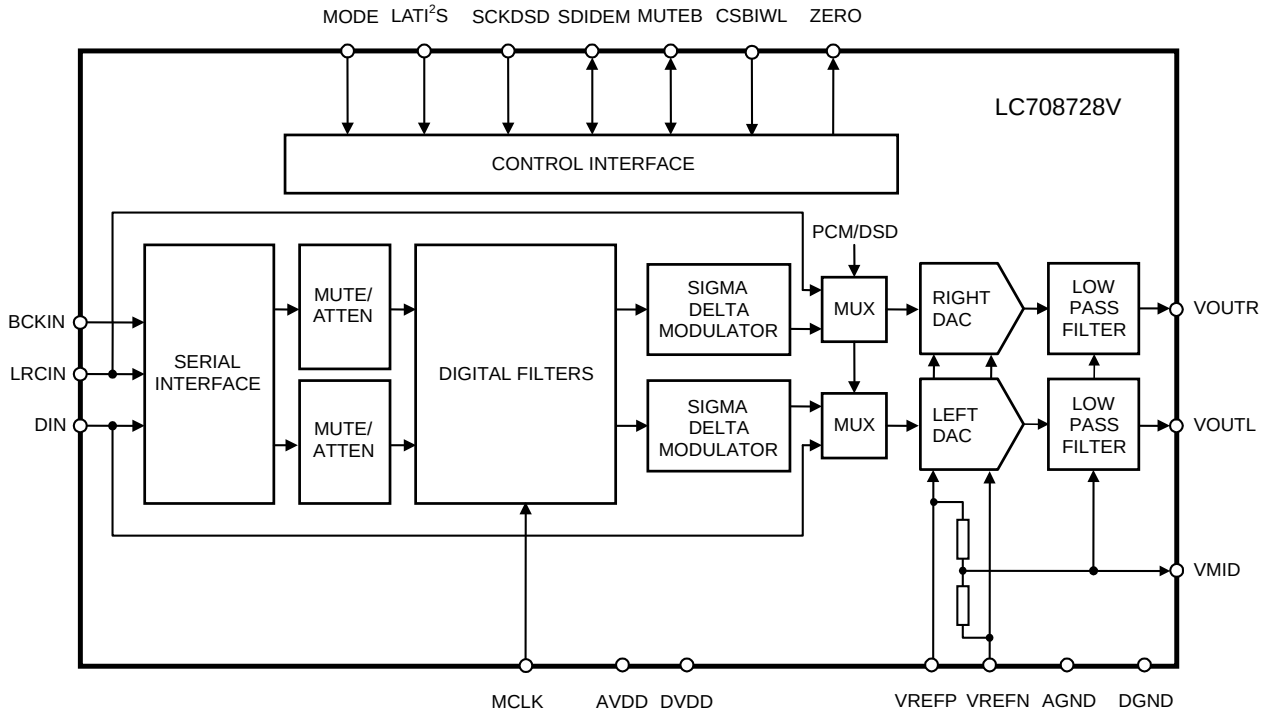


SANYO: 20-pin SSOP

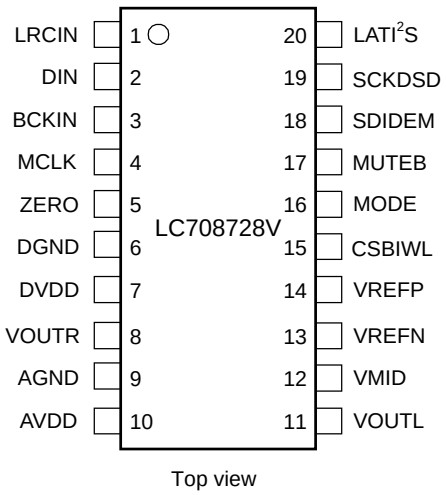
Symbols	Dimendions (mm)		
	MIN	NOM	MAX
A	——	——	2.0
A_1	0.05	——	——
A_2	1.65	1.75	1.85
b	0.22	——	0.38
c	0.09	——	0.25
D	6.90	7.20	7.50
e	0.65 BSC		
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
θ	0°	4°	8°
REF:	JEDEC.95, MO-150		

Notes: A. Linear dimensions are all stated in mm.
B. This figure is subject to change without notification.
C. The body dimensions do not include burrs and protrusions of up to 0.20 mm.
D. Complies with JEDEC.95 MO-150, VARIATION=AE. Further details are provided in these specifications.

Block Diagram



Pin Assignment



Top view

Pin Functions

Pin No.	Pin	Type	Function
1	LRCIN	Digital input	D/A converter sampling rate clock input: PCM input mode Right channel DSD bit stream input: DSD input mode
2	DIN	Digital input	Serial audio data input: PCM input mode Left channel DSD bit stream input: DSD input mode
3	BCKIN	Digital input	Audio data bit clock input
4	MCLK	Digital input	Master clock input
5	ZERO	Digital output (open drain)	IZD detection flag
6	DGND	Power supply	Digital GND
7	DVDD	Power supply	Digital V_{DD}
8	VOUTR	Analog output	Right channel D/A converter output
9	AGND	Power supply	Analog GND
10	AVDD	Power supply	Analog V_{DD}
11	VOUTL	Analog output	Left channel D/A converter output
12	VMID	Analog output	Mid-rail decoupling point
13	VREFN	Power supply	D/A converter n-channel VREF pin. Connect this pin to AGND. (Do not supply a level lower than AGND to this pin.)
14	VREFP	Power supply	D/A converter p-channel VREF pin. Connect this pin to AV_{DD}. (Do not supply a level lower than AV_{DD} to this pin.)
15	CSBIWL	Digital input (pulled up)	Software mode: 3-wire serial control chip select Hardware mode: Input word length
16	MODE	Digital input (pulled down)	Control mode selection (Low: hardware, high: software)
17	MUTEB	Bidirectional digital	Muting control (Low: muting on, high: muting off, high impedance (Z) : enable auto-muting)
18	SDIDEM	Bidirectional digital	Software mode: 3-wire or 2-wire serial control data input Hardware mode: Deemphasis selection
19	SCKDSD	Digital input (pulled down)	Software mode: 3-wire or 2-wire serial control clock input Hardware mode: DSD bit stream operation selection
20	LATI²S	Digital input (pulled up)	Software mode: 3-wire serial control load input Hardware mode: Input data format selection

Note: Each digital input pin is provided with a Schmitt trigger input buffer.

Absolute Maximum Ratings

The absolute maximum ratings given here are only stress ratings. This device may be permanently damaged if it is operated continuously above any of these limits. Device function operating limits under the specified test conditions and the guaranteed performance specifications are shown in the electrical characteristics.

ESD Sensitive Device. This device is fabricated in a CMOS process. As a result, it can be easily damaged by excessive electrostatic voltages. Appropriate anti-static measures must be taken when handling or storing this device.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Digital system supply voltage			–0.3		+7	V
Analog system supply voltage			–0.3		+7	V
Digital input voltage range			DGND – 0.3		DVDD + 0.3	V
Analog input voltage range			AGND – 0.3		AVDD + 0.3	V
Master clock frequency					50	MHz
Operating temperature	Topr		–25		+85	°C
Storage temperature	Tstg		–65		+150	°C
Maximum mounting temperature (soldering time: 10 s)					+240	°C
Maximum mounting temperature (soldering time: 2 m)					+183	°C

Note: The potential difference between the analog system ground and the digital system ground must be 0.3 V or less.

Allowable Operating Ranges

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
Digital system supply voltage	DVDD		3.0		5.5	V
Analog system supply voltage	AVDD		3.0		5.5	V
GND	AGND, DGND			0		V
Potential difference between DGND and AGND			–0.3	0	+0.3	V
Analog system supply current		AVDD = 5 V		19		mA
Digital system supply current		DVDD = 5 V		8		mA
Analog system supply current		AVDD = 3.3 V		18		mA
Digital system supply current		DVDD = 3.3 V		4		mA

Electrical Characteristics

Test conditions at Ta = 25°C, AVDD, DVDD = 5 V, AGND = 0 V, DGND = 0 V, fs = 48 kHz, MCLK = 256 fs (Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
[Digital Logic Levels (TTL levels)]						
Low-level input voltage	V_{IL}				0.8	V
High-level input voltage	V_{IH}		2.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1 mA			AGND + 0.3 V	V
High-level output voltage	V_{OH}	I_{OH} = 1 mA	AVDD – 0.3 V			V
[Analog Reference Levels]						
Reference voltage		VMID	(VREFP – VREFN) / 2 – 50 mV	(VREFP – VREFN) / 2	(VREFP – VREFN) / 2 + 50 mV	V
Voltage divider resistance	R_{VMID}			12		kΩ

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
[D/A Converter Output (Load = 10 kΩ, 50 pF)]						
0 dB Fs, Full scale output voltage		At DAC outputs		1.1 × AVDD/5		Vrms
SNR (*1, 2, 3)		A-weighted when fs = 48 kHz	100	106		dB
SNR (*1, 2, 3)		A-weighted when fs = 96 kHz		106		dB
SNR (*1, 2, 3)		A-weighted when fs = 192 kHz		106		dB
SNR (*1, 2, 3)		A-weighted when fs = 48 kHz AVDD, DVDD = 3.3 V		105		dB
SNR (*1, 2, 3)		A-weighted when fs = 96 kHz AVDD, DVDD = 3.3 V		103		dB
SNR (*1, 2, 3)		Not 'A' weighted when fs = 48 kHz		106		dB
THD (*1, 2, 3)		1 kHz, 0 dBFs		–97		dB
THD + N (Dynamic range, *2)		1 kHz, –60 dBFs	100	106		dB
D/A converter channel separation				100		dB
[Analog Output Levels]						
Output level		Load = 10 kΩ, 0 dBFs		1.1		V_{RMS}
		Load = 10 kΩ, 0 dBFs, (AVDD = 3.3 V)		0.726		V_{RMS}
Inter-channel gain mismatch				±1		%FSR
Minimum load resistance		To midrail or a.c. coupled		1		kΩ
		To midrail or a.c. coupled (AVDD = 3.3 V)		600		Ω
Maximum load capacitance		5 V or 3.3 V		100		pF
DC output level				(VREFP – VREFN) / 2		V
[Power On Reset (POR)]						
POR threshold value				2.4		V

Notes: *1. SNR is measured for the 20 to 20 kHz bandwidth with a 1 kHz full scale input and a silent input (all bits 0) and with an A-weighting filter inserted.

*2. All characteristics measurements are performed with both a 20 kHz low-pass filter and an A-weighting filter inserted. Measurement in this state results in a higher THD + N and a lower SNR than those of the normal electrical characteristics. The low-pass filter is also effective for out-of-band noise, and although it has no audible effect, it does influence the characteristics shown above.

*3. VMID must be decoupled with 10 µF and 0.1 µF capacitors.
(Using values smaller than these will degrade the device characteristics.)

Power Supply Timing

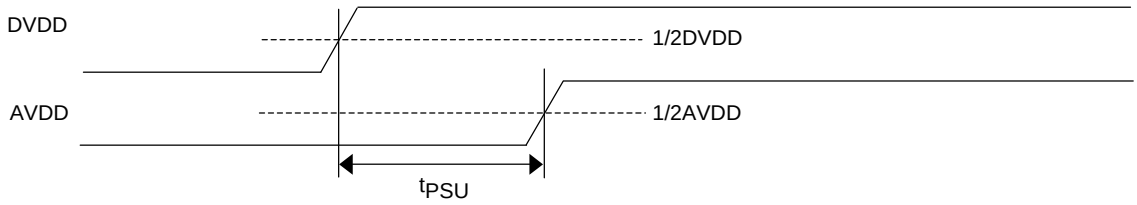


Figure 1 Power Supply Timing Requirements

Test conditions at Ta = 25°C, AVDD, DVDD = 5 V, AGND = 0 V, DGND = 0 V, fs = 48 kHz, MCLK = 256 fs (Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
[Power Application Timing]						
DVDD setup time after the rise of AVDD	t_{PSU}	Time interval between DVDD/2 and AVDD/2	10			ms

Master Clock Timing

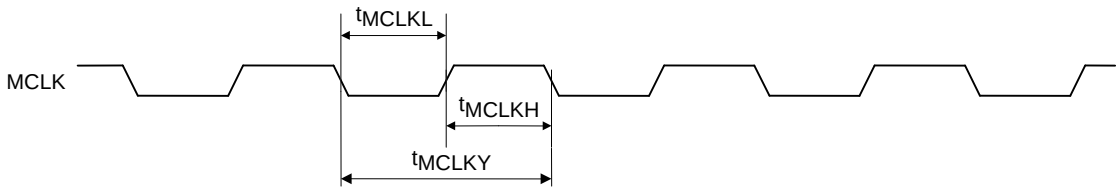


Figure 2 Master Clock Timing Overview

Test conditions at Ta = 25°C, AVDD, DVDD = 5 V, AGND = 0 V, DGND = 0 V, fs = 48 kHz, MCLK = 256 fs (Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
[Master Clock Timing]						
MCLK master clock pulse width (high)	t_{MCLKH}		13			ns
MCLK master clock pulse width (low)	t_{MCLKL}		13			ns
MCLK master clock cycle time	t_{MCLKY}		26			ns
MCLK duty cycle			40:60		60:40	

Digital Audio Interface

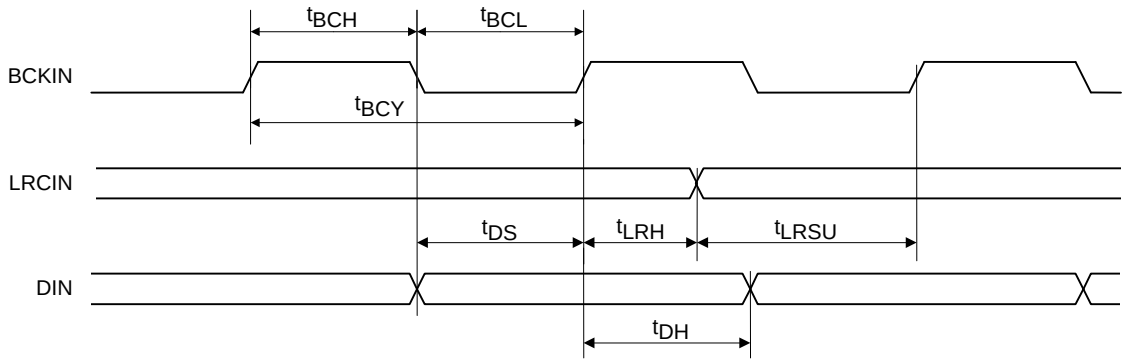


Figure 3 Digital Audio Interface Timing

Test conditions at Ta = 25°C, AVDD, DVDD = 5 V, AGND = 0 V, DGND = 0 V, fs = 48 kHz, MCLK = 256 fs (Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
[Audio Data Input Timing]						
BCKIN cycle time	t_{BCY}		40			ns
BCKIN pulse width (high)	t_{BCH}		16			ns
BCKIN pulse width (low)	t_{BCL}		16			ns
LRCIN setup time before the BCKIN rising edge	t_{LRSU}		8			ns
LRCIN hold time from the BCKIN rising edge	t_{LRH}		8			ns
DIN setup time before the BCKIN rising edge	t_{DS}		8			ns
DIN hold time from the BCKIN rising edge	t_{DH}		8			ns

DSD Audio Monophase Interface

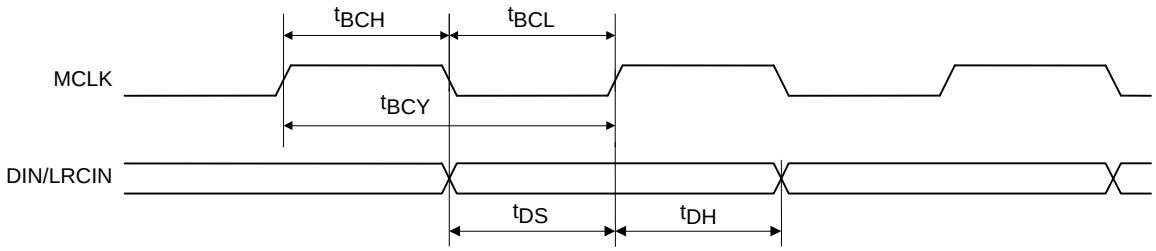


Figure 4 Normal DSD Timing Overview

Test conditions at Ta = 25°C, AVDD, DVDD = 5 V, AGND = 0 V, DGND = 0 V, fs = 48 kHz, MCLK = 256 fs (Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
[Audio Data Input Timing]						
MCLK cycle time	t_{BCY}			344		ns
MCLK pulse width (high)	t_{BCH}		160			ns
MCLK pulse width (low)	t_{BCL}		160			ns
DIN/LRCIN setup time before the MCLK rising edge	t_{DS}		10			ns
DIN/LRCIN hold time from the MCLK rising edge	t_{DH}		10			ns

DSD Audio Biphase Interface

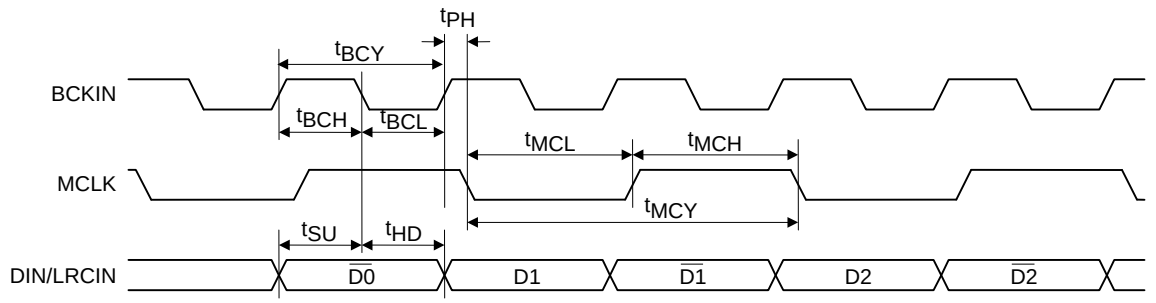


Figure 5 Biphase DSD Timing Overview

Test conditions at Ta = 25°C, AVDD, DVDD = 5 V, AGND = 0 V, DGND = 0 V, fs = 48 kHz, MCLK = 256 fs (Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
[Audio Data Input Timing]						
BCKIN cycle time	t_{BCY}			162.8		ns
BCKIN pulse width (high)	t_{BCH}		80	81.4		ns
BCKIN pulse width (low)	t_{BCL}		80	81.4		ns
MCLK cycle time	t_{MCY}			325.5		ns
MCLK pulse width (high)	t_{MCH}		160	162.8		ns
MCLK pulse width (low)	t_{MCL}		160	162.8		ns
Phase shift between BCKIN and MCLK	t_{PH}				20	ns
Data setup time before the BCKIN falling edge	t_{SU}		10			ns
Data hold time before the BCKIN rising edge	t_{HD}		10			ns

Microcontroller Three-Wire Interface Timing

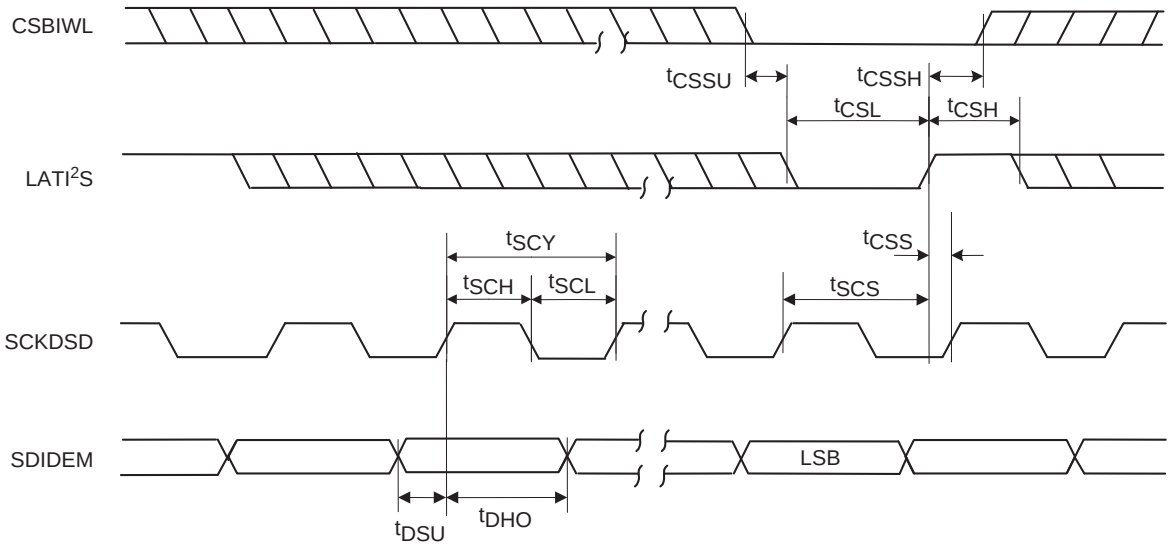


Figure 6 Program Register Input Timing - Three-Wire Serial Control Mode

Test conditions at Ta = 25°C, AVDD, DVDD = 5 V, AGND = 0 V, DGND = 0 V, fs = 48 kHz, MCLK = 256 fs (Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
[Program Register Input]						
From the SCKDSD rising edge to the LATI²S rising edge	t_{SCS}		40			ns
SCKDSD pulse cycle time	t_{SCY}		80			ns
SCKDSD pulse width (low)	t_{SCL}		20			ns
SCKDSD pulse width (high)	t_{SCH}		20			ns
Setup time from SDIDEM to SCKDSD	t_{DSU}		20			ns
Hold time from SCKDSD to SDIDEM	t_{DHO}		20			ns
LATI²S pulse width (low)	t_{CSL}		20			ns
LATI²S pulse width (high)	t_{CSH}		20			ns
From the LATI²S rising edge to the SCKDSD rising edge	t_{CSS}		20			ns
Setup time from CSBIWL to LATI²S	t_{CSSU}		20			ns
Hold time from LATI²S to CSBIWL	t_{CSSH}		20			ns

Microcontroller Two-Wire Interface Timing

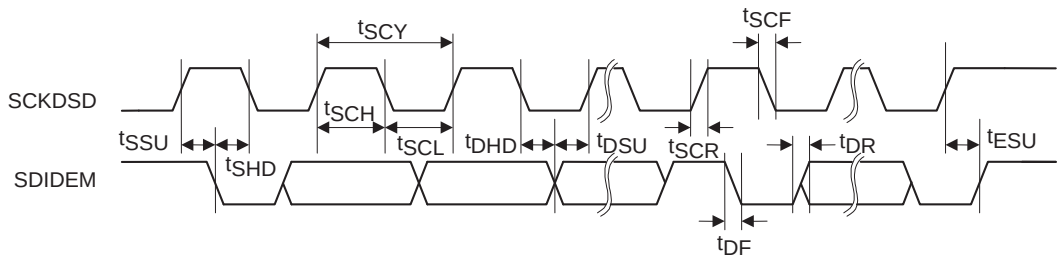


Figure 7 Program Register Input Timing - Two-Wire Serial Control Mode

Test conditions at Ta = 25°C, AVDD, DVDD = 5 V, AGND = 0 V, DGND = 0 V, fs = 48 kHz, MCLK = 256 fs (Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
[Program Register Input]						
SCKDSD pulse cycle time	t_{SCY}		80			ns
SCKDSD pulse width (low)	t_{SCL}		20			ns
SCKDSD pulse width (high)	t_{SCH}		20			ns
Data setup time for the start signal from SDIDEM to SCKDSD	t_{SSU}		10			ns
Data hold time for the start signal from SCKDSD to SDIDEM	t_{SHD}		10			ns
Data setup time from SDIDEM to SCKDSD	t_{DSU}		20			ns
Data hold time from SCKDSD to SDIDEM	t_{DHD}		20			ns
SCKDSD rise time	t_{SCR}		5			ns
SCKDSD fall time	t_{SCF}		5			ns
SDIDEM rise time	t_{DR}		5			ns
SDIDEM fall time	t_{DF}		5			ns
Data setup time for the stop signal from SDIDEM to SCKDSD	t_{ESU}		10			ns

Notes: 1. The device address in 2-wire mode is 001101X (binary). The last bit can be selected by the user.
2. The CSBIWL pin indicates the last bit of the chip address in 2-wire interface mode.
3. When using 2-wire mode, we recommend that the LATI²S pin be connected to either DGND or DV_{SS} to prevent the interface from being switched to 3-wire mode by noise.

Functional Description

Overview

The LC708728V is a high-performance D/A converter designed for digital audio equipment. This IC is optimal for DVD players, AV receivers, and other high-end audio equipment.

The LC708728V is a 2-channel high-performance stereo D/A converter that integrates digital interpolation filters, a multibit ∑Δ circuit, and smoothing filters in the output stage on the same chip. In addition to including an electronic volume control, the LC708728V also supports a variety of digital input signal formats and can be controlled over either a 2-wire or 3-wire microcontroller control interface. This microcontroller control interface can use the control signals from industry standard microcontrollers, DSPs, and other devices directly.

The LC708728V is controlled either by hardware control (pin level settings) or software control (control over a 2-wire or 3-wire serial interface). The MODE pin (pin 16) sets the control mode. The software interface can operate asynchronously with the audio data interface. In this case, the control data is synchronized within the IC with the processing of audio data.
The master clock frequency can be selected from 256, 384, 512, and 768 fs. The sampling rate is selected automatically in hardware mode, but can be controlled from the microprocessor in software mode. If an appropriate system clock is supplied, applications can select sampling rates from under 8 ks/s to 96 ks/s. If the master clock is set to either 128 or 192 fs, a sampling rate of 192 ks/s may be selected.

The LC708728V supports right justified, left justified, I^2S, and an extremely flexible DSP serial port interface as audio data interfaces. In hardware mode, the serial control interface pins are used to select the input data format. In this case, applications can set the input format type (I^2S or right justified), the input word length (20 or 24 bits), and deemphasis function.

A 64 fs data clock and independent bit streams for each of the left and right channels must be input in DSD mode. The bit stream data is input to the DIN and LRCIN pins, and that data is supplied to the internal D/A converters. In hardware mode, the SCKDSD pin (pin 19) input level controls switching between normal mode and DSD mode. See figure 4 for details.

Additionally, DSD mode supports phase modulation. Since in this method most of the audio spectral energy is removed from the data stream by supplying the audio data as a Manchester encoded bit stream, the digital signal corruption that occurs during analog output can be held to a minimum. The input data is sampled with a double-speed clock (BCKIN) to make it easier to demodulate the phase modulated data. See figure 5 for details.

This device is supplied in a miniature 20-pin SSOP package.

Clock Supply

In typical digital audio systems, there is only one clock system that is used to generate the reference clock that synchronizes all audio data processing. This clock is usually called the master clock. In the LC708728V, a master clock generated externally to the IC is directly supplied to the MCLK input pin, and no software settings are required to select the sampling rate.

In this IC, MCLK is used to drive the D/A converter path. The D/A converter sampling clock, the D/A converter digital filter clock, and the D/A converter digital audio interface timing and synchronization system are formed on the D/A converter path. When this IC is included in systems that have multiple signal sources used for reference clocks, the clock source with the lowest jitter must be selected to get the maximum characteristics from the D/A converters.

Since this IC only operates in slave mode, the master clock must be supplied from external circuits.

Digital Audio Interface

The audio data is sent to the internal D/A converter filters from the digital audio interface. This IC support the five most common audio formats.

- Left justified
- Right justified
- I²S mode
- DSP early mode
- DSP late mode

All of the above formats are MSB first and support 16-, 20-, 24-, and 32-bit word lengths. (However, 32-bit data is not supported in right justified mode.)
The data input (DIN) and the L/R clock input (LRCIN) can be sampled on either the rising or falling edge of the bit clock input (BCKIN).

In the left justified, right justified, and I²S modes, data is input through the DIN pin. This audio data is time division multiplexed data, and is divided into left and right channel data internally for processing according to the state of the L/R clock input at the LRCIN pin. The LRCIN input is also used as a timing reference that indicates the start or end of the data word. The minimum number of BCKIN cycles per one LRCIN period is twice the selected word length. Inversely, the LRCIN must hold the low or high level for the minimum word count of BCKIN inputs. When this condition is met, an arbitrary mark/space ratio can be used for the LRCIN input.

When one LRCIN period consists of 32 BCKIN imputs, this IC automatically invalidates all previous settings and switches to 16-bit mode. When one LRCIN period consists of any value other than 32 BCKIN periods, the preset values are used.

In DSP early or late mode, data is input through the DIN pin. This audio data is time division multiplexed data, and LRCIN is used as a frame synchronization signal to identify the MSB in the first word. The minimum number of BCKIN inputs per one LRCIN period is twice the selected word length. If the position of the rising edge is set accurately, an arbitrary mark/space ratio can be used for the LRCIN input. (See figures 11 and 12.)

Left Justified Mode

In left justified mode, the MSB is sampled on the first BCKIN rising edge following an LRCIN transition. LRCIN is high during left-channel data word input, and low during right-channel data word input.

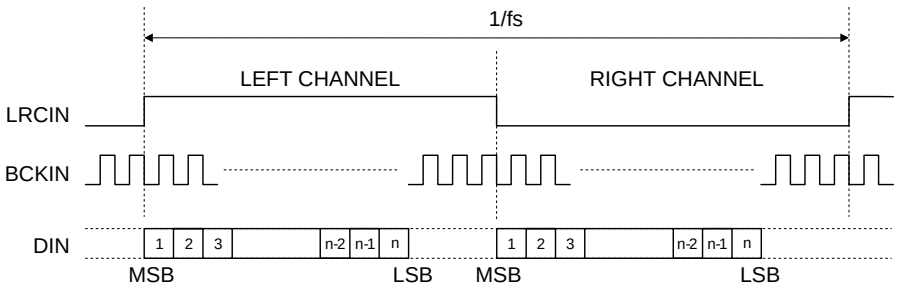


Figure 8 Left Justified Mode Timing Chart

Right Justified Mode

In right justified mode, the LSB is sampled on the BCKIN rising edge that precedes the LRCIN transition. LRCIN is high for the left data word and low for the right data word.

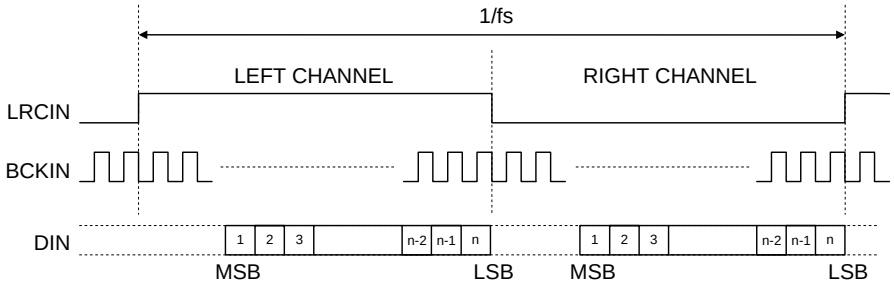


Figure 9 Right Justified Mode Timing Chart

I²S Mode

In I²S mode, the MSB is sampled on the second BCKIN rising edge following the LRCIN transition. LRCIN is low for the left data word and high for the right data word.

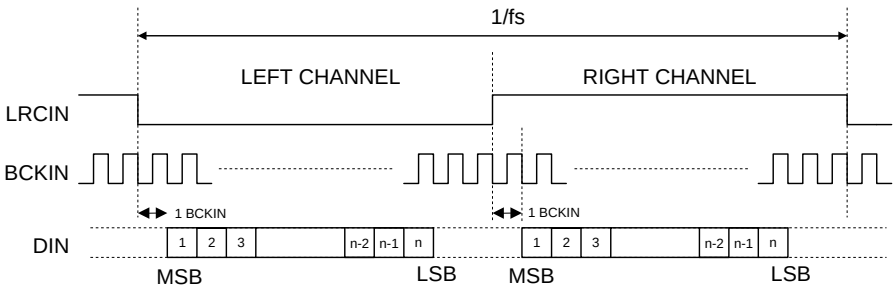


Figure 10 I²S Mode Timing Chart

DSP Early Mode

In DSP early mode, the first bit is sampled on the BCKIN rising edge that follows the BCKIN on which the LRCIN low to high transition was detected. BCKIN edges are not allowed between data words. The word order is left channel first, right channel second.

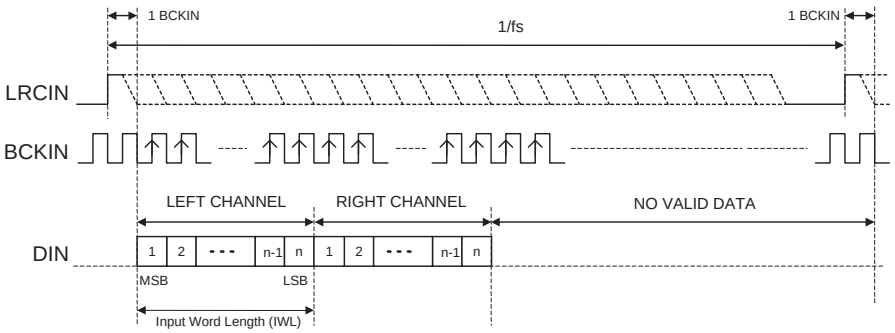


Figure 11 DSP Early Mode Timing Chart

DSP Late Mode

In DSP late mode, the first bit is sampled on the BCKIN rising edge on which the LRCIN low to high transition was detected. BCKIN edges are not allowed between data words. The word order is left channel first, right channel second.

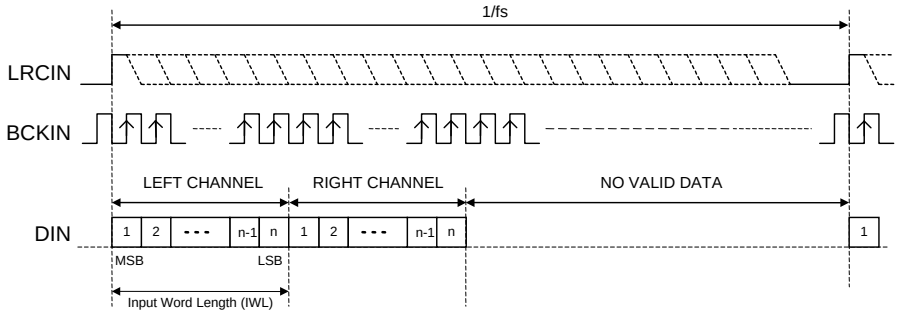


Figure 12 DSP Late Mode Timing Chart

Audio Data Sampling Rate

The LC708728V master clock supports audio sampling rates from 128 to 768 fs. Here, fs is the audio data sampling rate (LRCIN), and is one of 32, 44.1, 48, 96, or 128 kHz. In this IC, the internal digital filter and noise shaper circuits are operated using the master clock.

This IC includes a master clock detection circuit that automatically detects the relationship between the master clock frequency and the sampling rate. Although this detection circuit automatically corrects if the error is within ±32 clock cycles, if an error of over ±32 clock cycles occurs, D/A converter operation is stopped and the output is muted automatically.
We recommend that the master clock be synchronized with LRCIN. Also note that phase differences and jitter with respect to this clock are allowed. See table 1 for details.

Sampling rate	Master clock frequency (MHz) (MCLK)					
(LRCIN)	128 fs	192 fs	256 fs	384 fs	512 fs	768 fs
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1 kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48 kHz	6.114	9.216	12.288	18.432	24.576	36.864
96 kHz	12.288	18.432	24.576	36.864	None	None
192 kHz	24.576	36.864	None	None	None	None

Table 1 Master Clock Frequency vs. Sampling Rate

Hardware DSD Mode

DSD mode is set up by setting the MODE pin low and the SCKDSD pin high. In this mode, the built-in digital filters are bypassed and the bit stream data is supplied to the D/A converters directly. The data converted by the D/A converters passes through internal low-pass filters and is then output. See figures 27 to 30 for details.

Two data transfer formats are supported: monophase and biphase.

In monophase mode, the DSD data is directly sampled after the rising edge of the 64fs MCLK signal.

In biphase mode, data is supplied in a Manchester encoded format. In Manchester encoding, a bit transition occurs at every data bit. As a result, corruption of the analog output due to spectral energy is held to an absolute minimum. Based on a 128 fs clock signal input to the BCKIN pin, data is sampled on the BCKIN signal falling edge when MCLK is low.

See figures 4 and 5 for details.

Hardware Control Mode

The LC708728V operates in hardware mode when the MODE pin is set to the low level.

Muting and Auto-Mute Operation

Muting operation can be controlled directly by supplying an input to the MUTEB pin (pin 17) in either operating mode, hardware mode or software mode. The auto-mute function is also controlled with this pin. Normally, the MUTEB pin is an active-low input. However, when this pin is set to the open state (floating), it becomes an output pin and functions as an infinite zero detection pin. See table 2 for details. See the description of the ZERO pin (pin 5) for more information.

MUTEB pin	State
0	The D/A converter outputs are muted.
1	Normal operation
Open (floating)	IZD (auto-mute) mode. The MUTEB pin functions as the IZD state indicator flag. Low output: IZD detected High output: IZD not detected

Table 2 Muting and Auto-Mute Control

Figure 13 presents an overview of the start and stop of muting operation (48 kHz, full-scale sine wave). The upper signal is the D/A converter output level and the lower signal is the input to the MUTE pin. When muting is turned on, the D/A converter output starts to decay geometrically from the input sample DC level at the point muting started. The attenuation progresses so that the output level reaches the VMID level after 64 sample periods. When the muting is turned off, the output is restarted immediately from the sampled data at the point the muting is turned off.

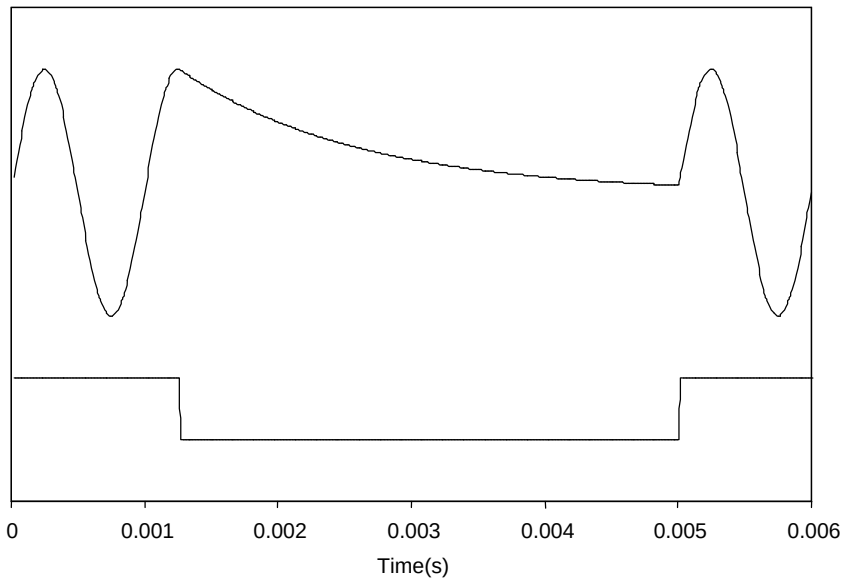


Figure 13 Soft Muting Start and Stop Overview

The auto-mute function monitors both the left and right channels to determine whether or not a zero level has been input for a period of 1024 samples. If the zero level continues for over 1024 in both the left and right channels, the auto-mute function activates and sets the IC internal AUTOMUTED flag to the active state. Since this flag is wired to the MUTEB pin through a 10 kΩ resistor, the auto-mute function will be enabled if the MUTEB pin is open (floating).

When the MUTEB pin is set to the high level, the auto-mute function is disabled. As a result, unless the IZD register bit is set in software, the mute function will not be turned on. When the MUTEB pin is used as an I/O pin (the case where it can be set to any of the high, low, and floating states), it is possible to both control the muting operation directly with an input to this pin and use the auto-mute function as well. When the MUTEB pin is set to the open (floating) state, the application can monitor the AUTOMUTED output. This allows the muting of the whole system that this IC is part of to be controlled by monitoring the state of this pin.

Figure 14 shows the internal equivalent circuit for the MUTEB pin.

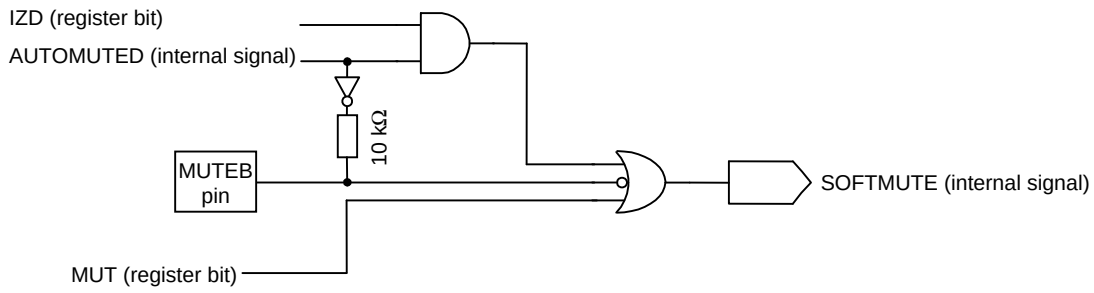


Figure 14 MUTEB Pin Internal Equivalent Circuit

Input Format Selection

In hardware control mode, the input data format is set with the LATI²S (pin 20) and CSBIWL (pin 15) pins. See table 3 for details.

LATI²S	CSBIWL	Input data mode
0	0	24-bit, right justified
0	1	20-bit, right justified
1	0	16-bit, I²S mode
1	1	24-bit, I²S mode

Table 3 Input Data Format Selection

Note: In 24-bit I²S mode, if there are both high and low periods in the input to the LRCIN pin that last for over 24 cycles of the BCKIN clock, the IC will support data formats with an arbitrary bit width up to 24 bits. If the LRCIN period is exactly 32 cycles of the CBKIN clock, this IC automatically sets up 16-bit data mode.

Deemphasis Control

In hardware control mode, deemphasis is controlled using the SDIDEM pin (pin 18). See table 4 for details.

SDIDEM	Deemphasis
0	Off
1	On

Table 4 Deemphasis Control

Software Control Interface

This IC can be set up and controlled over either a 2-wire or a 3-wire (SPI compatible) software interface.

Control Mode Setting

This IC's operating mode can be set to either hardware control mode or software control mode. The MODE pin is used to set the control mode.

Mode	Control mode
0	Hardware control mode
1	Software control mode

Table 5 Control Mode Selection

Three-Wire Control Mode (SPI Compatible)

In this mode, the IC is controlled using three pins: SDIDEM, SCKDSD, and LATI^{2}S. The program data is input to the SDIDEM pin, the program data latching clock signal is input to the SCKDSD pin, and the external signal that latches the whole program data word is applied to the LATI^{2}S pin. Figure 14 presents an overview of the SDIDEM, SCKDSD, and LATI^{2}S signal timing.

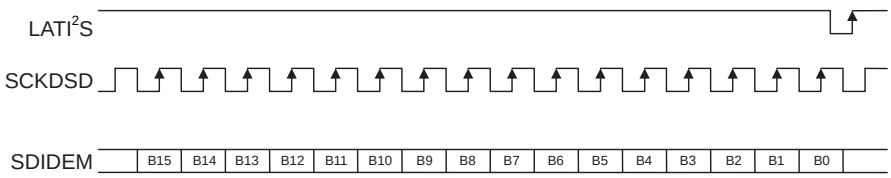


Figure 15 Three-Wire Control Mode Timing Overview

Notes:
1. B[15:9] are the control address bits.
2. B[8:0] are the control data bits.
3. The CSBIWL pin must be held at the low level when data is written. (See figure 6.)

Two-Wire Control Mode

In this mode, the IC is controlled using two pins: SDIDEM and SCKDSD. The program data is input to the SDIDEM pin and external the program data latching clock signal is input to the SCKDSD pin. Figure 16 presents an overview of the timing.

This IC has the address 001101X (binary), which indicates that it is an audio device. Of these bits, the value of the last address bit (shown as an X) depends on the input to the CSBIWL pin. The CSBIWL pin must be connected to either DVDD or DVSS. In 2-wire control mode, two LC708728V chips in the same system can be controlled referencing this addresss and using by the same control signal by setting the CSBIWL pin low on one chip and high on the other.

Since the LATI²S pin is not used in 2-wire control mode, it must be connected to either DVDD or DVSS. Note that if the input level on the LATI²S pin goes from low to high or high to low during a control operation in 2-wire mode, the operating mode will switch to 3-wire mode. If the LC708728V switches from 2-wire control mode to 3-wire control mode, it will not return to 2-wire mode unless the MODE pin input is changed or power to the device is turned off.

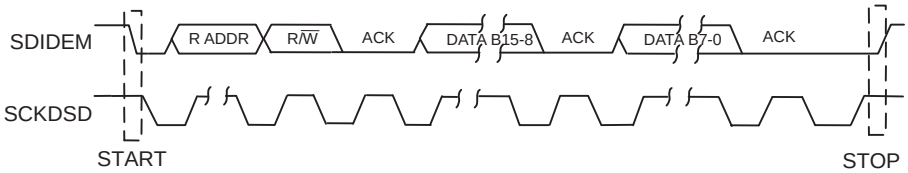


Figure 16 Two-Wire Control Mode Timing Overview

Register Map

The LC708728V includes four 16-bit program registers. Data is transferred to these register by inputting that data from the SDIMEM pin in either 2-wire control mode or 3-wire control mode.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
M0	0	0	0	0	0	0	0	UPDATEL	LAT7	LAT6	LAT5	LAT4	LAT3	LAT2	LAT1	LAT0
M1	0	0	0	0	0	0	1	UPDATAR	RAT7	RAT6	RAT5	RAT4	RAT3	RAT2	RAT1	RAT0
M2	0	0	0	0	0	1	0	0	0	0	IW2	IW1	IW0	PWDN	DEEMPH	MUT
M3	0	0	0	0	0	1	1	IZD	0	0	BCP	REV	0	ATC	LRP	I²S
	Address							Data								

Table 6 Program Register Mapping

Register address (A3, A2, A1, A0)	Bits	Symbol	Default	Description
0000	[7:0]	LAT [7:0]	11111111 (0 dB)	Left channel attenuation data for the 0.5 dB step attenuator. See table 9.
DACL attenuation	8	UPDATEL	0	Left channel attenuator load control 0: Save DACL in an intermediate register. (The output does not change.) 1: Save DACL and update the attenuation in both channels.
0001	[7:0]	RAT [7:0]	11111111 (0 dB)	Right channel attenuation data for the 0.5 dB step attenuator. See table 9.
DACR attenuation	8	UPDATER	0	Right channel attenuator load control 0: Save DACL in an intermediate register. (The output does not change.) 1: Save DACL and update the attenuation in both channels.
0010	0	MUT	0	Soft muting control 0: Muting off 1: Muting on
D/A converter control	1	DEEMPH	0	Deemphasis control 0: Deemphasis off 1: Deemphasis on
	2	PWDN	0	Low power mode control 0: Normal operation. The output is active. 1: Low power mode. The output is muted.
	[5:3]	IW [2:0]	0	Audio data format selection. See table 14.
0011	0	I^2S	0	Audio data format selection. See table 14.
Interface control	1	LRP	0	LRCIN/DSP mode selection 0: LRCIN normal/DSP late mode 1: LRCIN inverted/DSP early mode
	2	ATC	0	Attenuator control 0: Use the set attenuations for the left and right channels. 1: Use the left channel attenuation data for the right channel.
	4	REV	0	Output phase inversion
	5	BCP	0	BCKIN polarity 0: Normal 1: Inverted
	8	IZD	0	IZD and auto-mute control 0: IZD function disabled 1: IZD function enabled

Table 7 Register Bit Allocations

Attenuation Control

Both the left and right channels provide digital attenuation control in the signal path prior to conversion to analog by the A/D converter. While the default attenuation is 0 dB, the level can be controlled over the range 0 dB to 127.5 dB in 0.5 dB steps with the 8-bit attenuation control register. The attenuation control registers have a dual structure so that after the left and right channel attenuation values are set in the corresponding registers, the left and right outputs can be set to the modified values with the same timing. Attenuation values set in advance can be reflected in the output by controlling the UPDATE bit in each of these registers. See table 8 for details.

Register address	Bits	Symbol	Default	Description
0000 D/A converter left	[7:0]	LAT [7:0]	11111111 (0 dB)	D/A converter left channel attenuation data In 0.5 dB steps
channel attenuation control	8	UPDATEL	0	Attenuation data load control 0: The value of LAT[7:0] is transferred to an internal register. (The output does not change) 1: The left channel attenuation value is changed to that of the internal register, and the left and right channel attenuation values are both changed. (The output value changes.)
0001 D/A converter right	[7:0]	RAT [7:0]	11111111 (0 dB)	D/A converter right channel attenuation data In 0.5 dB steps
channel attenuation control	8	UPDATER	0	Attenuation data load control 0: The value of RAT[7:0] is transferred to an internal register. (The output does not change.) 1: The right channel attenuation value is changed to that of the internal register, and the left and right channel attenuation values are both changed. (The output value changes.)

Table 8 Attenuation Control Register Map

Notes:

1. The UPDATE bits are not latched internally. As a result, when the UPDATEL (or UPDATER) bit is 0, the set attenuation value is transferred to the internal register, but is not reflected in the D/A converter output. However, when UPDATEL (or UPDATER) is set to 1, either the internal register value or the value written to LAT (or RAT)[7:0] when the UPDATE bit was set is reflected in the output starting with the next input sample after the UPDATE bit was set.
2. Changing the attenuation value rapidly or over a large level can result in “zipper” noise appearing in the output. Therefore, care is required when changing the attenuation value.

Output Attenuation

The left and right channel attenuation is controlled using the values set in the LAT and RAT registers. Table 9 shows the correspondence between the attenuation setting value and the actual attenuation level.

XAT [7:0]	Attenuation level
00 (hex)	–∞ dB (mute)
01 (hex)	–127.5 dB
:	:
:	:
:	:
FE (hex)	–0.5 dB
FF (hex)	0 dB

Table 9 Attenuation Control Levels

Mute Mode (Software Mute)

The software muting function is controlled by setting the MUT register.

Register address	Bit	Symbol	Default value	Description
0010 D/A converter control	0	MUT	0	Soft muting selection 0: Normal operation 1: Soft muting enabled (both left and right channels)

Table 10 Software Mute Control

De-Emphasis Mode

The deemphasis function is controlled by setting the DEEMPH register.

Register address	Bit	Symbol	Default value	Description
0010 D/A converter control	1	DEEMPH	0	Deemphasis mode selection 0: Deemphasis off 1: Deemphasis on

Table 11 Deemphasis Setting

Power Down Mode

The power down mode is controlled by setting the PWDN register. In power down mode, the left and right channel D/A converter outputs are set to the VMID level and the IC internal operations transits to a power down operating mode. Note that when the IC switches to power down mode, all previously input audio data and control register values are cleared. When returning to normal operation from power down mode, the first 16 samples of the audio data input after returning to normal mode are ignored to initialize the internal FIR filters.

Register address	Bit	Symbol	Default value	Description
0010 D/A converter control	2	PWDN	0	Power down mode selection 0: Normal operation 1: Power down mode

Table 12 Power Down Mode Control

Digital Audio Interface Control Register

The LC708728V features a digital audio interface that is an expanded version of the digital audio interface provided by the Wolfson Microelectronics WM8716. The digital audio input format is set using the IWL[2:0] bits in the M2 register and the I^2S bit in the M3 register.

Register address	Bit	Symbol	Default value	Description
0010 D/A converter control	5:3	IWL [2:0]	000000	Input data format selection
0011 Interface control	0	I^2S	0	Input data format selection

Table 13 Digital Audio Input Data Format Selection

IW2	I²S	IWL1	IWL0	Digital audio data input format (*)
0	0	0	0	16 bits Right justified mode
0	0	0	1	20 bits Right justified mode
0	0	1	0	24 bits Right justified mode
0	0	1	1	24 bits Left justified mode
0	1	0	0	16 bits I²S mode
0	1	0	1	24 bits I²S mode
0	1	1	0	20 bits I²S mode
0	1	1	1	20 bits Left justified mode
1	0	0	0	16 bits DSP mode
1	0	0	1	20 bits DSP mode
1	0	1	0	24 bits DSP mode
1	0	1	1	32 bits DSP mode
1	1	0	0	16 bits Left justified mode

Table 14 Digital Audio Data Input Format Settings

*: In all of the above modes, the input data is signed two's complement data. Also, only 24-bit data is input to the digital filters. When the data format is either 16 or 20 bits, zeros are automatically inserted in the unused bits in the low order end of the word. When a 32-bit data format is used, the lower 8 bits of the data are handled as being 0.

LRCIN (Left/right clock) Polarity selection

In left justified, right justified, and I²S mode, the polarity of the L/R clock input to the LRCIN pin is controlled by the LRP register setting. When this bit is set to 1, the LRCIN polarity is set to the opposite state of that shown in figures 8, 9, and 10. While the left and right channel signals can be swapped by using this function, note that using this function results in the occurrence of a 1-sample phase difference.

Register address	Bit	Symbol	Default value	Description
0011 Interface control	1	LRP	0	LRCIN polarity setting 0: Normal operation 1: Left and right channels swapped

Table 15 LRCIN Polarity Selection

Also note that this bit is used to switch between early and late modes in DSP mode. (See figures 11 and 12.)

Register address	Bit	Symbol	Default value	Description
0011 Interface control	1	LRP	0	DSP mode format setting 0: DSP late mode 1: DSP early mode

Table 16 Input Format Control in DSP Mode

In DSP early mode, data sampling starts from the second BCKIN rising edge counted from the LRCIN rising edge. In contrast, data sampling starts from the BCKIN rising edge immediately after the LRCIN rising edge in DSP late mode. BCKIN edges are not allowed between words in either of these modes. Note that the order of the data is left channel first, then right channel.

Attenuator Control Mode

Control of left and right channel attenuation can be performed with just the left channel attenuation control by setting the ATC register. That is, after the ATC register is set, the left channel attenuation data (the LAT register value) is used as the attenuation data for both the left and right channels. The set value of the ATC register is applied starting with the first audio sample after ATC is set.

Register address	Bit	Symbol	Default value	Description
0011 Interface control	2	ATC	0	Attenuator control mode 0: Normal operation (The RAT value is used for right channel attenuator control.) 1: ATC enabled (The LAT value is used for right channel attenuator control.)

Table 17 Attenuator Control Mode

Output Phase Inversion Mode

The phase of the output signal can be inverted by setting the REV register bit.

Register address	Bit	Symbol	Default value	Description
0011 Interface control	4	REV	0	Analog output phase setting 0: Normal phase 1: Inverted phase

Table 18 Output Phase Inversion Mode Control

BCKIN Polarity Control Mode

Normally, LRCIN and DIN are sampled on the BCKIN rising edge. Thus it is desirable that LRCIN and DIN change value on the BCKIN falling edge. This IC can be used in a system in which LRCIN and DIN change value on the BCKIN rising edge by setting this register. If the BCP register is set to 1, the BCKIN polarity shown in figures 8 to 12 is inverted.

Register address	Bit	Symbol	Default value	Description
0011 Interface control	5	BCP	0	BCKIN polarity control 0: Normal phase (Data is latched on the BCKIN rising edge.) 1: Inverted phase (Data is latched on the BCKIN falling edge.)

Table 19 BCKIN Polarity Control Mode

IZD Detection Mode

Applications can set whether or not auto-muting is performed when over 1024 samples of 0-valued data are input by setting the IZD register.

Register address	Bit	Symbol	Default value	Description
0011 Interface control	8	IZD	0	IZD detection control and auto-mute control 0: IZD detection function disabled (Auto-mute disabled) 1: IZD detection function enabled (Auto-mute enabled)

Table 20 IZD Detection Mode Control

Digital Filter Characteristics

Parameter	Symbol	Test Conditions	Ratings			Unit
			min	typ	max	
Pass band edge		–3 dB		0.487 fs		
Pass band ripple		f < 0.444 fs			±0.05	dB
Stop band attenuation		f > 0.555 fs	–60			dB

Table 21 Digital Filter Characteristics

D/A Converter and Digital Filter Response

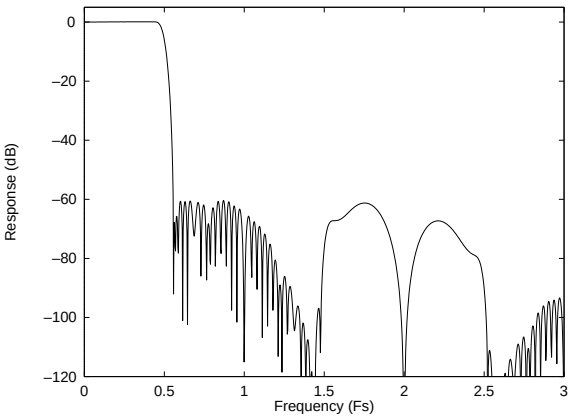


Figure 17 D/A Converter and Digital Filter Frequency Response – 44.1, 48 and 96 kHz

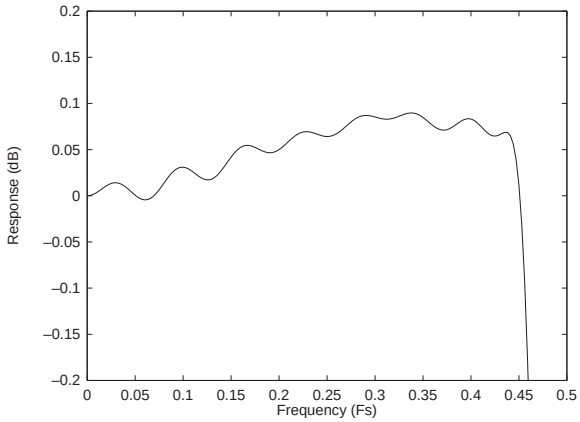


Figure 18 D/A Converter and Digital Filter Ripple – 44.1, 48 and 96 kHz

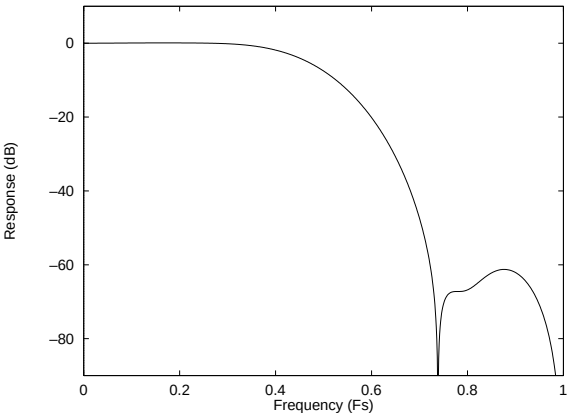


Figure 19 D/A Converter and Digital Filter Frequency Response – 192 kHz

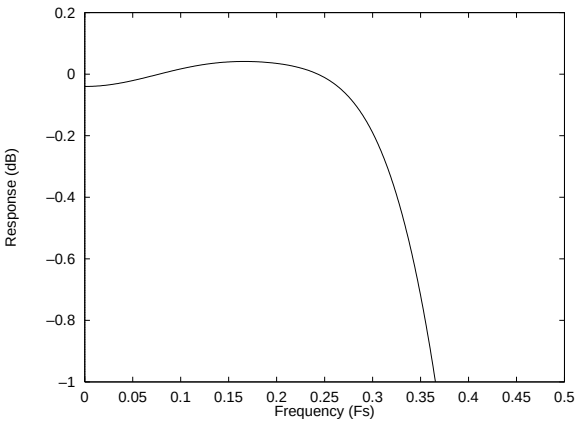


Figure 20 D/A Converter and Digital Filter Ripple – 192 kHz

Digital Deemphasis Characteristics

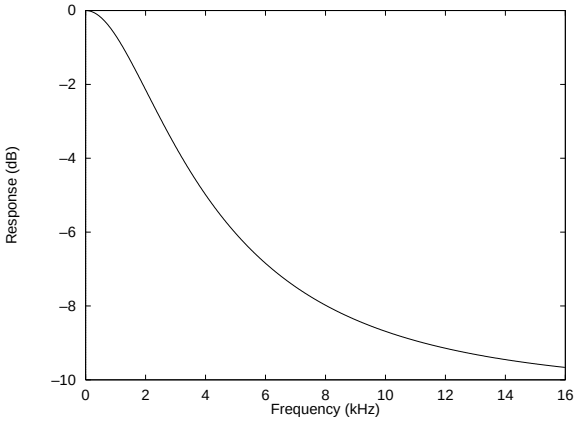


Figure 21 Deemphasis Frequency Response (32 kHz)

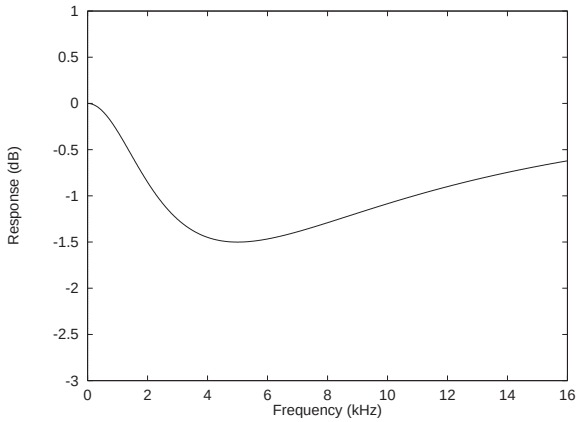


Figure 22 Deemphasis Error (32 kHz)

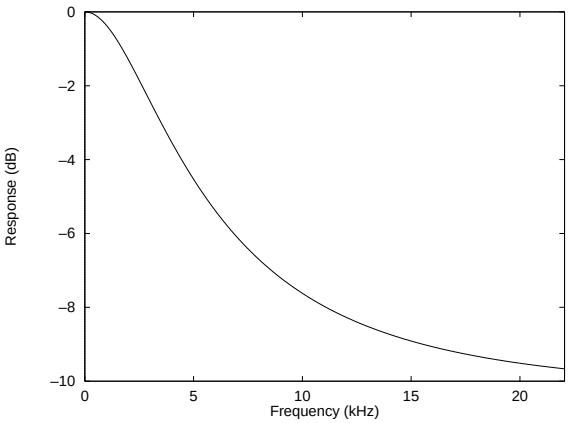


Figure 23 Deemphasis Frequency Response (44.1 kHz)

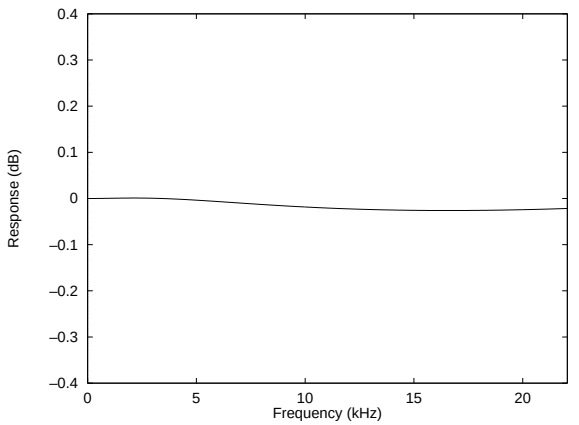


Figure 24 Deemphasis Error (44.1 kHz)

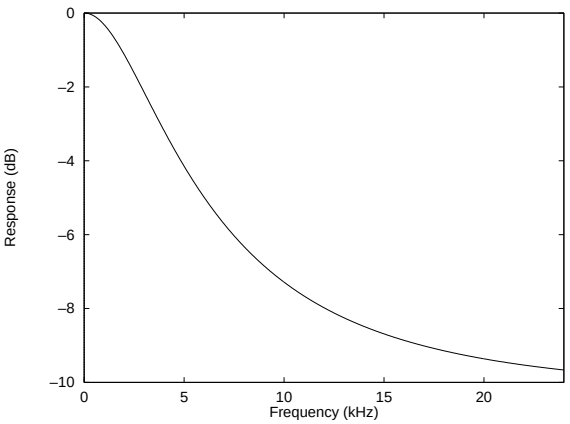


Figure 25 Deemphasis Frequency Response (48 kHz)

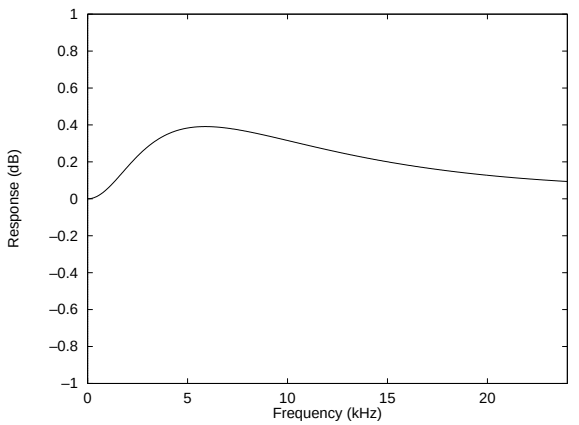


Figure 26 Deemphasis Error (48 kHz)

DSD Mode Characteristics

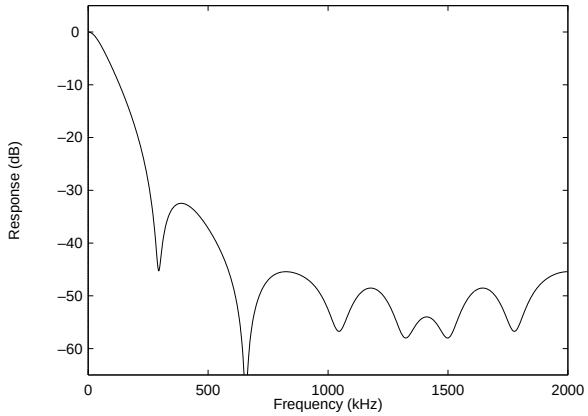


Figure 27 DSD Frequency Response – No post filter

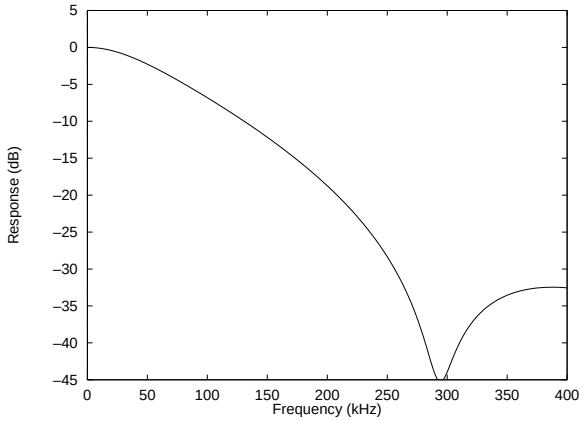


Figure 28 DSD Frequency Response – No post filter

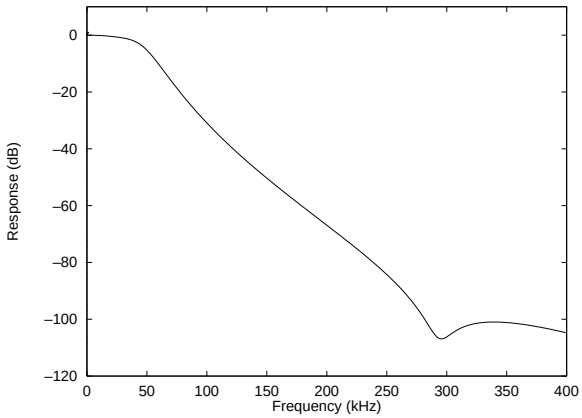


Figure 29 DSD Frequency Response – Fourth-order post filter

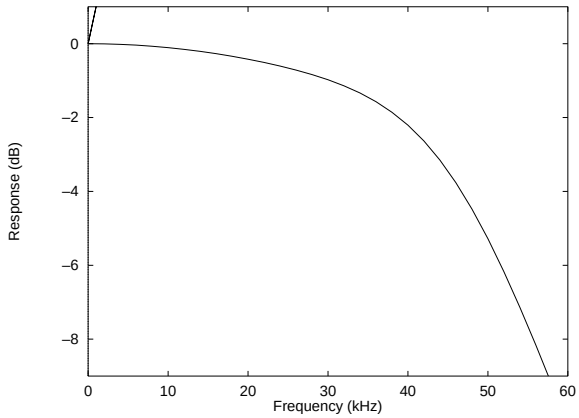
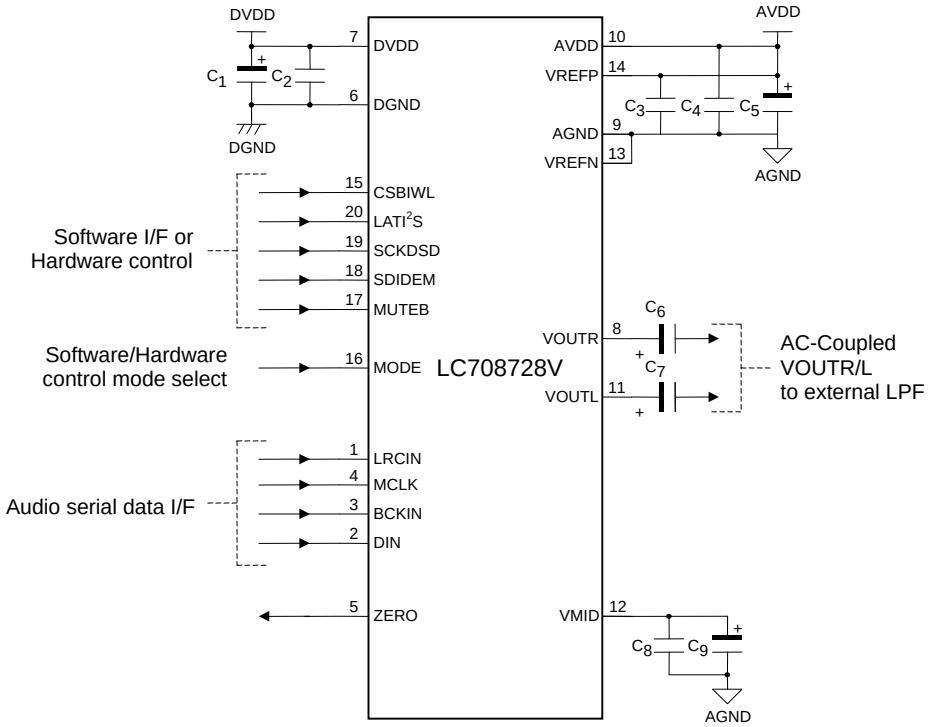


Figure 30 DSD Frequency Response – Fourth-order post filter

Application Circuit Example



Notes: 1. AGND and DGND must be connected as close to the LC708728V itself as possible.
2. The C2, C3, C4, and C8 capacitors must be located as close to the LC708728V as possible.
3. We recommend using capacitors with the lowest ESR possible to get the best possible performance from the LC708728V.

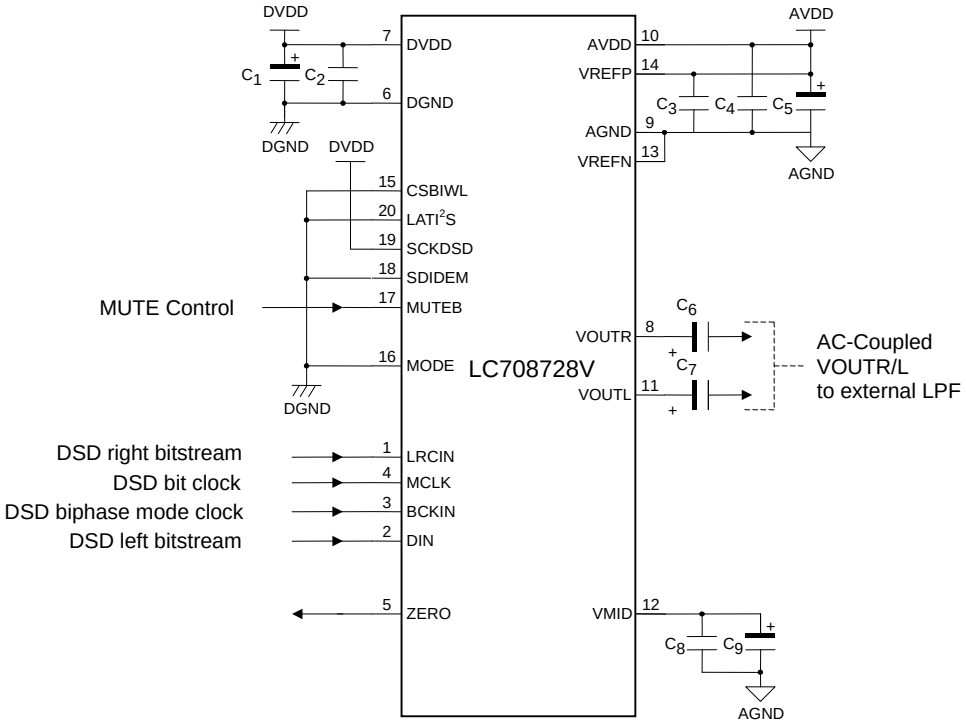
Figure 31 Application Circuit Example

Recommended Component Values for the Application Circuit Example

Component	Recommended value	Description
C1, C5	10 µF	DVDD and AVDD/VREFP decoupling
C2 to C4	0.1 µF	DVDD and AVDD/VREFP decoupling
C6, C7	10 µF	Output AC coupling capacitors used to exclude the midrail DC level from the output.
C8	0.1 µF	VMID pin reference decoupling capacitors
C9	10 µF	

Table 22 Recommended Component Values

Application Circuit Example (DSD mode)



Notes: 1. AGND and DGND must be connected as close to the LC708728V itself as possible.
2. The C_2, C_3, C_4, and C_8 capacitors must be located as close to the LC708728V as possible.
3. We recommend using capacitors with the lowest ESR possible to get the best possible performance from the LC708728V.
4. In monophase DSD mode, the BCKIN pin (pin 3) must be connected to DVDD. In biphase DSD mode, two BCKIN cycles must be applied for every bit input.

Figure 32 DSD Mode Application Circuit Example

Recommended Component Values for the DSD Mode Application Circuit Example

Component	Recommended value	Description
C1, C5	10 µF	DVDD and AVDD decoupling
C2 to C4	0.1 µF	DVDD and AVDD decoupling
C6, C7	10 µF	Output AC coupling capacitors used to exclude the midrail DC level from the output.
C8	0.1 µF	VMID pin reference decoupling capacitors
C9	10 µF	

Table 23 Recommended Component Values

DSD Mode Connection Example

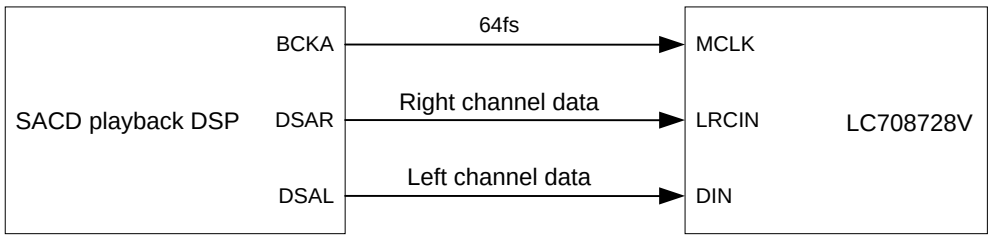


Figure 33 Monophase Mode Connection

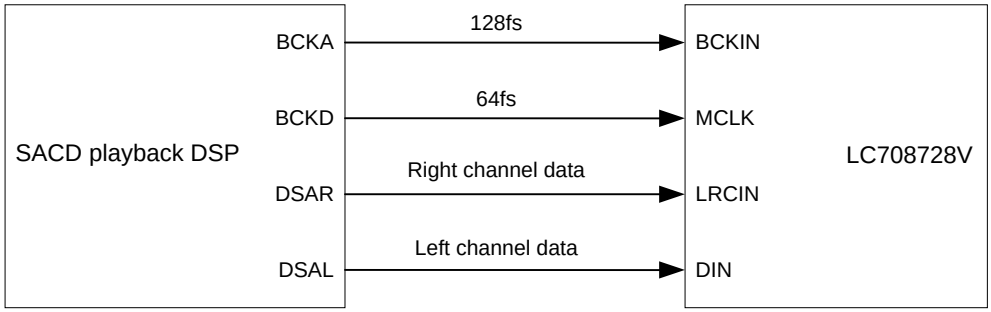


Figure 34 Biphase Mode Connection

- DSD mode is set up by setting the SCKDSD pin high while holding the MODE pin low.
- DSD mode can only be used in hardware mode.

Recommended Analog Low Pass Filter for the PCM Data Format (Option)

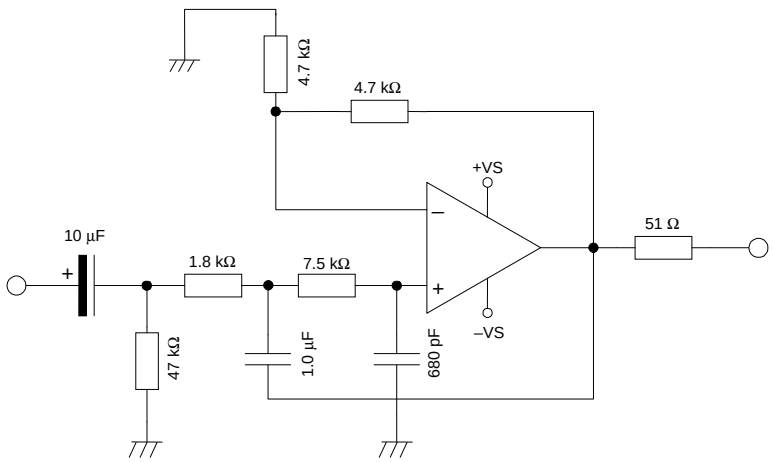


Figure 35 Recommended Low Pass Filter (Option)

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