Ordering number : ENA2089A

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

CMOS LSI

LC717A00AJ — Capacitance-Digital-Converter LSI for Electrostatic Capacitive Touch Sensors

Overview

The LC717A00AJ is a high-performance, low-cost capacitance-digital-converter LSI for electrostatic capacitive touch sensor, especially focused on usability. It has 8 channels capacitance-sensor input. The built-in logic circuit can detect the state (ON/OFF) of each input and output the result. This makes it ideal for various switch applications.
The calibration function is automatically performed by the built-in logic circuit during power activation or whenever there are environmental changes. In addition, since initial settings of parameters, such as gain, are configured, LC717A00AJ can operate as stand-alone when the recommended switch pattern is applied.
Also, since LC717A00AJ has a serial interface compatible with I^2C and SPI bus, parameters can be adjusted using external devices whenever necessary. Moreover, outputs of the 8-input capacitance data can be detected and measured as 8-bit data.

Features

- Detection system: Differential capacitance detection (Mutual capacitance type)
- Input capacitance resolution: Can detect capacitance changes in the femto Farad order
- Measurement interval (8 differential inputs): 18ms (Typ) (at initial configuration),
  3ms (Typ) (at minimum interval configuration)
- External components for measurement: Not required
- Current consumption: 320µA (Typ) (V_{DD} = 2.8V), 740µA (Typ) (V_{DD} = 5.5V)
- Supply voltage: 2.6V to 5.5V
- Detection operations: Switch
- Packages: SSOP30
- Interface: I^2C * compatible bus or SPI selectable.

* I^2C Bus is a trademark of Philips Corporation.

Specifications

Absolute Maximum Ratings at Ta = +25°C

Parameter	Symbol	Ratings (V_{SS} = 0V)	Unit	Remarks
Supply voltage	V_{DD}	-0.3 to +6.5	V	
Input voltage	V_{IN}	-0.3 to V_{DD}+0.3	V	*1
Output voltage	V_{OUT}	-0.3 to V_{DD}+0.3	V	*2
Power dissipation	Pd max	160	mW	Ta = +105°C, Mounted on a substrate *3
Peak output current	I_{OP}	±8	mA	per terminal, 50% Duty ratio *2
Total output current	I_{OA}	±40	mA	Output total value of LSI, 25% Duty ratio
Storage temperature	Tstg	-55 to +125	°C	

*1) Apply to Cin0 to 7, Cref, nRST, SCL, SDA, SA, SCK, SI, nCS, GAIN
*2) Apply to Cdrv, Pout0 to 7, SDA, SO, ERROR, INTOUT
*3) Single-layer glass epoxy board (76.1×114.3×1.6t mm)

Recommended Operating Conditions

Parameter	Symbol	Conditions	min	typ	max	Unit	Remarks
Operating supply voltage	V_{DD}		2.6		5.5	V	
Supply ripple + noise	Vpp				±20	mV	*1
Operating temperature	Topr		-40	25	105	°C	

*1) Inserting a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS} is recommended. In this case, the small-valued capacitor should be at least 0.1μF, and is mounted near the LSI.

Electrical Characteristics at V_{SS} = 0V, V_{DD} = 2.6 to 5.5V, Ta = -40 to +105°C

* Unless otherwise specified, the Cdrv drive frequency is f_{CDRV} = 143kHz.
* Not tested at low temperature before shipment.

Parameter	Symbol	Conditions	min	typ	max	Unit	Remarks
Capacitance detection resolution	N				8	bit	
Output noise RMS	N_{RMS}	minimum gain setting			±1.0	LSB	*1 *3
Input offset capacitance adjustment range	$Coff_{RANGE}$			±8.0		pF	*1 *3
Input offset capacitance adjustment resolution	$Coff_{RESO}$			8		bit	
Cin offset drift	Cin_{DRIFT}	minimum gain setting			±8	LSB	*1
Cin detection sensitivity	Cin_{SENSE}	minimum gain setting	0.04		0.12	LSB/fF	*2
Cin pin leak current	I_{Cin}	Cin = Hi-Z		±25	±500	nA	
Cin allowable parasitic input capacitance	Cin_{SUB}	Cin against V_{SS}			30	pF	*1 *3
Cdrv drive frequency	f_{CDRV}		100	143	186	kHz	
Cdrv pin leak current	I_{CDRV}	Cdrv = Hi-Z		±25	±500	nA	
nRST minimum pulse width	t_{NRST}		1			μs	*1
Power-on reset time	t_{POR}				20	ms	*1
Power-on reset operation condition: Hold time	t_{POROP}		10			ms	*1
Power-on reset operation condition: Input voltage	V_{POROP}				0.1	V	*1
Power-on reset operation condition: Power supply rise rate	t_{VDD}	0V to V_{DD}	1			V/ms	*1
Pin input voltage	V_{IH}	High input	0.8V_{DD}			V	*1 *4
	V_{IL}	Low input			0.2V_{DD}		
Pin output voltage	V_{OH}	High output (I_{OH} = +3mA)	0.8V_{DD}			V	*5
	V_{OL}	Low output (I_{OL} = -3mA)			0.2V_{DD}		

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Parameter	Symbol	Conditions	min	typ	max	Unit	Remarks
SDA pin leak current	V_{OL} I^2C	SDA Low output (I_{OL} = -3mA)			0.4	V	
Pin leak current	I_{LEAK}				±1	µA	*6
Current consumption	I_{DD}	When stand-alone configuration and non-touch V_{DD} = 2.8V		320	390	µA	*1 *3
		when stand-alone configuration and non-touch V_{DD} = 5.5V		740	900		
	I_{STBY}	During Sleep process			1	µA	*3

*1) Design-guaranteed values (not tested before shipment)
*2) Measurements conducted using the test mode in the LSI
*3) Ta = +25°C
*4) Apply to nRST, SCL, SDA, SA, SCK, SI, nCS, GAIN
*5) Apply to Cdrv, Pout0 to 7, SO, ERROR, INTOUT
*6) Apply to nRST, SCL, SDA, SA, SCK, SI, nCS, GAIN

I²C Compatible Bus Timing Characteristics at V_{SS} = 0, V_{DD} = 2.6 to 5.5V, Ta = -40 to +105°C
*Not tested at low temperature before shipment

Parameter	Symbol	Pin Name	Conditions	min	typ	max	Unit	Remarks
SCL clock frequency	f_{SCL}	SCL				400	kHz	
START condition hold time	$t_{HD;STA}$	SCL SDA		0.6			µs	
SCL clock low period	t_{LOW}	SCL		1.3			µs	
SCL clock high period	t_{HIGH}	SCL		0.6			µs	
Repeated START condition setup time	$t_{SU;STA}$	SCL SDA		0.6			µs	*1
Data hold time	$t_{HD;DAT}$	SCL SDA		0		0.9	µs	
Data setup time	$t_{SU;DAT}$	SCL SDA		100			µs	*1
SDA, SCL rise/fall time	t_r / t_f	SCL SDA				300	µs	*1
STOP condition setup time	$t_{SU;STO}$	SCL SDA		0.6			µs	
STOP-to-START bus release time	t_{BUF}	SCL SDA		1.3			µs	*1

*1) Design-guaranteed values (not tested before shipment)

SPI Bus Timing Characteristics at V_{SS} = 0, V_{DD} = 2.6 to 5.5V, Ta = -40 to +105°C
*Not tested at low temperature before shipment

Parameter	Symbol	Pin Name	Conditions	min	typ	max	Unit	Remarks
SCK clock frequency	f_{SCK}	SCK				5	MHz	
SCK clock Low time	t_{LOW}	SCK		90			ns	*1
SCK clock High time	t_{HIGH}	SCK		90			ns	*1
Input signal rise/fall time	t_r / t_f	nCS SCK SI				300	ns	*1
nCS setup time	$t_{SU;NCS}$	nCS SCK		90			ns	*1
SCK clock setup time	$t_{SU;SCK}$	nCS SCK		90			ns	*1
Data setup time	$t_{SU;SI}$	SCK SI		20			ns	*1
Data hold time	$t_{HD;SI}$	SCK SI		30			ns	*1
nCS hold time	$t_{HD;NCS}$	nCS SCK		90			ns	*1
SCK clock hold time	$t_{HD;SCK}$	nCS SCK		90			ns	*1
nCS standby pulse width	t_{CPH}	nCS		90			ns	*1
Output high impedance time from nCS	t_{CHZ}	nCS SO				80	ns	*1
Output data determination time	t_V	SCK SO				80	ns	*1
Output data hold time	$t_{HD;SO}$	SCK SO		0			ns	*1
Output low impedance time from SCK clock	t_{CLZ}	SCK SO		0			ns	*1

*1) Design-guaranteed values (not tested before shipment)

Power-on Reset (POR)

When power is turned on, power-on reset is enabled inside the LSI and its state is released after a certain power-on reset time, t_{POR}. Power-on reset operation condition: Power supply rise rate t_{VDD} must be at least 1V/ms.
Since INTOUT pin changes from "High" to "Low" at the same time as the released of power-on reset state, it is possible to verify the t_{POR} externally.
During power-on reset state, Cin, Cref and Pout are unknown.

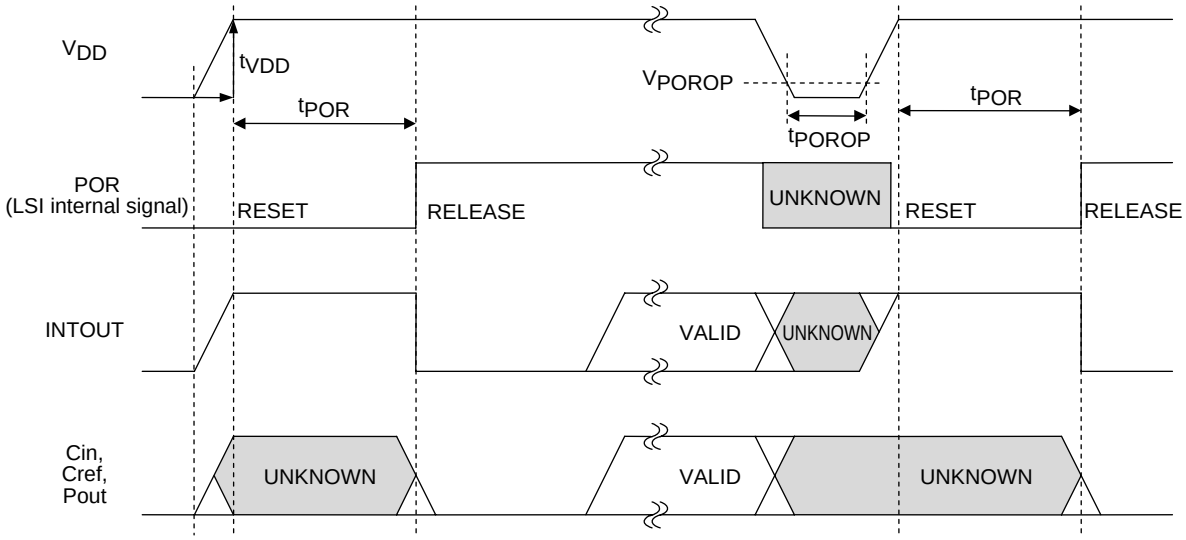


fig.1

I²C Compatible Bus Data Timing

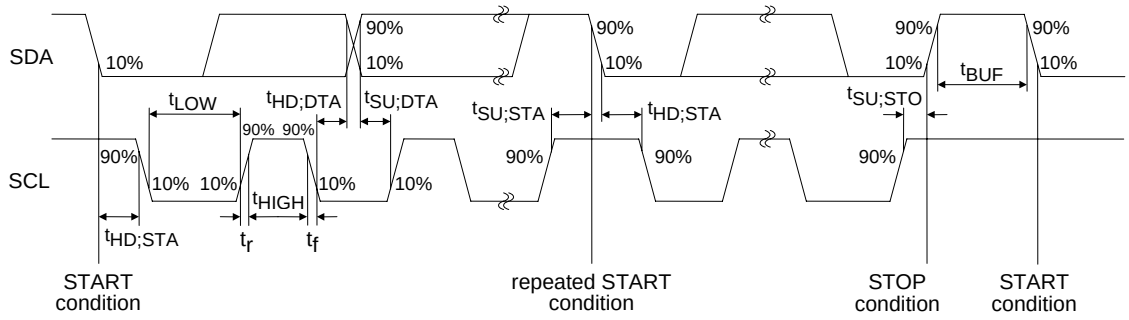


fig.2

I²C Compatible Bus Communication Formats

• Write format (data can be written into sequentially incremented addresses)

START	Slave Address	Write=L	ACK	Register Address (N)	ACK	Data written to Register Address (N)	ACK	Data written to Register Address (N+1)	ACK	STOP
			Slave		Slave		Slave		Slave	

fig.3

• Read format (data can be read from sequentially incremented addresses)

START	Slave Address	Write=L	ACK	Register Address (N)	ACK
			Slave		Slave

RESTART	Slave Address	Read=H	ACK	Data read from Register Address (N)	ACK	Data read from Register Address (N+1)	ACK	Data read from Register Address (N+2)	NACK	STOP
			Slave		Master		Master		Master	

fig.4

I²C Compatible Bus Slave Address

Selection of two kinds of addresses is possible through the SA terminal.

SA pin input	7bit Slave Address	Binary Notation	8bit Slave Address
Low	0x16	00101100b (Write)	0x2C
		00101101b (Read)	0x2D
High	0x17	00101110b (Write)	0x2E
		00101111b (Read)	0x2F

SPI Data Timing (SPI Mode 0 / Mode 3)

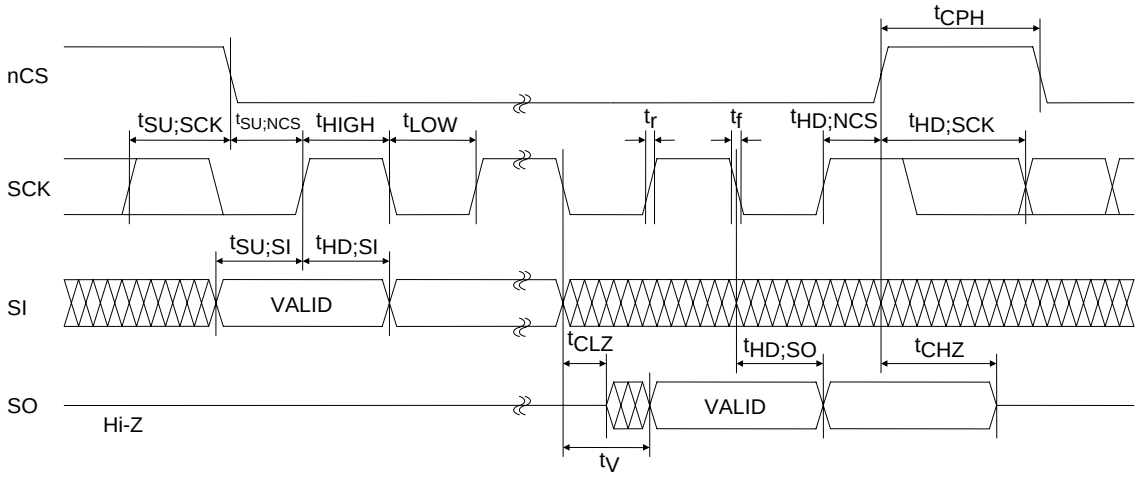


fig.5

SPI Communication Formats (Example of Mode 0)

• Write format (data can be written into sequentially incremented addresses while holding nCS = L)

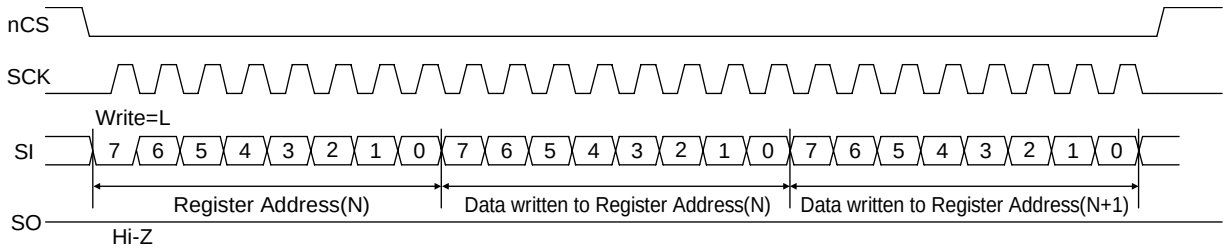


fig.6

• Read format (data can be read from sequentially incremented addresses while holding nCS = L)

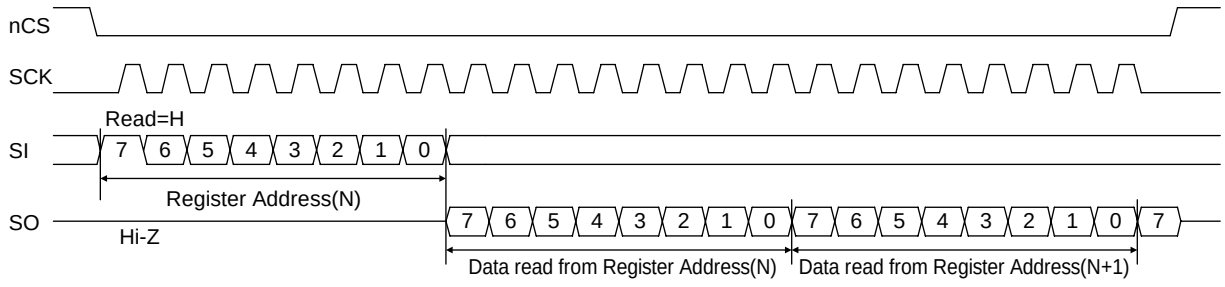
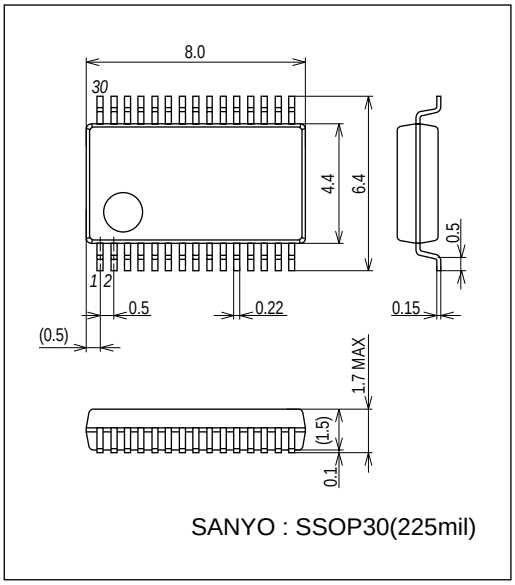


fig.7

Package Dimensions [LC717A00AJ]

unit : mm (typ)

3421



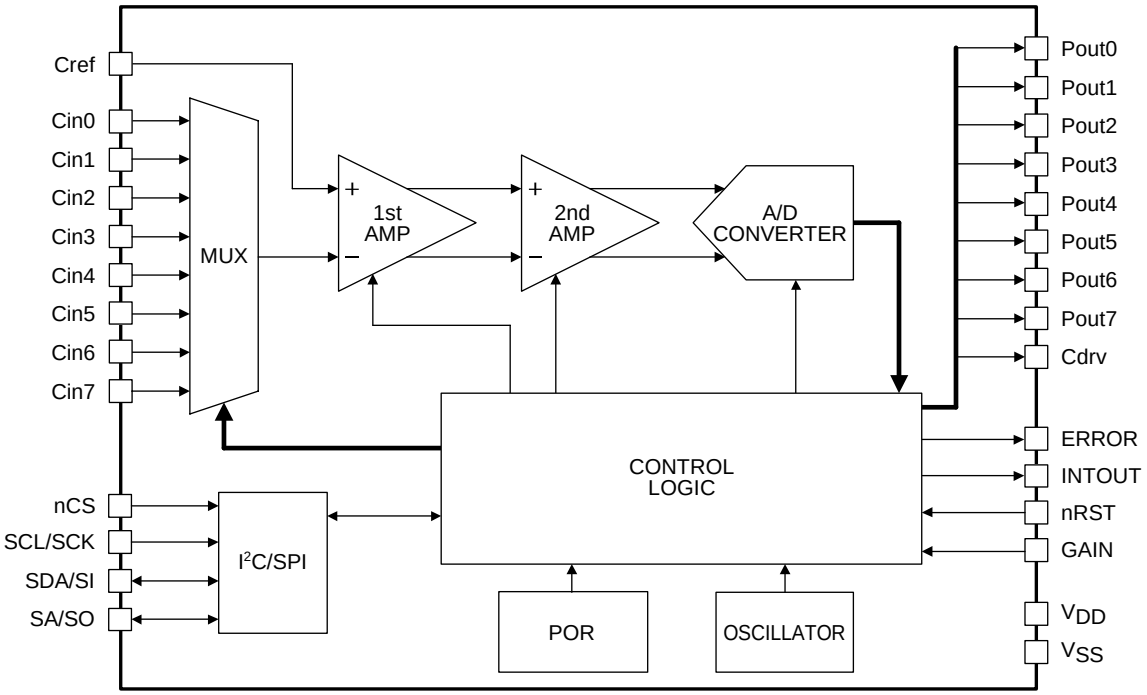
SANYO : SSOP30(225mil)

Pin Assignment

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DD}	16	Cref
2	V_{SS}	17	ERROR
3	Non Connect *1	18	Cdrv
4	Cin4	19	INTOUT
5	Cin5	20	GAIN
6	Cin6	21	SCL/SCK
7	Cin7	22	SDA/SI
8	Pout0	23	SA/SO
9	Pout1	24	nCS
10	Pout2	25	nRST
11	Pout3	26	Non Connect *1
12	Pout4	27	Cin0
13	Pout5	28	Cin1
14	Pout6	29	Cin2
15	Pout7	30	Cin3

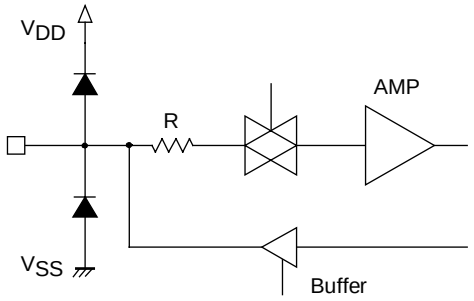
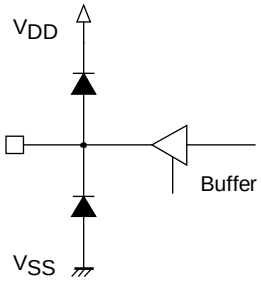
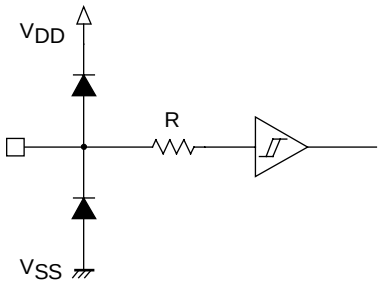
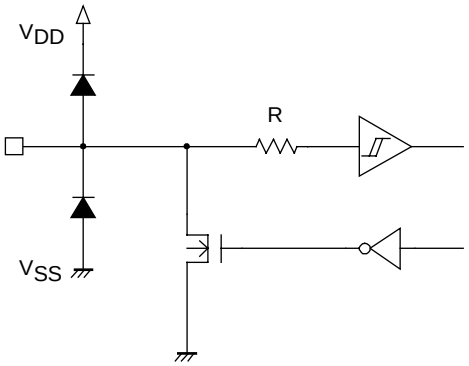
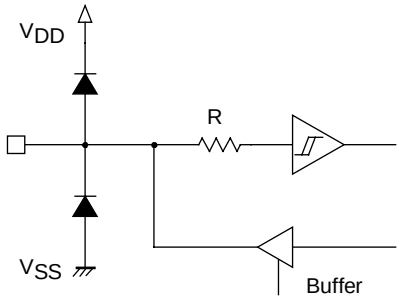
*1) connect to GND when mounted

Block Diagram



LC717A00AJ is capacitance-digital-converter LSI capable of detecting changes in capacitance in the femto Farad order. It consists of an oscillation circuit that generates the system clock, a power-on reset circuit that resets the system when the power is turned on, a multiplexer that selects the input channels, a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values, a A/D converter that converts the analog-amplitude values into digital data, and a control logic that controls the entire chip. Also, it has an I^2C compatible bus or SPI that enables serial communication with external devices as necessary.

Pin Functions

Pin Name	I/O	Pin Functions	Pin Type
Cin0	I/O	Capacitance sensor input	
Cin1	I/O	Capacitance sensor input	
Cin2	I/O	Capacitance sensor input	
Cin3	I/O	Capacitance sensor input	
Cin4	I/O	Capacitance sensor input	
Cin5	I/O	Capacitance sensor input	
Cin6	I/O	Capacitance sensor input	
Cin7	I/O	Capacitance sensor input	
Cref	I/O	Reference capacitance input	
Pout0	O	Cin0 judgment result output	
Pout1	O	Cin1 judgment result output	
Pout2	O	Cin2 judgment result output	
Pout3	O	Cin3 judgment result output	
Pout4	O	Cin4 judgment result output	
Pout5	O	Cin5 judgment result output	
Pout6	O	Cin6 judgment result output	
Pout7	O	Cin7 judgment result output	
ERROR	O	Error occurrence status output	
Cdrv	O	Output for capacitance sensors drive	
INTOUT	O	Interrupt output	
SCL/SCK	I	Clock input (I^2C) / Clock input (SPI)	
GAIN	I	Selection pin of the initial value of gain of the 2nd-amplifier	
nCS	I	Interface selection / Chip select inverting input (SPI)	
nRST	I	External reset signal inverting input	
SDA/SI	I/O	Data input and output (I^2C) / Data input (SPI)	
SA/SO	I/O	Slave address selection (I^2C) / Data output (SPI)	
V_{DD}		Power supply (2.6V to 5.5V) *1	
V_{SS}		Ground (Earth) *1 *2	

*1) Inserting a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS} is recommended. In this case, the small-valued capacitor should be at least 0.1μF, and is mounted near the LSI.

*2) When V_{SS} terminal is not grounded in battery-powered mobile equipment, detection sensitivity may be degraded.

Details of Pin Functions

●Cin0 to Cin7

These are the capacitance-sensor-input pins. These pins are used by connecting them to the touch switch pattern. Cin and the Cdrv wire patterns should be close to each other. By doing so, Cdrv and Cin patterns are capacitively coupled. Therefore, LSI can detect capacitance change near each pattern as 8bit digital data.
However, if the shape of each pattern or the capacitively coupled value of Cdrv is not appropriate, it may not be able to detect the capacitance change correctly.
In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. Cin0 to Cin7 are connected to the inverting input of the 1st amplifier.
During measurement process, channels other than the one being measured are all in "Low" condition.
Leave the unused terminals open.

●Cref

It is the reference-capacitance-input pin. It is used by connecting to the wire pattern like Cin pins or is used by connecting any capacitance between this pin and Cdrv pin.
In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. Cref is connected to the non-inverting input of the 1st amplifier.
Due to the parasitic capacitance generated in the wire connections of Cin pins and their patterns, as well as the one generated between the wire patterns of Cin and Cdrv pins, Cref may not detect capacitance change of each Cin pin accurately. In this case, connect an appropriate capacitance between Cref and Cdrv to detect capacitance change accurately.
However, if the difference between the parasitic capacitance of each Cin pin is extremely large, it may not detect capacitance change in each Cin pin correctly.

●Pout0 to Pout7

These are the detection-result-output pins. The capacitance detection results of Cin0 to Cin7 are compared with the threshold of the LSI. The pin outputs a "High" or a "Low" depending on the result.

●ERROR

It is the error-occurrence-status-output pin.
It outputs "Low" during normal operation. If there is a calibration error or a system error, it outputs "High" to indicate that an error occurred.

●Cdrv

It is the output pin for capacitance sensors drive. It outputs the pulse voltage which is needed to detect capacitance at Cin0 to Cin7.
Cdrv and Cin wire patterns should be close to each other so that they are capacitively coupled.

●INTOUT

It is the interrupt-output pin. It outputs "High" when a measurement process is completed.
Connect to a main microcomputer if necessary, and use as interrupt signal.
Leave the terminal open if not in used.

●SCL/SCK

Clock input (I^2C) / Clock input (SPI)
It is the clock input pin of the I^2C compatible bus or the SPI depending on the mode of operation.
If interface is not to be used, fix the pin to "High". However, even if interface is not to be used, providing a communication terminal on board is still recommended.

●GAIN

In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. It is the selection pin of the initial value of gain of the 2nd amplifier.
Even if this LSI is used alone, gain setting can still be selected through this terminal. At initialization of the LSI, it is set to 7-times higher than the minimum setting when GAIN pin is "Low", and is set to 14-times higher than the minimum setting when GAIN pin is "High".

●nCS

Interface selection / Chip-select-inverting input (SPI)

Selection of I^2C compatible bus mode or SPI mode is through this terminal. After initialization, the LSI is automatically in I^2C compatible bus mode. To continually use I^2C compatible bus mode, fix nCS pin to "High". To switch to SPI mode after LSI initialization, change the nCS input "High" → "Low". The nCS pin is used as the chip-select-inverting input pin of SPI, and SPI mode is kept until LSI is again initialized.

If interface is not to be used, fix the pin to "High".

●nRST

It is the external-reset-signal-inverting-input pin. When nRST pin is "Low", LSI is in the reset state.

Each pin (Cin0 to 7, Cref, Pout,0 to 7, ERROR) is "Hi-Z" during reset state.

●SDA/SI

Data input and output (I^2C) / Data input (SPI)

It is the data input and output pin of the I^2C compatible bus or the data input pin of the SPI depending on the mode of operation.

If interface is not to be used, fix the pin to "High". However, even if interface is not to be used, providing a communication terminal on board is still recommended.

●SA/SO

Slave address selection (I^2C) / Data output (SPI)

It is the slave address selection pin of the I^2C compatible bus or the data output pin of the SPI depending on the mode of operation.

If interface is not to be used, fix the pin to "High". However, even if interface is not to be used, providing a communication terminal on board is still recommended.