



Serial Interface Dialler

Overview

The LC73701M is a DTMP/pulse output dual-system dialler CMOS LSI for use in push-button telephones. It provides an on-chip serial interface and operates under the control of data sent over that serial interface. The LC73701M can be easily controlled by the system CPU using this dedicated interface.

Functions

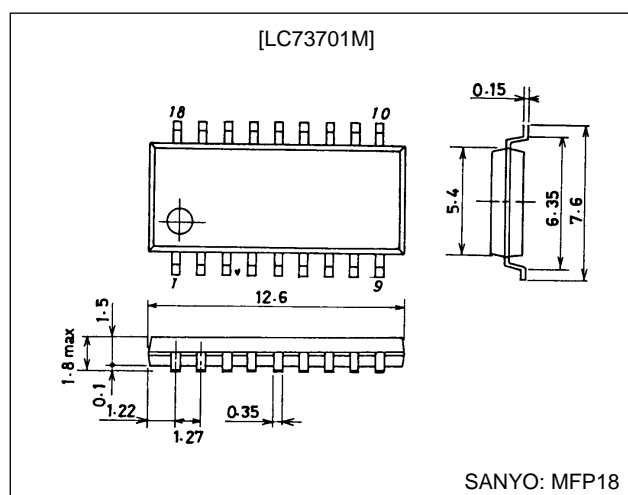
- Functions as a dialler that is controlled over a serial interface.
- The built-in oscillator circuit ($f_{OSC} = 4.19$ MHz) can use either a crystal oscillator or a ceramic resonator as its oscillator element.
- The adoption of a high-precision ($\pm 0.04\%$) DTMF signal frequency divider circuit allows a ceramic resonator to be used as the oscillator element.
- The buffer memory can store up to 32 digits of 5-bit data.
- Mode change and pause commands can also be stored as data in the buffer memory.
- Pauses can be inserted automatically on mode changes (auto-pause).
- A pause can be cancelled during that pause.
- The mode change function supports changing from pulse to tone (single direction).
- Generates all 16 DTMF signals.
- The pulse dialler output can be turned on or off arbitrarily.
- The pulse dialler output circuit can be selected to be either an n-channel open drain or a complementary circuit.
- The pulse dialler muting function can be turned on or off arbitrarily.
- A redial function is provided.
- Flash operation is supported. (Data can be received during flash operation.)
- The flash time can be switched to be either 277 or 707 ms.
- The pause time can be switched to be either 2 or 4 seconds.
- Hooking pause operation is supported. (1.2 s or 801 ms)
- The dial pulse rate can be specified to be either 10 pps or 20 pps.

- The dial pulse make ratio can be specified to be either 33 or 39%.
- Wide operating voltage range
Pulse mode: $V_{DD} = 1.5$ to 5.5 V
DTMF mode: $V_{DD} = 2.0$ to 5.5 V

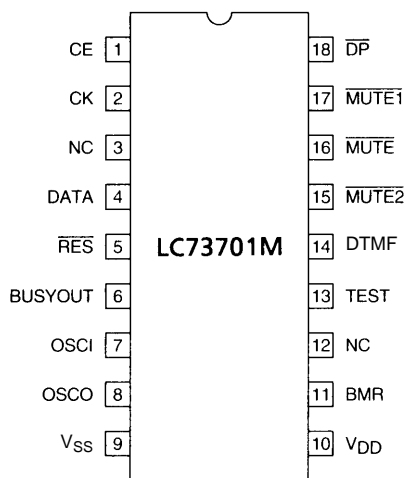
Package Dimensions

unit: mm

3095-MFP18



Pin Assignment



Top view

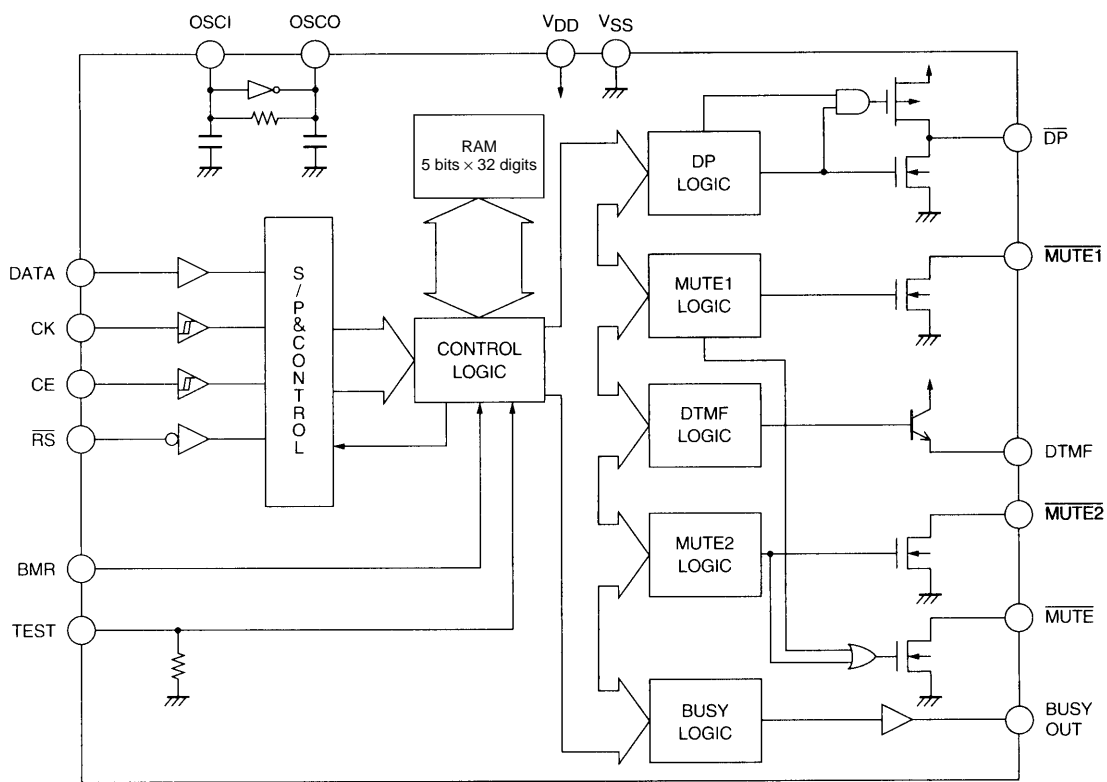
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Pin Functions

Pin No.	Pin	I/O	Pin function
1	CE	I	Set high when data is valid. This signal is also used when DTMF signals are issued consecutively in DTMF mode. The last DTMF signal is output until CE goes low.
2	CK	I	Data acquisition clock. Data is acquired on the rising edge of this signal.
3	NC		
4	DATA	I	Input for the 8-bit data.
5	$\overline{\text{RES}}$	I	Reset input. Apply a low level to this input to reset dialer operation when, for example, power is first applied.
6	BUSYOUT	O	Outputs a high level during dialer operation, including during pauses. This is a complementary output.
7	OSC1	I	Oscillator circuit connections. Connect either a crystal or ceramic 4.194304 MHz oscillator element to these pins.
8	OSCO	O	
9	V_{SS}		Power supply
10	V_{DD}		
11	BMR	I	Make ratio switching input. High: 33%, Low: 39%
12	NC		
13	TEST	I	LSI internal test pin. This pin either must be left open or must be tied low during normal operation.
14	DTMF	O	DTMF output. This is an npn emitter-follower output.
15	$\overline{\text{MUTE2}}$	O	DTMF mute output. This is an n-channel open-drain output.
16	$\overline{\text{MUTE}}$	O	DP and DTMF mute output. This is an n-channel open-drain output.
17	$\overline{\text{MUTE1}}$	O	DP mute output. This is an n-channel open-drain output.
18	$\overline{\text{DP}}$	O	DP output. This can be either an n-channel open-drain output or a complementary output.

Unused inputs must always be tied to an appropriate logic level, i.e. either ground or V_{DD} .

Block Diagram



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Input Code Table

D7	D6	D5	D4	D3	D2	D1	D0	WRITE TO RAM	Data interpretation and notes
X	0	0	0	0	0	0	0	YES	KEY D
X	0	0	0	0	0	0	1	YES	KEY 1
X	0	0	0	0	0	1	0	YES	KEY 2
X	0	0	0	0	0	1	1	YES	KEY 3
X	0	0	0	0	1	0	0	YES	KEY 4
X	0	0	0	0	1	0	1	YES	KEY 5
X	0	0	0	0	1	1	0	YES	KEY 6
X	0	0	0	0	1	1	1	YES	KEY 7
X	0	0	0	1	0	0	0	YES	KEY 8
X	0	0	0	1	0	0	1	YES	KEY 9
X	0	0	0	1	0	1	0	YES	KEY 0
X	0	0	0	1	0	1	1	YES	KEY *
X	0	0	0	1	1	0	0	YES	KEY #
X	0	0	0	1	1	0	1	YES	KEY A
X	0	0	0	1	1	1	0	YES	KEY B
X	0	0	0	1	1	1	1	YES	KEY C
X	0	0	1	0	0	0	0	NO	Illegal value
X	0	0	1	0	0	0	1	NO	Illegal value
X	0	0	1	0	0	1	0	NO	PAUSE clear (Only valid during a pause.)
X	0	0	1	0	0	1	1	NO	FLASH (707 or 277 ms)
X	0	0	1	0	1	0	0	NO	STOP (Forced termination of a the current dialing operation.)
X	0	0	1	0	1	0	1	NO	RD (redial)
X	0	0	1	0	1	1	0	NO	MUTE ST
X	0	0	1	0	1	1	1	NO	MUTE END
X	0	0	1	1	0	0	0	NO	ON-HOOK
X	0	0	1	1	0	0	1	NO	OFF-HOOK
X	0	0	1	1	1	0	0	YES	MODE-CH (Pulse to tone single-direction change)
X	0	0	1	1	1	0	1	YES	PAUSE (Pause for either 2.0 or 4.0 seconds.)

X : Don't care
Only bits D0 to D4 are written to RAM.

Mode Settings Command Table

D7	D6	D5	D4	D3	D2	D1	D0
X	MODE	TEST	DPSEL	PAUSE	FLASH	P/T	DPR
X	(1)	(0)	(0) N-CH OD	(0) 4.0 s	(0) 707.0 ms	(0) Tone	(0) 20 pps
X	(1)	(0)	(0) CMP	(1) 2.0 s	(1) 277.3 ms	(1) Pulse	(1) 10 pps

Flash time Hooking pause time
707.0 ms.....800.8 ms
277.3 ms.....1.23 s

Note that a hooking pause of 804.7 ms is also inserted automatically on a DP-off operation.

Mode Settings at Power On

When power is first applied, the initial settings listed in the table below are established according to the state of the BMR pin.

BMR PIN	DPSEL	PAUSE	FLASH	P/T	DPR
H (33.3%)	(0) N-CH OD	(0) 4.0 s	(0) 707.0 ms	(1) Pulse	(1) 10 pps
L (39.2%)	(0) N-CH OD	(0) 4.0 s	(0) 707.0 ms	(0) Tone	(1) 10 pps

Specifications

Absolute Maximum Ratings at Ta = 25°C, fOSC = 4.194304 MHz

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max		-0.3 to +6.5	V
Maximum input voltage	V _{IN} max		-0.3 to V _{DD} +0.3	V
Maximum output voltage	V _{OUT} max		-0.3 to V _{DD} +0.3	V
Allowable power dissipation	Pd max	Ta 70°C	180	mW
Minimum load resistance	R _L min	Between the DTMF and the V _{SS} pins	1	k
Operating temperature	T _{opr}		-30 to +70	°C
Storage temperature	T _{stg}		-40 to +125	°C

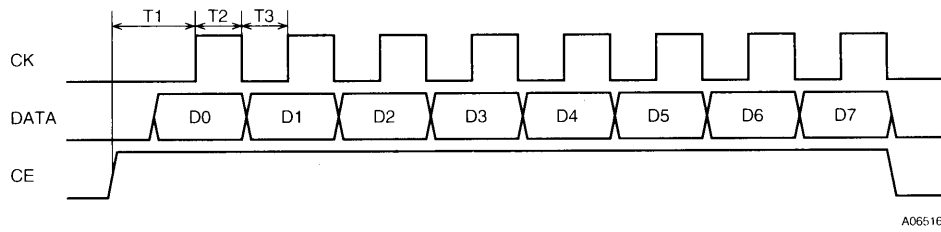
Allowable Operating Ranges at Ta = 25°C, fOSC = 4.194304 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V _{DDP}	Pulse mode	1.5		5.5	V
	V _{DDT}	DTMF mode	2.0		5.5	V
Input high-level voltage	V _{IHS}	CK and CE input pins	0.8 V _{DD}		V _{DD}	V
	V _{IH}	Input pins other than CK and CE	0.7 V _{DD}		V _{DD}	V
Input low-level voltage	V _{ILS}	CK and CE input pins	V _{SS}		0.2 V _{DD}	V
	V _{IL}	Input pins other than CK and CE	V _{SS}		0.3 V _{DD}	V
Oscillator pin rating	f	Center frequency = 4.194304 MHz	-1.4		+1.4	%
	R _S				100	

Electrical Characteristics at Ta = 25°C, fOSC = 4.194304 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current drain	I _{DDP}	In dial pulse output mode, output open V _{DD} = 3.0 V : V _{DD}		0.3	0.5	mA
	I _{DDT}	In DTMF output mode, output open, V _{DD} = 3.0 V : V _{DD}		0.5	1.0	mA
	I _{DD(ST)}	Standby mode, output open V _{DD} = 1.5 to 5.5 V : V _{DD}			1	μA
Memory retention voltage	V _{DR}	Between V _{DD} and V _{SS} : V _{DD}	1			V
Memory retention current	I _{DR}	V _{DD} = 1.0 V : V _{DD}			0.5	μA
Input pin current	I _{IHI}	V _{IH} = V _{DD} , V _{DD} = 5.5 V : DATA, CK, CE, BMR, \overline{RS}			1	μA
	I _{ILI}	V _{IL} = V _{SS} , V _{DD} = 5.5 V : DATA, CK, CE, BMR, \overline{RS}	-1			μA
	I _{IHIT}	V _{IH} = V _{DD} , V _{DD} = 5.5 V : TEST		160	330	μA
	I _{ILIT}	V _{IL} = V _{SS} , V _{DD} = 5.5 V : TEST	-1			μA
Output pin leakage current	I _{OFF}	V _{OH} = V _{DD} , V _{DD} = 5.5 V, when the output is off: BUSYOUT			1	μA
Output pin voltage	V _{OH1}	V _{DD} = 1.5 V, I _{OH} = -250 μA : BUSYOUT	V _{DD} -0.5			V
	V _{OH2}	V _{DD} = 5.5 V, I _{OH} = -1 mA : BUSYOUT, \overline{DP} , MUTE1, MUTE2, MUTE	V _{DD} -1			V
	V _{OL1}	V _{DD} = 1.5 V, I _{OL} = 250 μA : BUSYOUT, \overline{DP} , MUTE1, MUTE2, MUTE			0.4	V
	V _{OL2}	V _{DD} = 5.5 V, I _{OL} = 1 mA : BUSYOUT, \overline{DP} , MUTE1, MUTE2, MUTE			0.4	V

Dialer Input Format



The serial data is input starting with the LSB.

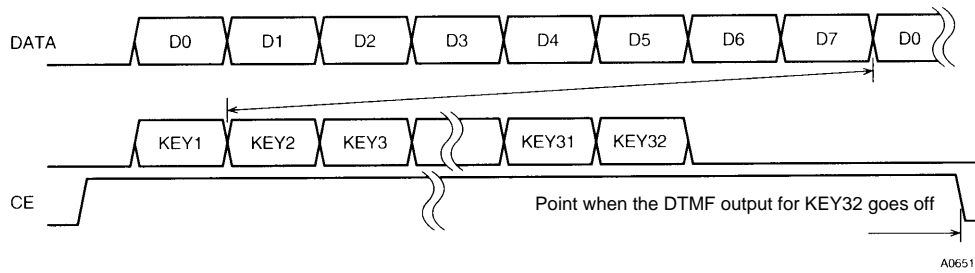
T1 must be at least 6.5 μ s (When an external clock is supplied to OSC1.)

If an oscillator element is used, T1 depends on the oscillator startup time for that oscillator element.

*: For example, for ceramic oscillators, T1 will be about 1 ms ($V_{DD} = 3.0$ to 5.5 V).

T2 and T3 must be at least 1.0 μ s.

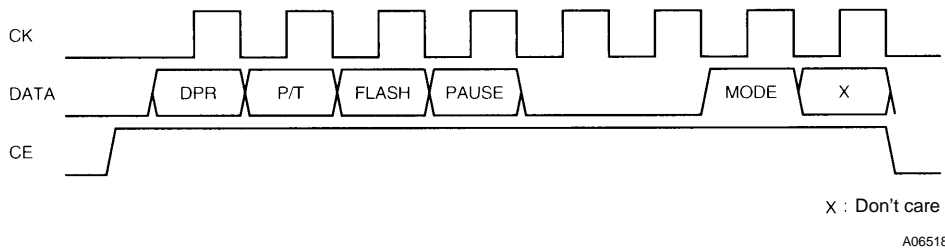
Serial Data Sequential Input Format



KEY1 to KEY31 are guaranteed by the DTMF output time.

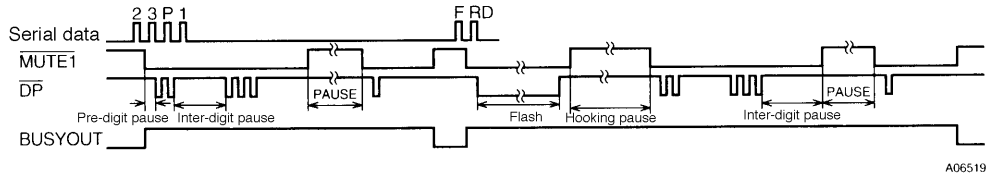
*: Continuous input is limited to dial data. Continuous input of mode setting commands is not possible.

Mode Settings Format

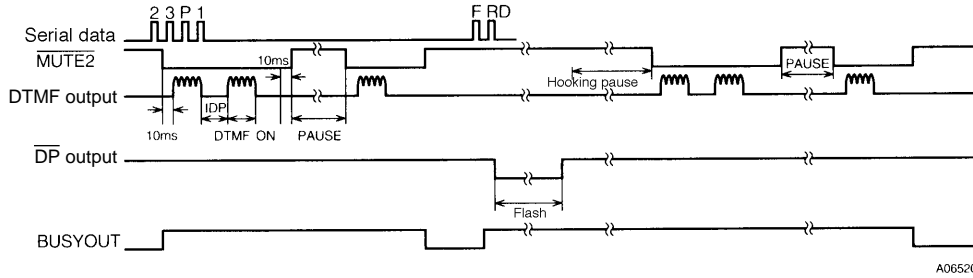


Timing Charts

(1) Pulse mode



(2) Tone mode



AC Characteristics at Ta = 25°C, fOSC = 4.194304 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Pause time	T _{AP}	When the D3 mode setting code is low (0)		4.0		s
		When the D3 mode setting code is high (1)		2.0		s
DTMF output time	T _{MFON}			100.6		ms
DTMF inter-digit pause time	T _{MFOFF}	For the first and later digits		114.0		ms
		For the last digit		109.9		ms
Flash time	T _{FL}	When the D2 mode setting code is low (0)		707.0		ms
		When the D2 mode setting code is high (1)		277.3		ms
Hooking pause time	T _{HKP}	When the D2 mode setting code is low (0)		800.8		ms
		When the D2 mode setting code is high (1)		1.23		s
Low tone amplitude	V _{OR}	V _{DD} = 3.5 V, R _L = 10 k	165	200	240	mVrms
Tone output ratio	dBCR	V _{DD} = 2.0 to 5.5 V, R _L = 10 k	1	2	3	dB
Tone output distortion	%DIS	V _{DD} = 2.0 to 5.5 V, R _L = 10 k			10	%

Pulse Output at Ta = 25°C, fOSC = 4.194304 MHz

DPR	BMR	Dial pulse rate	Pre-digit pause	Inter-digit pause	Make ratio
H	H	9.97 PPS	33.3 + 10 ms	839.0 ms	33.3%
H	L	9.97 PPS	39.2 + 10 ms	844.9 ms	39.2%
L	H	19.93 PPS	16.7 + 10 ms	571.6 ms	33.3%
L	L	19.93 PPS	19.7 + 10 ms	574.6 ms	39.2%

DTMF Output Frequencies at Ta = 25°C, fOSC = 4.194304 MHz

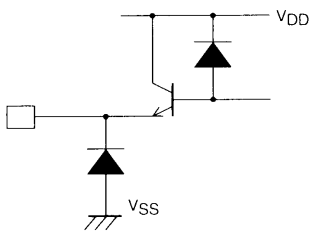
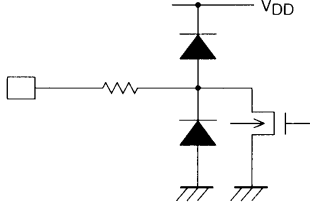
Input	Output frequency (Hz)		Deviation (%)
	Rating	LC73701	
R1	697	697.2	+0.027
R2	770	769.9	-0.016
R3	852	851.8	-0.023
R4	941	941.3	+0.029
C1	1209	1209.4	+0.036
C2	1336	1335.8	-0.018
C3	1477	1476.9	-0.009
C4	1633	1633.3	+0.018

Internal Pin Circuits

Pin No.	Pin	Internal circuit
1 2	CE CK	<p>A06521</p>
4 5 11	DATA $\overline{\text{RES}}$ BMR	<p>A06522</p>
6 18	BUSYOUT $\overline{\text{DP}}$	<p>A06523</p>
7 8	OSCI OSCO	<p>A06524</p>
15 16 17	$\overline{\text{MUTE2}}$ $\overline{\text{MUTE}}$ $\overline{\text{MUTE1}}$	<p>A06525</p>
13	TEST	<p>A06526</p>

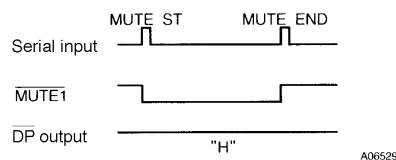
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Pin No.	Pin	Internal circuit
14	DTMF	 <p style="text-align: right;">A06527</p>
18	\overline{DP}	 <p style="text-align: right;">A06528</p>

Notes:

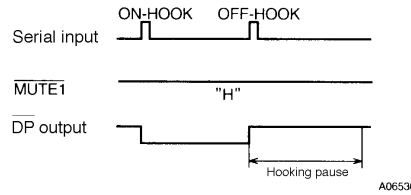
- (1) The LC73701M output ports are initialized to the following states when power is first applied.
 - BUSYOUT and \overline{DP} pins: Low
 - DTMF, $\overline{MUTE1}$, \overline{MUTE} , and $\overline{MUTE2}$ pins: High-impedance
 - OSC0 pin: High
- (2) The following methods can be used to forcibly terminate dial output.
 1. STOP command input
 - Output ports: The \overline{DP} and $\overline{MUTE1}$ pins hold their previous states, all others are initialized.
 - Redialing is possible after a STOP command is input. However, this requires that a dialing operation had been performed previously.
 2. Applying a low-level pulse (of at least 1 μ s) to the \overline{RES} pin.
 - The operation is identical to that of the STOP command.
 - However, redialing is not possible after this hardware reset.
 3. ON-HOOK command input
 - The \overline{DP} pin goes low, thus releasing the telephone line (circuit). Redialing is possible after an ON-HOOK command is input. However, if this dialing operation is performed, although DTMF signals will be output, since the \overline{DP} is low dial pulses will not be output. (Since the LSI performs a redial operation internally, the BUSYOUT pin will go high and the associated muting signal will also be output.)
 4. OFF-HOOK command input
 - A hooking pause will be inserted automatically after the OFF-HOOK command input. Redialing is possible.
 5. FLASH command input
 - A hooking pause will be inserted automatically after the FLASH command input. Redialing is possible.
- (3) The MUTE ST and MUTE END commands
 - These commands allows the $\overline{MUTE1}$ pin to be controlled arbitrarily. The other muting outputs cannot be controlled explicitly.
 - The figure below shows the timing.



When a MUTE ST command is input, the $\overline{MUTE1}$ pin goes low. During this low period, inputting pulse dial data will not cause the $\overline{MUTE1}$ pin to return to the high level. That is, the low level is held until the next MUTE END command is input.

(4) The ON-HOOK and OFF-HOOK commands

These commands allows the \overline{DP} pin to be controlled arbitrarily. The figure below shows the timing.



A hooking pause is inserted automatically when the OFF-HOOK command is input. The \overline{DP} pin goes low when an ON-HOOK command is input. During this low period, inputting pulse dial data will not cause the \overline{DP} pin to return to the high level. (Since the LSI performs a redial operation internally, the BUSYOUT pin will go high.) That is, the low level is held until the next OFF-HOOK command is input.

(5) The redial command

The redial operation re-outputs the dial data in the LC73701M's internal buffer memory. This buffer memory (redial memory) can hold up to 32 digits of dialing data. This means that if 33 or more digits of dialing data are input, earlier data will be overwritten starting with the thirty-third digit. After the following operations, the LC73701M will perform a redial operation if a redial command is input.

1. When a flash command is input after dialing data has been input
2. When an STOP command is input after dialing data has been input
3. When an ON-HOOK command is input after dialing data has been input
4. When an OFF-HOOK command is input after dialing data has been input

(6) Mode settings

The break/make ratio (BMR) is switched between 33% and 39% by the BMR pin. The BMR pin is initialized after power is first applied as shown in the table below.

BMR PIN	DPSEL	PAUSE	FLASH	P/T	DPR
H (33.3%)	(0) N-CH OD	(0) 4.0 s	(0) 707.0 ms	(1) Pulse	(1) 10 pps
L (39.2%)	(0) N-CH OD	(0) 4.0 s	(0) 707.0 ms	(0) Tone	(1) 10 pps

Settings other than BMR (i.e. DPR, P/T, FLASH, PAUSE, and DPSEL) are switched using mode commands. The information set by mode setting commands is stored internally by the LSI. Set the desired mode before inputting dial data. When dial data is written to the buffer memory, the P/T register data is attached to that dial data.

(7) Output pins during dialing and the redial operation

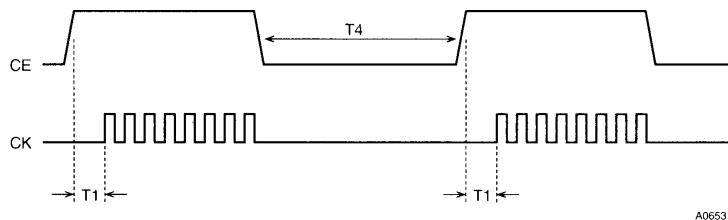
See the table below. The terms ON and OFF in the table below refer to the on or off state of the n-channel open drain output transistor.

	\overline{DP}	MUTE1	MUTE, MUTE2	BUSYOUT	Redial memory
Power on	ON (L)	OFF	OFF	L	Readout is illegal
RES pin	ON (L)	*1 OFF	OFF	L	Readout is illegal
STOP command	*2 OFF (H)	*3 OFF	OFF	L	Readout allowed
ON-HOOK command	ON (L)	Retains the previous state	OFF	L	Readout allowed
OFF-HOOK command	OFF (H)	Retains the previous state	OFF	*4 H	Readout allowed
MUTE-ST command	Retains the previous state	ON	OFF	L	Readout allowed
MUTE-END command	Retains the previous state	OFF	OFF	L	Readout allowed

Notes: *2 Turned off during dialing. However, since this command takes priority after an OFF-HOOK command is input, the on state is retained.
 *1, 3: Turned off during dialing. However, since this command takes priority after a MUTE-ST command is input, the on state is retained.
 *4: Since a hooking pause is inserted automatically, this output goes high during that operation.

(8) CE input format (When an oscillator element is used.)

The figure below shows the CE timing.



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Although in the timing shown in the previous figure, T1 depends on the oscillator element startup time, here, this time does not need to be provided in the T1 period as long as it can be provided by the T4 period. For example, assume that the oscillator startup time when a ceramic oscillator is used is about 1 ms (when $V_{DD} = 3.0$ to 5.5 V). In this case, this time must be provided by either setting $T1 = 1$ ms, or by setting $T4 = 1$ ms. However, note that T1 must be 6.5 μ s or greater and T4 must be 1 μ s or greater.

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