Ordering number : ENA1885

SANYO Semiconductors
DATA SHEET

LC749402PT — CMOS IC Silicon gate LCD Picture Quality Improvement IC

Overview

LC749402PT is a picture quality improvement IC that processes the output signals to the LCD panel for high picture quality display. This IC performs various picture quality adjustments to provide the ideal correction for the display panel. It can support up to WVGA/SVGA panels. *

Features

(1) Digital input/output
- Digital YCbCr/YPbPr 24bit (4:4:4) or 16bit (4:2:2) or 8bit (ITU-R BT.656) signal input
- Digital RGB 24bit signal input
- Digital RGB 18bit/24bit signal output
- Digital YCbCr 16bit (4:2:2)/24bit (4:4:4) signal output

(2) Image quality correction
- Y image quality correction: luminance adjustment, contour correction, CDEX (Color Depth Expander), dynamic-γ, black/white stretch
- C image quality correction: color exciter, flesh tone correction, hue, color gain
- RGB image quality correction: brightness, contrast, white balance, black balance, γ correction

(3) Panel interface
- Built-in panel driver timing controller
- Panel protection timing signal generation
- Backlight control PWM (video adaptive low power consumption processing)

*: The LC749402PT video input should satisfy the following conditions:
40MHz or less operating frequency, 896 dots or less horizontal size, 768 lines or less vertical size.

SANYO Semiconductor Co., Ltd.
http://semicon.sanyo.com/en/network

LSI Specifications

- Supply voltage Core: 1.2V
  I/O: 1.8V/2.85V/3.3V
- Maximum operating frequency: 40MHz
- Package: TQFP100

Principal Applications

- LCD display equipment

CDEX (Color Depth Expander)

Original

CDEX

Specifications

Absolute Maximum Ratings at Ta = 25°C, DV_{SS} = 0V, AV_{SS}_OSC = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (I/O)	DV_{DD}_IO		-0.3 to +3.96	V
Maximum supply voltage (core)	DV_{DD}_CORE AV_{DD}_OSC		-0.3 to +1.8	V
Digital input voltage	V_I		-0.3 to DV_{DD}_IO+0.3	V
Digital output voltage	V_O		-0.3 to DV_{DD}_IO+0.3	V
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta = -40 to +85°C, DV_{SS} = 0V, AV_{SS}_OSC = 0V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage (I/O)	DV_{DD}_IO		2.6	2.85	3.6	V
			1.7	1.8	1.9	V
Supply voltage (core)	DV_{DD}_CORE AV_{DD}_OSC		1.1	1.2	1.3	V
Input voltage range	V_{IN}		0		DV_{DD}_IO	V

DC Characteristics at Ta = -40 to +85°C, DV_{SS} = 0V, AV_{SS}_OSC = 0V,

DV_{DD}_IO = 1.7V to 1.9V or 2.6V to 3.6V, DV_{DD}_CORE = 1.1V to 1.3V

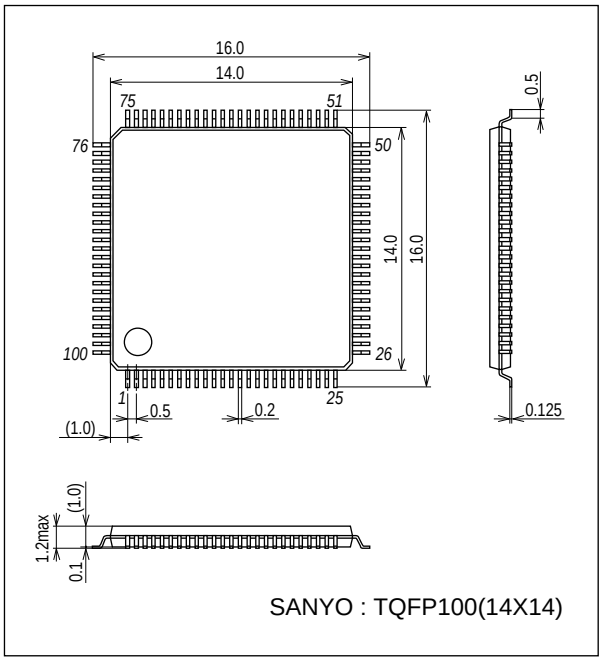
Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Input high-level voltage	V_{IH}	CMOS level inputs	0.7DV_{DD}_IO			V
		CMOS level schmitt inputs	0.7DV_{DD}_IO			V
Input low-level voltage	V_{IL}	CMOS level inputs			0.3DV_{DD}_IO	V
		CMOS level schmitt inputs			0.3DV_{DD}_IO	V
Input high-level current	I_{IH}	V_I=DV_{DD}_IO			10	µA
		V_I=DV_{DD}_IO, with pull-down resistance			100	µA
Input low-level current	I_{IL}	V_I=DV_{SS}	-10			µA
Output high-level voltage	V_{OH}	CMOS voltage: 2.6V to 3.6V Pin D: I_{OH}=-2mA Pin F: I_{OH}=-2mA (when set to 2mA) I_{OH}=-4mA (when set to 4mA) Pin G: I_{OH}=-4mA (when set to 4mA) I_{OH}=-8mA (when set to 8mA) Pin H: I_{OH}=-4mA	DV_{DD}_IO-0.4			V
		CMOS voltage: 1.7V to 1.9V Pin D: I_{OH}=-1mA Pin F: I_{OH}=-1mA (when set to 2mA) I_{OH}=-2mA (when set to 4mA) Pin G: I_{OH}=-2mA (when set to 4mA) I_{OH}=-4mA (when set to 8mA) Pin H: I_{OH}=-2mA	DV_{DD}_IO-0.45			V
Output low-level voltage	V_{OL}	CMOS			0.4	V
Output leak current	I_{OZ}	At output of high-impedance	-10		10	µA
Pull-down resistor	R_{DN}	Typical conditions: Ta=25°C DV_{DD}_IO=2.85V DV_{DD}_CORE=1.2V		98		kΩ
Dynamic supply current	I_{DDOP}	Typical conditions: Ta=25°C DV_{DD}_IO=2.85V DV_{DD}_CORE=1.2V tck=10MHz 10 steps		18		mA
		Typical conditions: Ta=25°C DV_{DD}_IO=2.85V DV_{DD}_CORE=1.2V tck=40MHz 10 steps		57		mA
Static supply current *1	I_{DDST}	Typical conditions: Ta=25°C DV_{DD}_IO=2.85V DV_{DD}_CORE=1.2V Outputs open V_I=DV_{SS} or DV_{DD}_IO		20		µA

*1: There is a input terminal which builds in pull down resistance. Please note that there is no guarantee about static consumption current depending on circuit composition.

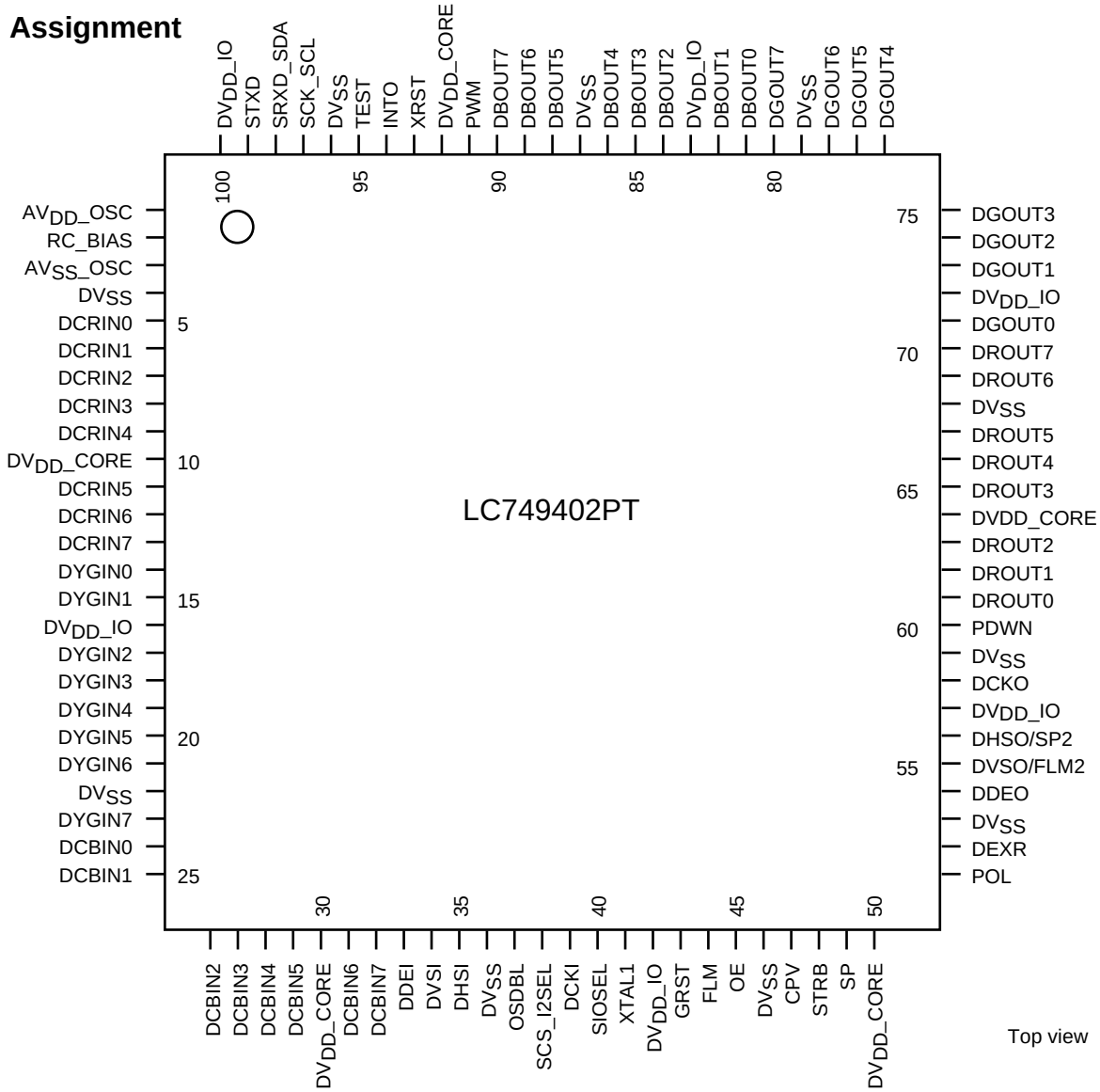
Package Dimensions

unit:mm (typ)

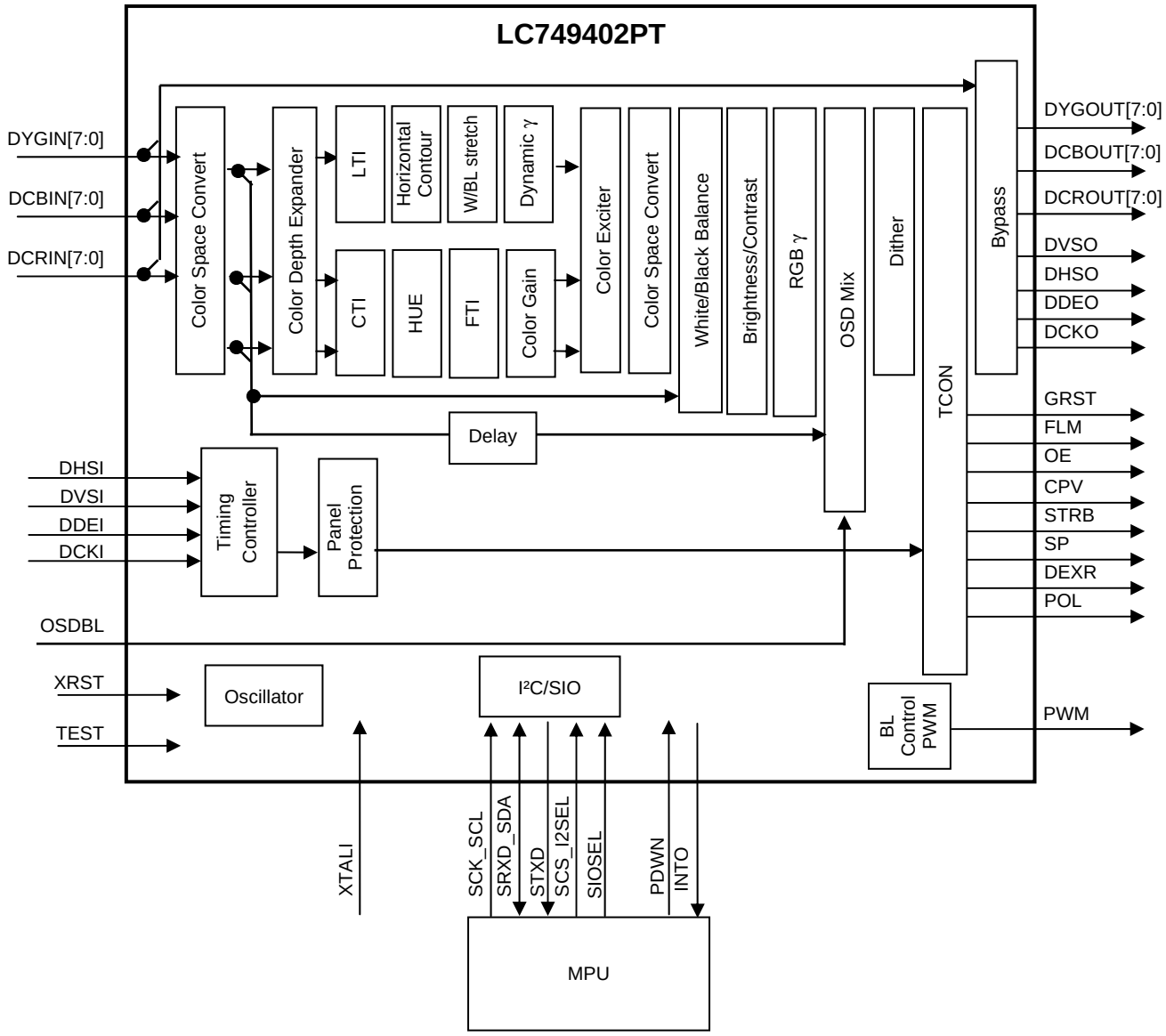
3274



Pin Assignment



Block Diagram



Pin Functions

Pin No.	Pin symbol	In/output format		Connecting destination		Remarks
		I/O	Format			
1	AV_{DD}_OSC	P	-	Core Voltage	Analog	
2	RC_BIAS	I	J	Resistor	Analog	Bias resistor connection (Connect to ground through 20kΩ resistor)
3	AV_{SS}_OSC	P	-	GND	Analog	
4	DV_{SS}	P	-	GND	Digital	
5	DCRIN0	I	C	CMOS	Digital	R/Cr video input. (LSB Connect to GND when not used.)
6	DCRIN1	I	C	CMOS	Digital	R/Cr video input. (Connect to GND when not used.)
7	DCRIN2	I	C	CMOS	Digital	R/Cr video input (Connect to GND when not used.)
8	DCRIN3	I	C	CMOS	Digital	R/Cr video input (Connect to GND when not used.)
9	DCRIN4	I	C	CMOS	Digital	R/Cr video input (Connect to GND when not used.)
10	DV_{DD}_CORE	P	-	Core Voltage	Digital	
11	DCRIN5	I	C	CMOS	Digital	R/Cr video input (Connect to GND when not used.)
12	DCRIN6	I	C	CMOS	Digital	R/Cr video input (Connect to GND when not used.)
13	DCRIN7	I	C	CMOS	Digital	R/Cr video input (MSB Connect to GND when not used.)
14	DYGIN0	I	C	CMOS	Digital	G/Y/656 video input (LSB Connect to GND when not used.)
15	DYGIN1	I	C	CMOS	Digital	G/Y/656 video input (Connect to GND when not used.)
16	DV_{DD}_IO	P	-	IO voltage	Digital	
17	DYGIN2	I	C	CMOS	Digital	G/Y/656 video input (Connect to GND when not used.)
18	DYGIN3	I	C	CMOS	Digital	G/Y/656 video input (Connect to GND when not used.)
19	DYGIN4	I	C	CMOS	Digital	G/Y/656 video input (Connect to GND when not used.)
20	DYGIN5	I	C	CMOS	Digital	G/Y/656 video input (Connect to GND when not used.)
21	DYGIN6	I	C	CMOS	Digital	G/Y/656 video input (Connect to GND when not used.)
22	DV_{SS}	P	-	GND	Digital	
23	DYGIN7	I	C	CMOS	Digital	G/Y/656 video input (MSB Connect to GND when not used.)
24	DCBIN0	I	C	CMOS	Digital	B/Cb/C video (LSB Connect to GND when not used.)
25	DCBIN1	I	C	CMOS	Digital	B/Cb/C video input (Connect to GND when not used.)
26	DCBIN2	I	C	CMOS	Digital	B/Cb/C video input (Connect to GND when not used.)
27	DCBIN3	I	C	CMOS	Digital	B/Cb/C video input (Connect to GND when not used.)
28	DCBIN4	I	C	CMOS	Digital	B/Cb/C video input (Connect to GND when not used.)
29	DCBIN5	I	C	CMOS	Digital	B/Cb/C video input (Connect to GND when not used.)
30	DV_{DD}_CORE	P	-	Core Voltage	Digital	
31	DCBIN6	I	C	CMOS	Digital	B/Cb/C video input (Connect to GND when not used.)
32	DCBIN7	I	C	CMOS	Digital	B/Cb/C video input (MSB Connect to GND when not used.)
33	DDEI	I	C	CMOS	Digital	Data enable signal. (Connect to GND when not used.)
34	DVSI	I	C	CMOS	Digital	Vertical sync signal
35	DHSI	I	C	CMOS	Digital	Horizontal sync signal.
36	DV_{SS}	P	-	GND	Digital	
37	OSDBL	I	C	CMOS	Digital	Data enable signal for external OSD. (Connect to GND when not used.)
38	SCS_I2SEL	I	A	CMOS	Digital	SIO chip enable / I^2C slave select
39	DCKI	I	C	CMOS	Digital	Video clock.
40	SIOSEL	I	C	CMOS	Digital	”L”: I^2C slave, ”H”: 4 wire SIO
41	XTAL1	I	C	CMOS	Digital	Extarnal clock input for panel protection. (Connect to GND when not used.)
42	DV_{DD}_IO	P	-	IO voltage	Digital	
43	GRST	O	F	CMOS	Digital	Gate driver reset signal.
44	FLM	O	F	CMOS	Digital	Start pulse signal for gate driver
45	OE	O	F	CMOS	Digital	Output enable signal for gate driver.
46	DV_{SS}	P	-	GND	Digital	
47	CPV	O	F	CMOS	Digital	Gate driver clock signal.
48	STRB	O	F	CMOS	Digital	Data strobe signal for source driver.
49	SP	O	F	CMOS	Digital	Start pulse signal for sourse driver.

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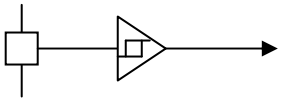
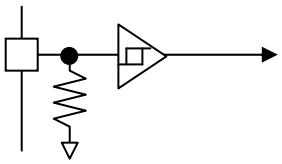
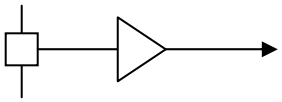
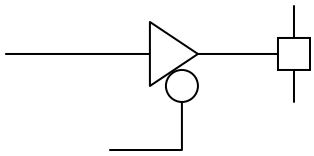
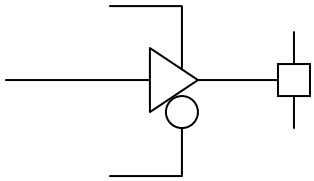
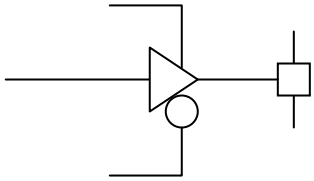
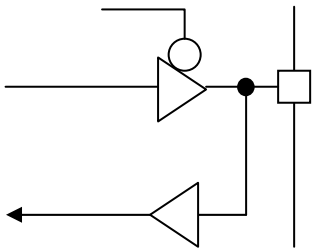
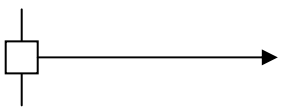
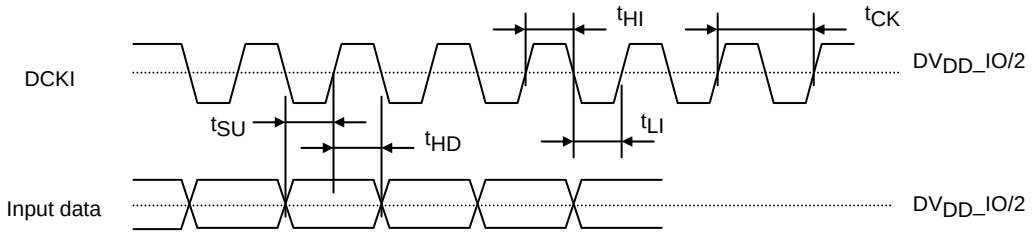
Pin No.	Pin symbol	In/output format		Connecting destination		Remarks
		I/O	Format			
50	DV_{DD}_CORE	P	-	Core Voltage	Digital	
51	POL	O	F	CMOS	Digital	Voltage polarity selection signal for the source driver.
52	DEXR	O	F	CMOS	Digital	Reversed video signal output for DTR. Low output when the DTR is OFF.
53	DV_{SS}	P	-	GND	Digital	
54	DDEO	O	F	CMOS	Digital	Data enable signal
55	DVSO / FLM2	O	F	CMOS	Digital	Vertical sync signal / Start pulse signal for gate driver
56	DHSO / SP2	O	F	CMOS	Digital	Horizontal sync signal / Start pulse signal for sourse driver
57	DV_{DD}_IO	P	-	IO voltage	Digital	
58	DCKO	O	G	CMOS	Digital	Video clock output
59	DV_{SS}	P	-	GND	Digital	
60	PDWN	I	A	CMOS	Digital	“H” power down control (Connect to GND when not used.)
61	DROUT0	O	F	CMOS	Digital	R/Cr video output (LSB when 8-bit output is selected)
62	DROUT1	O	F	CMOS	Digital	R/Cr video output
63	DROUT2	O	F	CMOS	Digital	R/Cr video output (LSB when 6-bit output is selected)
64	DV_{DD}_CORE	P	-	Core Voltage	Digital	
65	DROUT3	O	F	CMOS	Digital	R/Cr video output
66	DROUT4	O	F	CMOS	Digital	R/Cr video output
67	DROUT5	O	F	CMOS	Digital	R/Cr video output
68	DV_{SS}	P	-	GND	Digital	
69	DROUT6	O	F	CMOS	Digital	R/Cr video output
70	DROUT7	O	F	CMOS	Digital	R/Cr video output (MSB)
71	DGOUT0	O	F	CMOS	Digital	G/Y video output (LSB when 8-bit output is selected)
72	DV_{DD}_IO	P	-	IO voltage	Digital	
73	DGOUT1	O	F	CMOS	Digital	G/Y video output
74	DGOUT2	O	F	CMOS	Digital	G/Y video output (LSB when 6-bit output is selected)
75	DGOUT3	O	F	CMOS	Digital	G/Y video output
76	DGOUT4	O	F	CMOS	Digital	G/Y video output
77	DGOUT5	O	F	CMOS	Digital	G/Y video output
78	DGOUT6	O	F	CMOS	Digital	G/Y video output
79	DV_{SS}	P	-	GND	Digital	
80	DGOUT7	O	F	CMOS	Digital	G/Y video output (MSB)
81	DBOUT0	O	F	CMOS	Digital	B/Cb/C video output (LSB when 8-bit output is selected)
82	DBOUT1	O	F	CMOS	Digital	B/Cb/C video output
83	DV_{DD}_IO	P	-	IO voltage	Digital	
84	DBOUT2	O	F	CMOS	Digital	B/Cb/C video output (LSB when 6-bit output is selected)
85	DBOUT3	O	F	CMOS	Digital	B/Cb/C video output
86	DBOUT4	O	F	CMOS	Digital	B/Cb/C video output
87	DV_{SS}	P	-	GND	Digital	
88	DBOUT5	O	F	CMOS	Digital	B/Cb/C video output
89	DBOUT6	O	F	CMOS	Digital	B/Cb/C video output
90	DBOUT7	O	F	CMOS	Digital	B/Cb/C video output (MSB)
91	PWM	O	D	CMOS	Digital	Pulse width modulation waveform output
92	DV_{DD}_CORE	P	-	Core Voltage	Digital	
93	XRST	I	A	CMOS	Digital	System reset (“L” reset)
94	INTO	O	D	CMOS	Digital	Interrupt
95	TEST	I	B	CMOS	Digital	Test setting (Connect to GND normally)
96	DV_{SS}	P	-	GND	Digital	
97	SCK_SCL	I	C	CMOS	Digital	Bus clock (shared with SIO/I^2C)
98	SRXD_SDA	I/O	H	CMOS	Digital	SIO data input / I^2C data input/output
99	STXD	O	D	CMOS	Digital	SIO data
100	DV_{DD}_IO	P	-	IO voltage	Digital	

Pin Type

In/Output form	Function	Equivalent circuit	Application Terminal
A	Schmitt trigger CMOS input		XRST, PDWN, SCS_I2SEL
B	CMOS input with built-in pull-down resistor		TEST
C	CMOS input		SCK_SCL, SIOSEL, DVSI, DHSI, DDEI, OSDBL, DYGIN7, DYGIN6, DYGIN5, DYGIN4, DYGIN3, DYGIN2, DYGIN1, DYGIN0, DCBIN7, DCBIN6, DCBIN5, DCBIN4, DCBIN3, DCBIN2, DCBIN1, DCBIN0, DCRIN7, DCRIN6, DCRIN5, DCRIN4, DCRIN3, DCRIN2, DCRIN1, DCRIN0
D	2mA 3-STATE drive CMOS output		STXD, PWM, INTO
F	2mA/4mA switching 3-STATE drive CMOS output		DBOUT7, DBOUT6, DBOUT5, DBOUT4, DBOUT3, DBOUT2, DBOUT1, DBOUT0, DROUT7, DROUT6, DROUT5, DROUT4, DROUT3, DROUT2, DROUT1, DROUT0 DGOUT7, DGOUT6, DGOUT5, DGOUT4, DGOUT3, DGOUT2, DGOUT1, DGOUT0, DHSO/SP2, DVSO/FLM2, DDEO FLM, DEXR, POL, GRST, CPV, SP, OE, STRB
G	4mA/8mA switching 3-STATE drive CMOS output		DCKO
H	4mA 3-STATE drive CMOS input/output		SRXD_SDA
J	Analog input/output		RC_BIAS

I/O Timing

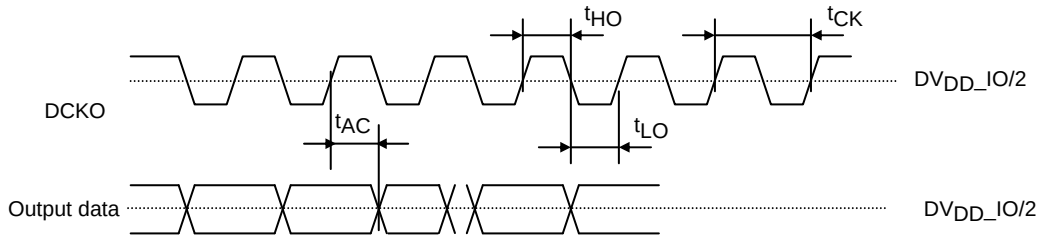
(1) Input data timing



Pin name	Parameter	Symbol	min	typ	max	unit
DCKI	Clock cycle	t_{CK}	25			ns
	Duty			50		%
DCRIN*, DYGIN*, DCBIN*, DVSI, DHSI, DDEI, OSDBL	Input data setup time (DV_{DD}_IO=2.6 to 3.6V)	t_{SU}	3			ns
	Input data setup time (DV_{DD}_IO=1.7 to 1.9V)	t_{SU}	3			ns
	Input data hold time (DV_{DD}_IO=2.6 to 3.6V)	t_{HD}	2			ns
	Input data hold time (DV_{DD}_IO=1.7 to 1.9V)	t_{HD}	2			ns

*: The recommended duty cycle of input clock is 50%

(2) Output data timing



Pin name	Parameter	Symbol	min	typ	max	unit
DCKO	Clock cycle	t_{CK}	25			ns
	Duty			50		%
DROUT*, DGOUT*, DBOUT*, DVSO, DHSO, DDEO, DEXR, POL, SP, STRB, CPV, OE, FLM, GRST	Output data delay time (DV_{DD}_IO=2.6 to 3.6V) Pin F: when set to 4mA Pin G: when set to 8mA	t_{AC}	-3		3	ns
	Output data delay time (DV_{DD}_IO=2.6 to 3.6V) Pin F: when set to 2mA Pin G: when set to 4mA	t_{AC}	-3		6	ns
	Output data delay time (DV_{DD}_IO=1.7 to 1.9V) Pin F: when set to 4mA Pin G: when set to 8mA	t_{AC}	-5		4	ns
	Output data delay time (DV_{DD}_IO=1.7 to 1.9V) Pin F: when set to 2mA Pin G: when set to 4mA	t_{AC}	-6		9	ns

* When DCKO is set to the forward rotation output. Output load capacity: 5pF