



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LC749403BG

CMOS IC

Silicon gate

LCD Picture Quality Improvement IC

Overview

LC749403BG is a IC which enables higher picture quality in LCD products by improving the signals outputed to the LCD panel. In addition to the function to improve the picture quality of the color equation and the brightness correction, smooth picture quality is realized by converting One Seg video from 15fps to 30fps using frame interpolation technique.

It supports up to WVGA resolution. *

Features

(1) Digital Input/Output

- Supports digital video input: YCbCr/YPbPr 24bit,16bit (4: 2: 2) signals or ITU-R BT.656 (8bit) input
- Digital RGB 24 bit signal input
- Digital RGB 18bit/24bit signal output
- Digital YCbCr 16bit/24bit signal output

(2) Picture Quality Improvement Function

- Y signal picture quality improvement: brightness adjustment, contour correction,CDEX (Color Depth Expander),
- C signal picture quality improvement: color exciter,skin color correction,color and hue adjustment
- RGB signal picture quality improvement: brightness, contrast, white balance, black balance, gamma correction

(3) Panel Interface

- Embedded timing controller for panel driver
- Automatic timing signal generation for panel protection
- PWM for backlight control (video adaptation low power consumption processing)

(4) Frame interpolation (×2) for One-Seg broadcast

- Double-speed (×2) mode (15fps ⇒ 30fps)
Intermediate image is predicted from the previous and next image.

*: Video input of the LC749403BG meets the following conditions:

- (1) horizontal resolution is under 880 dots, and (2) vertical resolution is under 480 lines.

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LSI Specifications

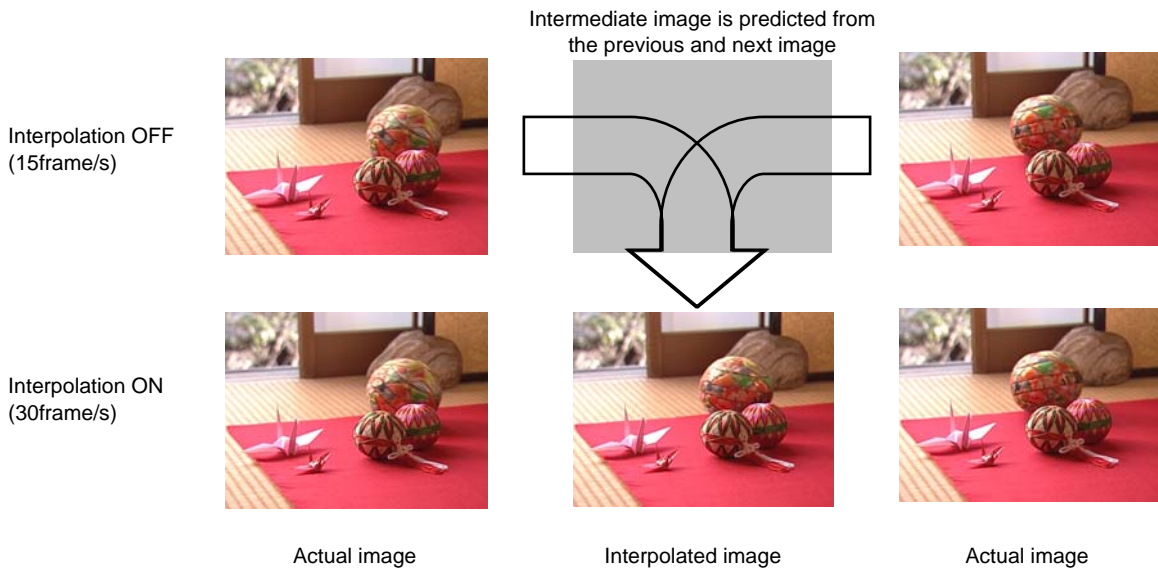
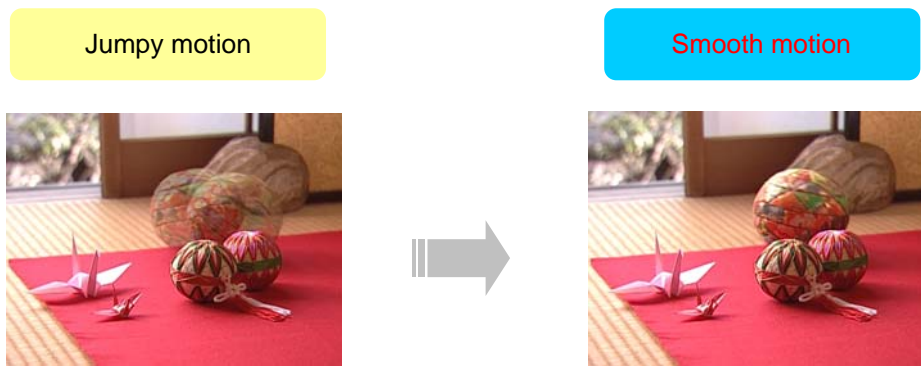
- Power supply voltage (typ)
 - Core block: 1.2V
 - SDRAM I/F block: 1.8V
 - I/O block: 1.8V/2.85V/3.3V selectable
- Maximum operating frequency
 - internal: 36MHz
 - SDRAM I/F block: 80MHz
- Package: FBGA144 11mm × 11mm (stacked MCP with SDRAM)

Target Application

- LCD display devices, One-Seg broadcast receiver (Car-Navigation, One-Seg TV, Portable DVD player, etc)

Frame interpolation (×2) example

Smooth image quality is realized by converting One Seg video from 15fps to 30fps using frame interpolation technique



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CDEX (Color Depth Expander) Example

This specification may be changed without any notices for product improvement.



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $DV_{SS} = 0\text{V}$, $AV_{SS_PLL} = 0\text{V}$, $AV_{SS_OSC} = 0\text{V}$, $SDV_{SS} = 0\text{V}$, $SDV_{SSQ} = 0\text{V}$

| Parameter | Symbol | Conditions | Ratings | unit |
|--|---|------------|---------------------------|------------------|
| Maximum supply voltage (I/O) | DV_{DD_IO} | | -0.3 to +3.96 | V |
| Maximum supply voltage (SDRAM, SDRAMIF I/O, PLL) | DV_{DD_SDIO} , AV_{DD_PLL} , SDV_{DD} , SDV_{DDQ} | | -0.3 to +2.6 | V |
| Maximum supply voltage (core, osc) | DV_{DD_CORE} AV_{DD_OSC} | | -0.3 to +1.8 | V |
| Digital input voltage | V_I | | -0.3 to $DV_{DD_IO}+0.3$ | V |
| Digital output voltage | V_O | | -0.3 to $DV_{DD_IO}+0.3$ | V |
| Operating temperature | T_{opr} | | -40 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |

Allowable Operation Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $DV_{SS} = 0\text{V}$, $AV_{SS_PLL} = 0\text{V}$, $AV_{SS_OSC} = 0\text{V}$, $SDV_{SS} = 0\text{V}$, $SDV_{SSQ} = 0\text{V}$

| Parameter | Symbol | Conditions | Ratings | | | unit |
|------------------------------|--|------------|---------|------|---------------|------|
| | | | min | typ | max | |
| Supply voltage (I/O) | DV_{DD_IO} | | 2.6 | 2.85 | 3.6 | V |
| | | | 1.7 | 1.8 | 1.95 | V |
| Supply voltage (SDRAMIF I/O) | DV_{DD_SDIO} | | 1.7 | 1.8 | 1.95 | V |
| Supply voltage (SDRAM, PLL) | SDV_{DD} , SDV_{DDQ} AV_{DD_PLL} | | 1.7 | 1.8 | 1.95 | V |
| Supply voltage (core, osc) | DV_{DD_CORE} AV_{DD_OSC} | | 1.14 | 1.2 | 1.26 | V |
| Input voltage range | V_{IN} | | 0 | | DV_{DD_IO} | V |

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DC Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $DV_{SS} = 0\text{V}$, $AV_{SS_PLL} = 0\text{V}$, $AV_{SS_OSC} = 0\text{V}$, $SDV_{SS} = 0\text{V}$,
 $SDV_{SSQ} = 0\text{V}$, $DV_{DD_IO} = 1.7$ to 3.6V , $DV_{DD_SDIO} = 1.7$ to 1.95V ,
 $DV_{DD_CORE} = 1.14$ to 1.26V , $SDV_{DD} = 1.7$ to 1.95V , $SDV_{DDQ} = 1.7$ to 1.95V

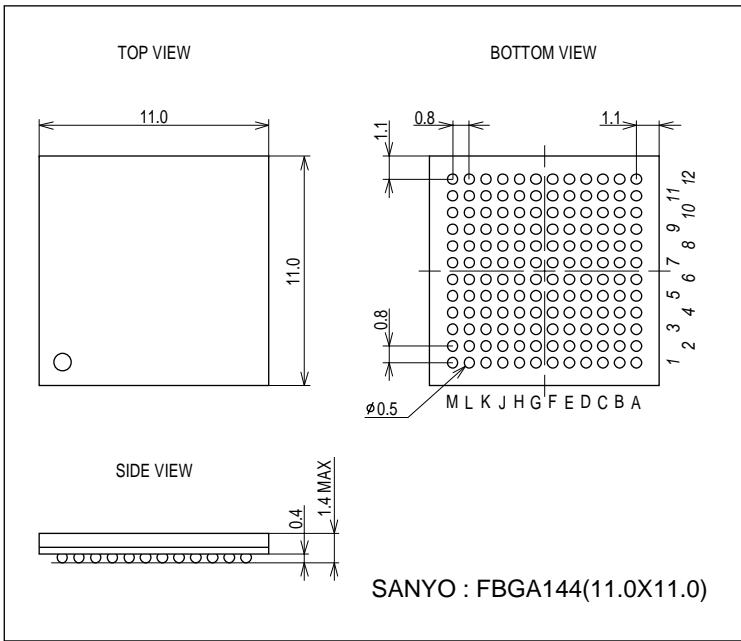
| Parameter | Symbol | Conditions | Ratings | | | unit |
|---------------------------|------------|--|---------------------|-----|------------------|------------------|
| | | | min | typ | max | |
| Input high-level voltage | V_{IH} | CMOS level inputs | $0.7DV_{DD_IO}$ | | | V |
| | | CMOS level schmitt inputs | $0.7DV_{DD_IO}$ | | | V |
| Input low-level voltage | V_{IL} | CMOS level inputs | | | $0.3DV_{DD_IO}$ | V |
| | | CMOS level schmitt inputs | | | $0.3DV_{DD_IO}$ | V |
| Input high-level current | I_{IH} | $V_I = DV_{DD_IO}$ | | | 10 | μA |
| | | $V_I = DV_{DD_IO}$, with pull-down resistor | | | 100 | μA |
| Input low-level current | I_{IL} | $V_I = DV_{SS}$ | -10 | | | μA |
| Output high-level voltage | V_{OH} | CMOS voltage: 2.6V to 3.6V, 1.7V to 1.9V I/O type D: $I_{OH} = -1\text{mA}$ I/O type E: $I_{OH} = -1\text{mA}$ (2mA mode) $I_{OH} = -2\text{mA}$ (4mA mode) I/O type F: $I_{OH} = -2\text{mA}$ (4mA mode) $I_{OH} = -4\text{mA}$ (8mA mode) I/O type G: $I_{OH} = -2\text{mA}$ I/O type H: $I_{OH} = -1\text{mA}$ (2mA mode) $I_{OH} = -2\text{mA}$ (4mA mode) | $DV_{DD_IO} - 0.4$ | | | V |
| Output low-level voltage | V_{OL} | CMOS | | | 0.4 | V |
| Output leakage current | I_{OZ} | In high-impedance output mode | | | 3 | μA |
| Pull-down resistance | RDN | condition : typ $T_a = 25^\circ\text{C}$ $DV_{DD_IO} = 2.85\text{V}$ $DV_{DD_CORE} = 1.2\text{V}$ | | 98 | | $\text{k}\Omega$ |
| | | condition : typ $T_a = 25^\circ\text{C}$ $DV_{DD_IO} = 1.8\text{V}$ $DV_{DD_CORE} = 1.2\text{V}$ | | 69 | | $\text{k}\Omega$ |
| Operating current drain | I_{DDOP} | condition : typ $T_a = 25^\circ\text{C}$ $DV_{DD_IO} = 2.85\text{V}$ $DV_{DD_CORE} = 1.2\text{V}$ QVGA, tck = 6.6MHz 10step | | 25 | | mA |
| | | condition : typ $T_a = 25^\circ\text{C}$ $DV_{DD_IO} = 2.85\text{V}$ $DV_{DD_CORE} = 1.2\text{V}$ WVGA, tck = 34.24MHz 10step | | 112 | | mA |
| Static current drain *1 | I_{DDST} | condition : typ $T_a = 25^\circ\text{C}$ $DV_{DD_IO} = 2.85\text{V}$ $DV_{DD_CORE} = 1.2\text{V}$ Output open, $V_I = DV_{SS}$ or DV_{DD_IO} | | 35 | | μA |

*1: Certain input pins have build-in pull-down resistors. Thus there are cases where, due to the circuit structure, the static current drain can not be guaranteed.

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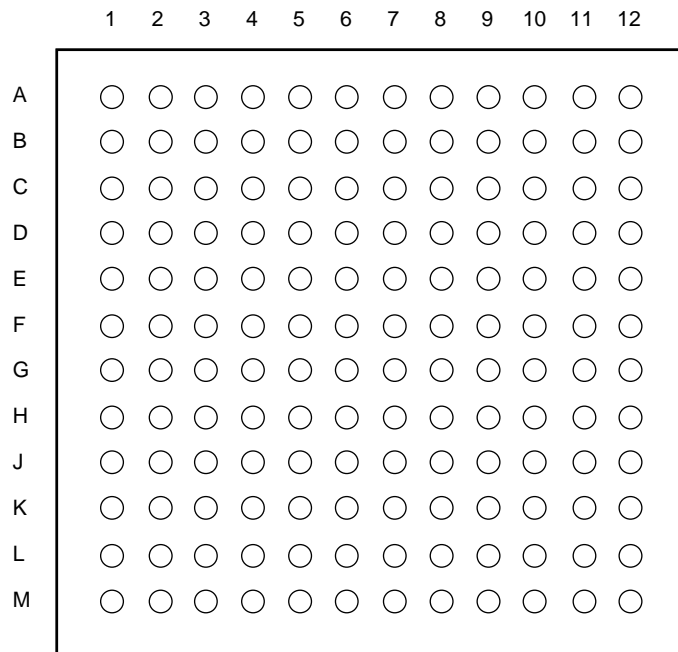
Package Dimensions

unit : mm (typ)
3409



Pin Assignment

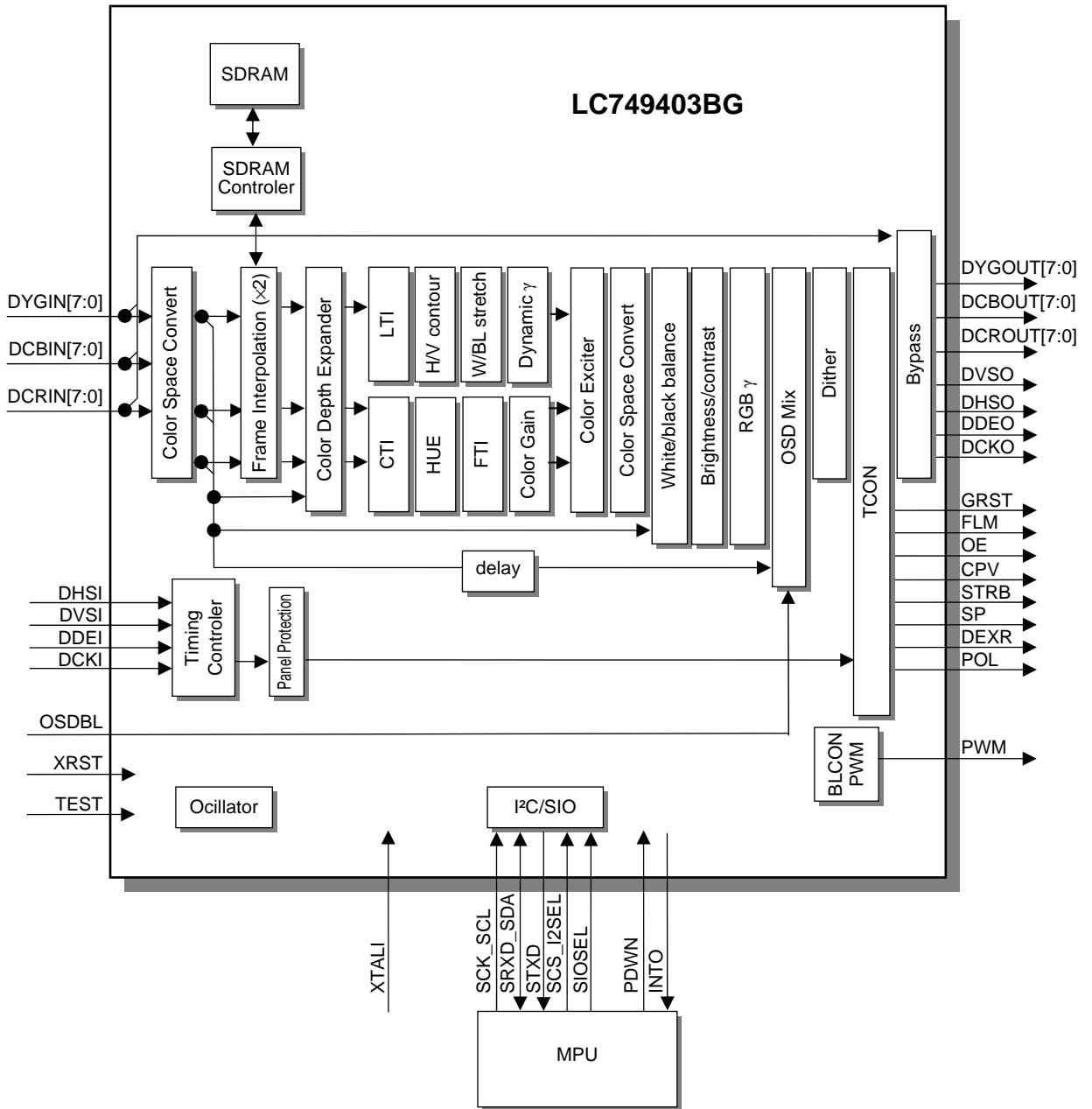
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Top View

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Block Diagram



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Pin Functions

| Pin No. | Pin symbol | I/O Format | | Connecting destination | | Remarks |
|---------|------------------------|------------|--------|------------------------|---------|--|
| | | I/O | Format | | | |
| A1 | AV _{DD} _OSC | P | - | Core voltage | Analog | |
| A2 | RC_BIAS | I | J | Resistor | Analog | Bias resistor connection (connect this pin to GND with a 20kΩ) |
| A3 | AV _{SS} _OSC | P | - | GND | Analog | |
| A4 | DHSI | I | C | CMOS | Digital | Horizontal synchronizing signal. |
| A5 | DDEI | I | C | CMOS | Digital | Data enable signal. Connect this pin to GND in the internal generation mode. |
| A6 | STXD | O | D | CMOS | Digital | SIO data |
| A7 | SCK_SCL | I | C | CMOS | Digital | Bus clock (common to SIO and I ² C) |
| A8 | XTALI | I | C | CMOS | Digital | Panel protection, PWM generation clock Connect this pin to GND when not to be used. |
| A9 | TEST | I | B | CMOS | Digital | Test (Normally, connect this pin to GND) |
| A10 | AV _{DD} _PLL | P | - | PLL voltage | Analog | |
| A11 | PDO | O | J | | Analog | Test (Normally, connect this pin to GND) |
| A12 | AV _{SS} _PLL | P | - | GND | Analog | |
| B1 | DCRIN2 | I | C | CMOS | Digital | R/Cr video. Connect this pin to GND when not to be used. |
| B2 | DV _{DD} _CORE | P | - | Core voltage | Digital | |
| B3 | DV _{SS} | P | - | GND | Digital | |
| B4 | DV _{SS} | P | - | GND | Digital | |
| B5 | DVSI | I | C | CMOS | Digital | Vertical synchronizing signal |
| B6 | SRXD_SDA | I/O | G | CMOS | Digital | SIO data input/I ² C data input/output |
| B7 | XRST | I | A | CMOS | Digital | System reset ("L" reset) |
| B8 | DCKI | I | C | CMOS | Digital | Video clock. |
| B9 | DV _{DD} _SDIO | P | - | IO voltage | Digital | |
| B10 | DV _{SS} | P | - | GND | Digital | |
| B11 | DV _{SS} | P | - | GND | Digital | |
| B12 | DCKO | O | F | CMOS | Digital | Video clock output |
| C1 | DCRIN1 | I | C | CMOS | Digital | R/Cr video. Connect this pin to GND when not to be used. |
| C2 | DCRIN0 | I | C | CMOS | Digital | R/Cr video. Connect this pin to GND when not to be used. |
| C3 | SDV _{SS} | P | - | GND | Digital | SDRAM ground |
| C4 | SDV _{SS} | P | - | GND | Digital | SDRAM ground |
| C5 | DV _{DD} _CORE | P | - | Core voltage | Digital | |
| C6 | INTO | O | D | CMOS | Digital | Interrupt |
| C7 | PDWN | I | A | CMOS | Digital | "L" power down Connect this pin to GND when not to be used. |
| C8 | SIOSEL | I | C | CMOS | Digital | "L": I ² C slave, "H": 3 wire SIO |
| C9 | DV _{SS} | P | - | GND | Digital | |
| C10 | DV _{SS} | P | - | GND | Digital | |
| C11 | DHSO/SP2 | O | E | CMOS | Digital | Horizontal synchronizing signal/Start pulse signal for source driver |
| C12 | DVSO/FLM2 | O | E | CMOS | Digital | Vertical synchronizing signal/Start pulse signal for gate driver |

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| Pin No. | Pin symbol | Input/output format | | Connecting destination | | Remarks |
|---------|------------------------|---------------------|--------|------------------------|---------|---|
| | | I/O | Format | | | |
| D1 | DCRIN3 | I | C | CMOS | Digital | R/Cr video. Connect this pin to GND when not to be used. |
| D2 | DCRIN4 | I | C | CMOS | Digital | R/Cr video. Connect this pin to GND when not to be used. |
| D3 | DCRIN5 | I | C | CMOS | Digital | R/Cr video. Connect this pin to GND when not to be used. |
| D4 | DV _{SS} | P | - | GND | Digital | |
| D5 | SDV _{SS} | P | - | GND | Digital | SDRAM ground |
| D6 | SDV _{SS} | P | - | GND | Digital | SDRAM ground |
| D7 | SDV _{DD} | P | - | IO voltage | Digital | SDRAM power |
| D8 | SDV _{DD} | P | - | IO voltage | Digital | SDRAM power |
| D9 | PWM | O | D | CMOS | Digital | Pulse width modulation waveform |
| D10 | OSDBL | I | C | CMOS | Digital | Data enable signal for external OSD. (Connect to GND when not used.) |
| D11 | SCS_I2SEL | I | A | CMOS | Digital | SIO chip enable/I ² C slave select |
| D12 | DDEO | O | E | CMOS | Digital | Data enable signal |
| E1 | DCRIN7 | I | C | CMOS | Digital | R/Cr video(MSB). Connect this pin to GND when not to be used. |
| E2 | DCRIN6 | I | C | CMOS | Digital | R/Cr video. Connect this pin to GND when not to be used. |
| E3 | DYGIN1 | I | C | CMOS | Digital | G/Y/656 video. Connect this pin to GND when not to be used. |
| E4 | DYGIN0 | I | C | CMOS | Digital | G/Y/656 video (LSB). Connect this pin to GND when not to be used. |
| E5 | DV _{DD} _IO | P | - | IO voltage | Digital | |
| E6 | DV _{DD} _IO | P | - | IO voltage | Digital | |
| E7 | DV _{DD} _IO | P | - | IO voltage | Digital | |
| E8 | DV _{DD} _CORE | P | - | Core voltage | Digital | |
| E9 | DBOUT4 | O | E | CMOS | Digital | B/Cb/C video |
| E10 | DBOUT5 | O | E | CMOS | Digital | B/Cb/C video |
| E11 | DBOUT6 | O | E | CMOS | Digital | B/Cb/C video |
| E12 | DBOUT7 | O | E | CMOS | Digital | B/Cb/C video (MSB) |
| F1 | DYGIN3 | I | C | CMOS | Digital | G/Y/656 video. Connect this pin to GND when not to be used. |
| F2 | DYGIN2 | I | C | CMOS | Digital | G/Y/656 video. Connect this pin to GND when not to be used. |
| F3 | DYGIN5 | I | C | CMOS | Digital | G/Y/656 video. Connect this pin to GND when not to be used. |
| F4 | DYGIN4 | I | C | CMOS | Digital | G/Y/656 video. Connect this pin to GND when not to be used. |
| F5 | DV _{DD} _CORE | P | - | Core voltage | Digital | |
| F6 | DV _{DD} _CORE | P | - | Core voltage | Digital | |
| F7 | DV _{DD} _IO | P | - | IO voltage | Digital | |
| F8 | DV _{DD} _CORE | P | - | Core voltage | Digital | |
| F9 | DBOUT1 | O | E | CMOS | Digital | B/Cb/C video |
| F10 | DBOUT3 | O | E | CMOS | Digital | B/Cb/C video |
| F11 | DBOUT0 | O | E | CMOS | Digital | B/Cb/C video (LSB) |
| F12 | DBOUT2 | O | E | CMOS | Digital | B/Cb/C video |

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| Pin No. | Pin symbol | Input/output format | | Connecting destination | | Remarks |
|---------|------------------------|---------------------|--------|------------------------|---------|--|
| | | I/O | Format | | | |
| G1 | DCBIN0 | I | C | CMOS | Digital | B/Cb/C video |
| G2 | DYGIN6 | I | C | CMOS | Digital | G/Y/656 video |
| G3 | DYGIN7 | I | C | CMOS | Digital | G/Y/656 video |
| G4 | DCBIN1 | I | C | CMOS | Digital | B/Cb/C video. Connect this pin to GND when not to be used. |
| G5 | DV _{DD} _CORE | P | - | Core Voltage | Digital | |
| G6 | DV _{DD} _CORE | P | - | Core Voltage | Digital | |
| G7 | DV _{DD} _SDIO | P | - | IO voltage | Digital | |
| G8 | DV _{DD} _SDIO | P | - | IO voltage | Digital | |
| G9 | DGOUT5 | O | E | CMOS | Digital | G/Y/656 video |
| G10 | DGOUT6 | O | E | CMOS | Digital | G/Y/656 video |
| G11 | DGOUT3 | O | E | CMOS | Digital | G/Y/656 video |
| G12 | DGOUT7 | O | E | CMOS | Digital | G/Y/656 video (MSB) |
| H1 | DCBIN4 | I | C | CMOS | Digital | B/Cb/C video |
| H2 | DCBIN3 | I | C | CMOS | Digital | B/Cb/C video |
| H3 | DCBIN2 | I | C | CMOS | Digital | B/Cb/C video |
| H4 | DCBIN5 | I | C | CMOS | Digital | B/Cb/C video |
| H5 | DV _{DD} _SDIO | P | - | IO voltage | Digital | |
| H6 | DV _{DD} _SDIO | P | - | IO voltage | Digital | |
| H7 | DV _{DD} _SDIO | P | - | IO voltage | Digital | |
| H8 | DV _{DD} _SDIO | P | - | IO voltage | Digital | |
| H9 | DGOUT0 | O | E | CMOS | Digital | G/Y/656 video (LSB) |
| H10 | DGOUT1 | O | E | CMOS | Digital | G/Y/656 video |
| H11 | DGOUT2 | O | E | CMOS | Digital | G/Y/656 video |
| H12 | DGOUT4 | O | E | CMOS | Digital | G/Y/656 video |
| J1 | CPV | I/O | H | CMOS | Digital | Clock signal for gate driver |
| J2 | STRB | I/O | H | CMOS | Digital | Data strobe signal for source driver |
| J3 | DEXR | O | E | CMOS | Digital | Video inverse signal output for DTR |
| J4 | DV _{SS} | P | - | GND | Digital | |
| J5 | DV _{SS} | P | - | GND | Digital | |
| J6 | DV _{SS} | P | - | GND | Digital | |
| J7 | DV _{SS} | P | - | GND | Digital | |
| J8 | DV _{SS} | P | - | GND | Digital | |
| J9 | DV _{SS} | P | - | GND | Digital | |
| J10 | DV _{SS} | P | - | GND | Digital | |
| J11 | DV _{SS} | P | - | GND | Digital | |
| J12 | DROUT7 | I/O | H | CMOS | Digital | R/Cr video (MSB) |

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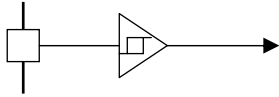
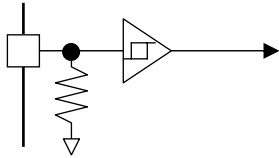
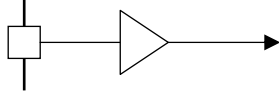
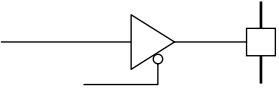
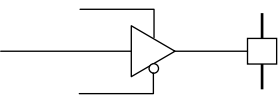
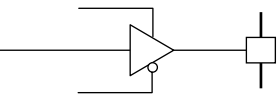
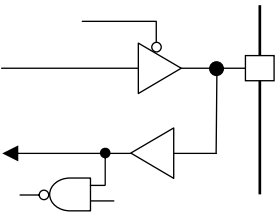
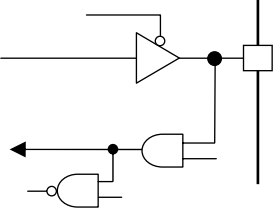
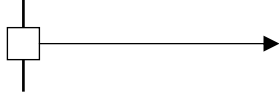
| Pin No. | Pin symbol | Input/output format | | Connecting destination | | Remarks |
|---------|--------------------|---------------------|--------|------------------------|---------|---|
| | | I/O | Format | | | |
| K1 | FLM | I/O | H | CMOS | Digital | Start pulse signal for gate driver |
| K2 | OE | I/O | H | CMOS | Digital | Output enable signal for gate driver |
| K3 | DV _{SS} | P | - | GND | Digital | |
| K4 | DV _{SS} | P | - | GND | Digital | |
| K5 | DV _{SS} | P | - | GND | Digital | |
| K6 | DV _{SS} | P | - | GND | Digital | |
| K7 | DV _{SS} | P | - | GND | Digital | |
| K8 | DV _{SS} | P | - | GND | Digital | |
| K9 | DV _{SS} | P | - | GND | Digital | |
| K10 | DV _{SS} | P | - | GND | Digital | |
| K11 | DROUT0 | I/O | H | CMOS | Digital | R/Cr video (LSB) |
| K12 | DROUT6 | I/O | H | CMOS | Digital | R/Cr video |
| L1 | DCBIN7 | I | C | CMOS | Digital | B/Cb/C video (MSB). Connect this pin to GND when not to be used. |
| L2 | SP | I/O | H | CMOS | Digital | Start pulse signal for source driver |
| L3 | SDV _{DDQ} | P | - | IO voltage | Digital | SDRAM power *1 |
| L4 | SDV _{DDQ} | P | - | IO voltage | Digital | SDRAM power *1 |
| L5 | SDV _{DDQ} | P | - | IO voltage | Digital | SDRAM power *1 |
| L6 | SDV _{DDQ} | P | - | IO voltage | Digital | SDRAM power *1 |
| L7 | SDV _{DDQ} | P | - | IO voltage | Digital | SDRAM power *1 |
| L8 | SDV _{DDQ} | P | - | IO voltage | Digital | SDRAM power *1 |
| L9 | SDV _{DDQ} | P | - | IO voltage | Digital | SDRAM power *1 |
| L10 | DV _{SS} | P | - | GND | Digital | |
| L11 | DROUT2 | I/O | H | CMOS | Digital | R/Cr video |
| L12 | DROUT5 | I/O | H | CMOS | Digital | R/Cr video |
| M1 | DCBIN6 | I | C | CMOS | Digital | B/Cb/C video. Connect this pin to GND when not to be used. |
| M2 | POL | O | E | CMOS | Digital | Voltage polarity selection signal for source driver |
| M3 | GRST | I/O | H | CMOS | Digital | Reset signal for gate driver |
| M4 | SDV _{SSQ} | P | - | GND | Digital | SDRAM ground *2 |
| M5 | SDV _{SSQ} | P | - | GND | Digital | SDRAM ground *2 |
| M6 | SDV _{SSQ} | P | - | GND | Digital | SDRAM ground *2 |
| M7 | SDV _{SSQ} | P | - | GND | Digital | SDRAM ground *2 |
| M8 | SDV _{SSQ} | P | - | GND | Digital | SDRAM ground *2 |
| M9 | SDV _{SSQ} | P | - | GND | Digital | SDRAM ground *2 |
| M10 | DROUT1 | I/O | H | CMOS | Digital | R/Cr video |
| M11 | DROUT3 | I/O | H | CMOS | Digital | R/Cr video |
| M12 | DROUT4 | I/O | H | CMOS | Digital | R/Cr video |

*1: We recommend isolated power to be supplied to SDRAM for improved noise immunity.

*2: We recommend isolated ground to be supplied to SDRAM for improved noise immunity.

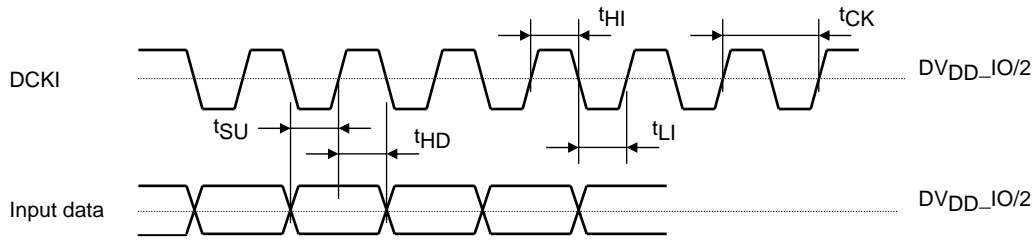
LC749403BG

Pin Circuits

| In/output form | Function | Equivalent circuit | Application Terminal |
|----------------|---|---|--|
| A | Schmitt trigger CMOS input |  | XRST, PDWN, SCS_I2SEL |
| B | CMOS input with built-in pull-down resistor |  | TEST |
| C | CMOS input |  | SCK_SCL, SIOSEL, DVSI, DSI, DDEI, OSDBL, DYGIN7, DYGIN6, DYGIN5, DYGIN4, DYGIN3, DYGIN2, DYGIN1, DYGIN0, DCBIN7, DCBIN6, DCBIN5, DCBIN4, DCBIN3, DCBIN2, DCBIN1, DCBIN0, DCRIN7, DCRIN6, DCRIN5, DCRIN4, DCRIN3, DCRIN2, DCRIN1, DCRIN0 |
| D | 2mA 3-STATE drive CMOS output |  | STXD, PWM, INTO |
| E | 2mA/4mA switching 3-STATE drive CMOS output |  | DBOUT7, DBOUT6, DBOUT5, DBOUT4, DBOUT3, DBOUT2, DBOUT1, DBOUT0, DGOUT7, DGOUT6, DGOUT5, DGOUT4, DGOUT3, DGOUT2, DGOUT1, DGOUT0, DHSO/SP2, DVSO/FLM2, DDEO FLM, DEXR, POL |
| F | 4mA/8mA switching 3-STATE drive CMOS output |  | DCKO |
| G | 4mA 3-STATE drive CMOS input/output |  | SRXD_SDA |
| H | 2mA/4mA switching 3-STATE CMOS input/output |  | DROUT7, DROUT6, DROUT5, DROUT4, DROUT3, DROUT2, DROUT1, DROUT0, GRST, CPV, SP, OE, STRB |
| J | Analog input/output |  | RC_BIAS |

Input/Output Timing

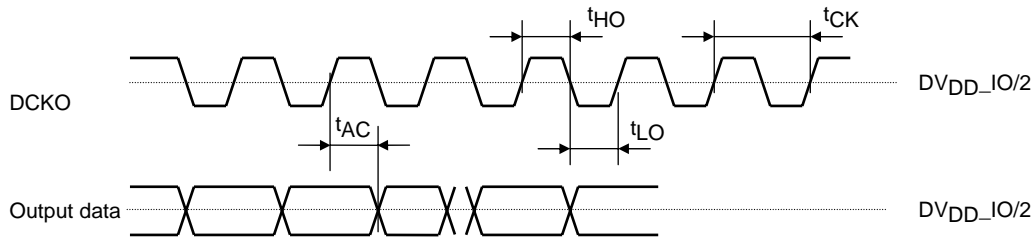
(1) Input data timing



| Pin Name | Parameter | Symbol | min | typ | max | unit |
|---|--|----------|-----|-----|-----|------|
| DCKI | Clock cycle | t_{CK} | 25 | | | ns |
| | Duty | | | 50 | | % |
| DCRIN*, DYGIN*, DCBIN*, DVSI, DHSI, DDEI, OSDBL | Input data set up time (DV _{DD_IO} =2.6 to 3.6V) | t_{SU} | 3 | | | ns |
| | Input data set up time (DV _{DD_IO} =1.7 to 1.95V) | t_{SU} | 3 | | | ns |
| | Input data hold time (DV _{DD_IO} =2.6 to 3.6V) | t_{HD} | 2 | | | ns |
| | Input data hold time (DV _{DD_IO} =1.7 to 1.95V) | t_{HD} | 2 | | | ns |

*: We recommend a 50% duty cycle for the input clock.

(2) Output data timing



| Pin Name | Parameter | Symbol | min | typ | max | unit |
|---|---|----------|-----|-----|-----|------|
| DCKO | Clock cycle | t_{CK} | 25 | | | ns |
| | Duty | | | 50 | | % |
| DROUT*, DGOUT*, DBOUT*, DVSO, DHSO, DDEO, DEXR, POL, SP, STRB, CPV, OE, FLM, GRST | Output data delay time (DV _{DD_IO} =2.6 to 3.6V) I/O typ E: 4mA setting I/O typ F: 8mA setting | t_{AC} | -3 | | 3 | ns |
| | Output data delay time (DV _{DD_IO} =2.6 to 3.6V) I/O typ E: 2mA setting I/O typ F: 4mA setting | t_{AC} | -3 | | 6 | ns |
| | Output data hold time (DV _{DD_IO} =1.7 to 1.95V) I/O typ E: 4mA setting I/O typ F: 8mA setting | t_{AC} | -5 | | 4 | ns |
| | Output data hold time (DV _{DD_IO} =1.7 to 1.95V) I/O typ E: 2mA setting I/O typ F: 4mA setting | t_{AC} | -6 | | 9 | ns |

*: When DCKO is set to the forward rotation output. Output load capacity: 5pF

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