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SANYO Semiconductors
DATA SHEET

LC749460W — CMOS IC Silicon gate Digital RGB Processor LSI

Overview

The LC749460W is RGB processor LSI which converts the interlace TV signal such as NTSC or PAL into progressive signal, optimizes and adjusts the image quality of these TV signals to the FPD devices such as LCD-TV, and output the signal that converts the resolution according to the connected panel. It optimizes LSI for the pixel display device which deals with image quality and high resolution image. A video signal processing system for flat panel display can be formatted easily by combining with microcomputer and LCD panel.

Features

(1) Analog input
- Built-in 4ch A/D converter
- CVBS × 2ch, S-Video, YCbCr/YPbPr input (supports 480i/576i, 480p/576p, 1080i, 720p) × 2ch

(2) Digital input/output
- Support digital video input: YCbCr 24-bit or YCbCr 16-bit (4:2:2) signal or ITU-R BT656 (8-bit) input
- Support DTV (480i/576i, 480p/576p, 1080i, 720p) input: YCbCr/YPbPr/RGB digital 24-bit signal input
- Digital RGB 30-bit (24-bit)/YCbCr 30-bit (24-bit) signal output

(3) YC separation video decoder (NTSC, PAL, SECAM)
- Adaptive 3D YC separation (NTSC)/Adaptive 3 or 5 line YC separation (PAL).
- Digital AGC. Digital ACC

(4) De-interlacing
- Motion adaptive Jaggy-less De-interlacing
- 2:3 pull-down, 2:2 pull-down

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SDPiC : SANYO Digital Picture Improvement Core

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(5) Resolution Conversion
- Resolution conversion (to WXGA)
- PIP/POP.

(6) Picture quality improvement
- Noise reduction (3D NR)
- Cross color/Cross luminance canceller
- Horizontal edge correction (LTI/CTI), Sharpness (horizontal/vertical), Shadow adjuster
- White/black stretch. Flesh tone improvement.
- Hue/Color gain adjustment/Color exciter (6 phase RGBYMC Independent saturation correction).
- Brightness/Contrast adjustment. White balance/Black balance adjustment.
- γ correction (RGB independent, LUT system programmable). Dithering (10-bit/8-bit). Clamp control.
- Clock generator (PLL)/various of Built-in interface (SDRAM IF, I^2C bus, 3 wire-bus)
- YUV to RGB conversion/YCbCr to RGB conversion/YPbPr to RGB conversion/RGB to YCbCr conversion

LSI Specifications
- Supply voltage Core: 1.2V, I/O block: 3.3V
- Maximum operating frequency: 85MHz
- Package: LQFP256

Principal Applications
- LCD TVs, monitors, and projectors, PDP TVs, progressive scan TVs, and projection TVs

1. Input
1-1 Input signal format (Digital input)

Digital data port supports the following signal input formats.
24bit (4:4:4) YCbCr/RGB: NTSC/PAL (480i/576i), 480p, 576p, HD (1080i/720p)
16bit (4:2:2) YCbCr: NTSC/PAL (480i/576i), 480p, 576p, HD (1080i/720p)
8bit Based on ITU-R BT656system (H/V sync input is needed): NTSC/PAL (480i/576i)
Digital 2 system input such as 16bit (4:2:2) YCbCr + 8bit (ITU-R BT656), 8bit (ITU-R BT656) + 8bit (ITU-R BT656) are possible

1-2 Input signal format (Analog input)

Analog port can be connected to all of the following input.
CVBS × 2ch: Composite input 2CH
S-Video: S video input 1CH
YPbPr input (Supports 480i/576i, 480p/576p, 1080i, 720p input): Component input 2 system

2. Digital Video Decoder Block
This LSI carries video decoder which converts the video signal of NTSC, PAL and SECAM or Component video signal into digital picture signal.
It decodes Digital picture data by inputting the video signals of NTSC, PAL and SECAM which are converted from Analog to Digital. It supports composite video signal, S video signal and component signal (480i).

3. De-interlacing Block
When inputting NTSC (480i) and PAL (576i), it can implement motion adaptive De-interlacing, cinema mode de-interlace, 3D noise reduction and cross color/cross luminance canceller. At 480p, 576p, 1080i, 720p, this block is set to the through state.

3-1. Motion adaptive De-interlacing

At De-interlacing block, it operates the movement detection to every pixel that inputted. As a result, it does interpolation between front and back field to the pixel that judged as static, and does interpolation inside field to the pixel that judged as move. So de-interlacing can be done. In that case, as for interpolation in between field of move part, it is possible to produce less notched (less-jaggy) and smooth image because of interpolation that considers the correlation of oblique direction.

3-2. Cinema mode De-interlacing (3-2/2-2 pull-down)
When NTSC/PAL interlace signal generated from film (cinema) source or 30p source such as cartoon are inputted, it does auto-discriminate cinema/30p source and cinema mode de-interlace that suitable for source.

3-3. 3D Noise reduction
This has built-in round type 3D noise reduction function that decreases the noise between frames. In this block luminance signal and color difference signal can be processed independently.

3-4. Cross color/Cross luminance canceller
This function can decrease the cross color, noise and cross luminance which are generated when NTSC input signal from composite terminal. By using this function, it can produce vivid image without color blotting and dot interruption.

4. Scaler block

It implement the up/down scaling of the various input signal of analog and digital that fixed to XGA, WXGA of output resolution. Full/panorama/zoom display is possible and maximum resolution is WXGA (1366 × 768 and 85MHz pixel clock). Additionally, this has built-in 2scaler system and enable to display 2screen such as POP/PIP.

5. Image quality adjustment block

This has various image quality blocks and enables to implement the image quality adjustment to fix with flat panel TV.

5-1. Horizontal edge correction (LTI/CTI)
LTI/CTI does edge correction of input signal. It improves the sharpness of image by making the transients of input signal steep. In this case, it is possible to make natural image because there is no peak such as overshoot and undershoot attached at the edge part of image. This function operates independently luminance signal and color difference signal.

5-2. Sharpness (Horizontal/Vertical)
Sharpness can do edge correction of input signal. In this function, unlike the above function, the moderate peak is added around edge correction. In this case, coring which emphasizes neither an amount of peak nor slight noise can be controlled by register. This function is operated only for luminance signal.

5-3. Shadow adjuster
Shadow adjuster add the moderate peak at front and back of detected edge of input signal and with added shadow of image, so it can produce sharpness image.

5-4.White/Black Stretch
As far as White-black stretch is concerned, it stretches the level of white side and black side of Y signal of YCbCr signal according to white-black peak inside picture of just before field, APL (Average Picture Level) of luminance, distribution information and microcomputer setting information. White and black peak are the max value and min value of input data in 1 field. When using white/black stretch, each setting value should be set properly.

5-5. Flesh color correction
Flesh color correction can extract flesh color and adjust the fresh color without influencing other colors.

5-6. Color phase/Color gain adjustment
The phase adjustment can adjust the hue on entire screen. The color gain adjustment can adjust the density of colors by controlling the gain of color phase signal. This function can adjust independently by Cb and Cr.

5-7. Color exciter
Color exciter can control the gain of chroma in red, green, blue, magenta, yellow, cyan respectively.

5-8. Brightness/Contrast
Brightness can adjust the brightness of entire screen, and contrast can adjust gain of brightness.

5-9. White balance/Black balance adjustment
This function can do white adjustment and black adjustment of LCD panel.

5-10. Gamma correction
It is possible to make the optional gamma curve that fix to LCD panel characteristic. It is also possible to adjust R, G and B independently by writing the adjustment value in LUT inside LSI

5-11. Dither
When the signal processing of internal 10/12bit is output by 8/10bits, the dither rounds the 2/4bits of LSB and output it.

6. Built-in OSD block

This function can do OSD (On Screen Display) on the image data after adjusting image quality.
The amount of the expression per pixel can be selected from 16 indexes (4 bits: CLUT4) and 256 indexes (8 bits: CLUT8). The color pallet of the index can set alfa 4-bit of blending coefficient and 8-bit of green, blue, and the red. Displayed character and icon, etc. need to set the αGBR color to the color pallet and transmit the BMP data in the state of CLUT 4/8. The drawing engine is built-in, besides, it is possible not only to draw the transmitted BMP data to SDRAM but also do the rectangle drawing (including point and line drawing) and copy inside SDRAM.

7. Output/I/F/others

7-1. Matrix conversion

The following Matrix conversion is possible for 2 systems after digital and analog input are selected.
YCbCr to RGB
YPbPr to RGB
YPbPr to YCbCr
RGB to YCbCr

7-2. Output format

Output is possible with the following format.
Digital RGB (30-bit/24-bit)
Digital YCbCr (30-bit/24-bit)

7-3. Clamp control

This can generate clamp signal in external LSI or in the built-in AD converter. In addition, it can generate optional pulse(“H”, “L”, “Hi-Z”) by comparing to the threshold value in the inside the LSI.

7-4. SDRAM interface

This built-in SDRAM interface, the system can be made up easily by connecting
64Mbits SDRAM (512word × 32bit × 4bank) 1 piece or 128Mbits SDRAM (1024word × 32bit × 4bank) 1 piece in directly. In this case, more than“-60” speed grade of SDRAM is recommended.

7-5. External OSD interface

This allows the interface with external OSD microcomputer using input pin 41 to 45 and output pin 36 to 38. It can display closed caption and teletext data.

7-6. I^2C interface/3 wire bus interface

It basically controls the internal register using I^2C interface.
The slave address can be a switch by controlling pin53 (I^2C SEL) according to the system.
The slave address is as follows.

I^2CSEL “L” “0111000+(R/W)”
I^2CSEL “H” “0111001+(R/W)”

A part of register can be controlled by 3wire bus interface as well.

I/O Specifications

1. Input Signals

The Kinds of Signals	The Number of Pins	Pin Symbol	Explanation	Remarks
Video signal	1	CVBS1	Analog video signal	NTSC/PAL input 1
	1	CVBS2		NTSC/PAL input 2
	1	ASYIN		S-Video input Y
	1	ASCIN		S-Video input C
	1	AYIN1		Component input Y1
	1	ACBIN1		Component input Cb1
	1	ACRIN1		Component input Cr1
	1	AYIN2		Component input Y2
	1	ACBIN2		Component input Cb2
	1	ACRIN2		Component input Cr2
	8	YGI	Digital video signal	Y or G or SY input
	8	CBI		Cb or B or YC input
	8	CRI		Cr or R or ITU-R BT656 input
Sync signal	1	HS1I	Horizontal sync signal	Horizontal sync signal for digital input 1
	1	VS1I	Vertical sync signal	Vertical sync signal for digital input 1
	1	HS2I	Horizontal sync signal	Horizontal sync signal for digital input 2
	1	VS2I	Vertical sync signal	Vertical sync signal for digital input 2
	1	SHSI	Horizontal sync signal	Horizontal sync signal for analog input
	1	SVSI	Vertical sync signal	Vertical sync signal for analog input
Data enable signal	1	HE1I	Data enable	Data enable (Horizontal/Composite) for digital input 1
	1	VE1I	Vertical data enable	Data enable (Vertical) for digital input 1
Field signal	1	FLD1I	Field	Field signal input for digital input 1
	1	FLD2I	Field	Field signal input for digital input 2
OSD signal	1	OSDG	External OSD signal G	
	1	OSDB	External OSD signal B	
	1	OSDR	External OSD signal R	
	1	OSDEN	External OSD enable	
	1	OSDAL	External OSD blending enable	
Pixel clock fixled oscillation	1	CK1I	Pixel clock	Pixel clock input for digital input 1
	1	CK2I	Pixel clock	Pixel clock input for digital input 2
	1	XTAL1	System clock	Fixed clock input 1
	1	XTAL2	System clock	Fixed clock input 2
System reset	1	XRST	System reset	System reset input negative-logic
Total	56	-	-	-

2. Output signal

The Kinds of Signals	The Number of Pins	Pin Symbol	Explanation	Remarks
Video signal	10	YGO	Digital video signal	RGB/YCbCr output Dithered 8bit output is possible.
	10	CBO		
	10	CRO		
	1	SVO	Analog video signal	Monitor output
Sync signal	1	HSO	Horizontal sync signal	
	1	VSO	Vertical sync signal	
Data enable signal	1	DEO	Data enable	
Field signal	1	FLDO	Field	Field output or vertical data enable output
Pixel clock	1	CKO	Pixel clock	
OSD signal	1	OSDHO	External OSD Horizontal sync signal	
	1	OSDVO	External OSD Vertical sync signal	
	1	OSDCKO	External OSD pixel clock	

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The Kinds of Signals	The Number of Pins	Pin Symbol	Explanation	Remarks
Clamp pulse	1	CLPP	Clamp pulse for External ADC	Pulse output to check AD clamp period
Clamp level	1	CLPCVBS1	Clamp level for CVBS1	Clamp level discriminator output (large: L, small: H, Coincident: Hi-Z)
	1	CLPCVBS2	Clamp level for CVBS2	
	1	CLPSY	Clamp level for SY	
	1	CLPSC	Clamp level for SC	
	1	CLPY1	Clamp level for Y1	
	1	CLPCB1	Clamp level for CB1	
	1	CLPCR1	Clamp level for CR1	
	1	CLPY2	Clamp level for Y2	
	1	CLPCB2	Clamp level for CB2	
	1	CLPCR2	Clamp level for CR2	
PWM output	1	PWMO	PWM	
Charge pump output	1	CHPMPDO	Charge pump for built-in PLL	
Total	52	-	-	-

3. Control signal

The Kinds of Signals	The Number of Pins	Pin Symbol	Explanation	Remarks
I^2C bus	1	SDA	I^2C data	
	1	SCL	I^2C clock	
	1	I^2CSEL	I^2C slave address switch	Low: “0111000+(R/W)” High: “0111001+(R/W)” Normally “L”
3-wire bus	1	AIDA	3-wire bus data input/output	
	1	AICS	3-wire bus chip select	
	1	AICK	3-wire bus clock	
Total	6	-	-	-

4. SDRAM control signal

The Kinds of Signals	The Number of Pins	Pin Symbol	Explanation	Remarks
clock	1	SDCKI	Clock input	
	1	SDCKO	Clock output	
Control system signal	1	SDRAS	Row address strobe signal output	
	1	SDCAS	Column address strobe signal output	
	1	SDWE	Write enable signal output	
Address system	11	SDAD	Address signal output	
	4	SDBS	Bank select signal output	
Data system	4	SDDQM	SDRAM data mask signal output	
	32	SDDQ	Data input/output	
Total	56	-	-	-

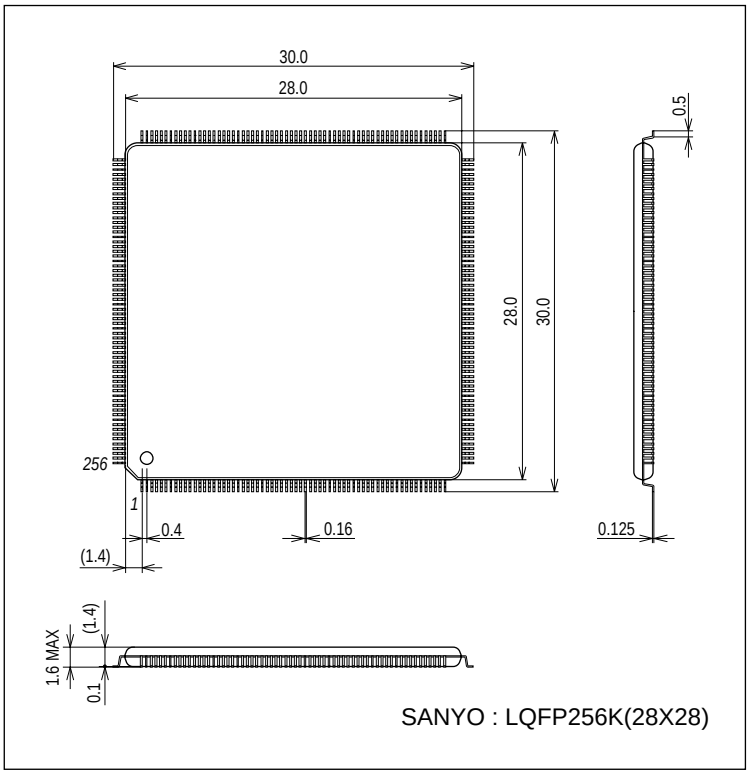
5. Other signals

The Kinds of Signals	The Number of Pins	Pin Symbol	Explanation	Remarks
SCAN test	1	SCANMD	SCAN test	Generally fixed as “L”
	1	SCANEN	SCAN test	Generally fixed as “L”
Test	2	TEST	Test setting	Generally fixed as “L”
ADC/AFE	4	VRT	Reference input for ADC	
	4	VRB		
	4	DACREFP	Reference output for ADC	
	4	DACREFM		
Total	20	-	-	-

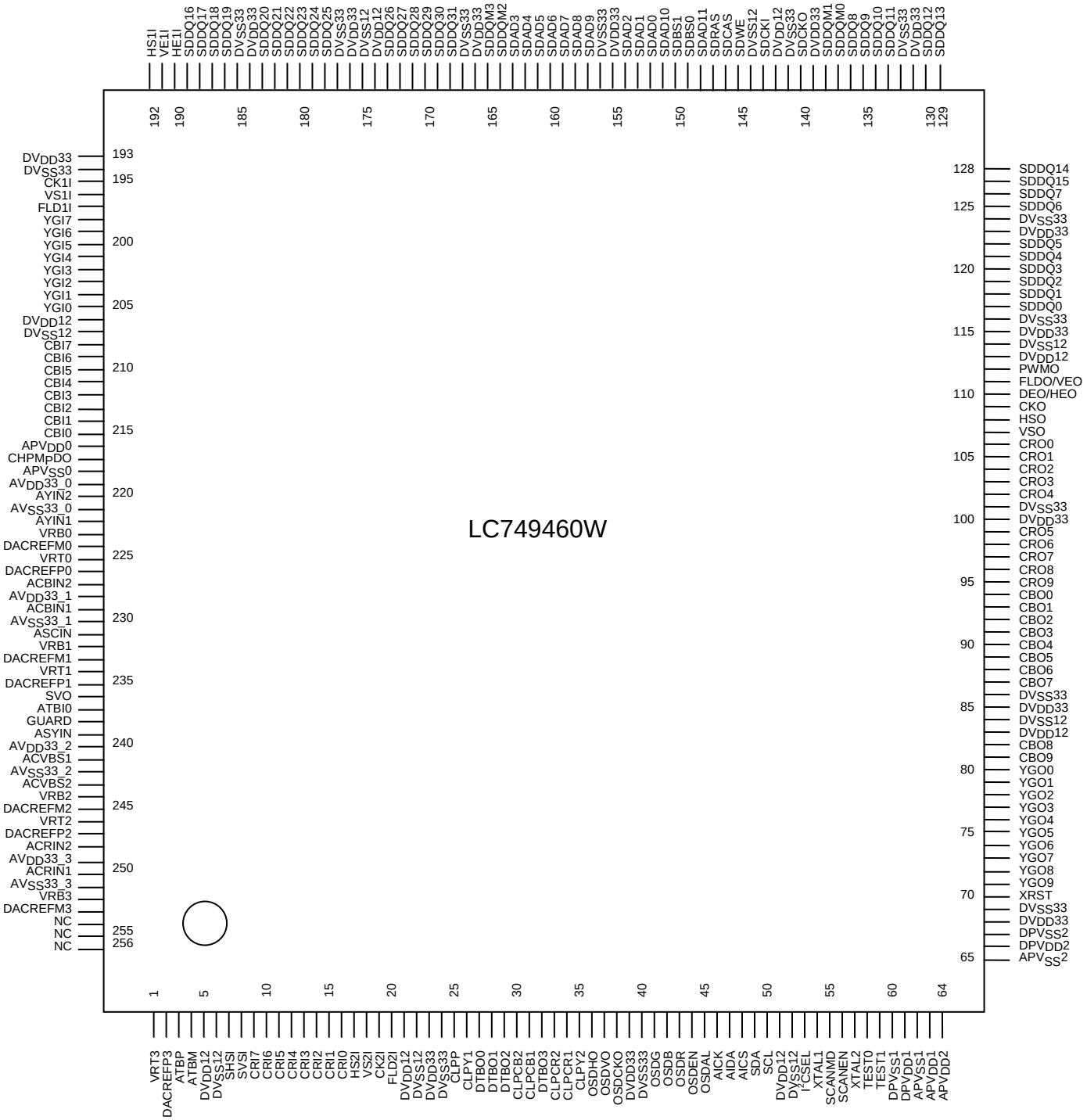
Package Dimensions

unit : mm (typ)

3365



Pin Assignment



Top view

Pin Functions

Pin No.	Pin symbol	In/output format		Connecting destination	Remarks
		I/O	Format		
1	VRT3	I	I		ADC3 reference power supply input
2	DACREFP3	O	I		ADC3 reference power supply output
3	ATBP	I	I	Open	ADC ATB (Analog Test Bus) Analog input + terminal
4	ATBM	I	I	Open	ADC ATB (Analog Test Bus) Analog input - terminal
5	$DV_{DD}12$	P		Power supply	Digital 1.2V system power supply
6	$DV_{SS}12$	P		GND	Digital 1.2V system GND
7	SHSI	I	C		External horizontal sync signal input
8	SVSI	I	D		External vertical sync signal input
9	CRI7	I	C		Cr/R signal input
10	CRI6	I			
11	CRI5	I			
12	CRI4	I			
13	CRI3	I			
14	CRI2	I			
15	CRI1	I			
16	CRI0	I			
17	HS2I	I	C		Horizontal sync signal input terminal for D2 input
18	VS2I	I	C		Vertical sync signal input terminal for D2 input
19	CK2I	I	A		Clock input terminal for D2 input
20	FLD2I	I	C		Field signal input terminal for D2 input
21	$DV_{DD}12$	P		Power supply	Digital 1.2V power supply
22	$DV_{SS}12$	P		GND	Digital 1.2V GND
23	$DV_{DD}33$	P		Power supply	Digital 3.3V power supply
24	$DV_{SS}33$	P		GND	Digital 3.3V GND
25	CLPP	O	E		Clamp pulse output terminal
26	CLPY1	O	F		Clamp control terminal
27	DTBO0	O		Open	Digital test output terminal
28	DTBO1	O		Open	
29	DTBO2	O		Open	
30	CLPCB2	O			Clamp control terminal
31	CLPCB1	O			
32	DTBO3	O		Open	Digital test output terminal
33	CLPCR2	O			Clamp control terminal
34	CLPCR1	O			
35	CLPY2	O			
36	OSDHO	O	E		External OSD Hsync signal output terminal
37	OSDVO	O			External OSD Vsync signal output terminal
38	OSDCKO	O			External OSD output pixel clock
39	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
40	$DV_{SS}33$	P		GND	Digital 3.3V system GND
41	OSDG	I	C		G signal input for OSD
42	OSDB	I			B signal input for OSD
43	OSDR	I			R signal input for OSD
44	OSDEN	I			OSD input enable
45	OSDAL	I			OSD blending enable
46	AICK	I	D		3-wire bus clock terminal
47	AIDA	B	H		3-wire bus data input/output terminal
48	AICS	I	D		3-wire bus chip select terminal
49	SDA	B	H	I^2C bus	I^2C bus data input/output terminal
50	SCL	I	D		I^2C bus clock terminal
51	$DV_{DD}12$	P		Power supply	Digital 1.2V system power supply

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Pin No.	Pin symbol	In/output format		Connecting destination	Remarks
		I/O	Format		
52	$DV_{SS}12$	P		GND	Digital 1.2V system GND
53	I^2CSEL	I	D		I^2C bus slave address selection input
54	XTAL1	I	A		XTAL (for PLL1) input terminal
55	SCANMD	I	D	Open	Test terminal
56	SCANEN	I	D		
57	XTAL2	I	A		XTAL (for PLL2) input terminal
58	TEST0	I	D	Open	Test terminal
59	TEST1	I			
60	$DPV_{SS}1$	P		GND	Digital GND for PLL1
61	$DPV_{DD}1$	P		Power supply	Digital 1.2V system power supply for PLL1
62	$APV_{SS}1$	P		GND	Analog GND for PLL1
63	$APV_{DD}1$	P		Power supply	Analog 3.3V system power supply for PLL1
64	$APV_{DD}2$	P		Power supply	Analog 3.3V system power supply for PLL2
65	$APV_{SS}2$	P		GND	Analog GND for PLL2
66	$DPV_{DD}2$	P		Power supply	Digital 1.2V system power supply for PLL2
67	$DPV_{SS}2$	P		GND	Digital GND for PLL2
68	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
69	$DV_{SS}33$	P		GND	Digital 3.3V system GND
70	XRST	I	B	Initial circuit	System reset terminal (“L” reset)
71	YGO9	O	E		Digital G signal output terminal
72	YGO8	O			
73	YGO7	O			
74	YGO6	O			
75	YGO5	O			
76	YGO4	O			
77	YGO3	O			
78	YGO2	O			
79	YGO1	O			
80	YGO0	O			
81	CBO9	O	E		Digital B signal output terminal
82	CBO8	O			
83	$DV_{DD}12$	P		Power supply	Digital 1.2V system power supply
84	$DV_{SS}12$	P		GND	Digital 1.2V system GND
85	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
86	$DV_{DD}33$	P		GND	Digital 3.3V system GND
87	CBO7	O	E		Digital B signal output terminal
88	CBO6	O			
89	CBO5	O			
90	CBO4	O			
91	CBO3	O			
92	CBO2	O			
93	CBO1	O			
94	CBO0	O			
95	CRO9	O	E		Digital R signal output terminal
96	CRO8	O			
97	CRO7	O			
98	CRO6	O			
99	CRO5	O			
100	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
101	$DV_{SS}33$	P		GND	Digital 3.3V system GND
102	CRO4	O	E		Digital R signal input terminal
103	CRO3	O			
104	CRO2	O			

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Terminal No.	Terminal symbol	In/output format		Connection destination	Remarks
		I/O	Format		
105	CRO1	O	E		Digital R signal input terminal
106	CRO0	O			
107	VSO	O	E		Vertical sync signal output terminal
108	HSO	O	E		Horizontal sync signal output terminal
109	CKO	O	G		Pixel clock output terminal
110	DEO/HEO	O	E		Data enable /horizontal data enable output terminal
111	FLDO/VEO	O	E		Field signal/vertical data enable output terminal
112	PWMO	O	G		PWM output terminal
113	$DV_{DD}12$	P		Power supply	Digital 1.2V system power supply
114	$DV_{SS}12$	P		GND	Digital 1.2V system GND
115	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
116	$DV_{SS}33$	P		GND	Digital 3.3V system GND
117	SDDQ0	B	H	SDRAM	SDRAM data input/output terminal
118	SDDQ1	B			
119	SDDQ2	B			
120	SDDQ3	B			
121	SDDQ4	B			
122	SDDQ5	B			
123	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
124	$DV_{SS}33$	P		GND	Digital 3.3V system GND
125	SDDQ6	B	H	SDRAM	SDRAM data input/output terminal
126	SDDQ7	B			
127	SDDQ15	B			
128	SDDQ14	B			
129	SDDQ13	B			
130	SDDQ12	B			
131	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
132	$DV_{SS}33$	P		GND	Digital 3.3V system GND
133	SDDQ11	B	H	SDRAM	SDRAM data input/output terminal
134	SDDQ10	B			
135	SDDQ9	B			
136	SDDQ8	B			
137	SDDQM0	O	G	SDRAM	SDRAM DQM0 output terminal
138	SDDQM1	O			SDRAM DQM1 output terminal
139	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
140	SDCKO	O	G	SDRAM	SDRAM clock output terminal
141	$DV_{SS}33$	P		GND	Digital 3.3V system GND
142	$DV_{DD}12$	P		Power supply	Digital 1.2V system power supply
143	SDCKI	I	A	SDRAM	SDRAM clock input terminal
144	$DV_{SS}12$	P		GND	Digital 1.2V system GND
145	SDWE	O	G	SDRAM	SDRAM write enable output terminal
146	SDCAS	O			SDRAM column address strobe output terminal
147	SDRAS	O			SDRAM low address strobe output terminal
148	SDAD11	O	G	SDRAM	SDRAM address output terminal
149	SDBS0	O	G	SDRAM	SDRAM bank 0 selection output terminal
150	SDBS1	O			SDRAM bank 1 selection output terminal
151	SDAD10	O	G	SDRAM	SDRAM address output terminal
152	SDAD0	O			
153	SDAD1	O			
154	SDAD2	O			
155	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
156	$DV_{SS}33$	P		GND	Digital 3.3V system GND
157	SDAD9	O	G	SDRAM	SDRAM address output terminal
158	SDAD8	O			

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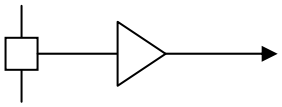
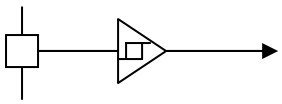
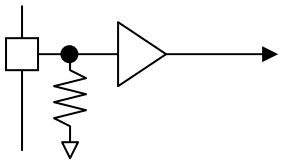
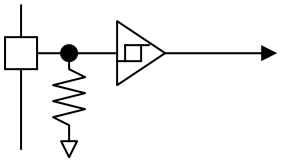
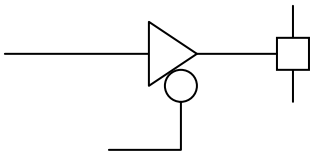
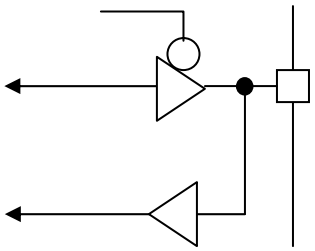
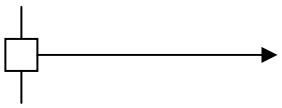
Terminal No.	Terminal symbol	In/output format		Connection destination	Remarks
		I/O	Format		
159	SDAD7	O	G	SDRAM	SDRAM address output terminal
160	SDAD6	O			
161	SDAD5	O			
162	SDAD4	O			
163	SDAD3	O			
164	SDDQM2	O	G	SDRAM	SDRAM DQM2 output terminal
165	SDDQM3	O			SDRAM DQM3 output terminal
166	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
167	$DV_{SS}33$	P		GND	Digital 3.3V system GND
168	SDDQ31	B	H	SDRAM	SDRAM data input/output terminal
169	SDDQ30	B			
170	SDDQ29	B			
171	SDDQ28	B			
172	SDDQ27	B			
173	SDDQ26	B			
174	$DV_{DD}12$	P		Power supply	Digital 1.2V system power supply
175	$DV_{SS}12$	P		GND	Digital 1.2V system GND
176	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
177	$DV_{SS}33$	P		GND	Digital 3.3V system GND
178	SDDQ25	B	H	SDRAM	SDRAM data input/output terminal
179	SDDQ24	B			
180	SDDQ23	B			
181	SDDQ22	B			
182	SDDQ21	B			
183	SDDQ20	B			
184	$DV_{DD}33$	P		Power supply	Digital 3.3V system power supply
185	$DV_{SS}33$	P		GND	Digital 3.3V system GND
186	SDDQ19	B	H	SDRAM	SDRAM data input/output terminal
187	SDDQ18	B			
188	SDDQ17	B			
189	SDDQ16	B			
190	HE1I	I	C		Horizontal data enable signal input terminal for digital input 1
191	VE1I	I	C		Vertical data enable signal input terminal for digital input 1
192	HS1I	I	C		Horizontal sync signal input terminal for digital input 1
193	$DV_{DD}33$	P		Power Supply	Digital 3.3V system power supply
194	$DV_{SS}33$	P		GND	Digital 3.3V system GND
195	CK1I	I	A		Pixel clock input terminal for digital input 1
196	VS1I	I	C		Vertical sync signal input terminal for digital input 1
197	FLD1I	I	C		Field discrimination signal input terminal for digital input 1
198	YGI7	I	C		SY/Y/G signal input
199	YGI6	I			
200	YGI5	I			
201	YGI4	I			
202	YGI3	I			
203	YGI2	I			
204	YGI1	I			
205	YGI0	I			
206	$DV_{DD}12$	P		Power Supply	1.2V system power supply
207	$DV_{SS}12$	P		GND	1.2V system GND
208	CBI7	I	C		C/Cb/B signal input
209	CBI6	I			
210	CBI5	I			

Continued on next page

Continued from preceding page.

Terminal No.	Terminal symbol	In/output format		Connection destination	Remark
		I/O	Format		
211	CBI4	I	C		C/Cb/B signal input
212	CBI3	I			
213	CBI2	I			
214	CBI1	I			
215	CBI0	I			
216	$APV_{DD}0$	P		Power Supply	Analog power supply for PLL0
217	CHPMPDO	O	I		Charge pump output
218	$APV_{SS}0$	P		GND	Analog GND for PLL0
219	$AV_{DD}33\_0$	P		Power Supply	Analog 3.3V system power supply for ADC0
220	AYIN2	I	I	Analog I/F	Analog Y2 signal input
221	$AV_{SS}33\_0$	P		GND	Analog 3.3V system GND for ADC0
222	AYIN1	I	I	Analog I/F	Analog Y1 signal input
223	VRB0	I	I		ADC0 reference power supply output
224	DACREFM0	O	I		ADC0 reference power supply output
225	VRT0	I	I		ADC0 reference power supply output
226	DACREFP0	O	I		ADC0 reference power supply output
227	ACBIN2	I	I	Analog I/F	Analog Cb2 signal input
228	$AV_{DD}33\_1$	P		Power supply	Analog 3.3V system power supply for ADC1
229	ACBIN1	I	I	Analog I/F	Analog Cb1 signal input
230	$AV_{SS}33\_1$	P		GND	Analog 3.3V system GND for ADC1
231	ASCIN	I	I	Analog I/F	Analog SC signal input
232	VRB1	I	I		ADC1 reference power supply input
233	DACREFM1	O	I		ADC1 reference power supply output
234	VRT1	I	I		ADC1 reference power supply input
235	DACREFP1	O	I		ADC1 reference power supply output
236	SVO	O	I	Analog I/F	Analog signal input
237	ATBI0	I	I	Open	Analog test input terminal
238	GUARD	I	I	GND	Analog guard band terminal
239	ASYIN	I	I	Analog I/F	Analog SY signal input
240	$AV_{DD}33\_2$	P		Power supply	Analog 3.3V system power supply for ADC2
241	ACVBS1	I	I	Analog I/F	Analog CVBS1 signal input
242	$AV_{SS}33\_2$	P		GND	Analog 3.3V system GND for ADC2
243	ACVBS2	I	I	Analog I/F	Analog CVBS2 signal input
244	VRB2	I	I		ADC2 reference power supply input
245	DACREFM2	O	I		ADC2 reference power supply output
246	VRT2	I	I		ADC2 reference power supply input
247	DACREFP2	O	I		ADC2 reference power supply output
248	ACRIN2	I	I	Analog I/F	Analog Cr2 signal input
249	$AV_{DD}33\_3$	P		Power supply	Analog 3.3V system power supply for ADC3
250	ACRIN1	I	I	Analog I/F	Analog Cr1 signal input
251	$AV_{SS}33\_3$	P		GND	Analog 3.3V system GND for ADC3
252	VRB3	I	I		ADC3 reference power supply input
253	DACREFM3	O	I		ADC3 reference power supply output
254	NC				
255	NC				
256	NC				

Pin Type

In/Output form	Function	Equivalent circuit	Application Terminal
A	5V tolerant input		CK1I, CK2I, XTAL1, XTAL2, SDCKI,
B	5V tolerant schmitt trigger input		XRST
C	5V tolerant with pulldown input		YGI0 to 7, CBI0 to 7, CRI0 to 7, HE1I, VE1I, HS1I, VS1I, FLD1I, HS2I, VS2I, FLD2I, SHSI, OSDG, OSDB, OSDR, OSDEN, OSDAL
D	5V tolerant with pull down schmitt trigger input		SVSI, AICK, AICS, SCL, I2CSEL, SCANMD, SCANEN (*No use OPEN), TEST0, TEST1
E	8mA 3-STATE drive input		YGO0 to 9, CBO0 to 9, CRO0 to 9 VSO, HSO, DEO/HEO, FLDO/VEO, CLPP, OSDHO, OSDVO, OSDCKO
F	8mA 3-STATE drive input		DTBO0 to 3, CLPY1 CLPCB1, CLPCR1, CLPY2 CLPCB2, CLPCR2
G	12mA 3-STATE drive input		CKO, SDCKO, PWMO, SDRAS, SDCAS, SDWE, SDAD0 to 11, SDBS0 to 1, SDDQM0 to 3
H	5V tolerant 12mA 3-STATE drive input/output		AIDA, SDA, SDDQ0 to 31
I	Analog input/output		VRT0 to 3, VRB0 to 3, DACREFP0 to 3, DACREFM0 to 3, ATBP, ATBM, CHPMPDO, SVO, GUARD, ACVBS1, ACVBS2, ASYIN, ASCIN, AYIN1, AYIN2, ACBIN1, ACBIN2, ACRIN1, ACRIN2, ATBI0

Electrical Characteristics

Absolute Maximum Ratings V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Max supply voltage (I/O)	$DV_{DD}33$ $AV_{DD}33$	-0.3 to +3.96	V
Max supply voltage (core)	$DV_{DD}12$ $AV_{DD}12$	-0.3 to +1.44	V
Input voltage	V_I	-0.5 to 6.0	V
Output voltage	V_O	-0.3 to V_{DD} +0.3	V
Storage temperature	Tstg	-55 to +125	°C
Operating temperature	Topr	-30 to +70	°C
Max supply current	Pd max	TDB	W

Allowable Operation Range at Ta = -30 to +70°C

Parameter	Symbol	min	typ	max	Unit
Supply voltage (I/O)	$DV_{DD}33$	3.15	3.3	3.45	V
Supply voltage (core)	$V_{DD}12$	1.08	1.2	1.32	V
Supply voltage (Analog)	$AV_{DD}33$	3.15	3.3	3.45	V
Supply voltage (PLL)	APV_{DD}	3.15	3.3	3.45	V
Input voltage range	V_{IN}	0		5.5	V

I/O terminal Capacitance at Ta = 25°C, $V_{DD} = V_I = 0V$

Parameter	Symbol	Conditions	min	typ	max	Unit
Input terminal	CIN	f=1MHz			10	pF
Output terminal	COUT	f=1MHz			10	pF
I/O terminal	CI/O	f=1MHz			10	pF

DC Characteristics at Ta = -30 to +70°C, $V_{DD}33$ = 3.15 to 3.45V, $V_{DD}12$ = 1.08V to 1.32V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level voltage	V_{IH}	Input with 5V tolerant	2.0		5.5	V
		Schmitt input with 5V tolerant	2.0		5.5	V
Input low-level voltage	V_{IL}	Input with 5V tolerant	-0.3		+0.8	V
		Schmitt input with 5V tolerant	-0.3		+0.8	V
Input high-level current	I_{IH}	$V_I=V_{DD}$	-10		+10	µA
		$V_I=V_{DD}$, with pull-down resistance	+10		+100	µA
Input low-level current	I_{IL}	$V_I=V_{SS}$	-10		+10	µA
Output high-level voltage	V_{OH}	CMOS	2.4			V
Output low-level voltage	V_{OL}	CMOS			0.4	V
Output leak current	IOZ	At output of high-impedance	-10		+10	µA
Pull-down resistor	RDN		50	97	272	kΩ
Dynamic supply current	IDDOP	t_{CK}=85MHz		TBD		mA
Static supply current *1	IDDST	Output release, $V_I=V_{SS}$ or V_{DD}		TBD		µA

*1: There is a input terminal which builds in pull down resistance. Please note that there is no guarantee about static consumption current depending on circuit composition.

A/D Convertor Characteristics at Ta = -30 to +70°C, DV_{SS} = 0V, AV_{SS} = 0V

Electric characteristic

Parameter	Symbol	Conditions	min	typ	max	unit
Sampling frequency	FCLK		10		80	MHz
Clamp pulse width	Tcl		0.45			µs
Analog input coupling capacitor	Cal			0.1		µF
Analog input frequency	Fal				30	MHz
Analog input amplitude	Val				1.0	Vp-p
SVO amplifier bandwidth	FSVO				5	MHz
SVO amplifier output load capacitor	CSVO				20	pF
External between DACREFP/DACREFM capacitor	CEXT		0.08	0.1	1	µF

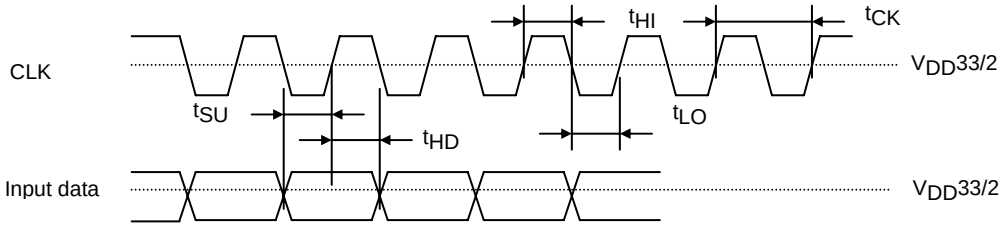
ADC Characteristics

Parameter	Symbol	Conditions	min	typ	max	Unit
resolution	NOB			10		bits
ENOB	ENOB	*1		8		bits
		*2		7.5		bits
Derivative linearity error	DNL	*1		0.5		LSB
		*2		0.5		LSB
Integral linearity error	INL	*1		2		LSB
		*2		2		LSB
Operation power current 3.3V power	$I_{DD}3$	*2, *3		60		mA
1.2V power	I_{DD}	*2, *3		1.5		mA
Standby power current 3.3V power	$I_{SB}3$	*3	-10		+10	µA
1.2V power	I_{SB}	*3	-10		+10	µA

*1 $V_{DD}3$=3.3V, Fclk=27MHz, Fin=100KHz
*2 $V_{DD}3$=3.3V, Fclk=80MHz, Fin=100KHz
*3 It describes value per 1ch
Note: ADC cannot standby. Apply a square wave with a constant frequency when ADC is not to be used.

I/O Data Timing

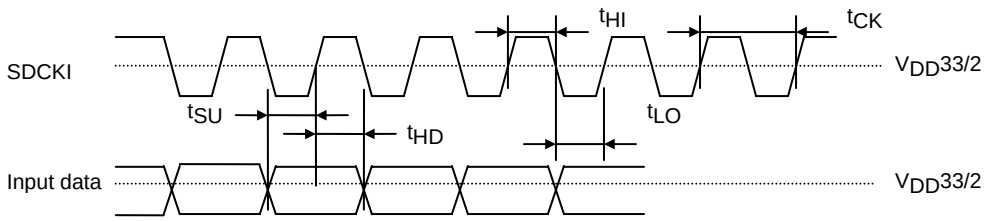
(1) Input data timing 1



Pin name	Parameter	Symbol	min	max	Unit
CK1I, CK2I	Clock L-level time	t_{LO}	6.25		ns
	Clock H-level time	t_{HI}	6.25		ns
	Clock cycle	t_{CK}	12.5		ns
YGI [7:0], CBI [7:0], CRI [7:0], HE1I, VE1I, HS1I, VS1I, FLD1I, HS2I, VS2I, FLD2I	Input data setup time	t_{SU}	2		ns
	Input data hold time	t_{HD}	1		ns

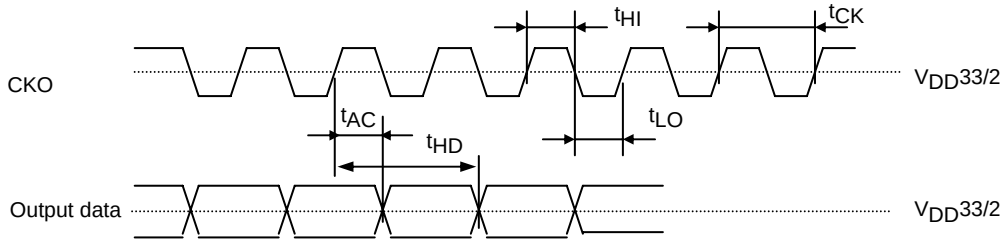
* The recommended duty cycle of input clock is 50%

(2) Input data timing 2



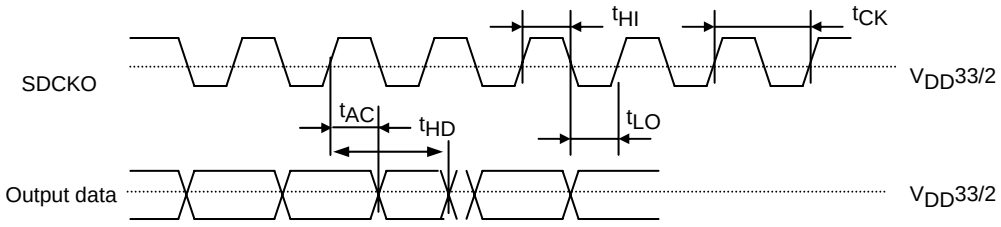
Pin name	Parameter	Symbol	min	max	Unit
SDCKI	Clock L-level time	t_{LO}	3.00		ns
	Clock H-level time	t_{HI}	3.00		ns
	Clock cycle	t_{CK}	6.00		ns
SDDQ [31:0]	Input data setup time	t_{SU}	2		ns
	Input data hold time	t_{HD}	1		ns

(3) Output data timing 1



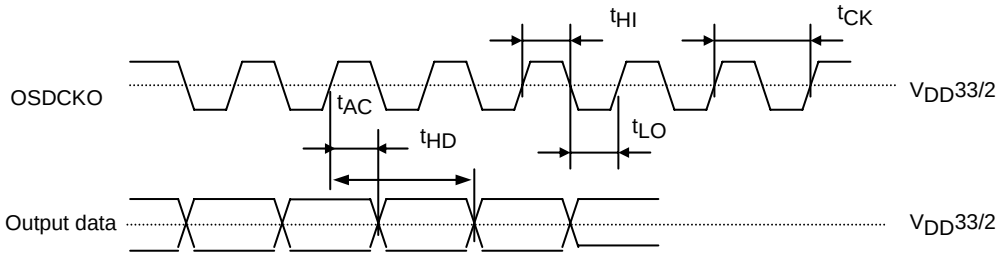
Pin name	Parameter	Symbol	min	max	Unit
CKO	Clock L-level time	t_{LO}	5.88		ns
	Clock H-level time	t_{HI}	5.88		ns
	Clock cycle	t_{CK}	11.76		ns
YGO [9:0], CBO [9:0], CRO [9:0], VSO, HSO, DEO/HEO, FLDO/VEO, OSDHO, OSDVO, OSDCKO	Output data delay time	t_{AC}	-1.5	+1.5	ns
	Output data hold time	t_{HD}	9.00		ns

(4) Output data timing 2



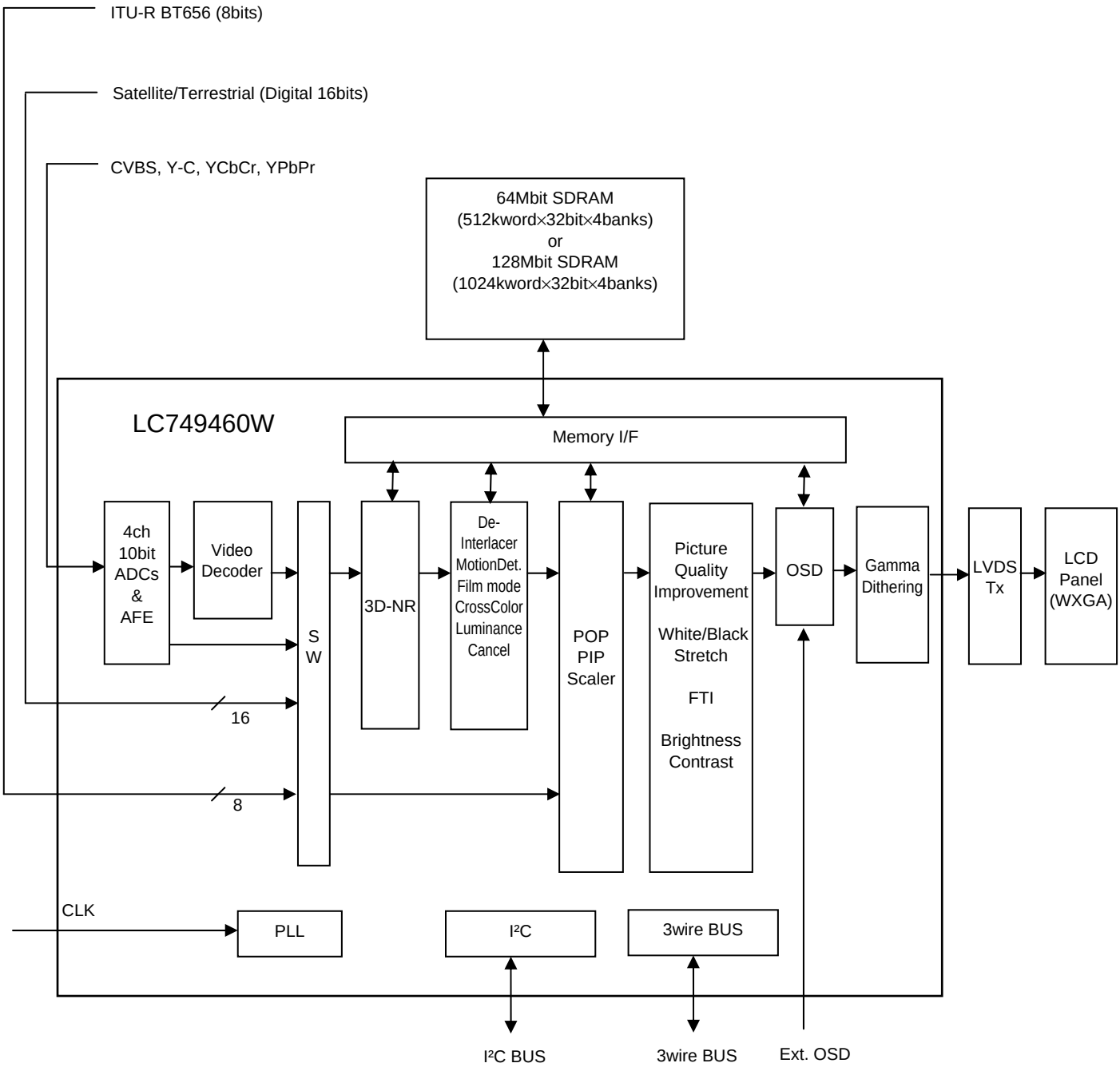
Pin name	Parameter	Symbol	min	max	Unit
SDCKO	Clock L-level time	t_{LO}	3.00		ns
	Clock H-level time	t_{HI}	3.00		ns
	Clock cycle	t_{CK}	6.00		ns
SDRAS, SDCAS, SDWE, SDAD [11:0], SDBS [1:0], SDDQM [3:0]	Output data delay time	t_{AC}	-1.0	+1.0	ns
	Output data hold time	t_{HD}	4		ns

(5) Output data timing 3



Pin name	Parameter	Symbol	min	max	Unit
OSDCKO	Clock L-level time	t_{LO}	5.88		ns
	Clock H-level time	t_{HI}	5.88		ns
	Clock cycle	t_{CK}	11.76		ns
OSDHO, OSDVO, OSDCKO	Output data delay time	t_{AC}	-1.5	+1.5	ns
	Output data hold time	t_{HD}	9.00		ns

Block Diagram



Application Circuit example