Ordering number : ENN7713

SANYO Semiconductors

DATA SHEET

LC74986NWF
LC74986NWV

CMOS IC

LCD TV Scan Converter IC

Overview

The LC74986NWF and LC74986NWV are video signal processing ICs that perform resolution conversion, interlaced to progressive scan (IP) conversion, and image quality improvement without requiring the use of external field (frame) memory. These ICs can display a wide variety of video signals and formats on a flat panel display. These ICs also provide image quality improvement and adjustment functions to create the optimal image quality for the flat panel display used. They also include an OSD function that displays characters with the sizes optimal for the size of panel used. A flat panel TV monitor with the necessary video signal processing circuits can be formed easily by combining one of these ICs with a video decoder, A/D converters, a microcontroller, and an LCD panel.

Features

- Multi-source support
  - NTSC, PAL, and DTV (480i and 480p) inputs
  - Progressive scan inputs up to XGA (The LC74986NWV supports up to SVGA.)
  - Supports both RGB and YCbCr (4:4:4 24 bits, 4:2:2 16 bits or 8 bits) inputs (built-in YCbCr to RGB converter).
- Resolution conversion
  - Independent horizontal and vertical expansion and reduction in the horizontal direction
  - Interlaced to progressive scan conversion
- Image quality correction
  - Sharpness, color, tint, white/black stretch, brightness, contrast, white balance, black balance
  - Built-in lookup table based gamma correction circuit (Common characteristics for each 8-bit RGB value can be programmed.)
- Panel interface
  - Single RGB 24-bit or 18-bit, or dual RGB 48-bit or 36-bit signal output (built-in dither processing)
  - Horizontal sync signal, vertical sync signal, data enable signal, and pixel clock outputs
- Other features
  - No external frame memory required (The input and output have the same frame period.)
  - Built-in OSD function (510 characters, 8 colors, built-in 8-character font RAM)
  - I^2C bus interface (The OSD function can also be controlled over a 3-wire bus.)
  - Low-power design

IC Specifications

- Supply voltage: I/O: 3.3V, core: 2.5V (LC74986NWF) or 1.8V (LC74986NWV) dual power supply system
- Maximum operating frequency: 85MHz (LC74986NWF), 40MHz (LC74986NWV)
- Package: 144-pin SQFP

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Applications

- LCD TVs and LCD monitors
- Car TVs and car monitors
- PDP TVs

Specifications

Absolute Maximum Ratings at Ta = 25°C, DV_{SS} = 0V, AV_{SS} = 0V. Values in parentheses apply to the LC74986NWV. These are provisional specifications for the LC74986NWF.

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD}1$		–0.3 to +3.6	V
	$V_{DD}2$		–0.3 to +4.6	V
Input voltage	V_I		–0.3 to $V_{DD}2$+0.3	V
Output voltage	V_O		–0.3 to $V_{DD}2$+0.3	V
Allowable power dissipation	Pd max		TBD (0.6)	W
Storage temperature	Tstg		–55 to +125	°C
Operating temperature	Topr		–30 to +70	°C

Allowable Operating Ranges at Ta = –30 to +70°C. Values in parentheses apply to the LC74986NWV. These are provisional specifications for the LC74986NWF.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	$DV_{DD}1$	2.3 (1.7)	2.5 (1.8)	2.7 (1.9)	V
	$V_{DD}2$	$DV_{DD}2$, AV_{DD}	3.0	3.3	3.6	V
Input voltage range	V_{IN}		0		3.6	V

DC Characteristics at $V_{DD}1$ = 2.5V (LC74986NWF) or 1.8V (LC74986NWV), $V_{DD}2$ = 3.3V, Ta = –30 to +70°C. These are provisional specifications for the LC74986NWF.

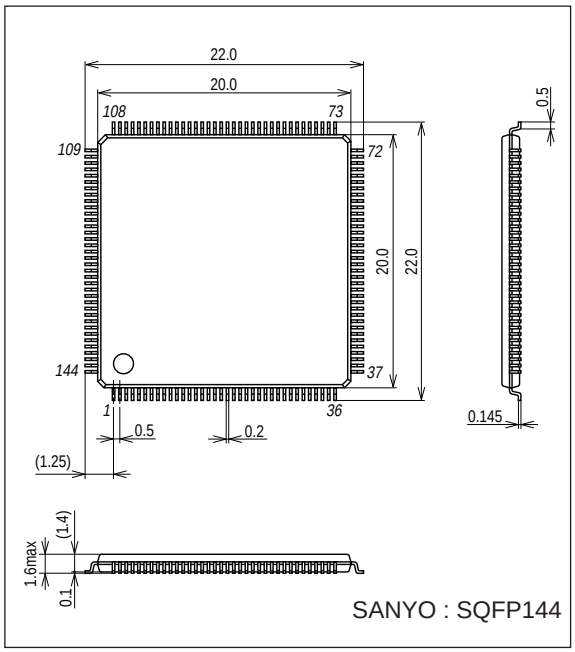
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	V_{IH}	CMOS level inputs	0.7$V_{DD}2$			V
		CMOS level Schmitt inputs	0.75$V_{DD}2$			V
Input low-level voltage	V_{IL}	CMOS level inputs			0.2$V_{DD}2$	V
		CMOS level Schmitt inputs			0.15$V_{DD}2$	V
Input high-level current	I_{IH}	V_I=$V_{DD}2$	–10		+10	µA
		V_I = $V_{DD}2$, with a pull-down resistor used	+10		+100	µA
Input low-level current	I_{IL}	V_I=V_{SS}	–10		+10	µA
Output high-level voltage	V_{OH}	B4 type, I_{OH}=–2mA	$V_{DD}2$–0.4			V
		B8 type, I_{OH}=–4mA	$V_{DD}2$–0.4			V
		B12 type, I_{OH}=–6mA	$V_{DD}2$–0.4			V
Output low-level voltage	V_{OL}	B4 type, I_{OL}=2mA			0.4	V
		B8 type, I_{OL}=4mA			0.4	V
		B12 type, I_{OL}=6mA			0.4	V
Output leakage current	I_{OZ}	In high-impedance output mode	–10		+10	µA
Pull-down resistance	R_{DN}			126		kΩ
Quiescent current	$I_{DD}1$	Outputs open, VI=V_{SS} or $V_{DD}1$			300	µA
Quiescent current*	$I_{DD}2$	Outputs open, VI=V_{SS} or $V_{DD}2$			10	µA

*: Certain input pins have built-in pull-down resistors. Thus there are cases where, due to the circuit structure, the quiescent current characteristics cannot be guaranteed.

Package Dimensions

unit : mm

3214



Input and Output Signals

• Input Signals Items shown in parentheses are alternate functions that can be selected by setting a register.

Signal type	Number of pins	Symbol	Description	Notes
Video signals	8	VPA1	Input port A	• 24-bit RGB • 24-bit YCbCr, 16-bit or 8-bit 4:2:2
	8	VPA2		
	8	VPA3		
	8	VPB1 (ROUT_2)	Input port B (External video or dual output)	
	8	VPB2 (GOUT_2)		
	8	VPB3 (BOUT_2)		
Sync signals	1	HSI	Port A system horizontal sync signal	• The input polarity is arbitrary. The IC discriminates the polarity automatically.
	1	VSI	Port A system vertical sync signal	
	1	VPBH	Port B system horizontal sync signal	• The input polarity is arbitrary. The IC discriminates the polarity automatically.
	1	VPBV (AICS/PDOWN2)	Port B system vertical sync signal (Three-wire bus chip select, power down)	• The input polarity is arbitrary. The IC discriminates the polarity automatically. • The pin can be selected by setting an internal register.
Data enable signals	1	DEHI	Port A system horizontal data enable, port A system composite enable	• The input polarity is arbitrary. It can be inverted internally. • DEVI must be held fixed at 1 when a composite video signal is input.
	1	DEVI	Port A system vertical data enable	• The input polarity is arbitrary. It can be inverted internally.
	1	VPBDEN (VPBEN)	Port B system composite data enable (External video enable)	• Only H/V composite signals are supported. • The input polarity is arbitrary. It can be inverted internally.

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Signal type	Number of pins	Symbol	Description	Notes
Pixel clock	1	CLKI	Port A system clock	• Max85MHz(LC74986NWF), Max40MHz(LC74986NWV)
	1	DCLKI	Display clock	• Max85MHz(LC74986NWF), Max40MHz(LC74986NWV)
	1	VPBCK	Port B system clock	• Max85MHz(LC74986NWF), Max40MHz(LC74986NWV)
Clock enable	1	CLKIEN	Port A system clock enable	• Positive logic
Fixed oscillator	1	XTAL	Used for the control bus and various detection functions	• Max85MHz(LC74986NWF), Max40MHz(LC74986NWV)
System reset	1	RST	System reset	• Inverted logic
External video	8	VPB1	External video signal (input port B, dual output)	• Inputs a video signal synchronized with the output • Dither processing possible. Image quality adjustments not possible. • 6-bit input also possible
	8	VPB2		
	8	VPB3		
	1	VPBEN (VPBDEN)	External video signal enable (port B system composite data enable)	• Positive logic

• Output Signals

Signal type	Number of pins	Symbol	Description	Notes
Video signals	8	ROUT	R	• Dithered 6-bit output also possible • Dual output also possible. (Odd/even inversion possible) • First data
	8	GOUT	G	
	8	BOUT	B	
	8	ROUT_2 (VPB1)	Dual output (input port B, external video signal)	• Dedicated dual system output. (Odd/even inversion possible) • Second data
	8	GOUT_2 (VPB2)		
	8	BOUT_2 (VPB3)		
Sync signals	1	HSO	Horizontal sync signal	• The sync signal, position, and polarity can be set.
	1	VSO	Vertical sync signal, composite signal	
Data enable signals	1	DEHO	Horizontal data enable	• The polarity can be set.
	1	DEVO	Vertical data enable, composite enable	• The polarity can be set.
Pixel clocks	1	CLKIO	Outputs the input clock	• The polarity can be inverted.
	1	DCLKO	Display clock	• The polarity can be inverted. Divided-by-two output possible in dual output mode.
Clamp pulse	1	CLPP	Used for A/D conversion	• Output at the clamp position. The position can be changed. The pulse width can be changed.
Clamp levels	1	CLPVPA1	VP1 clamp level	• Clamp level discrimination output (Too large: low, too small: high, match: high impedance)
	1	CLPVPA2	VP2 clamp level	
	1	CLPVPA3	VP3 clamp level	
Divided output signal for external PLL circuit	1	PLLHIO	For an external PLL circuit	

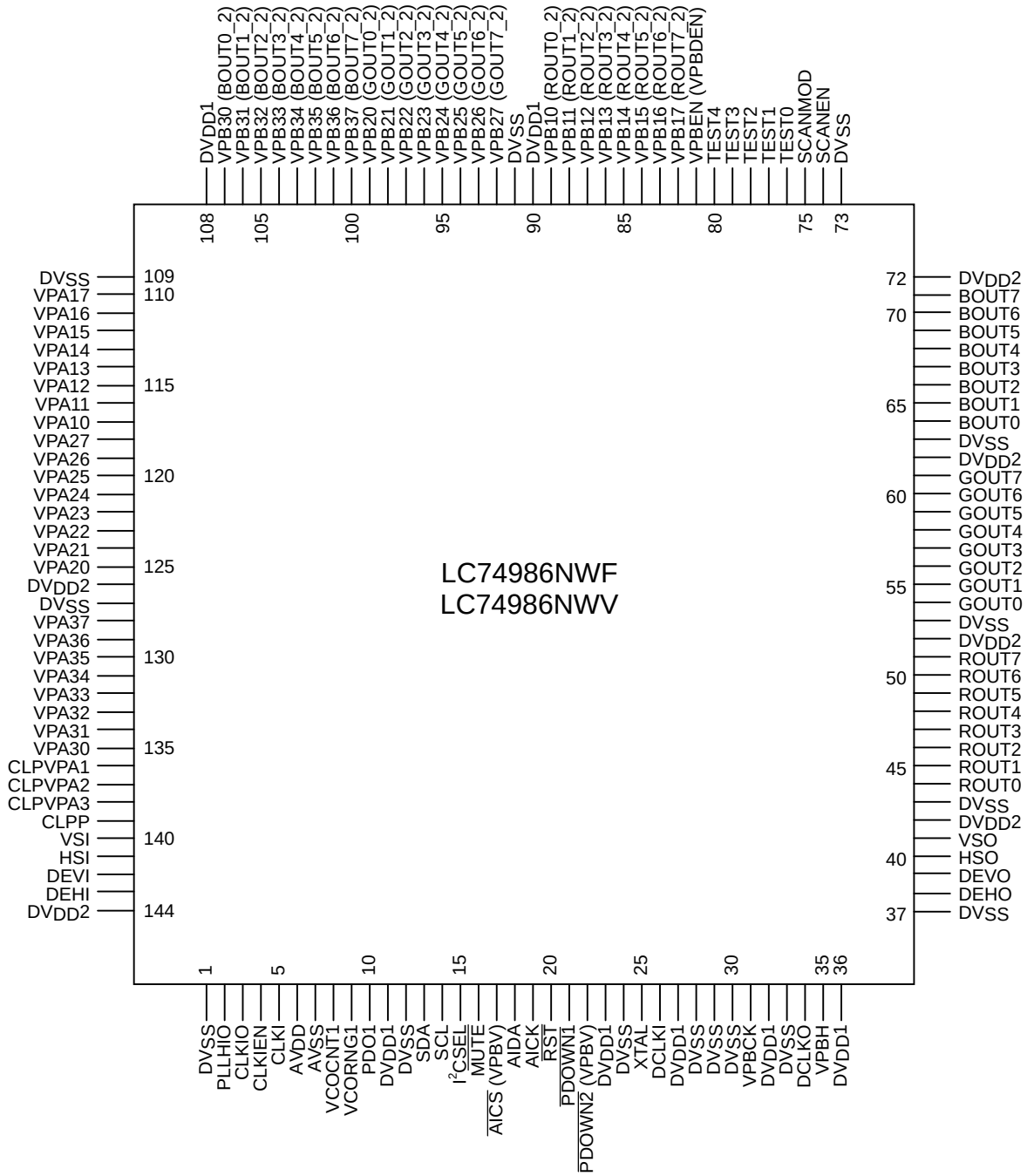
• Control Signals

Signal type	Number of pins	Symbol	Description	Notes
Three-wire bus signals	1	AICS (VPBV)	Three-wire bus chip select (port B system vertical sync signal)	• For OSD control (Normally, the I²C bus is used.)
	1	AIDA	Data bus	
	1	AICK	Bus clock	
I²C bus signals	1	SDA	Data bus	• Used for setting internal registers and for internal status output. • The slave address is 0111000 + (R/W) • OSD control, gamma correction control
	1	SCL	Bus clock	
	1	I²CSEL	Slave switching	• Normally low. 0111000 + (R/W) • Switches the IC to 0111001 + (R/W) when high.

• Other Signals

Signal type	Number of pins	Symbol	Description	Notes
Forcible mute signal	1	MUTE	Muting	• The output can be forcibly muted from this pin. Inverted logic
Power down (low-power mode) signal	2	PDOWN1 PDOWN2 (VPBV)	Low-power mode (Port B system vertical sync signal)	• Low-power mode used when the IC is not operating. This pin is normally held at the high level.
Test signals	1	SCANEN	Test	• Used for test settings. This pin must be held at the low level during normal operation.
	1	SCANMOD	Test	• Used for test settings. This pin must be held at the low level during normal operation.
	5	TEST	Test	• Used for test settings. This pin must be held at the low level during normal operation.

Pin Assignments



Top view

Pin Functions Items in parentheses apply to the LC74986NWV.

Pin number	Symbol	I/O and type		Function	Notes
		I/O	Type		
1	DV_{SS}	P	—	Digital system ground	
2	PLLHIO	O	gqcio19	Input or external PLL divided clock output	The divider ratio can be set over the I²C bus.
3	CLKIO	O	gqcio20	Outputs the input clock	Has the same period as the input system. The output can be inverted by a setting controllable over the I²C bus.
4	CLKIEN	I	gqcio02	Port A system input clock enable	This input is normally held fixed at the high level. (Positive logic.)
5	CLKI	I	gqcio02	Port A system input clock	Input signal pixel clock
6	AV_{DD}	P	—	Analog system power supply: 3.3V	Connect to $DV_{DD}2$ if unused.
7	AV_{SS}	P	—	Analog system ground	
8	VCOCNT1	I	gqcio10	PLL VCO control voltage input	Connect to AV_{SS} if unused.
9	VCORNG1	I	gqcio10	PLL range setting resistor connection	Connect to AV_{SS} if unused.
10	PDO1	O	gqcio09	PLL phase comparator output	Leave open if unused.
11	$DV_{DD}1$	P	—	Digital system power supply: 2.5V (1.8V)	
12	DV_{SS}	P	—	Digital system ground	
13	SDA	B	gqcio22	I²C bus data	Used for setting internal registers and for reading out IC status. Also used for OSD control and gamma correction settings.
14	SCL	I	gqcio03	I²C bus clock	
15	I²CSEL	I	gqcio18	I²C bus slave address switching	Normally left open (slave address: 70h) or connected to DV_{SS}.
16	MUTE	I	gqcio02	Muting control	Inverted logic
17	AICS (VPBV)	I	gqcio03	Chip select or port B system vertical sync signal	Three-wire bus: use is optional. Only used for OSD control (Normally, the I²C bus is used.) The AICS pin uses inverted logic. VPBP can be used by setting a register.
18	AIDA	I	gqcio03	Data	
19	AICK	I	gqcio03	Clock	
20	RST	I	gqcio03	Initial reset	Inverted logic
21	PDOWN1	I	gqcio02	Power down	Normally held fixed at the high level (Used for testing.)
22	PDOWN2 (VPBV)	I	gqcio03	Power down or port B system vertical sync signal	(Used for testing.) VPBV can be used by setting a register.
23	$DV_{DD}1$	P	—	Digital system power supply: 2.5V (1.8V)	
24	DV_{SS}	P	—	Digital system ground	
25	XTAL	I	gqcio02	Clock input for the detection functions	Connection for the fixed-frequency oscillator
26	DCLKI	I	gqcio02	Display clock input	Display processing pixel clock
27	$DV_{DD}1$	P	—	Digital system power supply: 2.5V (1.8V)	
28	DV_{SS}	P	—	Digital system ground	
29	DV_{SS}	P	—	Digital system ground	
30	DV_{SS}	P	—	Digital system ground	
31	VPBCK	I	gqcio02	Port B system input clock	Port B system input signal pixel clock
32	$DV_{DD}1$	P	—	Digital system power supply: 2.5V (1.8V)	
33	DV_{SS}	P	—	Digital system ground	
34	DCLK0	O	gqcio20	LCD panel module clock output	Has the same period as DCLKI. Alternatively, may have 1/2 the period.
35	VPBH	I	gqcio03	Port B system horizontal sync signal	Port B system input horizontal sync signal
36	$DV_{DD}1$	P	—	Digital system power supply: 2.5V (1.8V)	
37	DV_{SS}	P	—	Digital system ground	
38	DEHO	O	gqcio19	FPD module horizontal enable	The polarity can be selected over the I²C bus.
39	DEVO	O	gqcio19	FPD module vertical enable	A composite signal can be output from DEVO.
40	HSO	O	gqcio19	FPD module horizontal sync signal	The polarity and pulse width can be set over the I²C bus.
41	VSO	O	gqcio19	FPD module vertical sync signal	A composite sync signal can be output from VSO.
42	$DV_{DD}2$	P	—	Digital system power supply: 3.3V	
43	DV_{SS}	P	—	Digital system ground	
44	ROUT0	O	gqcio19	FPD module R output	LSB (The ROUT5:0 pins are used for 6-bit output.) When 2-phase output is used, the first byte is data. (MSB when 6-bit output is selected)
45	ROUT1	O	gqcio19		
46	ROUT2	O	gqcio19		
47	ROUT3	O	gqcio19		
48	ROUT4	O	gqcio19		
49	ROUT5	O	gqcio19		
50	ROUT6	O	gqcio19		
51	ROUT7	O	gqcio19		MSB
52	$DV_{DD}2$	P	—	Digital system power supply: 3.3V	
53	DV_{SS}	P	—	Digital system ground	

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Pin number	Symbol	I/O and type		Function	Notes
		I/O	Type		
54	GOUT0	O	gqcio19	FPD module G output	LSB
55	GOUT1	O	gqcio19		(The ROUT5:0 pins are used for 6-bit output.)
56	GOUT2	O	gqcio19		When 2-phase output is used, the first byte is data.
57	GOUT3	O	gqcio19		(MSB when 6-bit output is selected)
58	GOUT4	O	gqcio19		
59	GOUT5	O	gqcio19		
60	GOUT6	O	gqcio19		
61	GOUT7	O	gqcio19		MSB
62	$DV_{DD}2$	P	—	Digital system power supply: 3.3V	
63	DV_{SS}	P	—	Digital system ground	
64	BOUT0	O	gqcio19	FPD module B output	LSB
65	BOUT1	O	gqcio19		(The ROUT5:0 pins are used for 6-bit output.)
66	BOUT2	O	gqcio19		When 2-phase output is used, the first byte is data.
67	BOUT3	O	gqcio19		(MSB when 6-bit output is selected)
68	BOUT4	O	gqcio19		
69	GOUT5	O	gqcio19		
70	GOUT6	O	gqcio19		
71	GOUT7	O	gqcio19		MSB
72	$DV_{DD}2$	P	—	Digital system power supply: 3.3V	
73	DV_{SS}	P	—	Digital system ground	
74	SCANEN	I	gqcio18	Test settings	Normally left open or connected to DV_{SS}
75	SCANMOD	I	gqcio18		
76	TEST0	I	gqcio18		
77	TEST1	I	gqcio18		
78	TEST2	I	gqcio18		
79	TEST3	I	gqcio18		
80	TEST4	I	gqcio18		
81	VPBEN (VPBDEN)	I	gqcio03	External video input enable or port B system enable	Enable: positive logic. Connect to DV_{SS} if unused.
82	VPB17 (ROUT7_2)	I/O	gqcio35	Video data input (R) or port B system input or 2-phase output	MSB
83	VPB16 (ROUT6_2)	I/O	gqcio35		(MSB when 6-bit input or output mode selected)
84	VPB15 (ROUT5_2)	I/O	gqcio35		(Data is input to VPB15 to VPB10 in 6-bit input mode.)
85	VPB14 (ROUT4_2)	I/O	gqcio35		Second data in 2-phase output mode
86	VPB13 (ROUT3_2)	I/O	gqcio35		Connect to DV_{SS} if unused.
87	VPB12 (ROUT2_2)	I/O	gqcio35		
88	VPB11 (ROUT1_2)	I/O	gqcio35		
89	VPB10 (ROUT0_2)	I/O	gqcio35		LSB
90	$DV_{DD}1$	P	—	Digital system power supply: 2.5V (1.8V)	
91	DV_{SS}	P	—	Digital system ground	
92	VPB27 (GOUT7_2)	I/O	gqcio35	Video data input (G) or port B system input or 2-phase output	MSB
93	VPB26 (GOUT6_2)	I/O	gqcio35		(MSB when 6-bit input or output mode selected)
94	VPB25 (GOUT5_2)	I/O	gqcio35		(Data is input to VPB25 to VPB20 in 6-bit input mode.)
95	VPB24 (GOUT4_2)	I/O	gqcio35		Second data in 2-phase output mode
96	VPB23 (GOUT3_2)	I/O	gqcio35		Connect to DV_{SS} if unused.
97	VPB22 (GOUT2_2)	I/O	gqcio35		
98	VPB21 (GOUT1_2)	I/O	gqcio35		
99	VPB20 (GOUT0_2)	I/O	gqcio35		LSB
100	VPB37 (BOUT7_2)	I/O	gqcio35	Video data input (B) or port B system input or 2-phase output	MSB
101	VPB36 (BOUT6_2)	I/O	gqcio35		(MSB when 6-bit input or output mode selected)
102	VPB35 (BOUT5_2)	I/O	gqcio35		(Data is input to VPB35 to VPB30 in 6-bit input mode.)
103	VPB34 (BOUT4_2)	I/O	gqcio35		Second data in 2-phase output mode
104	VPB33 (BOUT3_2)	I/O	gqcio35		Connect to DV_{SS} if unused.
105	VPB32 (BOUT2_2)	I/O	gqcio35		
106	VPB31 (BOUT1_2)	I/O	gqcio35		
107	VPB30 (BOUT0_2)	I/O	gqcio35		LSB
108	$DV_{DD}1$	P	—	Digital system power supply: 2.5V (1.8V)	
109	DV_{SS}	P	—	Digital system ground	

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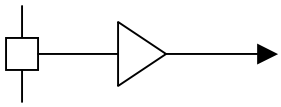
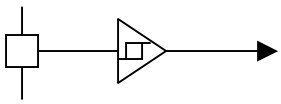
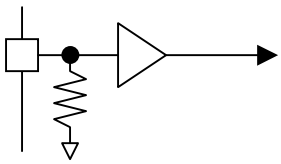
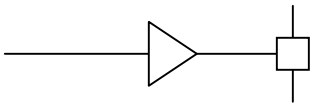
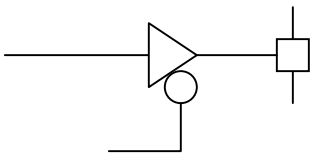
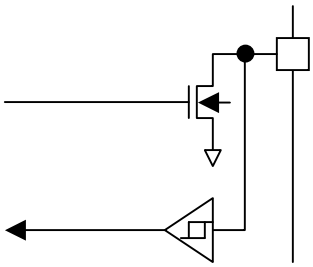
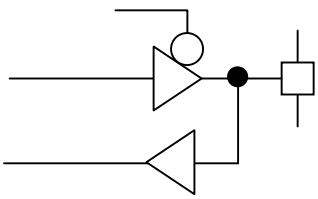
Pin number	Symbol	I/O and type		Function	Notes
		I/O	Type		
110	VPA17	I	gqcio02	Port A system input	MSB
111	VPA16	I	gqcio02		Y/R/YCbCr multiplexed
112	VPA15	I	gqcio02		Connect to DV_{SS} if unused.
113	VPA14	I	gqcio02		
114	VPA13	I	gqcio02		
115	VPA12	I	gqcio02		
116	VPA11	I	gqcio02		
117	VPA10	I	gqcio02		LSB
118	VPA27	I	gqcio02	Port A system input	MSB
119	VPA26	I	gqcio02		Cb/G/CbCr multiplexed or YCbCr multiplexed
120	VPA25	I	gqcio02		Connect to DV_{SS} if unused.
121	VPA24	I	gqcio02		
122	VPA23	I	gqcio02		
123	VPA22	I	gqcio02		
124	VPA21	I	gqcio02		
125	VPA20	I	gqcio02		LSB
126	$DV_{DD}2$	P	—	Digital system power supply: 3.3V	
127	DV_{SS}	P	—	Digital system ground	
128	VPA37	I	gqcio02	Port A system input	MSB
129	VPA36	I	gqcio02		Cr/B/YCbCr multiplexed
130	VPA35	I	gqcio02		Connect to DV_{SS} if unused.
131	VPA34	I	gqcio02		
132	VPA33	I	gqcio02		
133	VPA32	I	gqcio02		
134	VPA31	I	gqcio02		
135	VPA30	I	gqcio02		LSB
136	CLPVPA1	O	gqcio21	VPA1 clamp level detection output	The clamp level can be set over the I^2C bus.
137	CLPVPA2	O	gqcio21	VPA2 clamp level detection output	
138	CLPVPA3	O	gqcio21	VPA3 clamp level detection output	
139	CLPP	O	gqcio05	Clamp pulse output	The clamp position and width can be set over the I^2C bus.
140	VSI	I	gqcio03	Vertical sync signal input	Arbitrary polarity. The IC discriminates the polarity automatically.
141	HSI	I	gqcio03	Horizontal sync signal input	
142	DEVI	I	gqcio03	Vertical data enable input	Arbitrary polarity. A composite signal can be input to DEHI.
143	DEHI	I	gqcio03	Horizontal data enable input	Hold DEVI fixed at the high level if a composite signal is used.
144	$DV_{DD}2$	P	—	Digital system power supply: 3.3V	

Pin Type

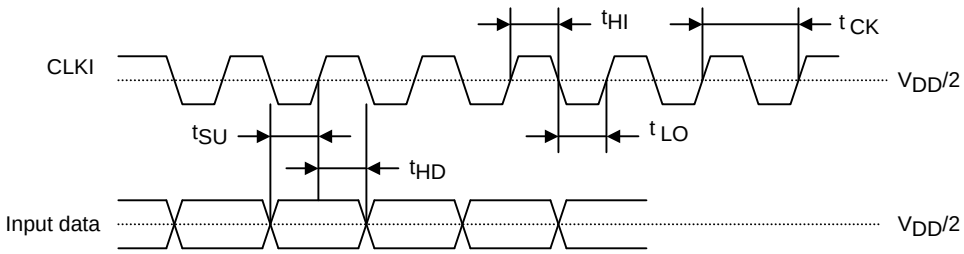
Input or output circuit type	Function	Equivalent circuit	Applicable pins
gqcio02	Input		CLKIEN, CLKI, XTAL, DCLKI, PDOWN1, VPA10 to VPA17, VPA20 to VPA27, VPA30 to VPA37, MUTE, VPBCK
gqcio03	Schmitt trigger input		SCL, AICS, AIDA, AICK, RST, VPBEN, VSI, HSI, DEVI, DEHI, PDOWN2, VPBH
gqcio18	Input with built-in pull-down resistor		I^2CSEL, SCANEN, SCAMOD, TEST0 to TEST4*
gqcio05	4mA drive output		CLPP*
gqcio19	8mA drive output		PLLHIO, DEHO, DEVO, HSO, VSO, ROUT0 to ROUT7, GOUT0 to GOUT7, BOUT0 to BOUT7*
gqcio20	12mA drive output		CLKIO, DCLKO*
gqcio21	4mA 3-state drive output		CLPVPA1, CLPVPA2, CLPVPA3*
gqcio22	Open-drain I/O		SDA
gqcio10	Analog through		VCOCNT1, VCORNG1
gqcio09	Analog through		PDO1*
gqcio35	8mA drive bidirectional		VPB10 to VPB17, VPB20 to VPB27, VPB30 to VPB37

Notes:

- Pins marked with an asterisk (*) must be left open if unused.
- If noise or other problems due to external factors can be expected, input pins with built-in pull-down resistors must be connected to DV_{SS}.
- All of the DV_{DD}* and DV_{SS} pins must be connected to the corresponding power supply system. These pins must not be left open.
- All of the AV_{DD} and AV_{SS} pins must be connected to the corresponding power supply system. These pins must not be left open.

Input and Output Data Timing

• Input Data Timing 1

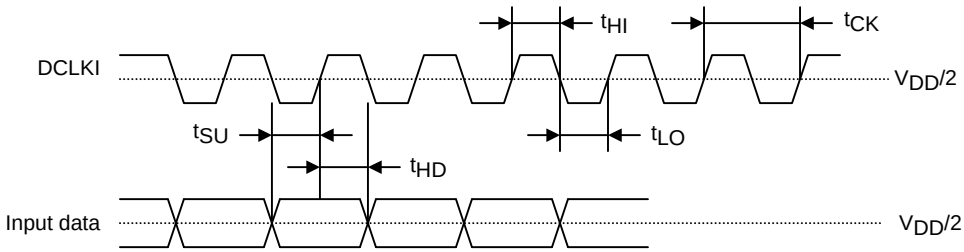


Items in parentheses refer to the LC74986NWV.

Pin Name	Parameter	Symbol	min	max	unit
CLKI	Clock low level time	t_{LO}	5.5 (12.5)	—	ns
	Clock high level time	t_{HI}	5.5 (12.5)	—	ns
	Clock period	t_{CK}	11.0 (25.0)	—	ns
VPA1 [7:0], VPA2 [7:0]	Input data setup time	t_{SU}	3.0	—	ns
VPA3 [7:0], VSI, HSI, DEVI, DEHI, CLKIEN	Input data hold time	t_{HD}	3.0	—	ns

* : An input clock duty of 50% is recommended.

• Input Data Timing 2

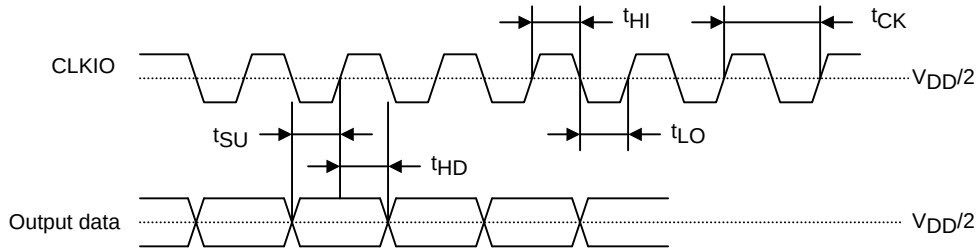


Items in parentheses refer to the LC74986NWV.

Pin Name	Parameter	Symbol	min	max	unit
DCLKI	Clock low level time	t_{LO}	5.5 (12.5)	—	ns
	Clock high level time	t_{HI}	5.5 (12.5)	—	ns
	Clock period	t_{CK}	11.0 (25.0)	—	ns
VPBEN, VPB1 [7:0], VPB2 [7:0], VPB3 [7:0]	Input data setup time	t_{SU}	3.0	—	ns
	Input data hold time	t_{HD}	3.0	—	ns

* : An input clock duty of 50% is recommended.

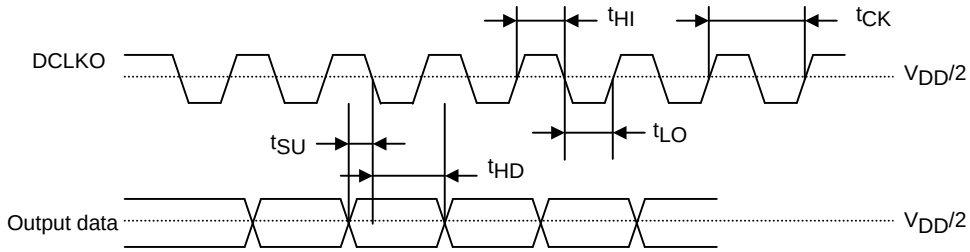
• Output Data Timing 1



Items in parentheses refer to the LC74986NWV.

Pin Name	Parameter	Symbol	min	max	unit
CLKIO	Clock low level time	t_{LO}	5.5 (12.5)	—	ns
	Clock high level time	t_{HI}	5.5 (12.5)	—	ns
	Clock period	t_{CK}	11.0 (25.0)	—	ns
CLPVPA1, CLPVPA2, CLPVPA3, CLPP, PLLHIO	Output data setup time	t_{SU}	2.0	—	ns
	Output data hold time	t_{HD}	2.0	—	ns

• Output Data Timing 2

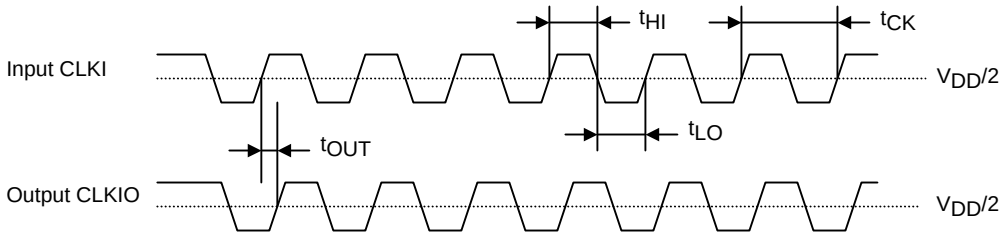


Items in parentheses refer to the LC74986NWV.

Pin Name	Parameter	Symbol	min	max	unit
DCLKO	Clock low level time	t_{LO}	5.5 (12.5)	—	ns
	Clock high level time	t_{HI}	5.5 (12.5)	—	ns
	Clock period	t_{CK}	11.0 (25.0)	—	ns
DEHO, DEVO, HSO, VSO, ROUT [7:0], GOUT [7:0], BOUT [7:0]	Output data setup time	t_{SU}	2.0	—	ns
	Output data hold time	t_{HD}	2.0	—	ns

Input and Output Clock Timing

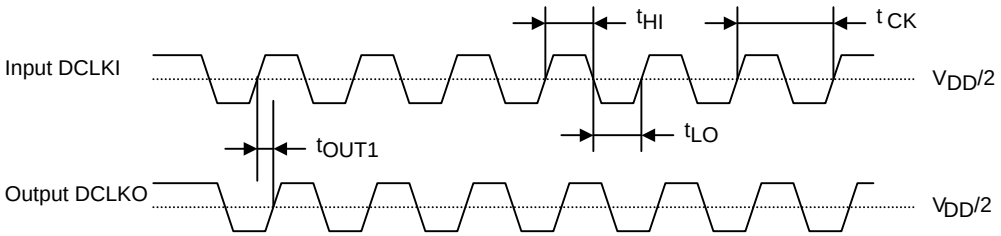
• Input System Clock Timing



Items in parentheses refer to the LC74986NWV.

Pin Name	Parameter	Symbol	min	max	unit
CLKI	Clock low level time	t_{LO}	5.5 (12.5)	—	ns
	Clock high level time	t_{HI}	5.5 (12.5)	—	ns
	Clock period	t_{CK}	11.0 (25.0)	—	ns
CLKIO	CLKIO delay time	t_{OUT}	0	17	ns

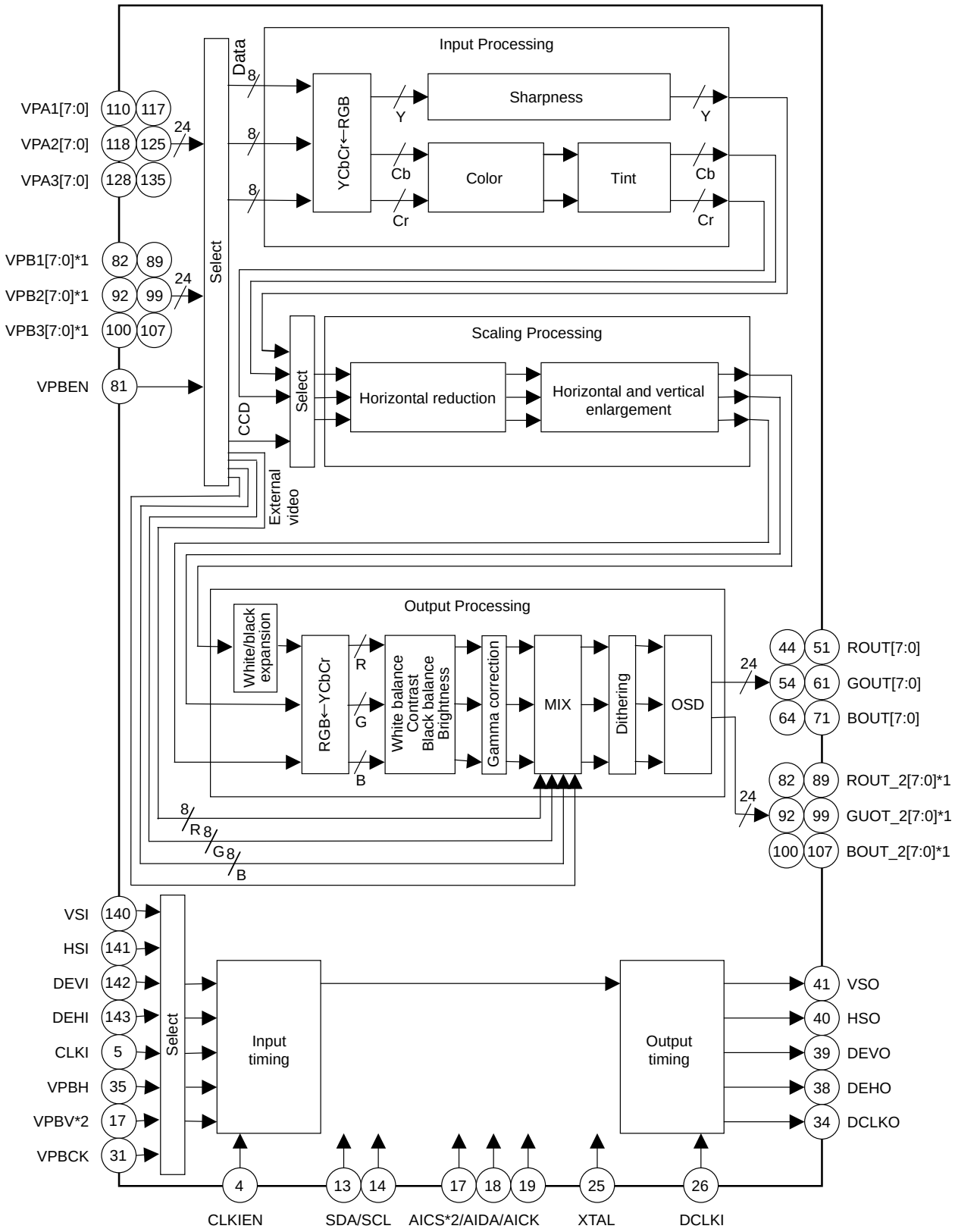
• Output System Clock Timing



Items in parentheses refer to the LC74986NWV.

Pin Name	Parameter	Symbol	min	max	unit
DCLKI	Clock low level time	t_{LO}	5.5 (12.5)	—	ns
	Clock high level time	t_{HI}	5.5 (12.5)	—	ns
	Clock period	t_{CK}	11.0 (25.0)	—	ns
DCLKO	DCLKO delay time	t_{OUT}	0	20	ns

Internal Block Diagram



*1, *2: Register selection