

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

				unit
Maximum Supply Voltage	$V_{DD}-V_{EE}$ max	$V_{DD}, V_{EE}, *1$	12	V
	V_{CC} max	$V_{CC}, *1$	$V_{SS} - 0.3$ to $V_{CC} + 7$	V
Maximum Input Voltage	V_{I1}	CLK, DI	$V_{SS} - 0.3$ to $V_{CC} + 0.3$	V
	V_{I2}	f1 to f7, IN1, IN2, S, TEST1	$V_{EE} - 0.3$ to $V_{DD} + 0.3$	V
Allowable Power Dissipation	P_d max	$T_a \leq 75^\circ\text{C}$	200	mW
Operating Temperature	T_{opg}		-30 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	*2	-40 to +125	$^\circ\text{C}$

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$, $V_{SS} = V_{EE} = 0\text{V}$

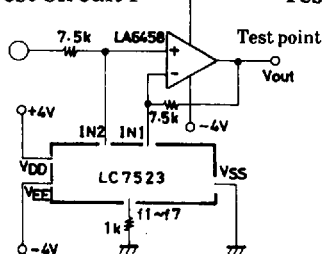
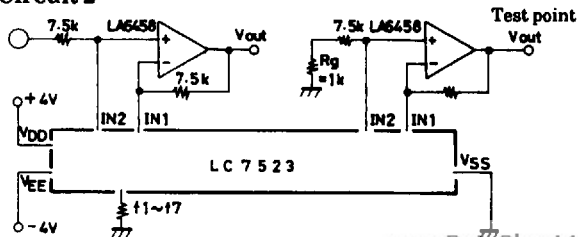
				unit
Supply Voltage	V_{DD}	V_{DD}	8.0	V
	V_{EE}	V_{EE}	0	V
	V_{CC}	V_{CC}	5.0	V

Allowable Operating Conditions at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

				unit
Supply Voltage	$V_{DD}-V_{EE}$	V_{DD}, V_{EE} ,	4.5 to 11.0	V
	V_{CC}	V_{CC}	4.0 to 5.5	V
Input 'H'-Level Voltage	V_{IH1}	CLK, DI, *3	$0.8V_{CC}$ to V_{CC}	V
	V_{IH2}	S	$0.9(V_{DD} - V_{EE}) + V_{EE}$ to V_{DD}	V
	V_{IH3}	IN1, IN2, f1 to f7	up to V_{DD}	Vp
Input 'L'-Level Voltage	V_{IL1}	CLK, DI	$0.2V_{CC}$	V
	V_{IL2}	S, TEST1	V_{EE} to $0.1(V_{DD} - V_{EE}) + V_{EE}$	V
	V_{IL3}	IN1, IN2, f1 to f7	V_{EE} or more	Vp
Input Pulse Width	$t_{\phi w}$	CLK	1 or more	μs
Setup Time	t_{setup}	DI	1 or more	μs
Hold Time	t_{hold}	DI	1 or more	μs
Operating Frequency	f_{opg}	CLK	up to 330	kHz

Electrical Characteristics at $T_a = 25^\circ\text{C}$

			min	typ	max	unit
Total Harmonic Distortion	THD1	Test Circuit 1, $V_{out} = 1\text{V}$, flat mode, $f = 20\text{kHz}$		0.005	0.010	%
	THD2	Test Circuit 1, $V_{out} = 1\text{V}$, flat mode, $f = 1\text{kHz}$		0.0015	0.003	%
	THD3	Test Circuit 1, $V_{out} = 1\text{V}$, boost mode, $f = 20\text{kHz}$		0.04	0.10	%
	THD4	Test Circuit 1, $V_{out} = 1\text{V}$, boost mode, $f = 1\text{kHz}$		0.04	0.10	%
Crosstalk	CT	Test Circuit 2, $f = 20\text{kHz}$, $V_{out} = 1\text{V}$		55		dB
Current Dissipation	I_{DD}	$V_{DD} - V_{EE} = 10\text{V}$			1	mA
	I_{CC}	$V_{CC} = 5\text{V}$			1	mA
Analog SW OFF Leak Current	I_{off}	f1 to f7			10	μA

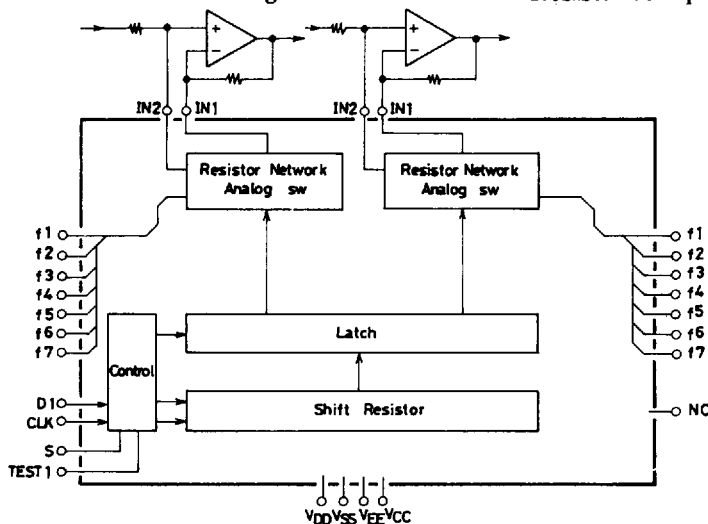
Test Circuit 1**Test Circuit 2**

*1 : Connect a capacitor of 1000pF or greater across each power supply pin and V_{SS} pin.

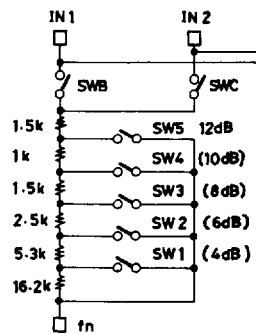
*2 : When mounting the MFP package on the board, do not dip it in solder.

*3 : When the control signal on the microcomputer side rises earlier than V_{DD} on the LC7523, connect a resistor of 2k Ω or greater halfway through DI, CLK lines.

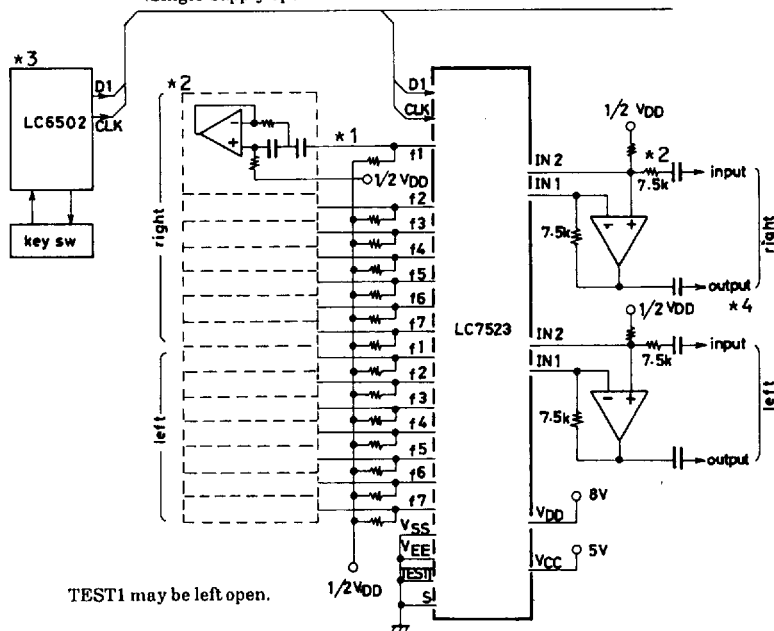
Equivalent Circuit Block Diagram



Resistance Equivalent Circuit (for one band)



Sample Application Circuit (Single-supply operation)



*1: It is recommended that $1/2V_{DD}$ is applied to pins f1 to f7 through resistors of $1M\Omega$ so that noise is minimized at the select mode.

*2: The optimum conditions for 2dB/step are as follows:

$V_{DD} = 8V$, feedback resistance of OP amp: $7.5k\Omega$, equivalent LC resonance impedance: $1k\Omega$
(For $V_{DD} = 14V$, the LC7522 is recommended.)

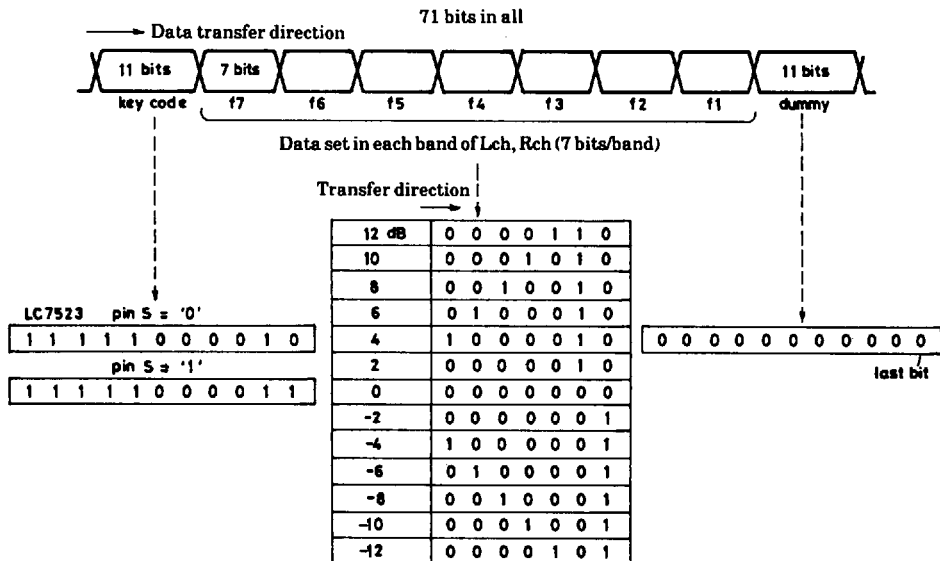
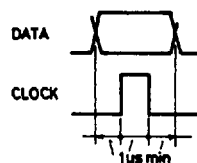
*3: The LC7060 is available as a standard controller.

*4: The LC7560 (LCD driver), LC7565 (FLT, LED driver) are available as spectrum analyzing display drivers for graphic equalizer output signal.

Data Code

Note 1. When power is applied, data '0' must be first transferred for 60 clocks (initial clock) or more. If data transfer is stopped halfway, the transfer of the remaining data must be completed or data transfer must be started after the initial clocks have been transferred.

Note 2. When the DI, CLK pins are shared with the LC7560, etc., the maximum initial clocks for such device must be transferred.



Pin Description

SANYO SEMICONDUCTOR CORP

Pin Name	Pin Configuration	Description
V _{DD} V _{SS} V _{EE}		Power supply pin. Power supply for audio signal. Power supply pin. 0V. Power supply pin. Power supply for audio signal, connected to V _{SS} at single-supply operation.
V _{CC}		Power supply pin. +5V typ. Must not rise earlier than V _{DD} .
DI		Used to input data from CPU. Schmitt inverter type.
CLK		Used to input clock from CPU. Schmitt inverter type.
IN1 IN2		Audio signal input pin. Normally, IN1 is connected to inverting input of OP amp. Normally, IN2 is connected to noninverting input of OP amp. Provided in Lch/Rch.
f1 to f7		Band filter connecting pin. f1 to f7 × 2(right/left) = 14 (total) pins.
S		Select pin at 2-chip used mode. To accept data under key code 7C3, S must be set to '1'. → Connected to V _{DD} . To accept data under key code 7C2, S must be set to '0'. → Connected to V _{EE} .
TEST1		IC test pin. Left open or connected to V _{EE} .
TEST2		May be left open during operation or connected to V _{SS} through a resistor of 1MΩ.
NC		No connection pin. Nothing must be connected to this pin.