Ordering number : ENN7332

CMOS LSI

LC75344M

Two-Channel Electronic Volume Control System

Overview

The LC75344M is a two-channel electronic volume control IC that is controlled by data input over a serial interface.

Functions

- Volume control: 0 dB to –50 dB in 1 dB steps, –52 dB to –78 dB in 2 dB steps, and –∞, for a total of 66 positions.
  A balance function can be implemented by controlling the left and right channels independently.

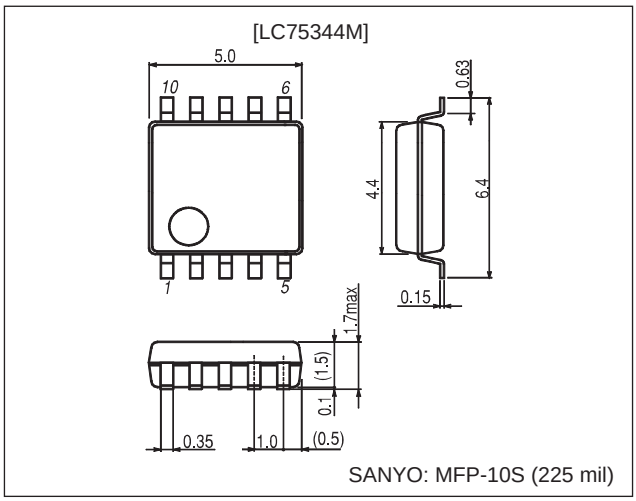
Features

- Built-in buffer amplifiers minimize the number of external components required.
- Fabricated in a silicon gate CMOS process to minimize the switching noise generated by internal switches.
- Built-in reference voltage generation circuit for the analog ground level.
- All settings are controlled by data input over a serial interface that conforms to the CCB specifications.

Package Dimensions

unit: mm

3086B-MFP10S



- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}		11	V
Maximum input voltage	V_{IN} max	CE, DI, CL		–0.3 to +11	V
		LIN, RIN		V_{SS} – 0.3 to V_{DD} + 0.3	
Allowable power dissipation	Pd max		Ta ≤ 75°C *1: When mounted on a PCB.	300	mW
Operating temperature	Topr			–30 to +75	°C
Storage temperature	Tstg			–40 to +125	°C

Note : *1 114.3 × 76.1 × 1.6mm glass epoxy board

Allowable Operating Ranges at Ta = –30 to +75°C, V_{SS} = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	V_{DD}	V_{DD}		4.5		10	V
Input high-level voltage	V_{IH}	CL, DI, CE		2.0		10	V
Input low-level voltage	V_{IL}	CL, DI, CE	7.5 ≤ V_{DD} ≤ 10	V_{SS}		0.8	V
			4.5 ≤ V_{DD} < 7.5	V_{SS}		0.3	
Input voltage amplitude	V_{IN}	LIN, RIN		V_{SS}		V_{DD}	Vp-p
Input pulse width	tøW	CL		1			µs
Setup time	tsetup	CL, DI, CE		1			µs
Hold time	thold	CL, DI, CE		1			µs
Operating frequency	fopg	CL				500	kHz

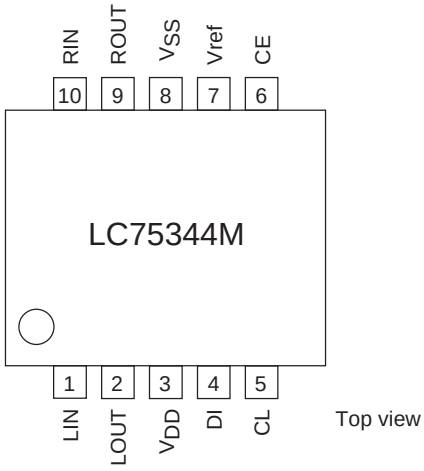
Electrical Characteristics at Ta = 25°C, V_{DD} = 9 V, V_{SS} = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	Rin	LIN, RIN			50		kΩ

Overall Characteristics

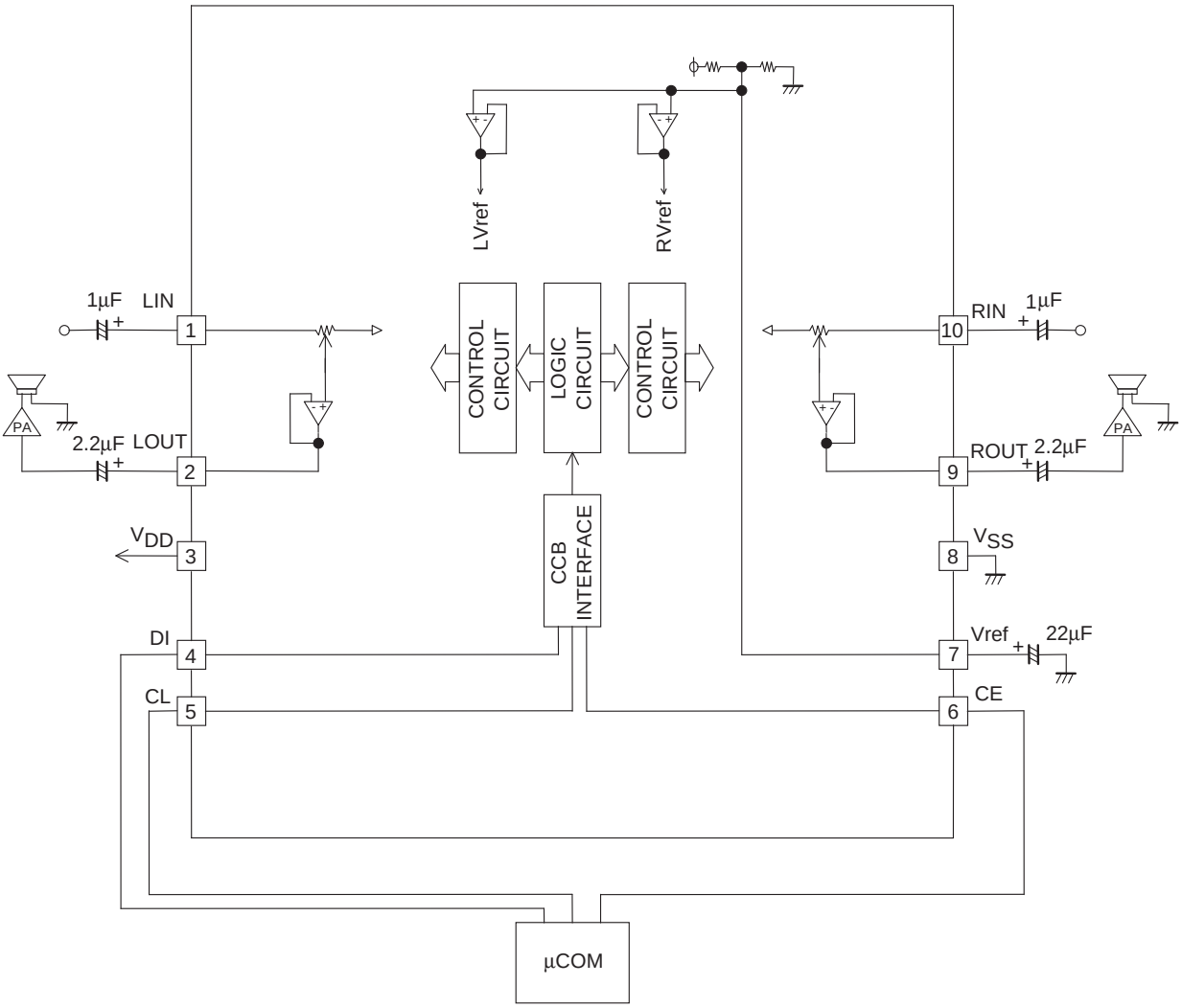
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz With all settings flat overall		0.002	0.01	%
		V_{IN} = 1 Vrms, f = 20 kHz With all settings flat overall		0.003		
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, Rg = 1 kΩ With all settings flat overall	90			dB
Output noise voltage	VN	80 kHz L.P.F, Rg = 1 kΩ With all settings flat overall		6.0		µV
Maximum attenuation	Vomin	V_{IN} = 1 Vrms, f = 1 kHz With all settings flat overall		–92		dB
Current drain	I_{DD}	V_{DD} – V_{SS} = +9 V		12		mA
Input high-level current	I_{IH}	CL, DI, CE: V_{IN} = 10 V			10	µA
Input low-level current	I_{IL}	CL, DI, CE: V_{IN} = 0 V	–10			µA

Pin Assignment



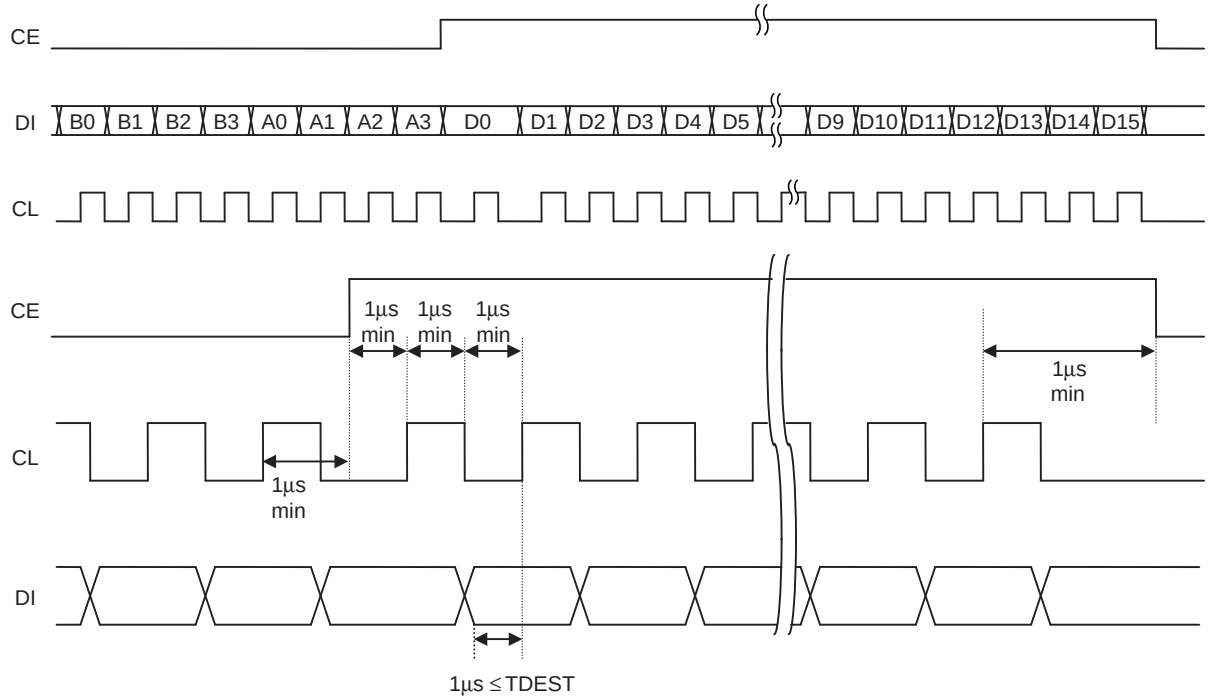
Top view

Equivalent Circuit



Control System Timing and Data Format

The LC75344M is controlled by inputting the stipulated data serially to the CL, DI, and CE pins. The data consists of a total of 24 bits, of which 8 bits are the address and 16 bits are the data.



- Address Code (B0 to A3)
  The data has an 8-bit address field, and conforms to the Sanyo CCB serial bus specifications.

Address code

B0	B1	B2	B3	A0	A1	A2	A3	
(LSB) 0	0	0	1	0	0	0	1	(88HEX)

• Control Code Allocations
Volume control

D0	D1	D2	D3	D4	D5	D6	D7	Operation
0	0	0	0	0	0	0	0	0dB
1	0	0	0	0	0	0	0	–1dB
0	1	0	0	0	0	0	0	–2dB
1	1	0	0	0	0	0	0	–3dB
0	0	1	0	0	0	0	0	–4dB
1	0	1	0	0	0	0	0	–5dB
0	1	1	0	0	0	0	0	–6dB
1	1	1	0	0	0	0	0	–7dB
0	0	0	1	0	0	0	0	–8dB
1	0	0	1	0	0	0	0	–9dB
0	1	0	1	0	0	0	0	–10dB
1	1	0	1	0	0	0	0	–11dB
0	0	1	1	0	0	0	0	–12dB
1	0	1	1	0	0	0	0	–13dB
0	1	1	1	0	0	0	0	–14dB
1	1	1	1	0	0	0	0	–15dB
0	0	0	0	1	0	0	0	–16dB
1	0	0	0	1	0	0	0	–17dB
0	1	0	0	1	0	0	0	–18dB
1	1	0	0	1	0	0	0	–19dB
0	0	1	0	1	0	0	0	–20dB
1	0	1	0	1	0	0	0	–21dB
0	1	1	0	1	0	0	0	–22dB
1	1	1	0	1	0	0	0	–23dB
0	0	0	1	1	0	0	0	–24dB
1	0	0	1	1	0	0	0	–25dB
0	1	0	1	1	0	0	0	–26dB
1	1	0	1	1	0	0	0	–27dB
0	0	1	1	1	0	0	0	–28dB
1	0	1	1	1	0	0	0	–29dB
0	1	1	1	1	0	0	0	–30dB
1	1	1	1	1	0	0	0	–31dB
0	0	0	0	0	1	0	0	–32dB
1	0	0	0	0	1	0	0	–33dB
0	1	0	0	0	1	0	0	–34dB
1	1	0	0	0	1	0	0	–35dB
0	0	1	0	0	1	0	0	–36dB
1	0	1	0	0	1	0	0	–37dB
0	1	1	0	0	1	0	0	–38dB
1	1	1	0	0	1	0	0	–39dB
0	0	0	1	0	1	0	0	–40dB

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Volume control

D0	D1	D2	D3	D4	D5	D6	D7	Operation
1	0	0	1	0	1	0	0	–41dB
0	1	0	1	0	1	0	0	–42dB
1	1	0	1	0	1	0	0	–43dB
0	0	1	1	0	1	0	0	–44dB
1	0	1	1	0	1	0	0	–45dB
0	1	1	1	0	1	0	0	–46dB
1	1	1	1	0	1	0	0	–47dB
0	0	0	0	1	1	0	0	–48dB
1	0	0	0	1	1	0	0	–49dB
0	1	0	0	1	1	0	0	–50dB
0	0	1	0	1	1	0	0	–52dB
0	1	1	0	1	1	0	0	–54dB
0	0	0	1	1	1	0	0	–56dB
0	1	0	1	1	1	0	0	–58dB
0	0	1	1	1	1	0	0	–60dB
0	1	1	1	1	1	0	0	–62dB
0	0	0	0	0	0	1	0	–64dB
0	1	0	0	0	0	1	0	–66dB
0	0	1	0	0	0	1	0	–68dB
0	1	1	0	0	0	1	0	–70dB
0	0	0	1	0	0	1	0	–72dB
0	1	0	1	0	0	1	0	–74dB
0	0	1	1	0	0	1	0	–76dB
0	1	1	1	0	0	1	0	–78dB
0	0	0	0	1	0	1	0	–∞

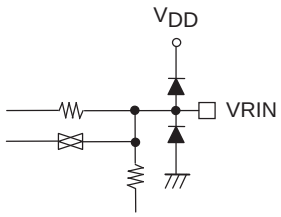
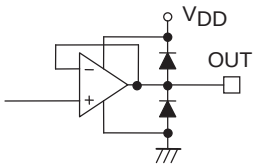
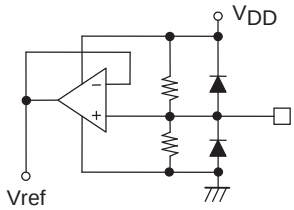
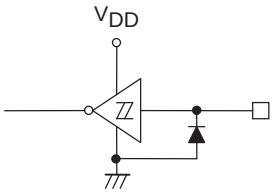
Channel selection

D8	D9	Operation
1	0	RCH
0	1	LCH
1	1	Left and right channels together

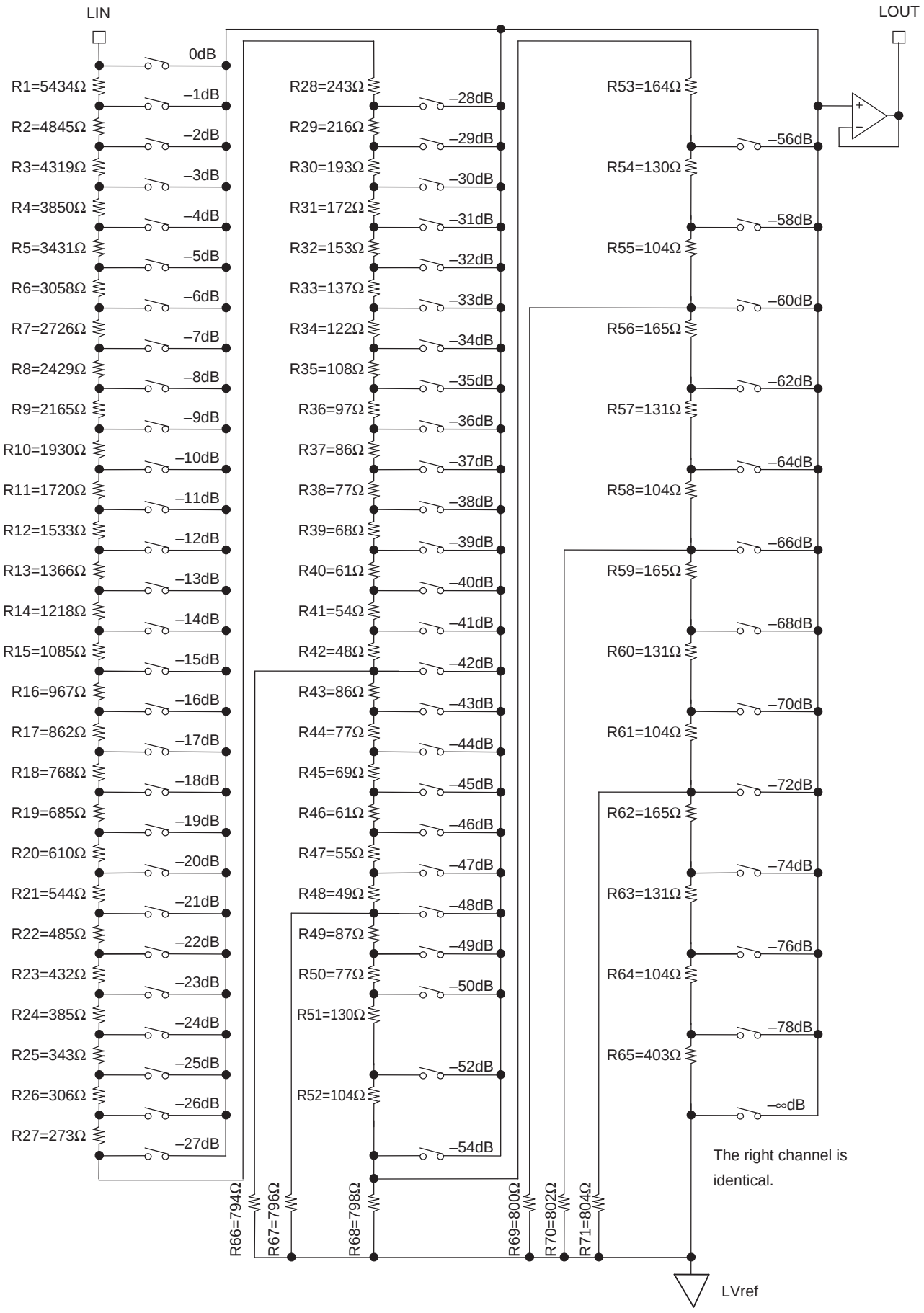
Test mode

D10	D11	D12	D13	D14	D15	Operation
0	0	0	0	0	0	
These bits specify the IC test mode. They must be set to zero for normal operation.						

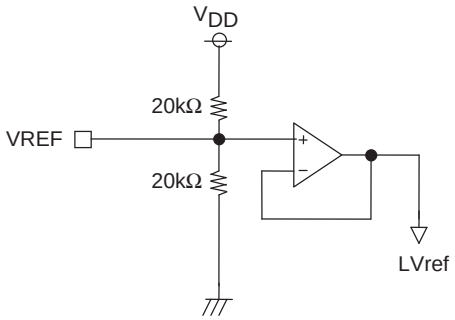
Pin Functions

Pin No.	Pin	Function	Notes
1 10	LIN RIN	Volume control inputs	
2 9	LOUT ROUT	Volume control outputs	
7	Vref	$V_{DD} \times 0.5$ voltage generator block for the analog ground level. A capacitor with a value a few times 10 µF must be inserted between Vref and AV_{SS} (V_{SS}) to minimize power supply ripple.	
8	V_{SS}	Ground	
3	V_{DD}	Power supply	
6	CE	Chip enable The internal latch data is written and the analog switches operate at the point this pin goes from high to low. Data transfer is enabled when this pin is at the high level.	
4 5	DI CL	Serial data and clock inputs for IC control.	

Internal Equivalent Circuit



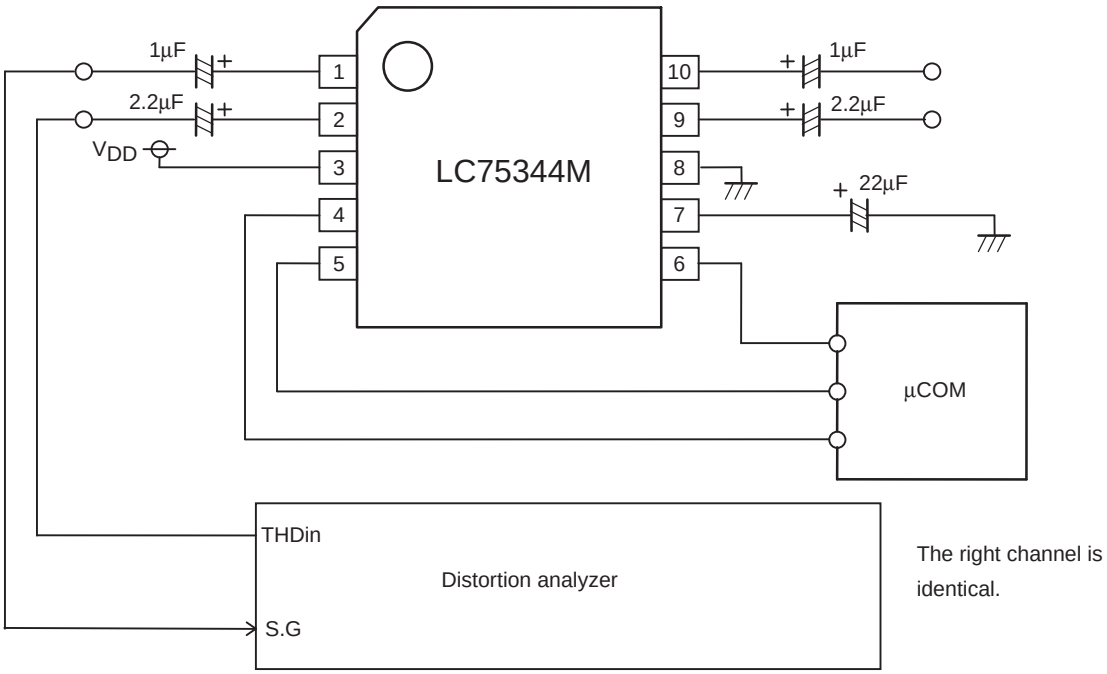
Reference Voltage Generator Equivalent Circuit



The right channel is identical.

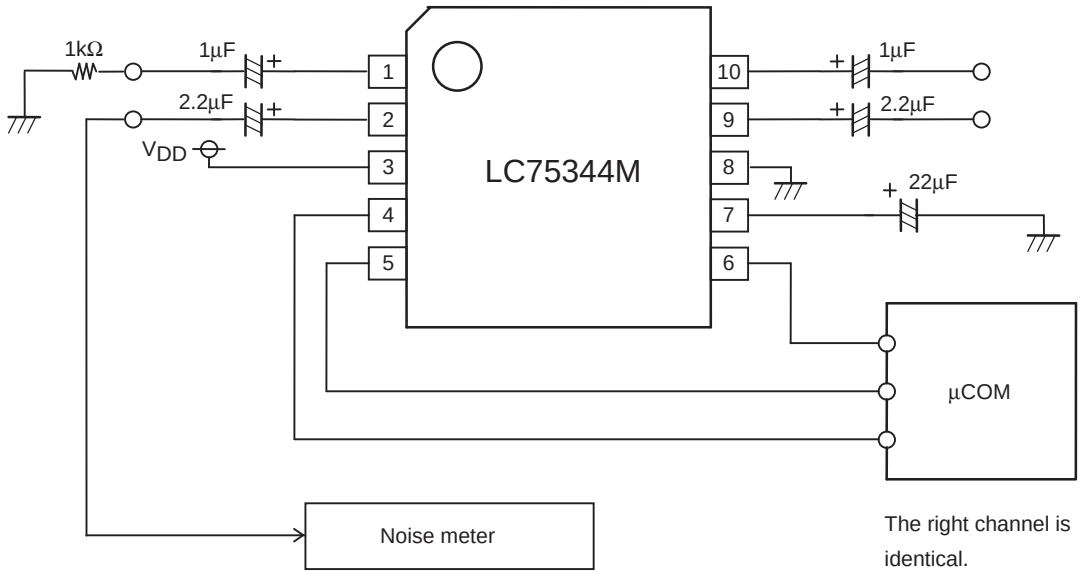
Test Circuits

• Total harmonic distortion

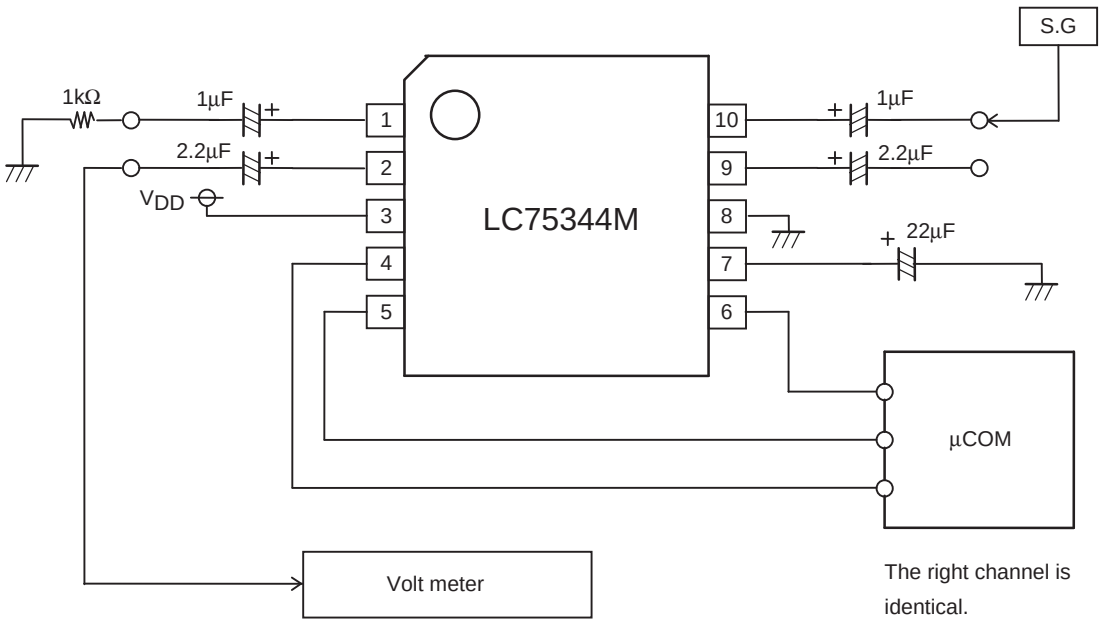


The right channel is identical.

• Output noise voltage



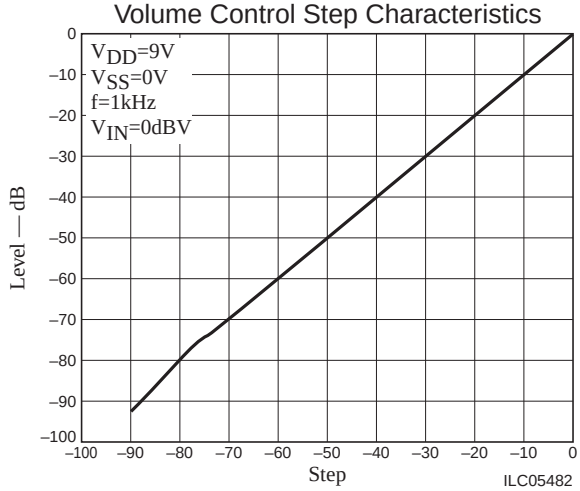
• Crosstalk



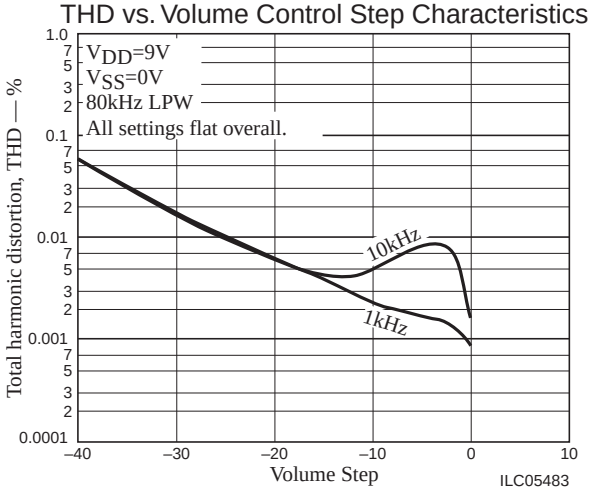
Usage Notes

- The states of the internal analog switches are undefined after power is first applied. Muting must be applied externally until the control data has been sent.
- When performing the initial settings after power is first applied, both the left and right channel initial settings data must be sent before releasing the external mute.
- Either cover the CL, DI, and CE lines with the ground pattern or use shielded lines to prevent high-frequency digital noise from entering the analog signal system from these lines.

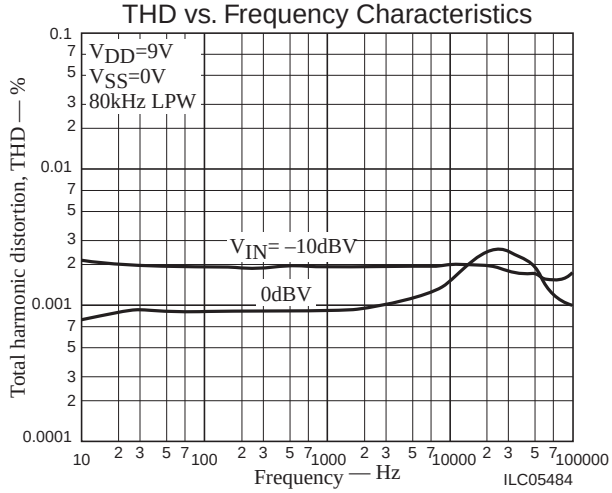
Volume Control Step Characteristics



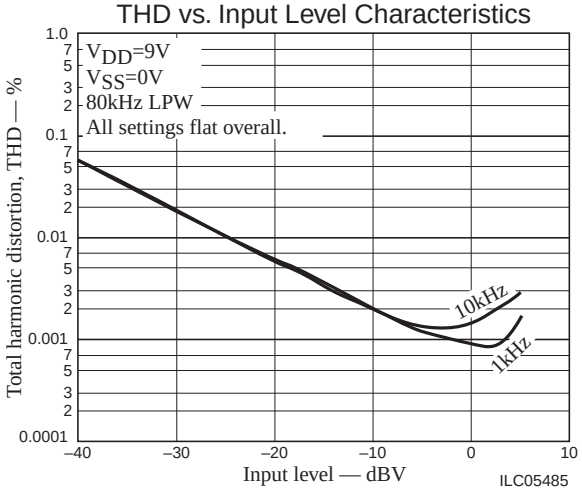
THD vs. Volume Control Step Characteristics



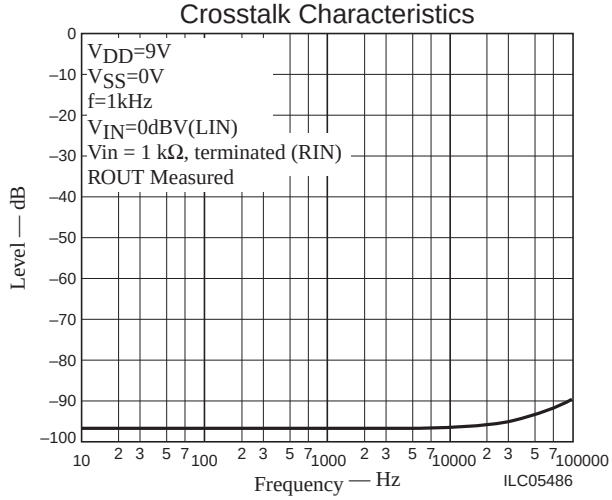
THD vs. Frequency Characteristics



THD vs. Input Level Characteristics



Crosstalk Characteristics



THD vs. Supply Voltage Characteristics