Ordering number : ENN6144A

CMOS IC

LC75817NE, 75817NW

1/8 to 1/10 Duty Dot Matrix LCD Display Controllers/Drivers with Key Input Function

Overview

The LC75817NE and LC75817NW are 1/8 to 1/10 duty dot matrix LCD display controllers/drivers that support the display of characters, numbers, and symbols. In addition to generating dot matrix LCD drive signals based on data transferred serially from a microcontroller, the LC75817NE and LC75817NW also provide on-chip character display ROM and RAM to allow display systems to be implemented easily. These products also provide up to 4 general-purpose output ports and incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

Features

- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- Controls and drives a 5 × 7, 5 × 8, or 5 × 9 dot matrix LCD.
- Supports accessory display segment drive (up to 60 segments)
- Display technique: 1/8 duty 1/4 bias drive (5 × 7 dots)
  1/9 duty 1/4 bias drive (5 × 8 dots)
  1/10 duty 1/4 bias drive (5 × 9 dots)
- Display digits: 12 digits × 1 line (5 × 7 dots, 5 × 8 dots)
  11 digits × 1 line (5 × 9 dots)
- Display control memory
  CGROM: 240 characters (5 × 7, 5 × 8, or 5 × 9 dots)
  CGRAM: 16 characters (5 × 7, 5 × 8, or 5 × 9 dots)
  ADRAM: 12 × 5 bits
  DCRAM: 48 × 8 bits
- Instruction function
  Display on/off control
  Display shift function
- Sleep mode can be used to reduce current drain.
- Built-in display contrast adjustment circuit
- Up to 4 general-purpose output ports are included.
- Serial data I/O supports CCB format communication with the system controller.
- Independent LCD driver block power supply VLCD
- A voltage detection type reset circuit is provided to initialize the IC and prevent incorrect display.
- The $\overline{\text{INH}}$ pin is provided. This pin turns off the display, disables key scanning, and forces the general-purpose output ports to the low level.
- RC oscillator circuit

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

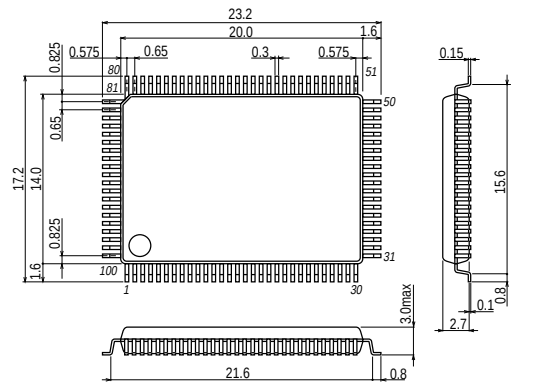
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Package Dimensions

unit: mm

3151-QFP100E

[LC75817NE]

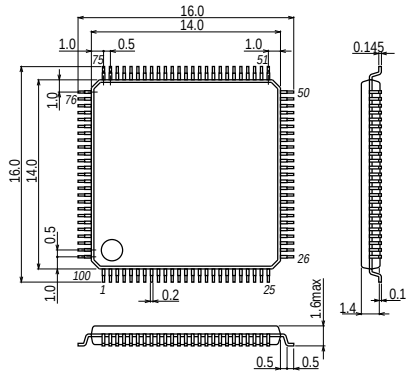


SANYO: QFP100E

unit: mm

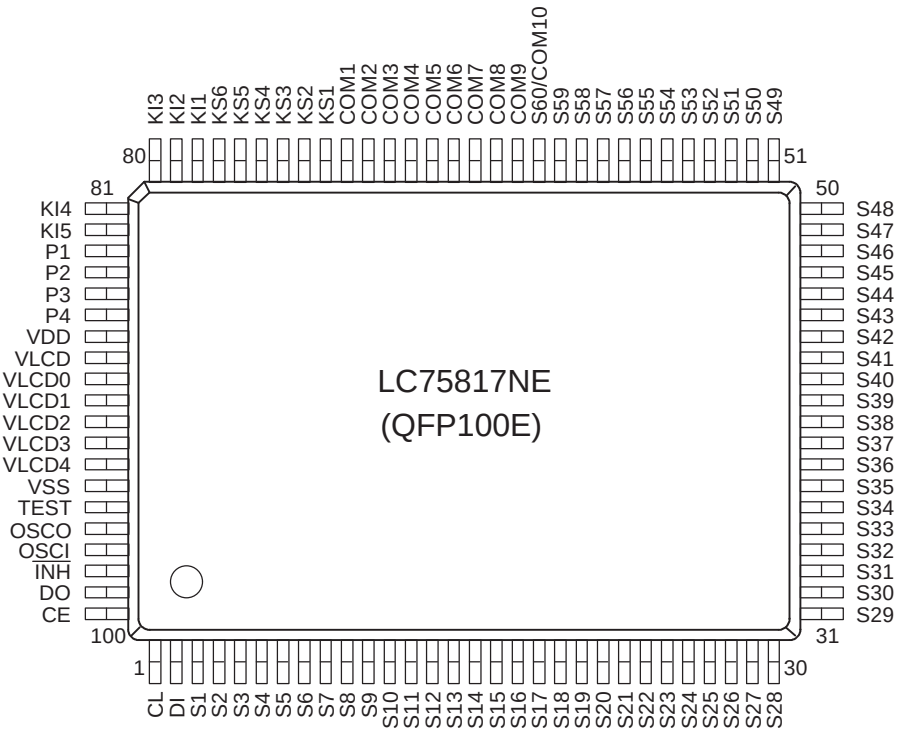
3181B-SQFP100

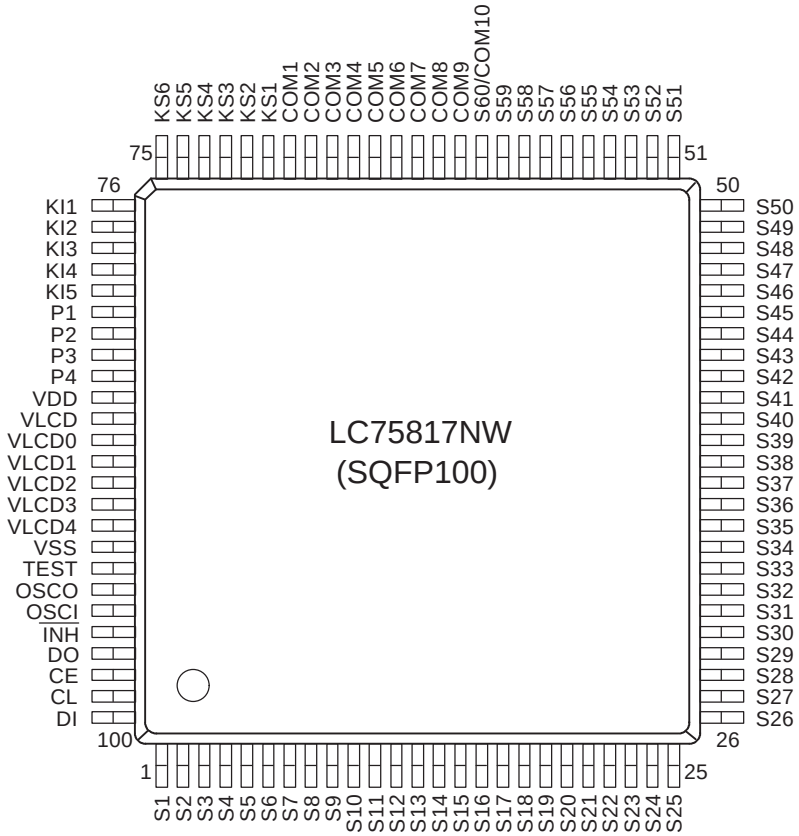
[LC75817NW]



SANYO: SQFP100

Pin Assignments (Top View)





Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	–0.3 to +11.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	–0.3 to +7.0	V
	$V_{IN}2$	OSCI, KI1 to KI5, TEST	–0.3 to V_{DD} + 0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, $V_{LCD}4$	–0.3 to V_{LCD} + 0.3	
Output voltage	$V_{OUT}1$	DO	–0.3 to +7.0	V
	$V_{OUT}2$	OSCO, KS1 to KS6, P1 to P4	–0.3 to V_{DD} + 0.3	
	$V_{OUT}3$	$V_{LCD}0$, S1 to S60, COM1 to COM10	–0.3 to V_{LCD} + 0.3	
Output current	$I_{OUT}1$	S1 to S60	300	µA
	$I_{OUT}2$	COM1 to COM10	3	mA
	$I_{OUT}3$	KS1 to KS6	1	
	$I_{OUT}4$	P1 to P4	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		6.0	V
	V_{LCD}	V_{LCD}: When the display contrast adjustment circuit is used.	7.0		10.0	
		V_{LCD}: When the display contrast adjustment circuit is not used.	4.5		10.0	
Output voltage	$V_{LCD}0$	$V_{LCD}0$	$V_{LCD}4$+4.5		V_{LCD}	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		3/4 ($V_{LCD}0$–$V_{LCD}4$)	$V_{LCD}0$	V
	$V_{LCD}2$	$V_{LCD}2$		2/4 ($V_{LCD}0$–$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}3$	$V_{LCD}3$		1/4 ($V_{LCD}0$–$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}4$	$V_{LCD}4$	0		1.5	
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.8 V_{DD}		6.0	V
	$V_{IH}2$	OSCI	0.7 V_{DD}		V_{DD}	
	$V_{IH}3$	KI1 to KI5	0.6 V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$, KI1 to KI5	0		0.2 V_{DD}	V
	$V_{IL}2$	OSCI	0		0.3 V_{DD}	
Recommended external resistance	R_{OSC}	OSCI, OSCO		33		kΩ
Recommended external capacitance	C_{OSC}	OSCI, OSCO		220		pF
Guaranteed oscillation range	f_{OSC}	OSC	150	300	600	kHz
Data setup time	t_{ds}	CL, DI: Figure 2	160			ns
Data hold time	t_{dh}	CL, DI: Figure 2	160			ns
CE wait time	t_{cp}	CE, CL: Figure 2	160			ns
CE setup time	t_{cs}	CE, CL: Figure 2	160			ns
CE hold time	t_{ch}	CE, CL: Figure 2	160			ns
High level clock pulse width	tøH	CL: Figure 2	160			ns
Low level clock pulse width	tøL	CL: Figure 2	160			ns
DO output delay time	t_{dc}	DO, R_{PU} = 4.7kΩ, C_L = 10pF*1: Figure 2			1.5	µs
DO rise time	t_{dr}	DO, R_{PU} = 4.7kΩ, C_L = 10pF*1: Figure 2			1.5	µs

Note: *1. Since DO is an open-drain output, these times depend on the values of the pull-up resistor R_{PU} and the load capacitance C_L.

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$, KI1 to KI5		0.1 V_{DD}		V
Power-down detection voltage	V_{DET}		2.5	3.0	3.5	V
Input high level current	I_{IH}	CE, CL, DI, $\overline{INH}$, OSCI: V_I = 6.0 V			5.0	µA
Input low level current	I_{IL}	CE, CL, DI, $\overline{INH}$, OSCI: V_I = 0 V	–5.0			µA
Input floating voltage	V_{IF}	KI1 to KI5			0.05 V_{DD}	V
Pull-down resistance	R_{PD}	KI1 to KI5: V_{DD} = 5.0 V	50	100	250	kΩ
Output off leakage current	I_{OFFH}	DO: V_O = 6.0 V			6.0	µA
Output high level voltage	$V_{OH}1$	S1 to S60: I_O = –20 µA	$V_{LCD}0$ – 0.6			V
	$V_{OH}2$	COM1 to COM10: I_O = –100 µA	$V_{LCD}0$ – 0.6			
	$V_{OH}3$	KS1 to KS6: I_O = –500 µA	V_{DD} – 1.0	V_{DD} – 0.5	V_{DD} – 0.2	
	$V_{OH}4$	P1 to P4: I_O = –1 mA	V_{DD} – 1.0			
	$V_{OH}5$	OSCO: I_O = –500 µA	V_{DD} – 1.0			
Output low level voltage	$V_{OL}1$	S1 to S60: I_O = 20 µA			$V_{LCD}4$ + 0.6	V
	$V_{OL}2$	COM1 to COM10: I_O = 100 µA			$V_{LCD}4$ + 0.6	
	$V_{OL}3$	KS1 to KS6: I_O = 25 µA	0.2	0.5	1.5	
	$V_{OL}4$	P1 to P4: I_O = 1 mA			1.0	
	$V_{OL}5$	OSCO: I_O = 500 µA			1.0	
	$V_{OL}6$	DO: I_O = 1 mA		0.1	0.5	
Output middle level voltage*2	$V_{MID}1$	S1 to S60: I_O = ±20 µA	$2/4\,(V_{LCD}0 - V_{LCD}4) - 0.6$		$2/4\,(V_{LCD}0 - V_{LCD}4) + 0.6$	V
	$V_{MID}2$	COM1 to COM10: I_O = ±100 µA	$3/4\,(V_{LCD}0 - V_{LCD}4) - 0.6$		$3/4\,(V_{LCD}0 - V_{LCD}4) + 0.6$	
	$V_{MID}3$	COM1 to COM10: I_O = ±100 µA	$1/4\,(V_{LCD}0 - V_{LCD}4) - 0.6$		$1/4\,(V_{LCD}0 - V_{LCD}4) + 0.6$	
Oscillator frequency	f_{OSC}	OSCI, OSCO: R_{OSC} = 33 kΩ, C_{OSC} = 220 pF	210	300	390	kHz
Current drain	$I_{DD}1$	V_{DD}: sleep mode			100	µA
	$I_{DD}2$	V_{DD}: V_{DD} = 6.0 V, output open, f_{OSC} = 300 kHz		500	1000	
	$I_{LCD}1$	V_{LCD}: sleep mode			5	
	$I_{LCD}2$	V_{LCD}: V_{LCD} = 10.0 V, output open, f_{OSC} = 300 kHz When the display contrast adjustment circuit is used.		450	900	
	$I_{LCD}3$	V_{LCD}: V_{LCD} = 10.0 V, output open, f_{OSC} = 300 kHz When the display contrast adjustment circuit is not used.		200	400	

Note: *2. Excluding the bias voltage generation divider resistor built into the $V_{LCD}0$, $V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, and $V_{LCD}4$. (See Figure 1.)

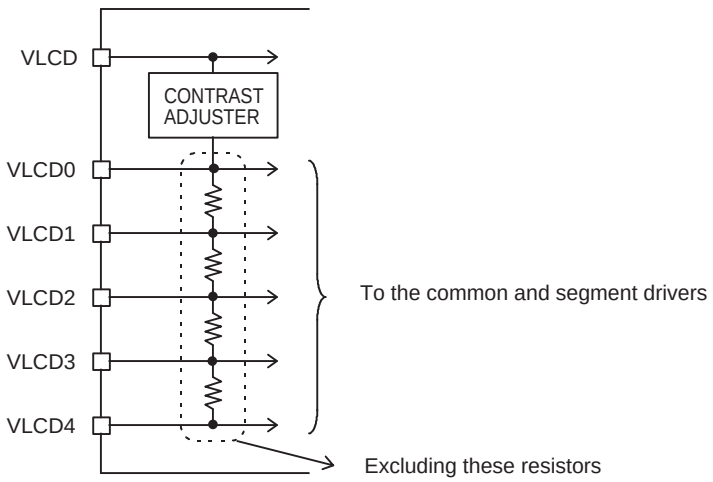
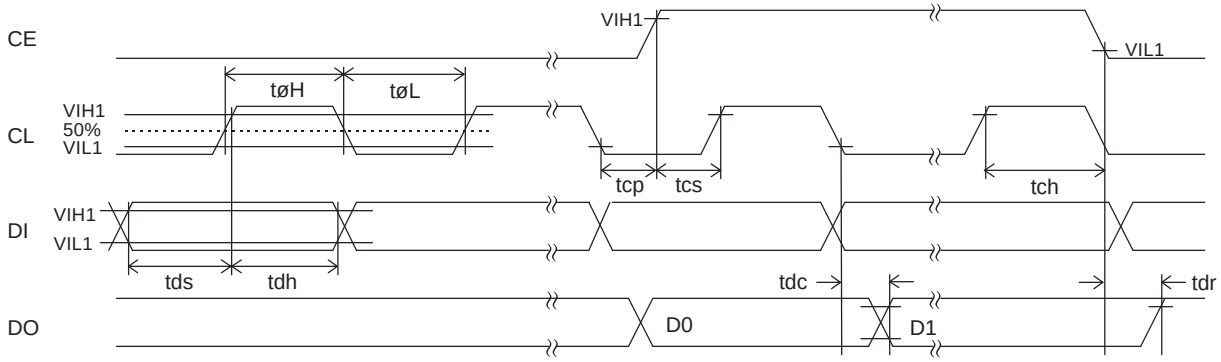


Figure 1

• When CL is stopped at the low level



• When CL is stopped at the high level

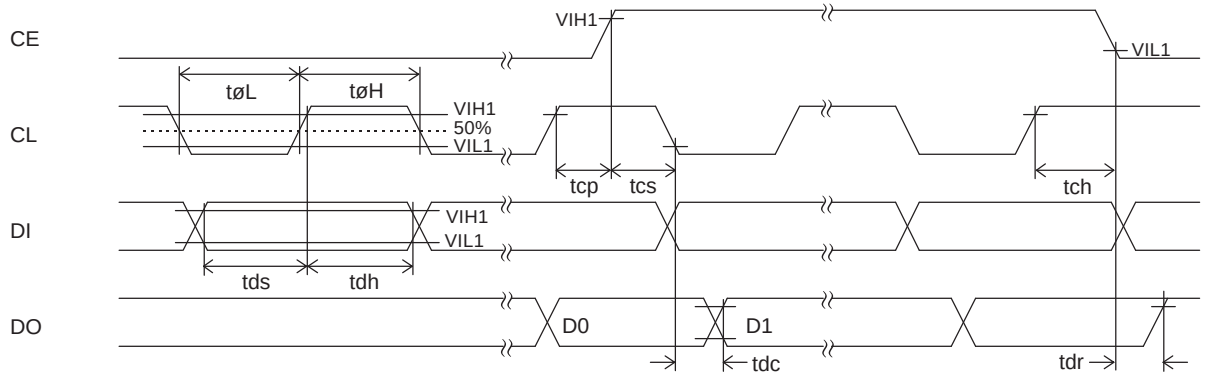
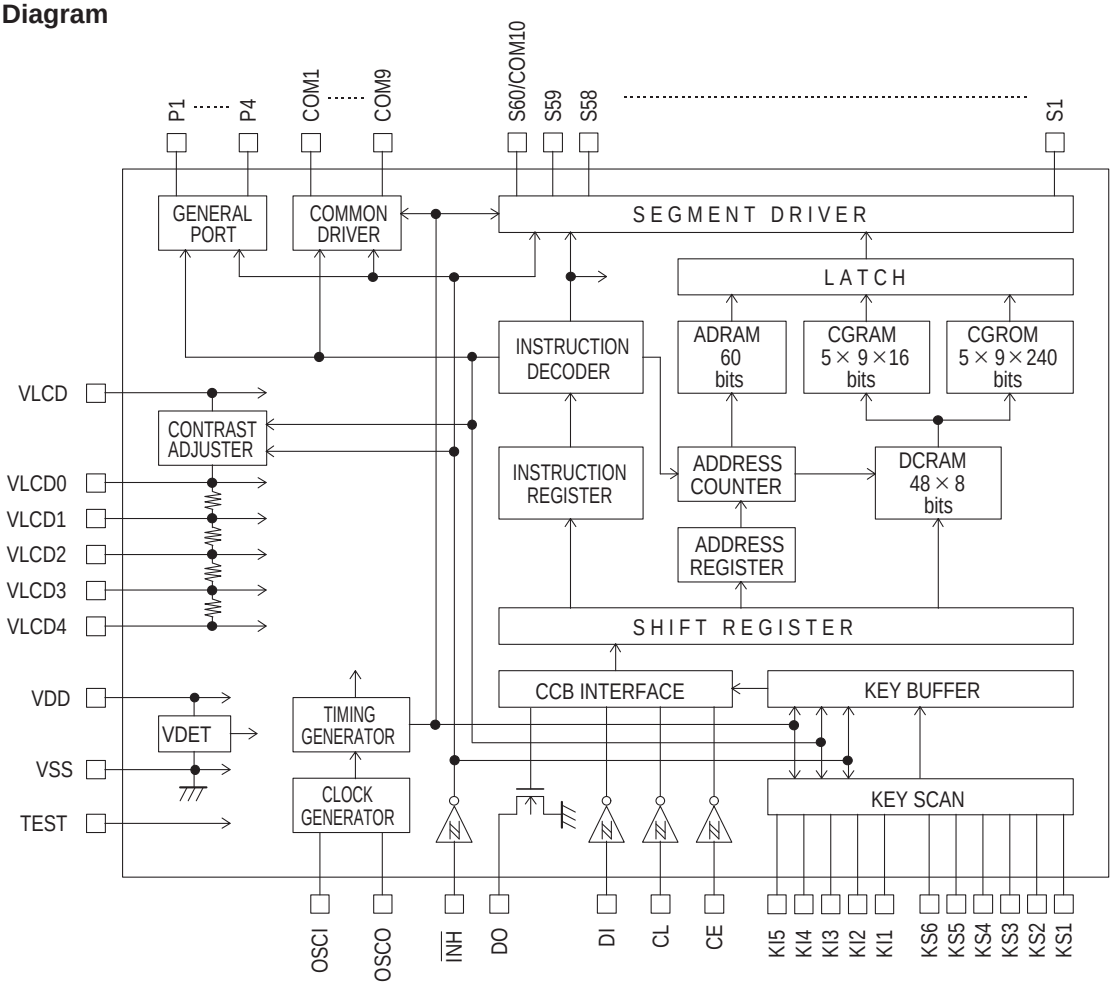


Figure 2

Block Diagram



Pin Functions

Pin	Pin No.		Function	Active	I/O	Handling when unused
	LC75817NE	LC75817NW				
S1 to S59 S60/COM10	3 to 61 62	1 to 59 60	Segment driver outputs. The S60/COM10 pin can be used as common driver output under the “set display technique” instruction.	—	O	OPEN
COM1 to COM9	71 to 63	69 to 61	Common driver outputs.	—	O	OPEN
KS1 to KS6	72 to 77	70 to 75	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix.	—	O	OPEN
KI1 to KI5	78 to 82	76 to 80	Key scan inputs. These pins have built-in pull-down resistors.	H	I	GND
P1 to P4	83 to 86	81 to 84	General-purpose output ports	—	O	OPEN
OSCI	97	95	Oscillator connections. An oscillator circuit is formed by connecting an external resistor and capacitor at these pins.	—	I	GND
OSCO	96	94		—	O	OPEN
CE	100	98	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE : Chip enable CL : Synchronization clock DI : Transfer data DO : Output data	H	I	GND
CL	1	99		↑	I	
DI	2	100		—	I	
DO	99	97		—	O	OPEN
$\overline{INH}$	98	96	Input that turns the display off, disables key scanning, and forces the general-purpose output ports low. • When $\overline{INH}$ is low (V_{SS}): • Display off S1 to S59 = “L” ($V_{LCD}4$). S60/COM10 = “L” ($V_{LCD}4$). COM1 to COM9 = “L” ($V_{LCD}4$). • General-purpose output ports P1 to P4 = low (V_{SS}) • Key scanning disabled: KS1 to KS6 = low (V_{SS}) • All the key data is reset to low. • When $\overline{INH}$ is high (V_{DD}): • Display on • The state of the general-purpose output ports can be set by executing a "Set general-purpose output port state" instruction. • Key scanning is enabled. However, serial data can be transferred when the $\overline{INH}$ pin is low.	L	I	V_{DD}
TEST	95	93	This pin must be connected to ground.	—	I	—
$V_{LCD}0$	89	87	LCD drive 4/4 bias voltage (high level) supply pin. The level on this pin can be changed by the display contrast adjustment circuit. However, ($V_{LCD}0$ – $V_{LCD}4$) must be greater than or equal to 4.5 V. Also, external power must not be applied to this pin since the pin circuit includes the display contrast adjustment circuit.	—	O	OPEN
$V_{LCD}1$	90	88	LCD drive 3/4 bias voltage (middle level) supply pin. This pin can be used to supply the 3/4 ($V_{LCD}0$ – $V_{LCD}4$) voltage level externally.	—	I	OPEN
$V_{LCD}2$	91	89	LCD drive 2/4 bias voltage (middle level) supply pin. This pin can be used to supply the 2/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	—	I	OPEN
$V_{LCD}3$	92	90	LCD drive 1/4 bias voltage (middle level) supply pin. This pin can be used to supply the 1/4 ($V_{LCD}0$ – $V_{LCD}4$) voltage level externally.	—	I	OPEN
$V_{LCD}4$	93	91	LCD drive 0/4 bias voltage (low level) supply pin. Fine adjustment of the display contrast can be implemented by connecting an external variable resistor to this pin. However, ($V_{LCD}0$ – $V_{LCD}4$) must be greater than or equal to 4.5 V, and VLCD4 must be in the range 0 V to 1.5 V, inclusive.	—	I	GND
V_{DD}	87	85	Logic block power supply connection. Provide a voltage of between 4.5 and 6.0 V.	—	—	—
V_{LCD}	88	86	LCD driver block power supply connection. Provide a voltage of between 7.0 and 10.0 V when the display contrast adjustment circuit is used and provide a voltage of between 4.5 and 10.0 V when the circuit is not used.	—	—	—
V_{SS}	94	92	Power supply connection. Connect to ground.	—	—	—

Block Functions

- AC (address counter)
  AC is a counter that provides the addresses used for DCRAM and ADRAM.
  The address is automatically modified internally, and the LCD display state is retained.
- DCRAM (data control RAM)
  DCRAM is RAM that is used to store display data expressed as 8-bit character codes. (These character codes are converted to 5×7, 5×8, or 5×9 dot matrix character patterns using CGROM or CGRAM.) DCRAM has a capacity of 48×8 bits, and can hold 48 characters. The table below lists the correspondence between the 6-bit DCRAM address loaded into AC and the display position on the LCD panel.

・When the DCRAM address loaded into AC is 00_H.

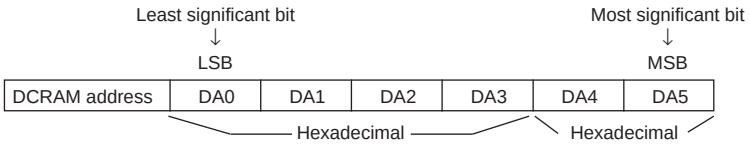
Display digit	1	2	3	4	5	6	7	8	9	10	11	12
DCRAM address (hexadecimal)	00	01	02	03	04	05	06	07	08	09	0A	0B

However, when the display shift is performed by specifying MDATA, the DCRAM address shifts as shown below.

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	
DCRAM address (hexadecimal)	01	02	03	04	05	06	07	08	09	0A	0B	0C	(Shift left)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	
DCRAM address (hexadecimal)	2F	00	01	02	03	04	05	06	07	08	09	0A	(Shift right)

Note: *3. The DCRAM address is expressed in hexadecimal.



Example: When the DCRAM address is $2E_H$.

DA0	DA1	DA2	DA3	DA4	DA5
0	1	1	1	0	1

Note: *4. 5×7 dots ... 12-digit display 5×7 dots
5×8 dots ... 12-digit display 5×8 dots
5×9 dots ... 12-digit display 4×9 dots

• ADRAM (Additional data RAM)
ADRAM is RAM that is used to store the ADATA display data. ADRAM has a capacity of 12 × 5 bits, and the stored display data is displayed directly without the use of CGROM or CGRAM. The table below lists the correspondence between the 4-bit ADRAM address loaded into AC and the display position on the LCD panel.

・When the ADRAM address loaded into AC is 0_H. (Number of digit displayed: 12)

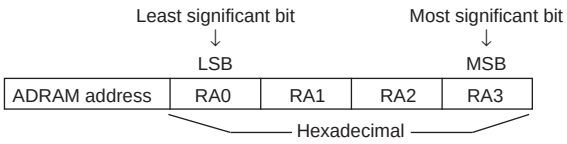
Display digit	1	2	3	4	5	6	7	8	9	10	11	12
ADRAM address (hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B

However, when the display shift is performed by specifying ADATA, the ADRAM address shifts as shown below.

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	
ADRAM address (hexadecimal)	1	2	3	4	5	6	7	8	9	A	B	0	(Shift left)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	
ADRAM address (hexadecimal)	B	0	1	2	3	4	5	6	7	8	9	A	(Shift right)

Note: *5. The ADRAM address is expressed in hexadecimal.



Example: When the ADRAM address is A_H

RA0	RA1	RA2	RA3
0	1	0	1

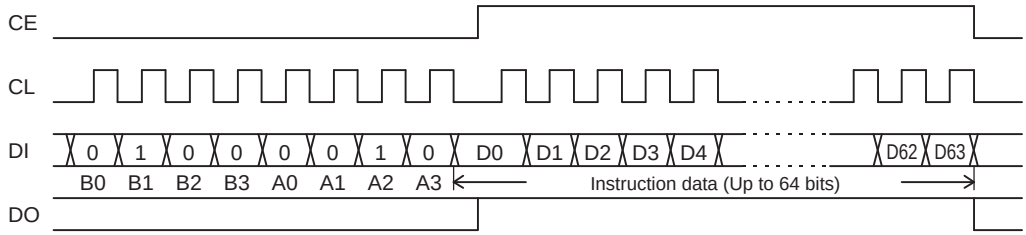
Note: *6. 5 × 7 dots ... 12-digit display 5 dots
5 × 8 dots ... 12-digit display 5 dots
5 × 9 dots ... 12-digit display 4 dots

• CGROM (Character generator ROM)
CGROM is ROM that is used to generate the 240 kinds of 5 × 7, 5 × 8, or 5 × 9 dot matrix character patterns from the 8-bit character codes. CGROM has a capacity of 240 × 45 bits. When a character code is written to DCRAM, the character pattern stored in CGROM corresponding to the character code is displayed at the position on the LCD corresponding to the DCRAM address loaded into AC.

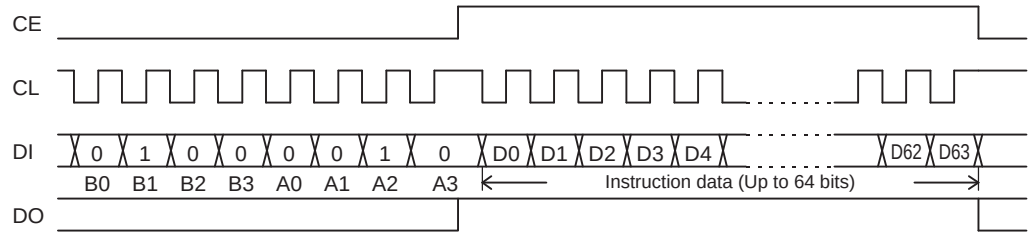
• CGRAM (Character generator RAM)
CGRAM is RAM to which user programs can freely write arbitrary character patterns. Up to 16 kinds of 5 × 7, 5 × 8, or 5 × 9 dot matrix character patterns can be stored. CGRAM has a capacity of 16 × 45 bits.

Serial Data Input

• When CL is stopped at the low level



• When CL is stopped at the high level



・B0 to B3, A0 to A3: CCB address 42H
・D0 to D63: Instruction data

The data is acquired on the rising edge of the CL signal and latched on the falling edge of the CE signal. When transferring instruction data from the microcontroller, applications must assure that the time from the transfer of one set of instruction data until the next instruction data transfer is significantly longer than the instruction execution time.

Instruction Table

| Instruction | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 | D17 | D18 | D19 | D20 | D21 | D22 | D23 | D24 | D25 | D26 | D27 | D28 | D29 | D30 | D31 | D32 | D33 | D34 | D35 | D36 | D37 | D38 | D39 | D40 | D41 | D42 | D43 | D44 | D45 | D46 | D47 | D48 | D49 | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D58 | D59 | D60 | D61 | D62 | D63 | Execution time *9 |
|---|---|---

Detailed Instruction Descriptions

• Set display technique ... <Sets the display technique>

Code							
D56	D57	D58	D59	D60	D61	D62	D63
DT1	DT2	X	X	0	0	0	1

X: don't care

DT1, DT2: Sets the display technique

DT1	DT2	Display technique	Output pins	
			COM9	S60/COM10
0	0	1/8 duty, 1/4 bias drive	Fixed at the $V_{LCD}4$ level	S60
1	0	1/9 duty, 1/4 bias drive	COM9	S60
0	1	1/10 duty, 1/4 bias drive	COM9	COM10

Note: *11 S60: Segment outputs
COMn (n = 9, 10): Common outputs

• Display on/off control ... <Turns the display on or off>

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	X	X	X	X	M	A	SC	SP	0	0	1	0

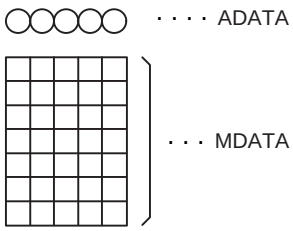
X: don't care

M, A: Specifies the data to be turned on or off

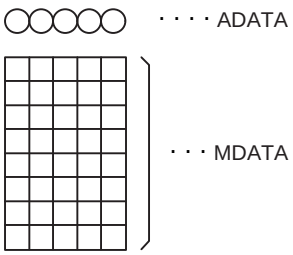
M	A	Display operating state
0	0	Both MDATA and ADATA are turned off (The display is forcibly turned off regardless of the DG1 to DG12 data.)
0	1	Only ADATA is turned on (The ADATA of display digits specified by the DG1 to DG12 data are turned on.)
1	0	Only MDATA is turned on (The MDATA of display digits specified by the DG1 to DG12 data are turned on.)
1	1	Both MDATA and ADATA are turned on (The MDATA and ADATA of display digits specified by the DG1 to DG12 data are turned on.)

Note: *12. MDATA, ADATA

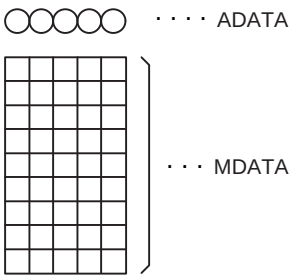
5 × 7 dot matrix display



5 × 8 dot matrix display



5 × 9 dot matrix display



DG1 to DG12: Specifies the display digit

Display digit	1	2	3	4	5	6	7	8	9	10	11	12
Display digit data	DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12

For example, if DG1 to DG6 are 1, and DG7 to DG12 are 0, then display digits 1 to 6 will be turned on, and display digits 7 to 12 will be turned off (blanked).

SC: Controls the common and segment output pins

SC	Common and segment output pin states
0	Output of LCD drive waveforms
1	Fixed at the $V_{LCD}4$ level (all segments off)

Note: *13. When SC is 1, the S1 to S60 and COM1 to COM10 output pins are set to the $V_{LCD}4$ level, regardless of the M, A, and DG1 to DG12 data.

SP: Controls the normal mode and sleep mode

SP	Mode
0	Normal mode
1	Sleep mode The common and segment pins go to the $V_{LCD}4$ level and the oscillator on the OSCI, OSCO pins is stopped (although it operates during key scan operations) to reduce current drain. Although the “display on/off control”, “set display contrast”, “set key scan output state”, and “set general-purpose output port state” instructions can be executed in this mode, applications must return the IC to normal mode to execute any of the other instruction settings.

• Display shift ... <Shifts the display>

Code							
D56	D57	D58	D59	D60	D61	D62	D63
M	A	R/L	X	0	0	1	1

X: don’t care

M, A: Specifies the data to be shifted

M	A	Shift operating state
0	0	Neither MDATA nor ADATA is shifted
0	1	Only ADATA is shifted
1	0	Only MDATA is shifted
1	1	Both MDATA and ADATA are shifted

R/L: Specifies the shift direction

R/L	Shift direction
0	Shift left
1	Shift right

• Set AC address... <Specifies the DCRAM and ADRAM address for AC>

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
DA0	DA1	DA2	DA3	DA4	DA5	X	X	RA0	RA1	RA2	RA3	0	1	0	0

X: don’t care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5
LSB					MSB
↑					↑
Least significant bit					Most significant bit

RA0 to RA3: ADRAM address

RA0	RA1	RA2	RA3
LSB			MSB
↑			↑
Least significant bit			Most significant bit

This instruction loads the 6-bit DCRAM address DA0 to DA5 and the 4-bit ADRAM address RA0 to RA3 into the AC.

• DCRAM data write ... <Specifies the DCRAM address and stores data at that address>

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM	X	X	X	0	1	0	1

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5

LSB ↑ Least significant bit

MSB ↑ Most significant bit

AC0 to AC7: DCRAM data (character code)

AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

LSB ↑ Least significant bit

MSB ↑ Most significant bit

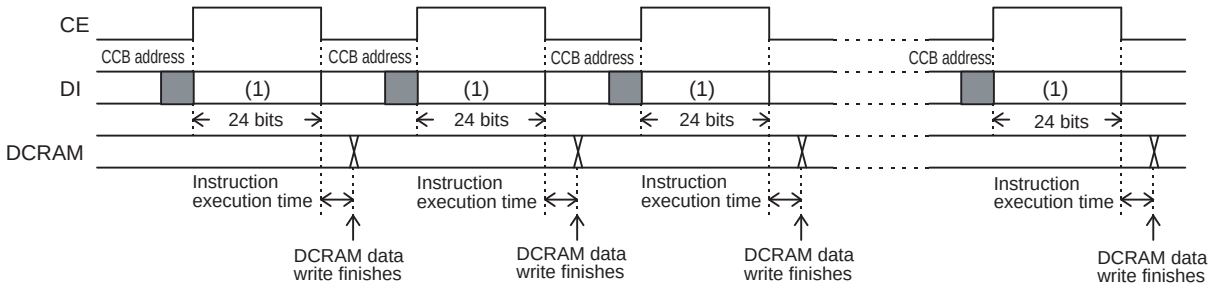
This instruction writes the 8 bits of data AC0 to AC7 to DCRAM. This data is a character code, and is converted to a 5×7, 5×8, or 5×9 dot matrix display data using CGROM or CGRAM.

IM: Sets the method of writing data to DCRAM

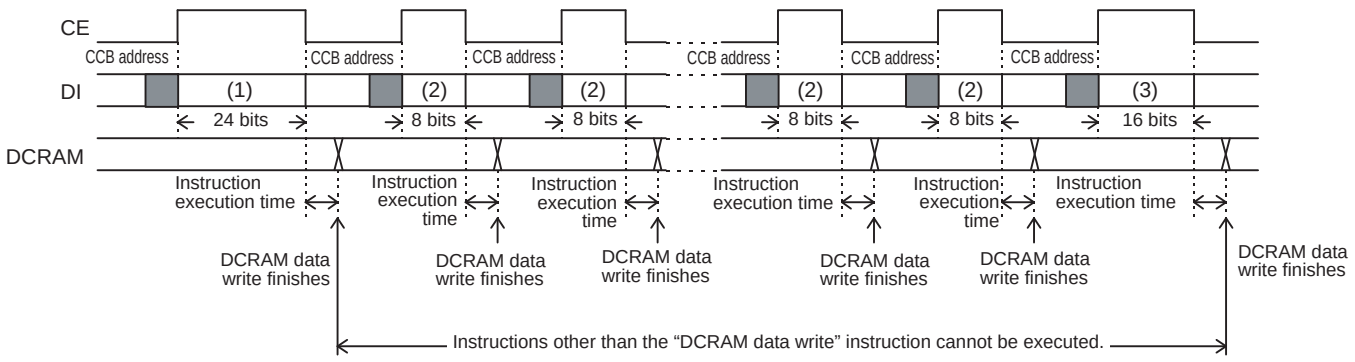
IM	DCRAM data write method
0	Normal DCRAM data write (Specifies the DCRAM address and writes the DCRAM data.)
1	Increment mode DCRAM data write (Increments the DCRAM address by +1 each time data is written to DCRAM.)

Notes: *14.

· DCRAM data write method when IM = 0



· DCRAM data write method when IM = 1 (Instructions other than the "DCRAM data write" instruction cannot be executed.)



Data format at (1) (24 bits)

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM	X	X	X	0	1	0	1

X: don't care

Data format at (2) (8 bits)

Code							
D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

Data format at (3) (16 bits)

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	0	X	X	X	0	1	0	1

X: don't care

• ADRAM data write ... <Specifies the ADRAM address and stores data at that address>

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	IM	X	X	X	0	1	1	0

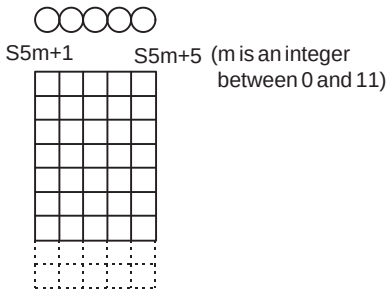
X: don't care

RA0 to RA3: ADRAM address

RA0	RA1	RA2	RA3
LSB			MSB
Least significant bit			Most significant bit

AD1 to AD5: ADATA display data

In addition to the 5 × 7, 5 × 8, or 5 × 9 dot matrix display data (MDATA), this IC supports direct display of the five accessory display segments provided in each digit as ADATA. This display function does not use CGROM or CGRAM. The figure below shows the correspondence between the data and the display. When ADn = 1 (where n is an integer between 1 and 5) the segment corresponding to that data will be turned on.



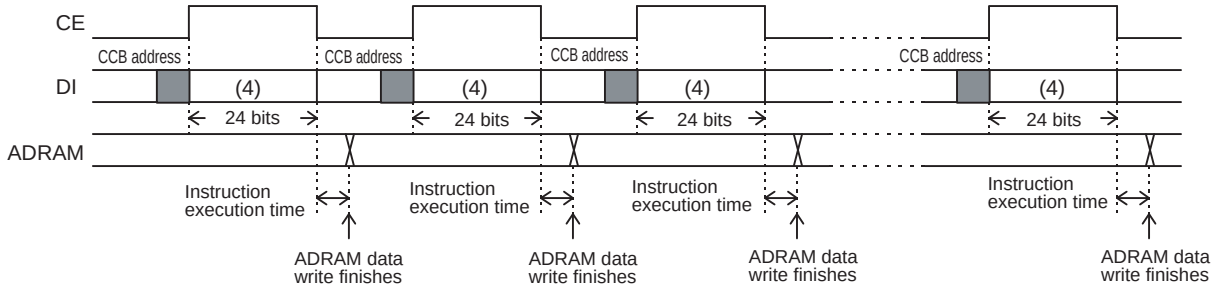
ADATA	Corresponding output pin
AD1	S5m + 1 (m is an integer between 0 and 11)
AD2	S5m + 2
AD3	S5m + 3
AD4	S5m + 4
AD5	S5m + 5

IM: Sets the method of writing data to ADRAM

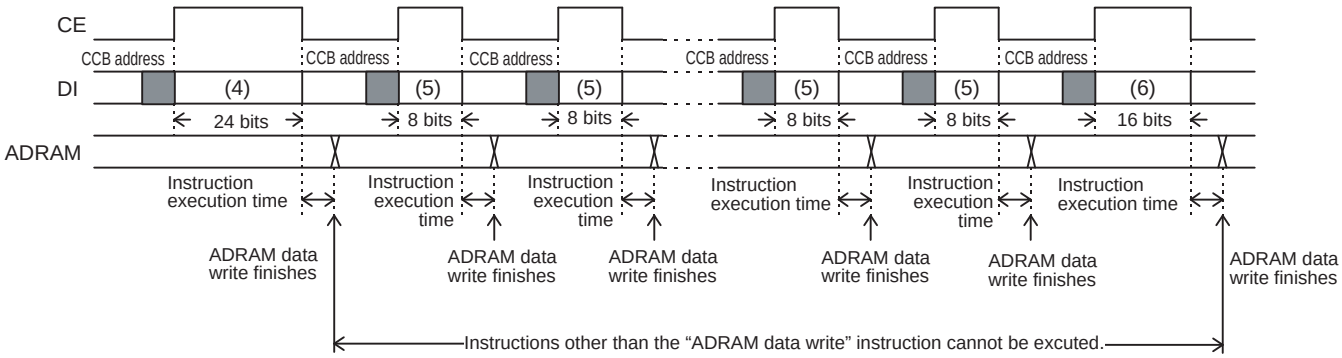
IM	ADRAM data write method
0	Normal ADRAM data write (Specifies the ADRAM address and writes the ADRAM data.)
1	Increment mode ADRAM data write (Increments the ADRAM address by +1 each time data is written to ADRAM.)

Notes: *15.

· ADRAM data write method when IM = 0



· ADRAM data write method when IM = 1 (Instructions other than the “ADRAM data write” instruction cannot be excuted.)



Data format at (4) (24 bits)

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	IM	X	X	X	0	1	1	0

X: don’t care

Data format at (5) (8 bits)

Code							
D56	D57	D58	D59	D60	D61	D62	D63
AD1	AD2	AD3	AD4	AD5	X	X	X

X: don’t care

Data format at (6) (16 bits)

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AD1	AD2	AD3	AD4	AD5	X	X	X	0	X	X	X	0	1	1	0

X: don’t care

• CGRAM data write ... <Specifies the CGRAM address and stores data at that address>

Code															
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
CD1	CD2	CD3	CD4	CD5	CD6	CD7	CD8	CD9	CD10	CD11	CD12	CD13	CD14	CD15	CD16

Code															
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
CD17	CD18	CD19	CD20	CD21	CD22	CD23	CD24	CD25	CD26	CD27	CD28	CD29	CD30	CD31	CD32

Code															
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
CD33	CD34	CD35	CD36	CD37	CD38	CD39	CD40	CD41	CD42	CD43	CD44	CD45	X	X	X

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	X	X	X	X	0	1	1	1

X: don't care

CA0 to CA7: CGRAM address

CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7
LSB ↑ Least significant bit							MSB ↑ Most significant bit

CD1 to CD45: CGRAM data (5×7, 5×8, or 5×9 dot matrix display data)
The bit CDn (where n is an integer between 1 and 45) corresponds to the 5×7, 5×8, or 5×9 dot matrix display data. The figure below shows that correspondence. When CDn is 1 the dots which correspond to that data will be turned on.

CD1	CD2	CD3	CD4	CD5
CD6	CD7	CD8	CD9	CD10
CD11	CD12	CD13	CD14	CD15
CD16	CD17	CD18	CD19	CD20
CD21	CD22	CD23	CD24	CD25
CD26	CD27	CD28	CD29	CD30
CD31	CD32	CD33	CD34	CD35
CD36	CD37	CD38	CD39	CD40
CD41	CD42	CD43	CD44	CD45

Note: *16. CD1 to CD35: 5×7 dot matrix display data
CD1 to CD40: 5×8 dot matrix display data
CD1 to CD45: 5×9 dot matrix display data

• Set display contrast ... <Sets the display contrast>

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
CT0	CT1	CT2	CT3	X	X	X	X	CTC	X	X	X	1	0	0	0

X: don't care

CT0 to CT3: Sets the display contrast (11 steps)

CT0	CT1	CT2	CT3	LCD drive 4/4 bias voltage supply $V_{LCD}0$ level
0	0	0	0	0.94 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 2)
1	0	0	0	0.91 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 3)
0	1	0	0	0.88 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 4)
1	1	0	0	0.85 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 5)
0	0	1	0	0.82 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 6)
1	0	1	0	0.79 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 7)
0	1	1	0	0.76 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 8)
1	1	1	0	0.73 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 9)
0	0	0	1	0.70 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 10)
1	0	0	1	0.67 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 11)
0	1	0	1	0.64 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 12)

CTC: Sets the display contrast adjustment circuit state

CTC	Display contrast adjustment circuit state
0	The display contrast adjustment circuit is disabled, and the $V_{LCD}0$ pin level is forced to the V_{LCD} level.
1	The display contrast adjustment circuit operates, and the display contrast is adjusted.

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it is also possible to apply fine adjustments to the contrast by connecting an external variable resistor to the $V_{LCD}4$ pin and modifying the $V_{LCD}4$ pin voltage. However, the following conditions must be met: ($V_{LCD}0 - V_{LCD}4$) ≥ 4.5 V, and 1.5 V ≥ $V_{LCD}4$ ≥ 0 V.

• Set key scan output state ... <Sets the key scan output pin states>

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
KC1	KC2	KC3	KC4	KC5	KC6	X	X	X	X	X	X	1	0	0	1

X: don't care

KC1 to KC6: Sets the key scan output pin KS1 to KS6 state

Output pin	KS1	KS2	KS3	KS4	KS5	KS6
Key scan output state setting data	KC1	KC2	KC3	KC4	KC5	KC6

For example, if KC1 to KC3 are set to 1, and KC4 to KC6 are set to 0, then the output pins KS1 to KS3 will output high levels (V_{DD}) and the output pins KS4 to KS6 will output low levels (V_{SS}) in the key scan standby state.
Note that key scan output signals are not output from output pins that are set low.

• Set general-purpose output port state ... <Sets the states of the general-purpose output ports>

Code							
D56	D57	D58	D59	D60	D61	D62	D63
PC1	PC2	PC3	PC4	1	0	1	0

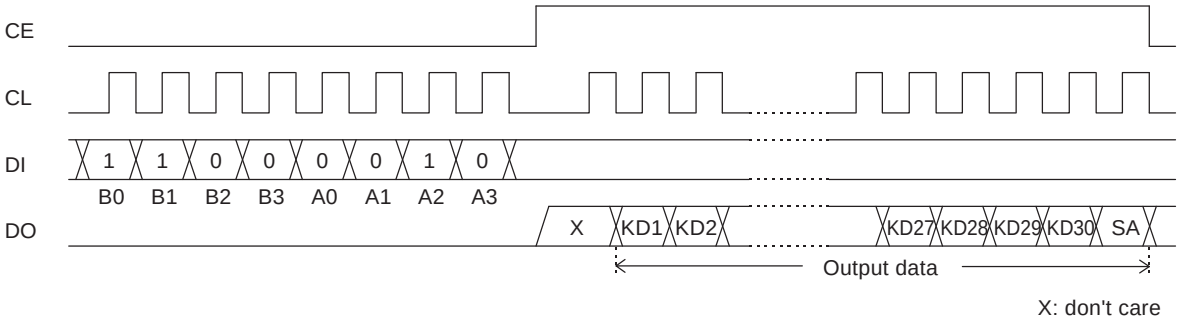
PC1 to PC4: Sets the general-purpose output port P1 to P4 state

Output pin	P1	P2	P3	P4
General-purpose output port state setting data	PC1	PC2	PC3	PC4

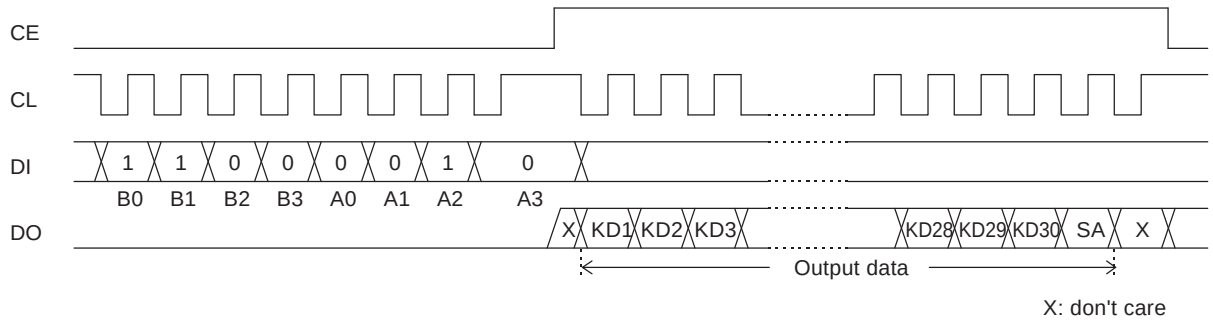
For example, if PC1 and PC2 are set to 1 and PC3 and PC4 are set to 0, then the output pins P1 and P2 will output high levels (V_{DD}) and the output pins P3 and P4 will output low levels (V_{SS}).

Serial Data Output

• When CL is stopped at the low level



• When CL is stopped at the high level



・ B0 to B3, A0 to A3 : CCB address 43H
・ KD1 to KD30 : Key data
・ SA : Sleep acknowledge data

Note: *17. If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data(SA) will be invalid.

Output Data

- KD1 to KD30 : Key data

  When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

	KI1	KI2	KI3	KI4	KI5
KS1	KD1	KD2	KD3	KD4	KD5
KS2	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

  When the states of the KS1 to KS6 output pins during key scan standby are set to low for KS1 and KS2 and to high for KS3 to KS6 with the “set key scan output state” instruction and a key matrix of up to 20 keys is formed from the KS3 to KS6 output pins and the KI1 to KI5 input pins, the KD1 to KD10 key data bits will be set to 0.

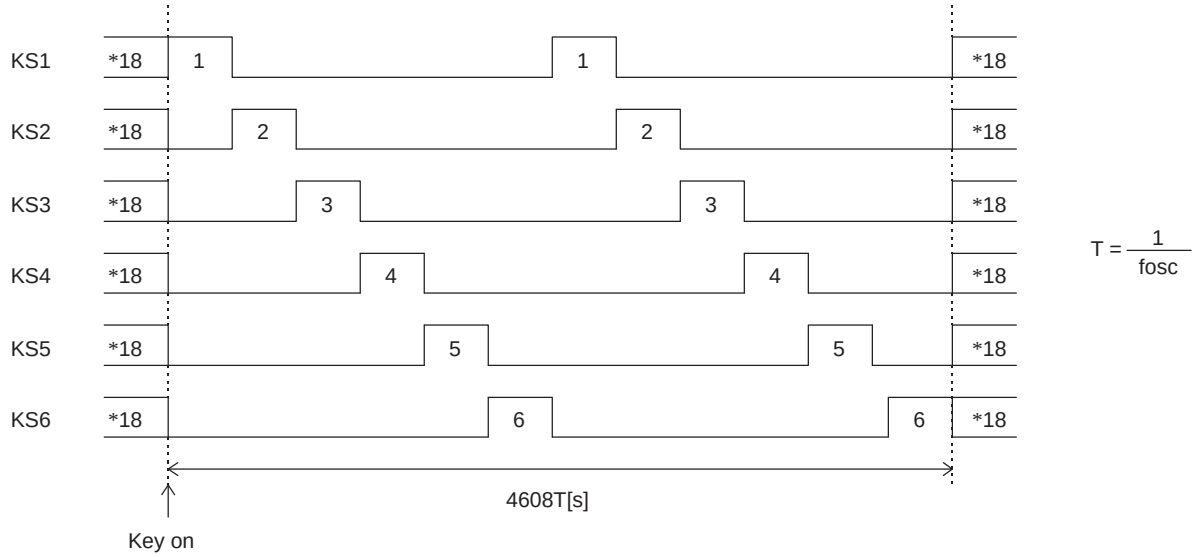
- SA : Sleep acknowledge data

  This output data bit is set to the state when the key was pressed. Also, while DO will be low in this case, if serial data is input and the mode is set (to normal or sleep mode) during this period, that mode will be set. SA will be 1 in sleep mode and 0 in normal mode.

Key Scan Operation Functions

• Key scan timing

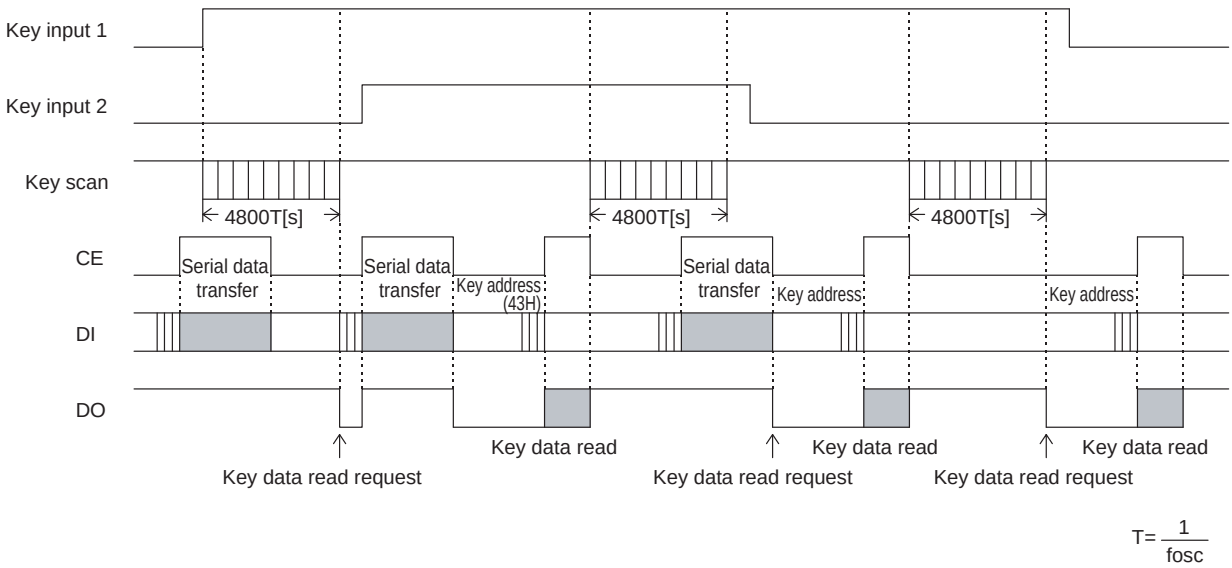
The key scan period is 2304T(s). To reliably determine the on/off state of the keys, the LC75817NE/NW scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 4800T(s) after starting a key scan. If the key data dose not agree and a key was pressed at that point, it scans the keys again. Thus the LC75817NE/NW cannot detect a key press shorter than 4800T(s).



Note: *18. Note that the high/low states of these pins are determined by the "set key scan output state" instruction, and that key scan output signals are not output from pins that are set to low.

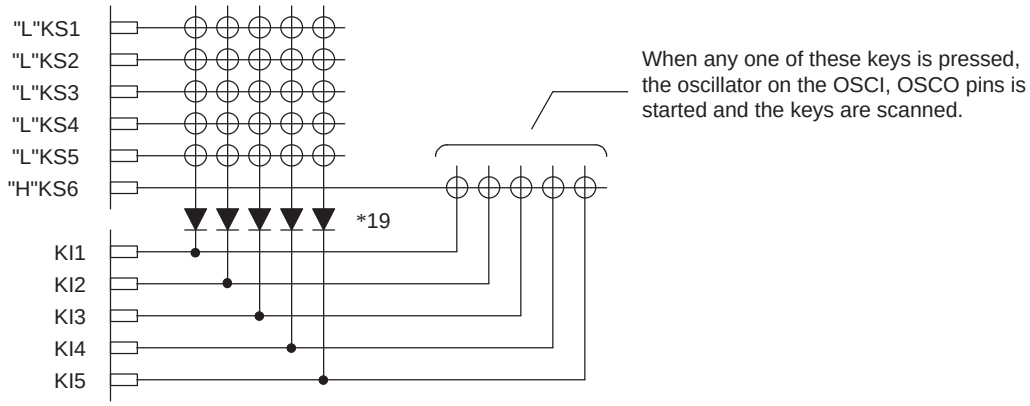
• In normal mode

- The pins KS1 to KS6 are set to high or low with the "set key scan output state" instruction.
- If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 4800T(s) (Where T= $\frac{1}{fosc}$) the LC75817NE/NW outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75817NE/NW performs another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10 kΩ).

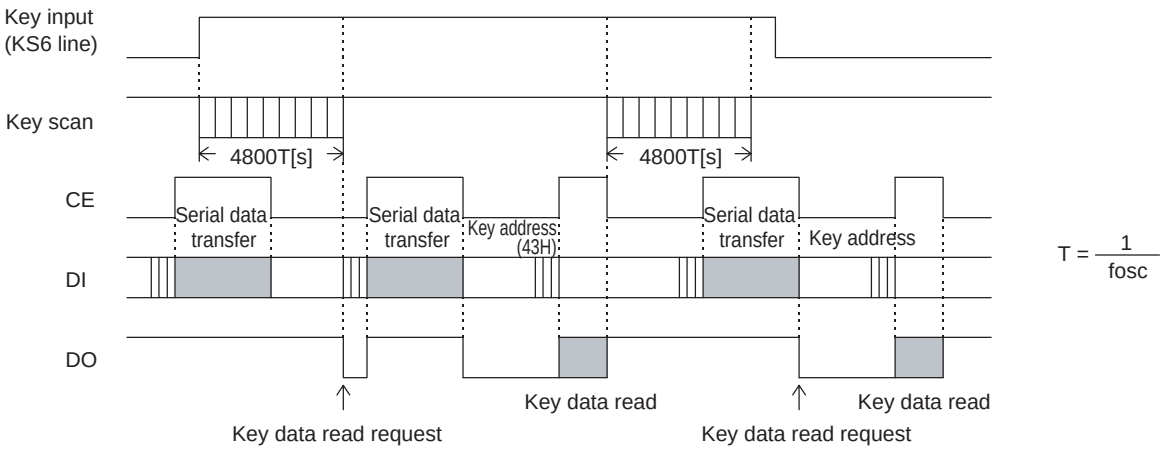


- In sleep mode
  - The pins KS1 to KS6 are set to high or low with the “set key scan output state” instruction.
  - If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSCI, OSCO pins is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
  - If a key is pressed for longer than 4800T(s)(Where T= $\frac{1}{fosc}$) the LC75817NE/NW outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
  - After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75817NE/NW performs another key scan. However, this dose not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10 kΩ).
  - Sleep mode key scan example

    Example: When a “display on/off control (SP = 1)” instruction and a “set key scan output state (KC1 to KC5 = 0, KC6 = 1)” instruction are executed (i.e. sleep mode with only KS6 high)



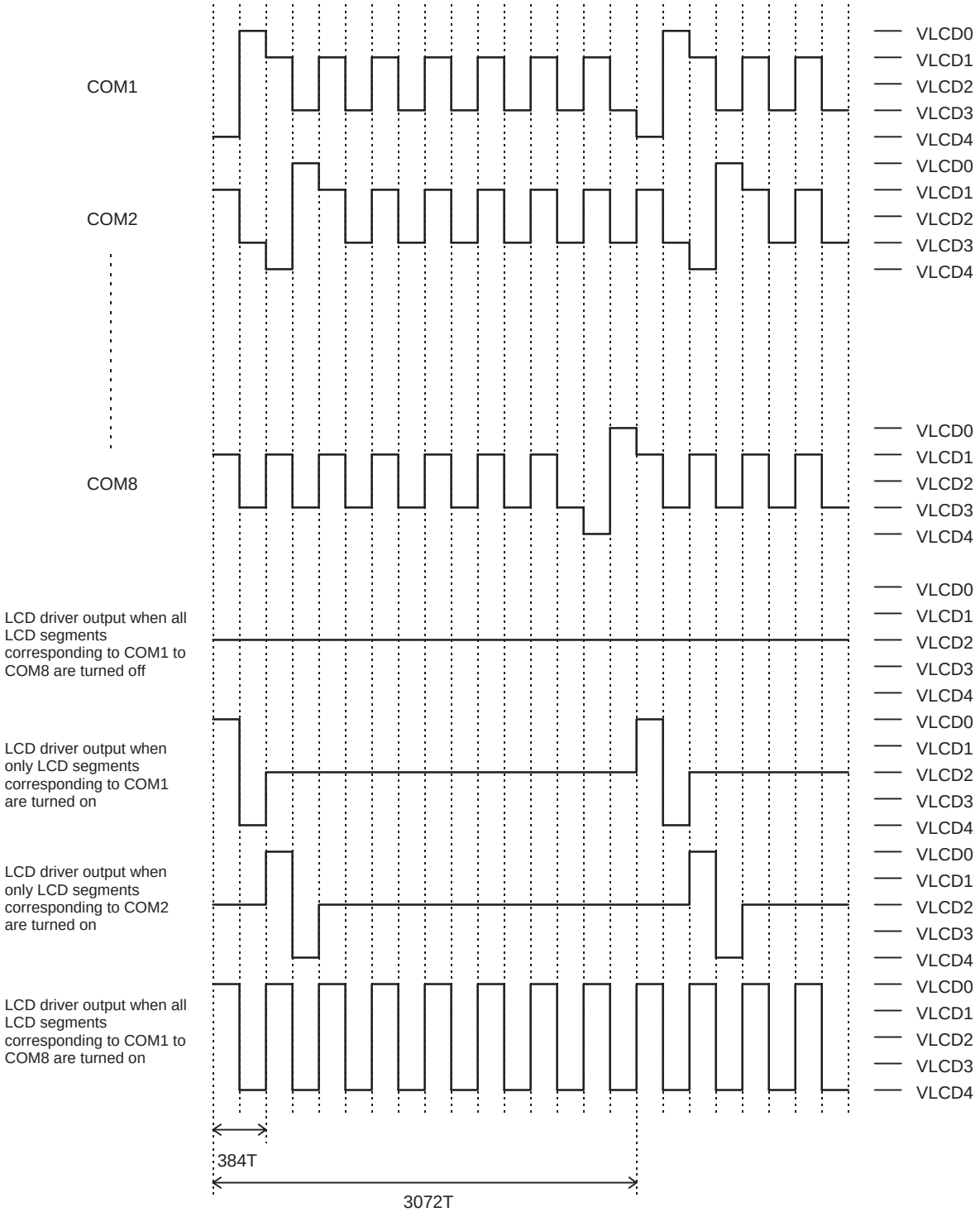
Note: *19. These diodes are required to reliably recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.



Multiple Key Presses

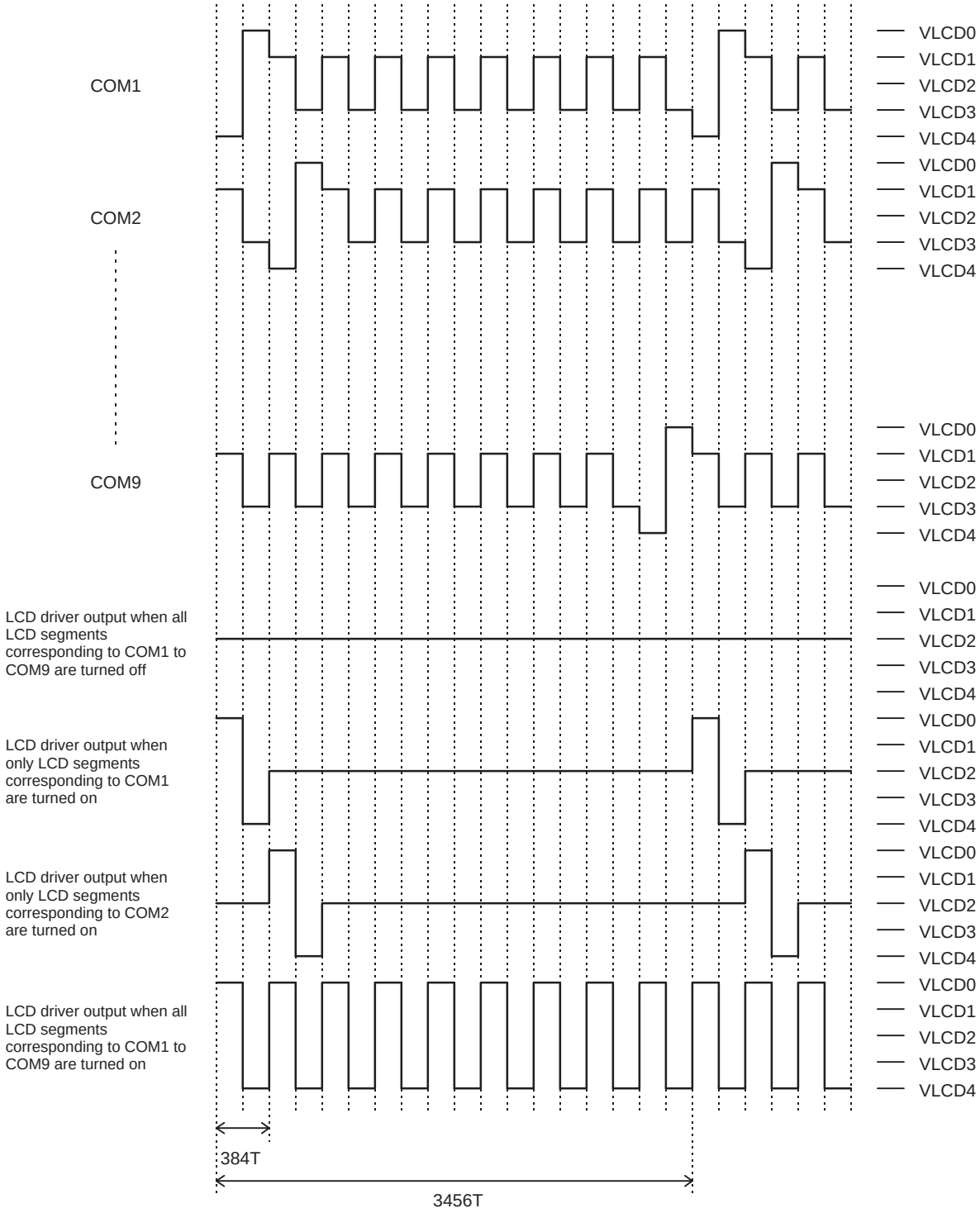
Although the LC75817NE/NW is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

1/8 Duty, 1/4 Bias Drive Technique



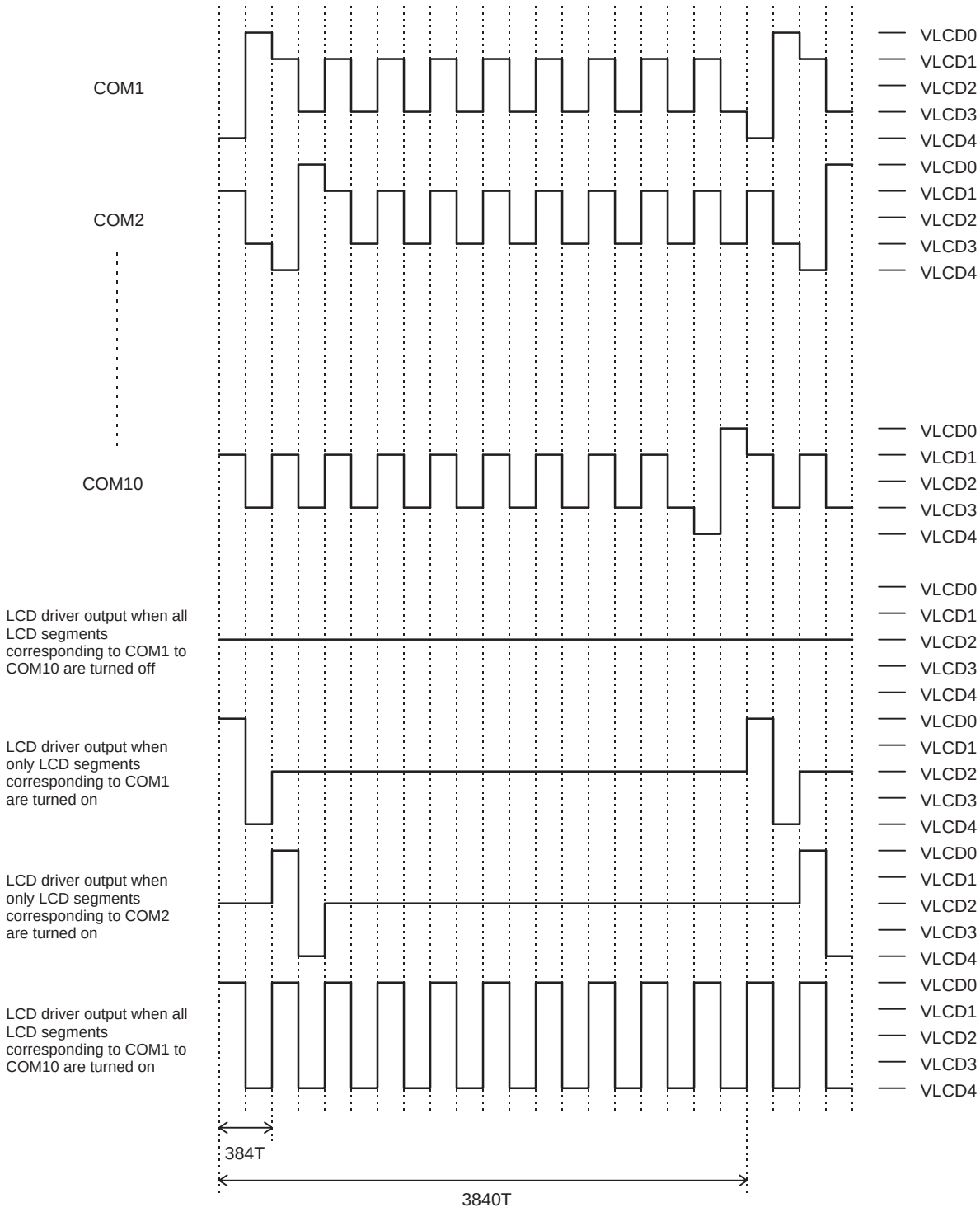
$$T = \frac{1}{fosc}$$

1/9 Duty, 1/4 Bias Drive Technique



$$T = \frac{1}{fosc}$$

1/10 Duty, 1/4 Bias Drive Technique



$$T = \frac{1}{fosc}$$

Voltage Detection Type Reset Circuit (VDET)

This circuit generates an output signal and resets the system when logic block power is first applied and when the voltage drops, i.e., when the logic block power supply voltage is less than or equal to the power down detection voltage VDET, which is 3.0V, typical. To assure that this function operates reliably, a capacitor must be added to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when the logic block power is first applied and the logic block power supply voltage V_{DD} fall time when the voltage drops are both at least 1 ms. (See Figure 3.)

Power Supply Sequence

The following sequences must be observed when power is turned on and off. (See Figure 3.)

- Power on :Logic block power supply(V_{DD}) on → LCD driver block power supply(V_{LCD}) on
- Power off:LCD driver block power supply(V_{LCD}) off → Logic block power supply(V_{DD}) off

However, if the logic and LCD driver blocks use a shared power supply, then the power supplies can be turned on and off at the same time.

System Reset

1. Reset function

The LC75817NE/NW performs a system reset with the VDET. When a system reset is applied, the display is turned off, key scanning is disabled, the key data is reset, and the general-purpose output ports are set to and held at the low level (V_{SS}). These states that are created as a result of the system reset can be cleared by executing the instruction described below. (See Figure 3.)

- Clearing the display off state

Display operation can be enabled by executing a “display on/off control” instruction. However, since the contents of the DCRAM, ADRAM, and CGRAM are undefined, applications must set the contents of these memories before turning on display with the “display on/off control” instruction. That is, applications must execute the following instructions.

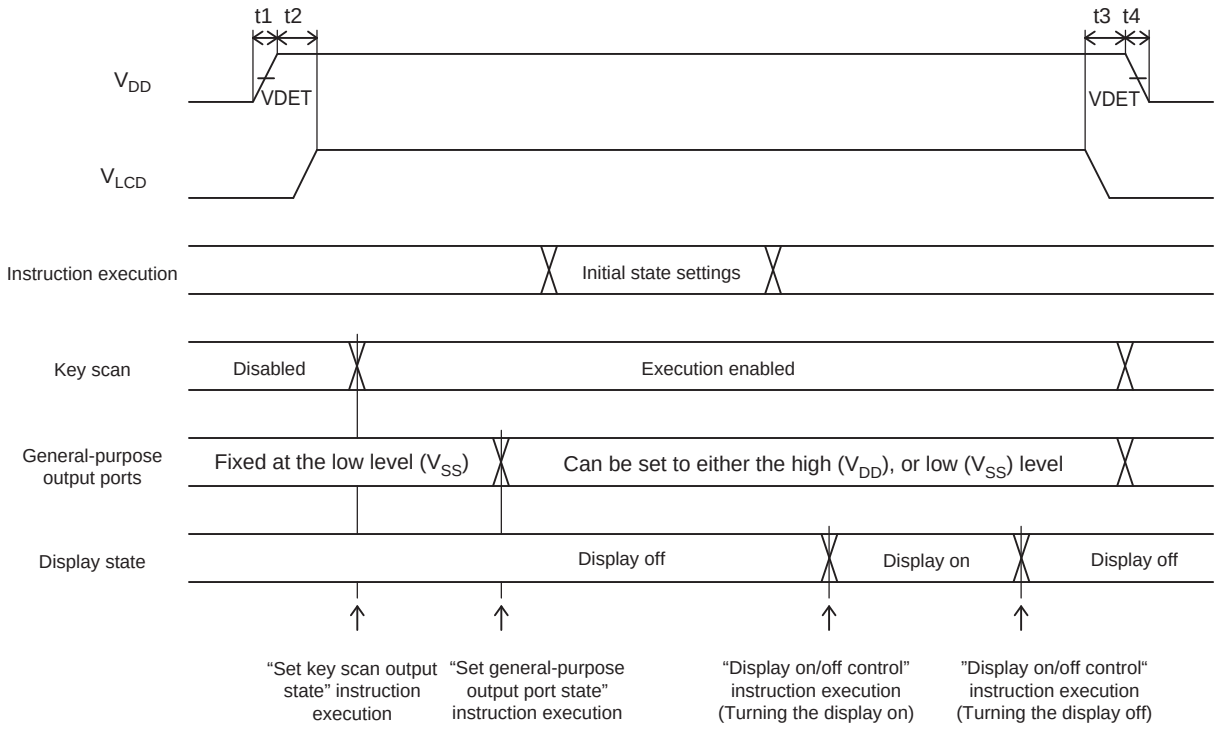
· Set display technique
· DCRAM data write
· ADRAM data write (If the ADRAM is used.)
· CGRAM data write (If the CGRAM is used.)
· Set AC address
· Set display contrast (If the display contrast adjustment circuit is used.)

After executing the above instructions, applications must turn on the display with a “display on/off control” instruction.

Note that when applications turn off in the normal mode, applications must turn off the display with a “display on/off control” instruction or the $\overline{INH}$ pin.

- Clearing the key scan disable and key data reset states
  Executing a “set key scan output state” instruction not only creates a state in which key scanning can be performed, but also clears the key data reset.

- Clearing the general-purpose output ports locked at the low level (V_{SS}) state
  Executing a “set general-purpose output port state” instruction clears the general-purpose output ports locked at the low level (V_{SS}) state and sets the states of the general-purpose output ports.



- t1 ≥ 1 ms (Logic block power supply voltage V_{DD} rise time)
- t2 ≥ 0 ms
- t3 ≥ 0 ms
- t4 ≥ 1 ms (Logic block power supply voltage V_{DD} fall time)
- Initial state settings
  Set display technique
  DCRAM data write
  ADRAM data write (If the ADRAM is used.)
  CGRAM data write (If the CGRAM is used.)
  Set AC address
  Set display contrast (If the display contrast adjustment circuit is used.)

Figure 3

2. Block states during a system reset

(1) CLOCK GENERATOR, TIMING GENERATOR

When a reset is applied, the oscillator on the OSCI, OSCO pins is started forcibly. This generates the base clock and enables instruction execution.

(2) INSTRUCTION REGISTER, INSTRUCTION DECODER

When a reset is applied, these circuits are forcibly initialized internally. Then, when instruction execution starts, the IC operates according to those instructions.

(3) ADDRESS REGISTER, ADDRESS COUNTER

When a reset is applied, these circuits are forcibly initialized internally. Then, the DCRAM and the ADRAM addresses are set when “Set AC address” instruction is executed.

(4) DCRAM, ADRAM, CGRAM

Since the contents of the DCRAM, ADRAM, and CGRAM become undefined during a reset, applications must execute “DCRAM data write”, “ADRAM data write (If the ADRAM is used.)”, and “CGRAM data write (If the CGRAM is used.)” instructions before executing a “display on/off control” instruction.

(5) CGROM

Character patterns are stored in this ROM.

(6) LATCH

Although the value of the data in the latch is undefined during a reset, the ADRAM, CGROM, and CGRAM data is stored by executing a “display on/off control” instruction.

(7) COMMON DRIVER, SEGMENT DRIVER

These circuits are forced to the display off state when a reset is applied.

(8) CONTRAST ADJUSTER

Display contrast adjustment circuit operation is disabled when a reset is applied. After that, the display contrast can be set by executing a “set display contrast” instruction.

(9) KEY SCAN, KEY BUFFER

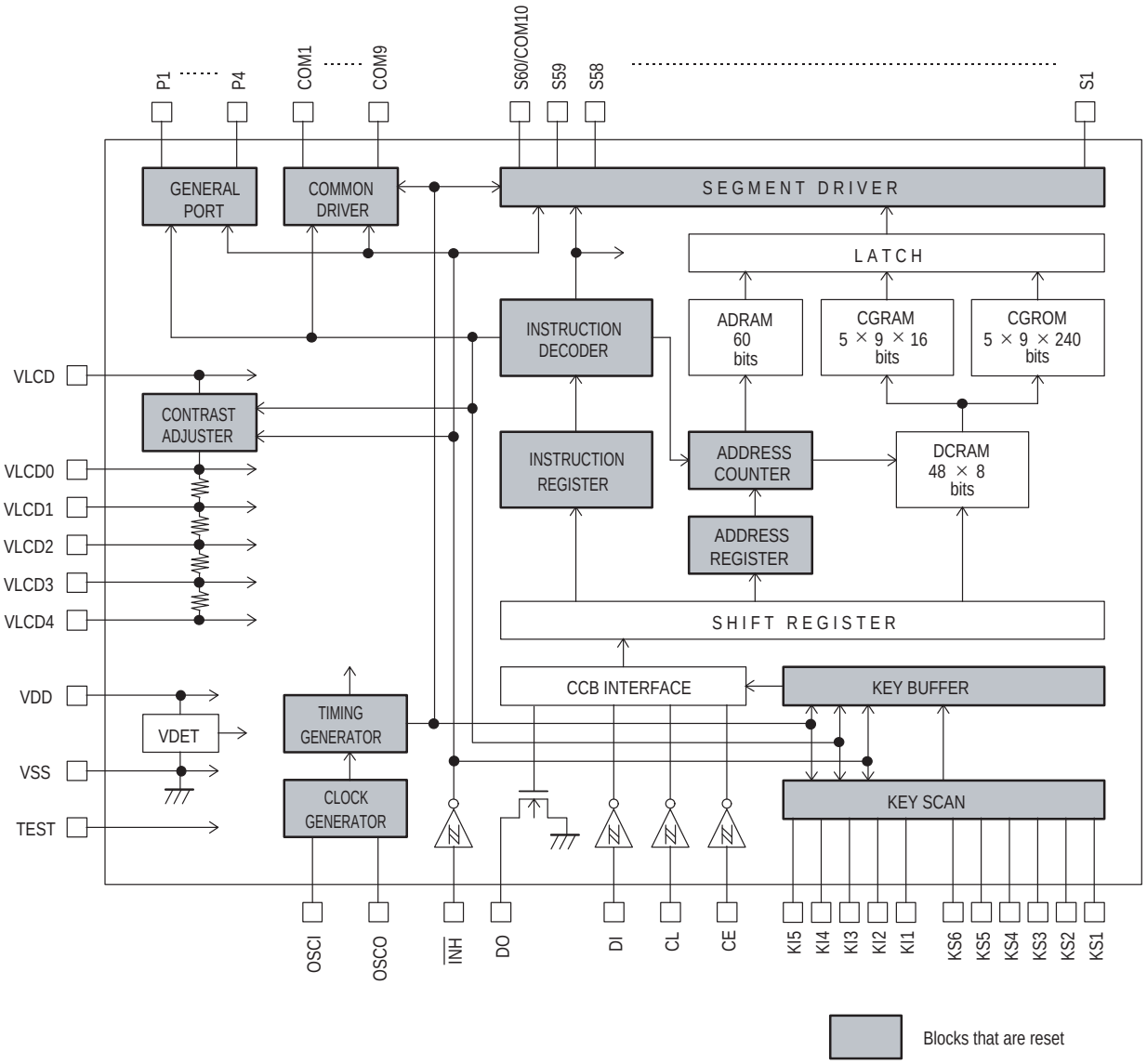
When a reset is applied, these circuits are forcibly initialized internally, and key scan operation is disabled. Also, the key data is all set to 0. After that, key scanning can be performed by executing a “set key scan output state” instruction.

(10) GENERAL PORT

The general-purpose output ports are fixed at the low level (V_{SS}) when a reset is applied.

(11) CCB INTERFACE, SHIFT REGISTER

These circuits go to the serial data input wait state.



3. Output pin states during the system reset

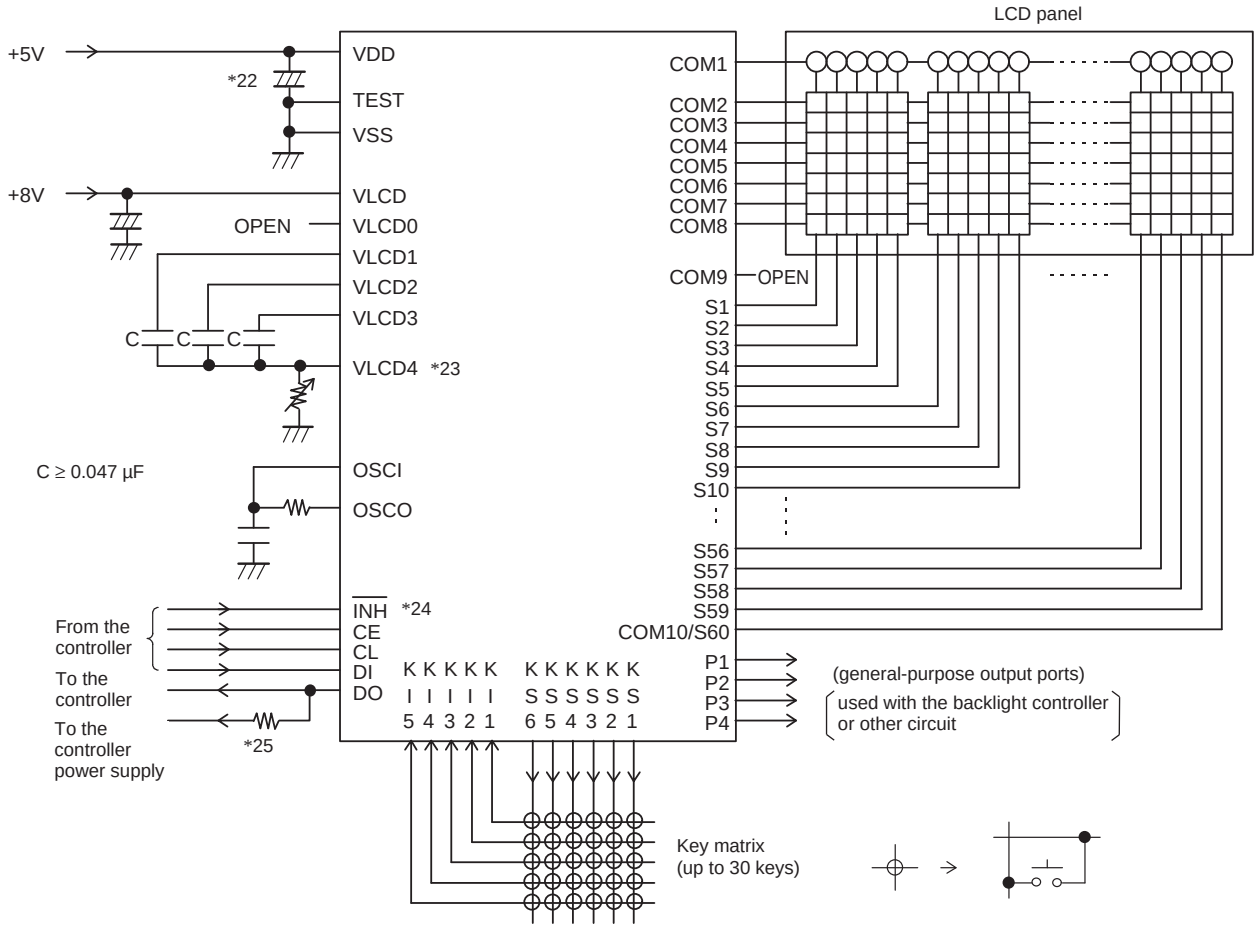
Output pin	State during reset
S1 to S59	L ($V_{LCD}4$)
S60/COM10	L ($V_{LCD}4$)*20
COM1 to COM9	L ($V_{LCD}4$)
KS1 to KS6	L (V_{SS})
P1 to P4	L (V_{SS})
DO	H *21

Notes: *20. This output pin is forcibly set to the segment output function and held at the low level ($V_{LCD}4$). However, when a “set display technique” instruction is executed, the segment output or the common output function is selected as specified by that instruction.

*21. Since this output pin is an open-drain output, a pull-up resistor (between 1 kΩ and 10 kΩ) is required. This pin is held at the high level even if a key data read operation is performed before executing a “set key scan output state” instruction.

Sample Application Circuit 1

1/8 duty, 1/4 bias drive technique (for use with normal panels)



Notes: *22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75817NE/NW is reset by the VDET.

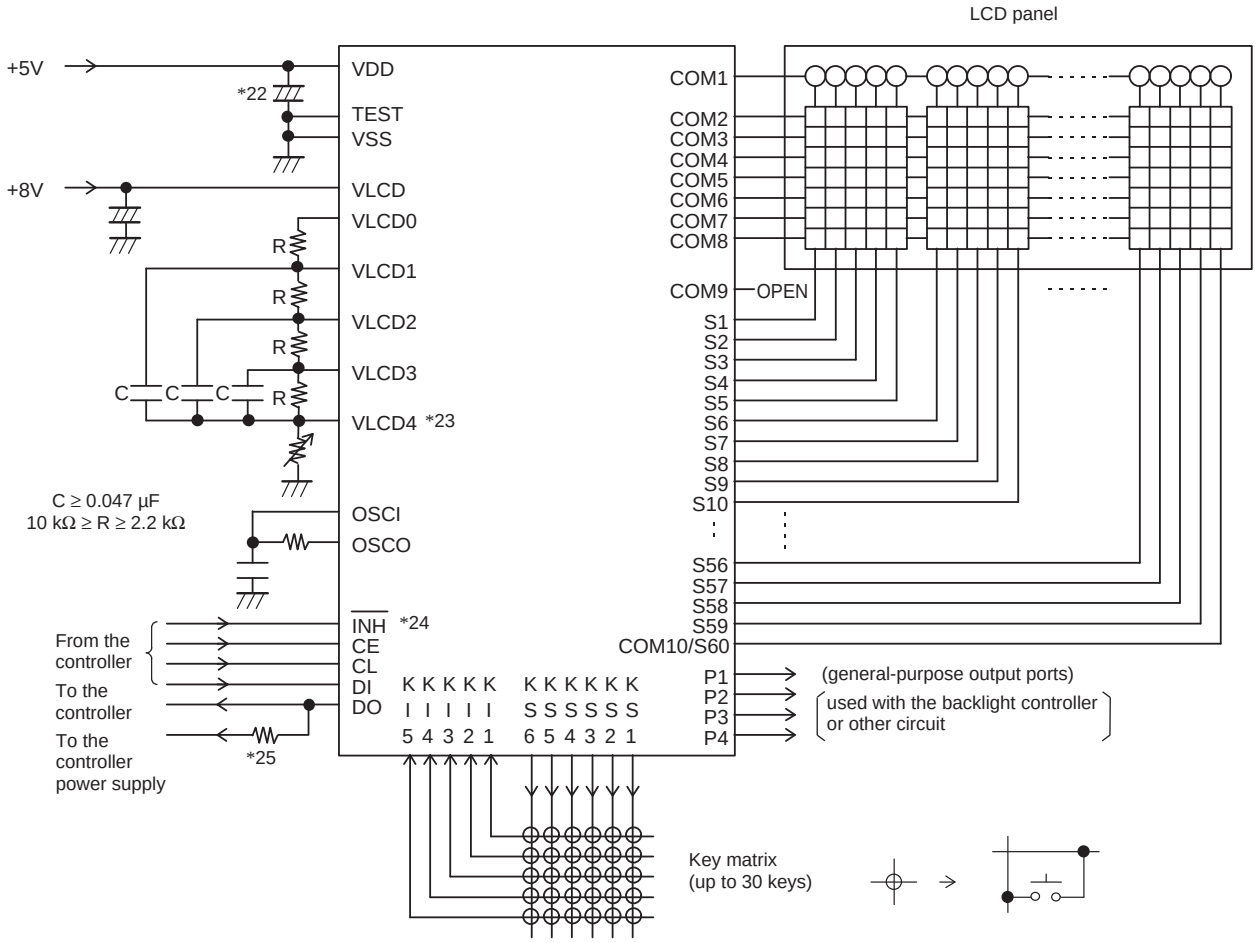
*23. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*24. If the function of $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*25. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 2

1/8 duty, 1/4 bias drive technique (for use with large panels)



Notes: *22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75817NE/NW is reset by the VDET.

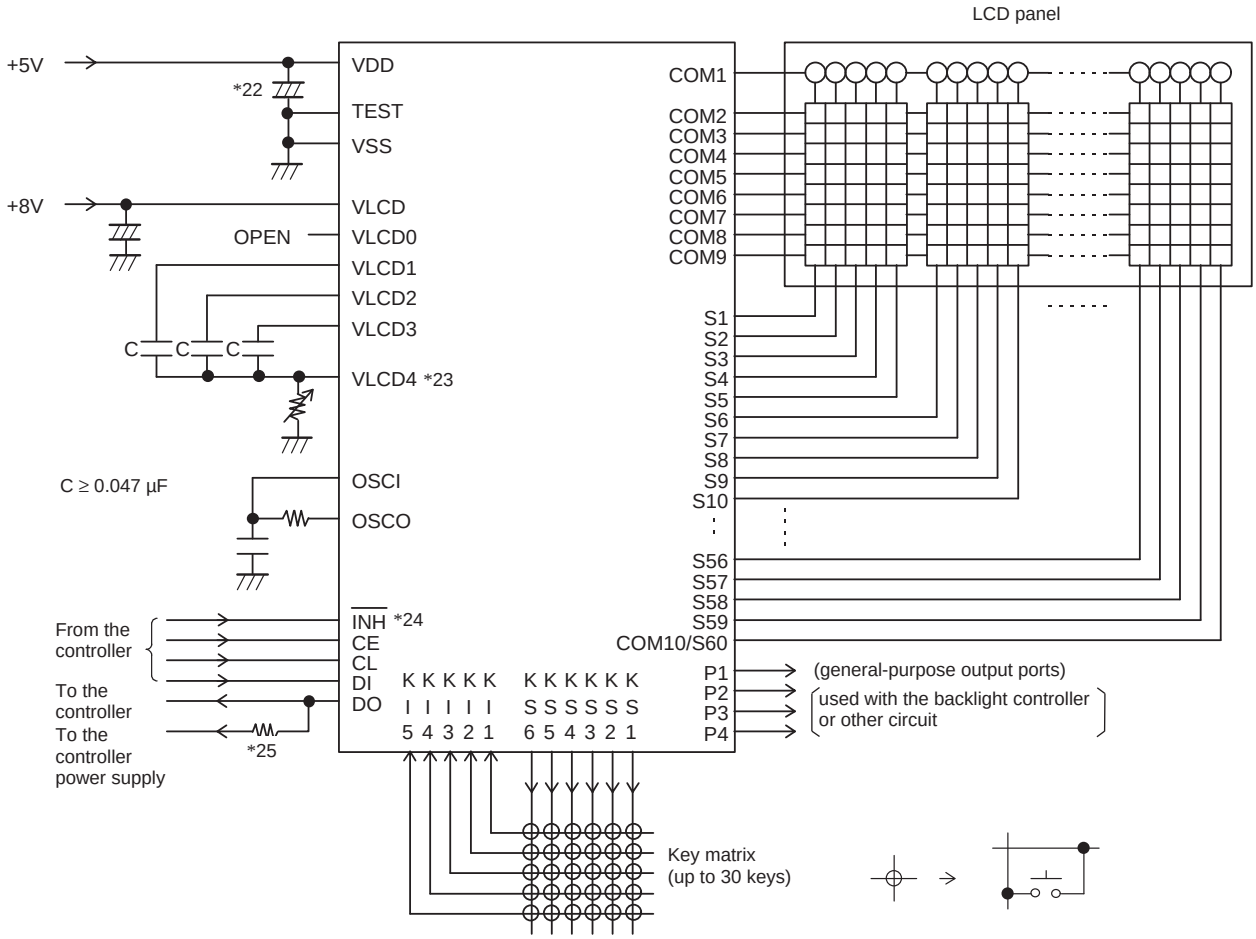
*23. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*24. If the function of $\overline{\text{INH}}$ pin is not used, the $\overline{\text{INH}}$ pin must be connected to the logic block power supply V_{DD}.

*25. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 3

1/9 duty, 1/4 bias drive technique (for use with normal panels)



Notes: *22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75817NE/NW is reset by the VDET.

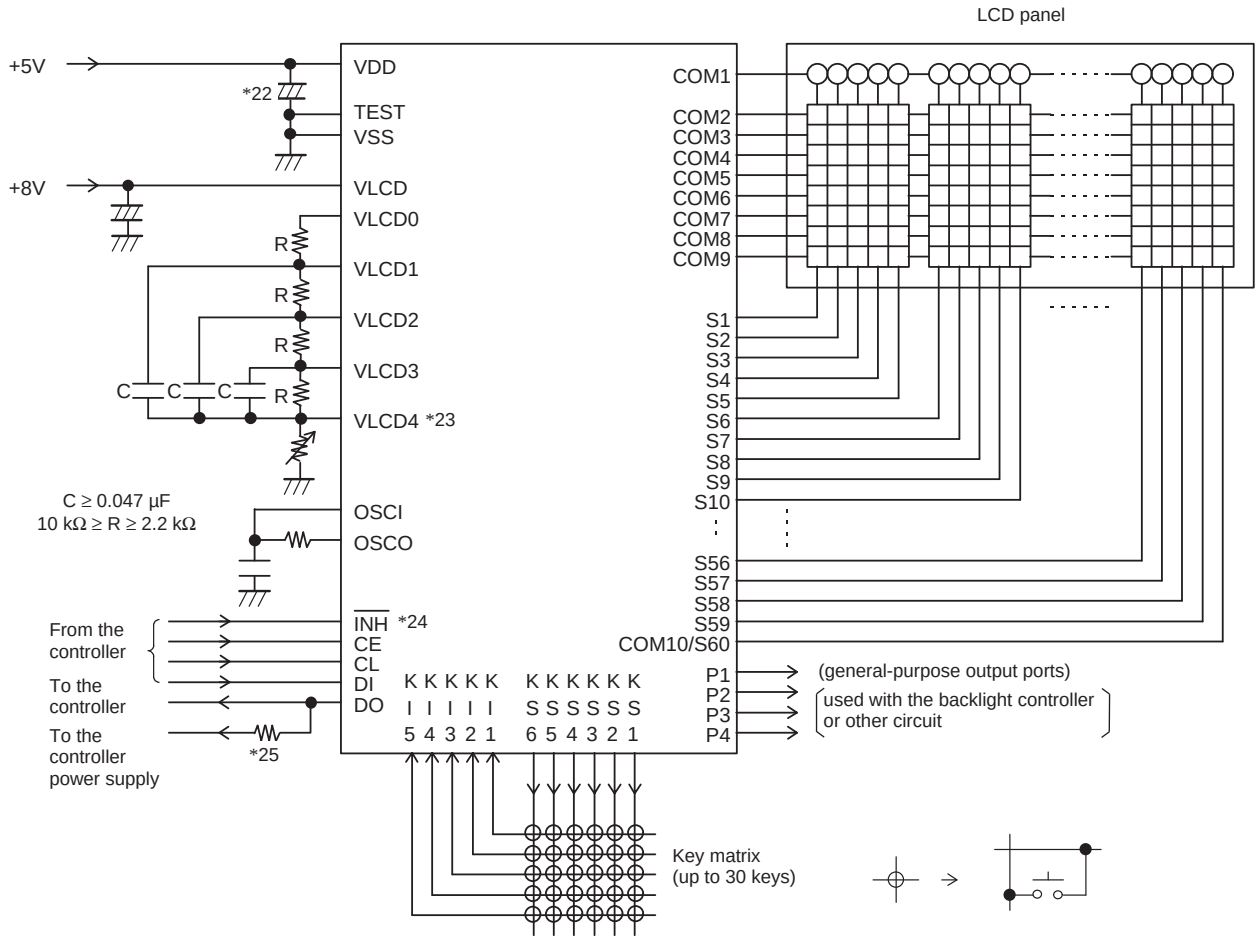
*23. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*24. If the function of $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*25. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 4

1/9 duty, 1/4 bias drive technique (for use with large panels)



Notes: *22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75817NE/NW is reset by the VDET.

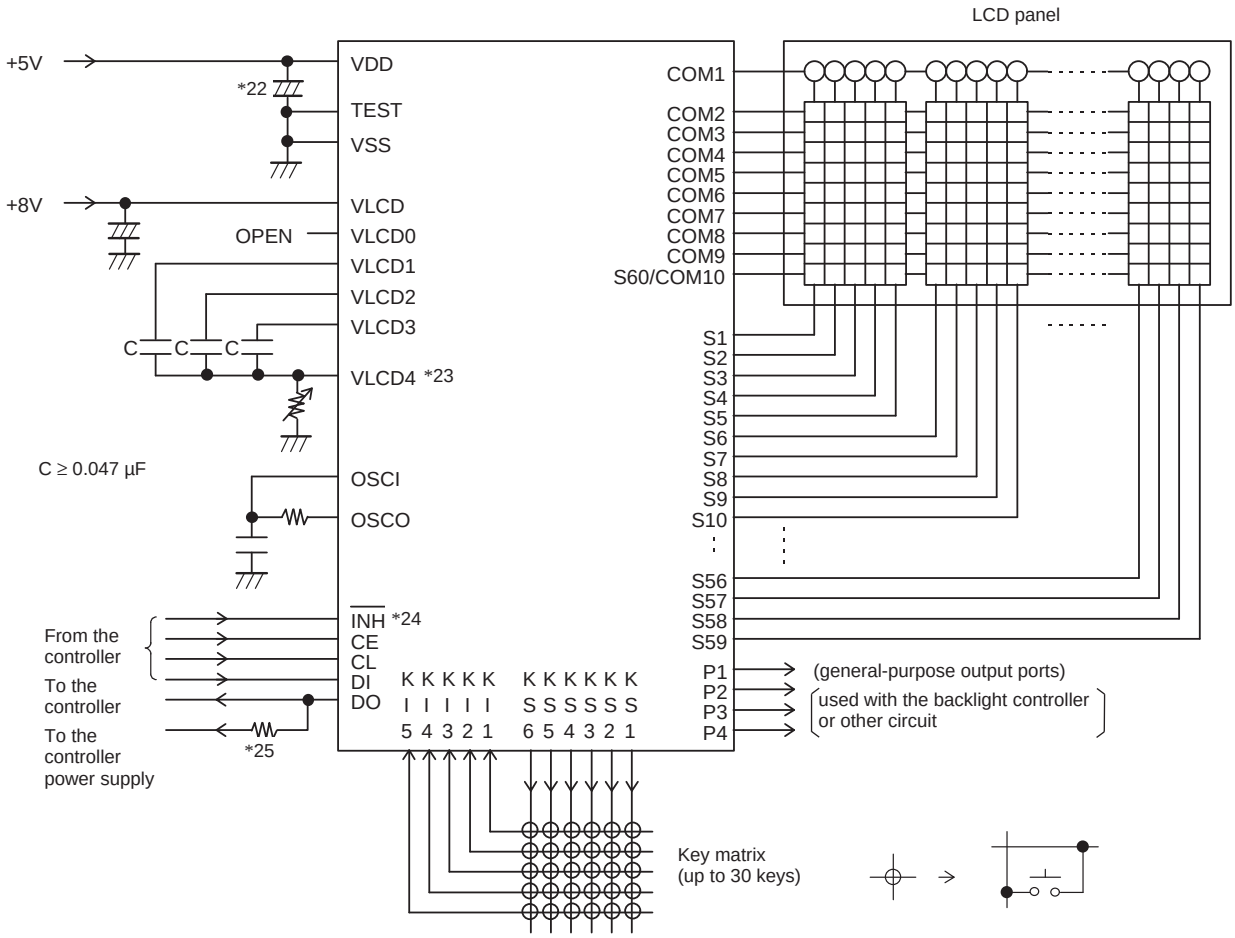
*23. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*24. If the function of $\overline{\text{INH}}$ pin is not used, the $\overline{\text{INH}}$ pin must be connected to the logic block power supply V_{DD}.

*25. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 5

1/10 duty, 1/4 bias drive technique (for use with normal panels)



Notes: *22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75817NE/NW is reset by the VDET.

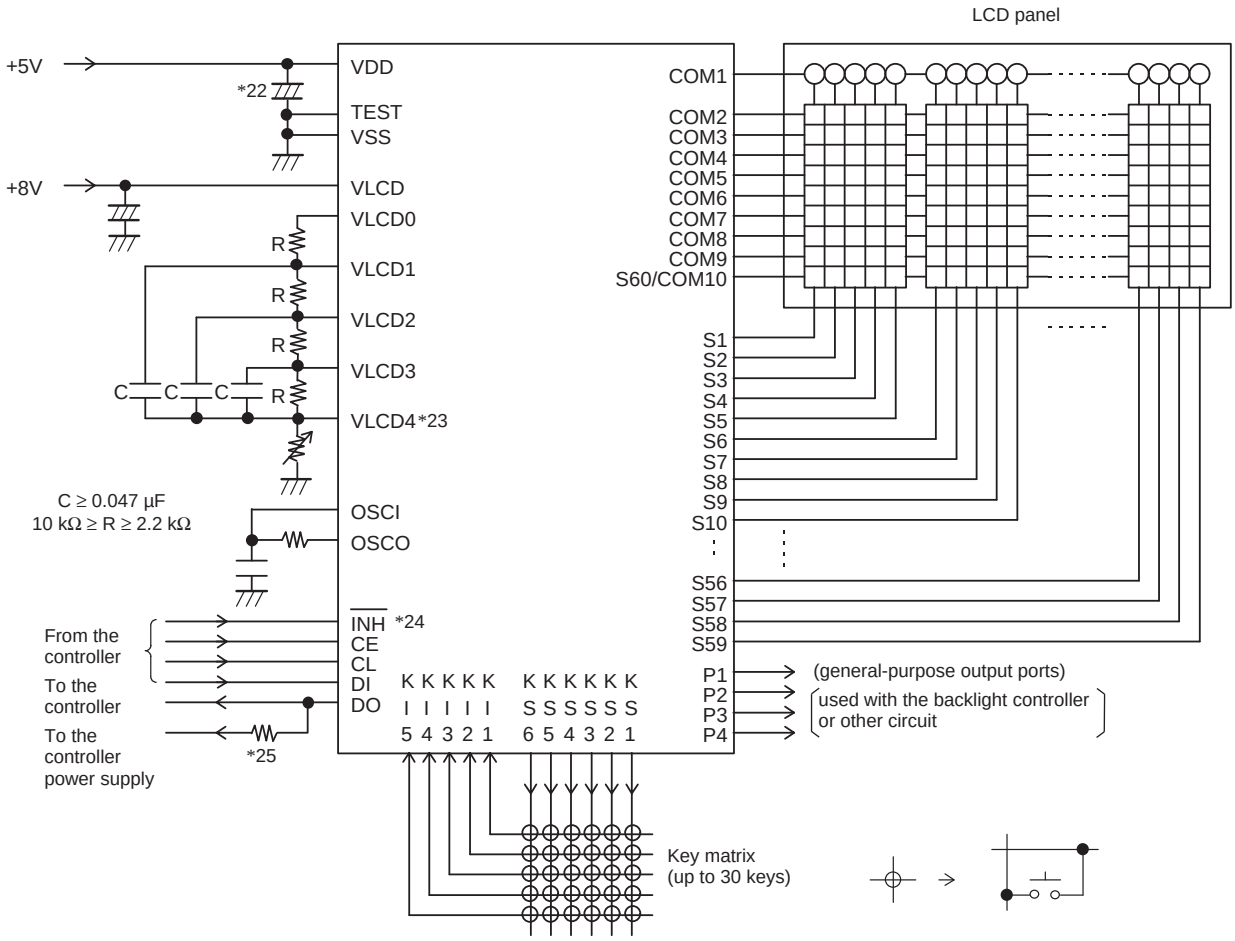
*23. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*24. If the function of $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*25. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 6

1/10 duty, 1/4 bias drive technique (for use with large panels)



Notes: *22. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75817NE/NW is reset by the VDET.

*23. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*24. If the function of $\overline{\text{INH}}$ pin is not used, the $\overline{\text{INH}}$ pin must be connected to the logic block power supply V_{DD}.

*25. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Correspondence between Instructions and the Display (When the LC75817N-8721 is used)

No.	Instruction (hexadecimal) LSB D40 to D43	D44 to D47	D48 to D51	D52 to D55	D56 to D59	MSB D60 to D63	Display	Operation
1	Power application (Initialization with the VDET.)							Initializes the IC. The display is in the off state.
2	Set display technique				0	8		Sets to 1/8 duty 1/4 bias display drive technique
3	DCRAM data write (increment mode)							
	0	2	0	0	1	A		Writes the display data " " to DCRAM address 00H
4	DCRAM data write (increment mode)				3	5		Writes the display data "S" to DCRAM address 01H
5	DCRAM data write (increment mode)				1	4		Writes the display data "A" to DCRAM address 02H
6	DCRAM data write (increment mode)				E	4		Writes the display data "N" to DCRAM address 03H
7	DCRAM data write (increment mode)				9	5		Writes the display data "Y" to DCRAM address 04H
8	DCRAM data write (increment mode)				F	4		Writes the display data "O" to DCRAM address 05H
9	DCRAM data write (increment mode)				0	2		Writes the display data " " to DCRAM address 06H
10	DCRAM data write (increment mode)				C	4		Writes the display data "L" to DCRAM address 07H
11	DCRAM data write (increment mode)				3	5		Writes the display data "S" to DCRAM address 08H
12	DCRAM data write (increment mode)				9	4		Writes the display data "I" to DCRAM address 09H
13	DCRAM data write (increment mode)				0	2		Writes the display data " " to DCRAM address 0AH
14	DCRAM data write (increment mode)				C	4		Writes the display data "L" to DCRAM address 0BH
15	DCRAM data write (increment mode)				3	4		Writes the display data "C" to DCRAM address 0CH
16	DCRAM data write (increment mode)				7	3		Writes the display data "7" to DCRAM address 0DH
17	DCRAM data write (increment mode)				5	3		Writes the display data "5" to DCRAM address 0EH
18	DCRAM data write (increment mode)				8	3		Writes the display data "8" to DCRAM address 0FH
19	DCRAM data write (increment mode)				1	3		Writes the display data "1" to DCRAM address 10H
20	DCRAM data write (increment mode)				7	3		Writes the display data "7" to DCRAM address 11H
21	DCRAM data write (increment mode)							
			E	4	0	A		Writes the display data "N" to DCRAM address 12H

Continued on next page.

Continued from preceding page.

No.	Instruction (hexadecimal) LSB D40 to D43	D44 to D47	D48 to D51	D52 to D55	D56 to D59	MSB D60 to D63	Display	Operation
22	Set AC address		0	0	0	2		Loads the DCRAM address 00H and the ADRAM address 0H into AC
23	Display on/off control						S A N Y O L S I L	
	F	F	F	X	1	4		Turns on the LCD for all digits (12 digits) in MDATA
24	Display shift						S A N Y O L S I L C	
					1	C		Shifts the display (MDATA only) to the left
25	Display shift						A N Y O L S I L C 7	
					1	C		Shifts the display (MDATA only) to the left
26	Display shift						N Y O L S I L C 7 5	
					1	C		Shifts the display (MDATA only) to the left
27	Display shift						Y O L S I L C 7 5 8	
					1	C		Shifts the display (MDATA only) to the left
28	Display shift						O L S I L C 7 5 8 1	
					1	C		Shifts the display (MDATA only) to the left
29	Display shift						L S I L C 7 5 8 1 7	
					1	C		Shifts the display (MDATA only) to the left
30	Display shift						L S I L C 7 5 8 1 7 N	
					1	C		Shifts the display (MDATA only) to the left
31	Display on/off control							
	0	0	0	X	8	4		Set to sleep mode, turns off the LCD for all digits
32	Display on/off control						L S I L C 7 5 8 1 7 N	
	F	F	F	X	1	4		Turns on the LCD for all digits (12 digits) in MDATA
33	Set AC address						S A N Y O L S I L	
			0	0	0	2		Loads the DCRAM address 00H and the ADRAM address 0H into AC

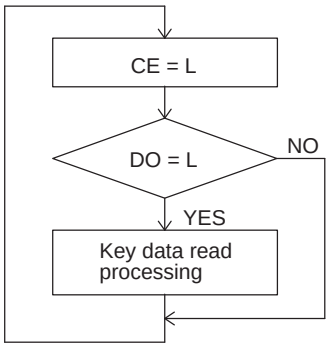
Note: *26. This sample above assumes the use of 12 digits 5 × 7 dot matrix LCD. CGRAM and ADRAM are not used.

X: don't care

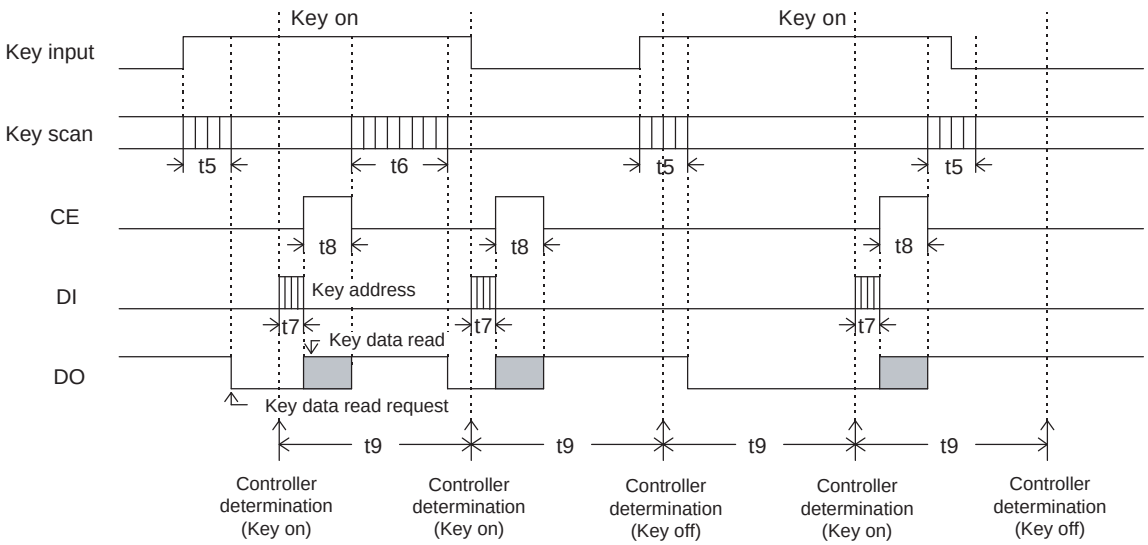
Notes on the controller key data read techniques

1. Timer based key data acquisition

• Flowchart



• Timing chart



t5: Key scan execution time when the key data agreed for two key scans. (4800T(s))

t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (9600T(s))

t7: Key address (43H) transfer time

t8: Key data read time

$$T = \frac{1}{fosc}$$

• Explanation

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t9 period without fail. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

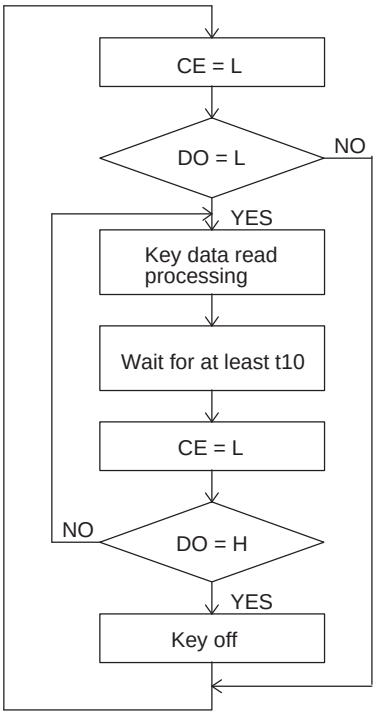
The period t9 in this technique must satisfy the following condition.

t9>t6+t7+t8

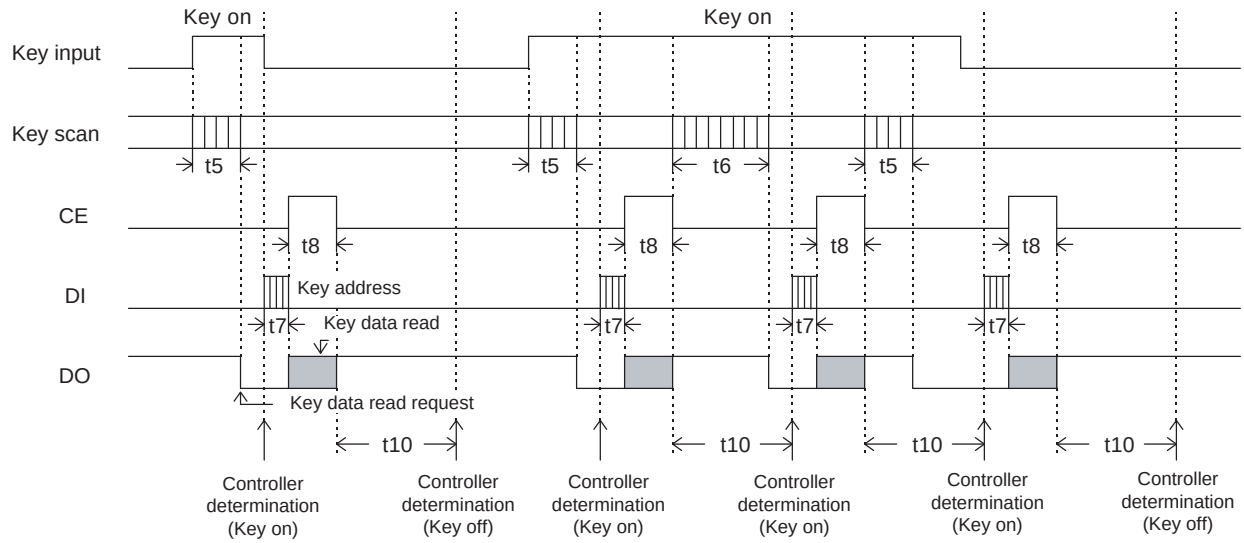
If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

2. Interrupt based key data acquisition

• Flowchart



• Timing chart



t5: Key scan execution time when the key data agreed for two key scans. (4800T(s))

t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (9600T(s))

t7: Key address (43H) transfer time

t8: Key data read time

$$T = \frac{1}{fosc}$$

• Explanation

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t10 has elapsed by checking the DO state when CE is low and reading the key data. The period t10 in this technique must satisfy the following condition.

$t10 > t6$

If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

LC75817N-8721 Character Font (Standard)

Lower 4bits \ Upper 4bits	MSB 0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM(1)	α		0	@	P	\	p	á	â	＼	｡	ﾀ	ﾐ	Á	Â
0001	(2)	β	!	1	A	Q	a	q	à	ä	。	ｱ	ﾁ	ﾑ	À	Ä
0010	(3)	±	”	2	B	R	b	r	é	ê	「	ｲ	ﾂ	ﾒ	É	Ê
0011	(4)	÷	#	3	C	S	c	s	è	ë	」	ｳ	ﾃ	ﾓ	È	Ë
0100	(5)	π	$	4	D	T	d	t	í	î	、	ｴ	ﾄ	ﾔ	Í	Î
0101	(6)	¿	%	5	E	U	e	u	ì	ï	・	ｵ	ﾅ	ﾕ	Ì	Ï
0110	(7)	Φ	&	6	F	V	f	v	ó	ô	ヲ	ｶ	ﾆ	ﾖ	Ó	Ô
0111	(8)	φ	’	7	G	W	g	w	ò	ö	ｧ	ｷ	ﾇ	ﾗ	Ò	Ö
1000	(9)	Æ	(	8	H	X	h	x	ú	û	ｨ	ｸ	ﾈ	ﾘ	Ú	Û
1001	(10)	æ	)	9	I	Y	i	y	ù	ü	ｩ	ｹ	ﾉ	ﾙ	Ù	Ü
1010	(11)	Œ	*	:	J	Z	j	z	Ñ	ñ	ｪ	ｺ	ﾊ	ﾚ	Ã	ã
1011	(12)	œ	+	;	K	[	k	{	Ç	ç	ｫ	ｻ	ﾋ	ﾛ	Õ	õ
1100	(13)	→	,	<	L	¥	l	|	Ş	ş	ｬ	ｼ	ﾌ	ﾜ	Å	å
1101	(14)	←	−	=	M	]	m	}	Ğ	ğ	ｭ	ｽ	ﾍ	ﾝ	a	o
1110	(15)	↑	.	>	N	^	n	—	İ	i	ｮ	ｾ	ﾎ	ﾞ	ń	ň
1111	(16)	↓	／	?	O	_	o	■	IJ	ij	ｯ	ｿ	ﾏ	ﾟ	ő	£

A10735

■ Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

■ SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

■ In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of February, 2002. Specifications and information herein are subject to change without notice.