


SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company


**LC75829PE,
LC75829PW**

CMOS IC

**1/4 and 1/3-Duty General-Purpose
LCD Display Driver**

Overview

The LC75829PE and LC75829PW are 1/4 duty and 1/3 duty general-purpose microprocessor-controlled LCD drivers that can be used in applications such as frequency display in products with electronic tuning.

In addition to being able to drive up to 208 segments directly, the LC75829PE and LC75829PW can also control up to 4 general-purpose output ports. Incorporation of an oscillation circuit helps to reduce the number of external resistors and capacitors required.

Features

- Support for 1/4-duty 1/3-bias or 1/3-duty 1/3-bias drive techniques under serial data control.
 - When 1/4-duty: Capable of driving up to 208 segments
 - When 1/3-duty: Capable of driving up to 159 segments
- Serial data input supports CCB format communication with the system controller. (Support 3.3V and 5V operation)
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port function. (Support for up to 4 general-purpose output ports)
- Support for clock output function of 1ch.
- Serial data control of the frame frequency of the common and segment output waveforms.
- Serial data control of switching between the internal oscillator operating mode and external clock operating mode.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- The INH pin allows the display to be forced to the off state.
- Incorporation of an oscillator circuit. (Incorporation of resistor and capacitor for an oscillation)

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- CCB is SANYO Semiconductor's original bus format. All bus addresses are managed by SANYO Semiconductor for this format.

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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|----------------------|-------------------------------------|----------------------|------------------|
| Maximum supply voltage | $V_{DD \text{ max}}$ | V_{DD} | -0.3 to +6.5 | V |
| Input voltage | V_{IN1} | CE, CL, DI, $\overline{\text{INH}}$ | -0.3 to +6.5 | V |
| | V_{IN2} | OSCI, V_{DD1} , V_{DD2} | -0.3 to $V_{DD}+0.3$ | |
| Output voltage | V_{OUT} | S1 to S53, COM1 to COM4, P1 to P4 | -0.3 to $V_{DD}+0.3$ | V |
| Output current | I_{OUT1} | S1 to S52 | 300 | μA |
| | I_{OUT2} | COM1 to COM4, S53 | 3 | mA |
| | I_{OUT3} | P1 to P4 | 5 | |
| Allowable power dissipation | $P_d \text{ max}$ | $T_a=85^\circ\text{C}$ | 200 | mW |
| Operating temperature | T_{opr} | | -40 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{V}$

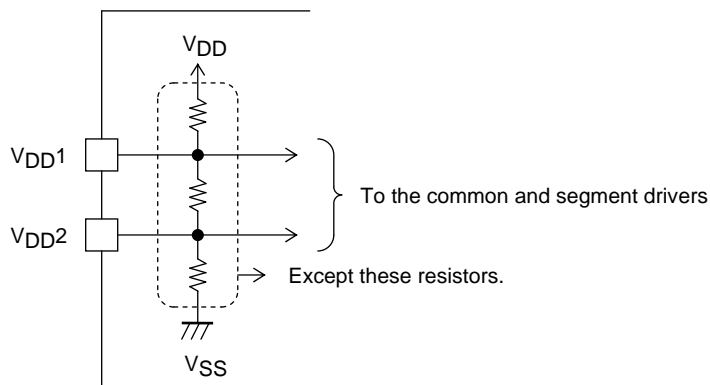
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|--------------|---|-------------|-------------|-------------|---------------|
| | | | min | typ | max | |
| Supply voltage | V_{DD} | V_{DD} | 4.5 | | 6.0 | V |
| Input voltage | V_{DD1} | V_{DD1} | | $2/3V_{DD}$ | V_{DD} | V |
| | V_{DD2} | V_{DD2} | | $1/3V_{DD}$ | V_{DD} | |
| Input high-level voltage | V_{IH1} | CE, CL, DI, $\overline{\text{INH}}$ | $0.4V_{DD}$ | | 6.0 | V |
| | V_{IH2} | OSCI: External clock operating mode | $0.4V_{DD}$ | | V_{DD} | |
| Input low-level voltage | V_{IL1} | CE, CL, DI, $\overline{\text{INH}}$ | 0 | | $0.2V_{DD}$ | V |
| | V_{IL2} | OSCI: External clock operating mode | 0 | | $0.2V_{DD}$ | |
| External clock operating frequency | f_{CK} | OSCI: External clock operating mode [Figure 4] | 10 | 300 | 600 | kHz |
| External clock duty cycle | D_{CK} | OSCI: External clock operating mode [Figure 4] | 30 | 50 | 70 | % |
| Data setup time | t_{ds} | CL, DI [Figure 2][Figure 3] | 160 | | | ns |
| Data hold time | t_{dh} | CL, DI [Figure 2][Figure 3] | 160 | | | ns |
| CE wait time | t_{cp} | CE, CL [Figure 2][Figure 3] | 160 | | | ns |
| CE setup time | t_{cs} | CE, CL [Figure 2][Figure 3] | 160 | | | ns |
| CE hold time | t_{ch} | CE, CL [Figure 2][Figure 3] | 160 | | | ns |
| High-level clock pulse width | $t_{\phi H}$ | CL [Figure 2][Figure 3] | 160 | | | ns |
| Low-level clock pulse width | $t_{\phi L}$ | CL [Figure 2][Figure 3] | 160 | | | ns |
| Rise time | t_r | CE, CL, DI [Figure 2][Figure 3] | | 160 | | ns |
| Fall time | t_f | CE, CL, DI [Figure 2][Figure 3] | | 160 | | ns |
| $\overline{\text{INH}}$ switching time | t_c | $\overline{\text{INH}}$, CE [Figure 5][Figure 6] | 10 | | | μs |

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Electrical Characteristics for the Allowable Operating Ranges

| Parameter | Symbol | Pin | Conditions | Ratings | | | Unit |
|--------------------------------|------------|------------------------------|--|-----------------|--------------|-----------------|---------|
| | | | | min | typ | max | |
| Hysteresis | V_H | CE, CL, DI, \overline{INH} | | | $0.03V_{DD}$ | | V |
| Input high-level current | I_{IH1} | CE, CL, DI, \overline{INH} | $V_I = 6.0V$ | | | 5.0 | μA |
| | I_{IH2} | OSCI | $V_I = V_{DD}$: External clock operating mode | | | 5.0 | |
| Input low-level current | I_{IL1} | CE, CL, DI, \overline{INH} | $V_I = 0V$ | -5.0 | | | μA |
| | I_{IL2} | OSCI | $V_I = 0V$: External clock operating mode | -5.0 | | | |
| Output high-level voltage | V_{OH1} | S1 to S53 | $I_O = -20\mu A$ | $V_{DD}-0.9$ | | | V |
| | V_{OH2} | COM1 to COM4 | $I_O = -100\mu A$ | $V_{DD}-0.9$ | | | |
| | V_{OH3} | P1 to P4 | $I_O = -1mA$ | $V_{DD}-0.9$ | | | |
| Output low-level voltage | V_{OL1} | S1 to S53 | $I_O = 20\mu A$ | | | 0.9 | V |
| | V_{OL2} | COM1 to COM4 | $I_O = 100\mu A$ | | | 0.9 | |
| | V_{OL3} | P1 to P4 | $I_O = 1mA$ | | | 0.9 | |
| Output middle-level voltage *1 | V_{MID1} | S1 to S53 | 1/3 bias $I_O = \pm 20\mu A$ | $2/3V_{DD}-0.9$ | | $2/3V_{DD}+0.9$ | V |
| | V_{MID2} | S1 to S53 | 1/3 bias $I_O = \pm 20\mu A$ | $1/3V_{DD}-0.9$ | | $1/3V_{DD}+0.9$ | |
| | V_{MID3} | COM1 to COM4 | 1/3 bias $I_O = \pm 100\mu A$ | $2/3V_{DD}-0.9$ | | $2/3V_{DD}+0.9$ | |
| | V_{MID4} | COM1 to COM4 | 1/3 bias $I_O = \pm 100\mu A$ | $1/3V_{DD}-0.9$ | | $1/3V_{DD}+0.9$ | |
| Oscillator frequency | fosc | Internal oscillator circuit | Internal oscillator operating mode | 240 | 300 | 360 | kHz |
| Current drain | I_{DD1} | V_{DD} | Power-saving mode | | | 100 | μA |
| | I_{DD2} | V_{DD} | $V_{DD} = 6.0V$ Output open Internal oscillator operating mode | | 800 | 1600 | |
| | I_{DD3} | V_{DD} | $V_{DD} = 6.0V$ Output open External clock operating mode $f_{CK} = 300kHz$ $V_{IH2} = 0.5V_{DD}$ $V_{IL2} = 0.1V_{DD}$ | | 800 | 1600 | |

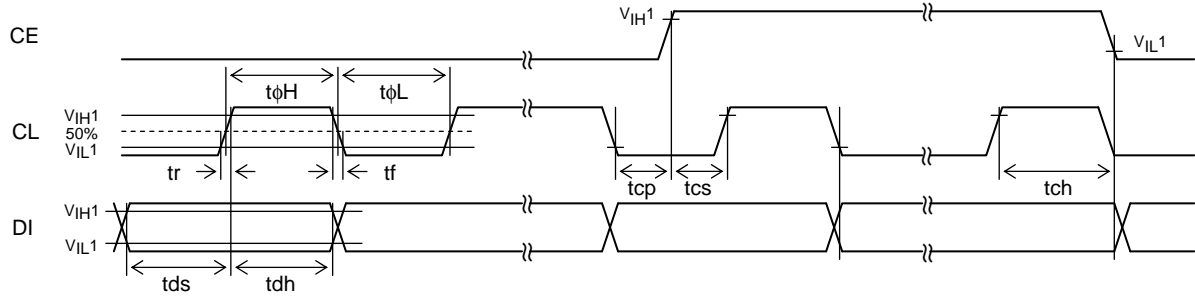
Note: *1 Excluding the bias voltage generation divider resistors built in the V_{DD1} and V_{DD2} . (See Figure 1.)



[Figure 1]

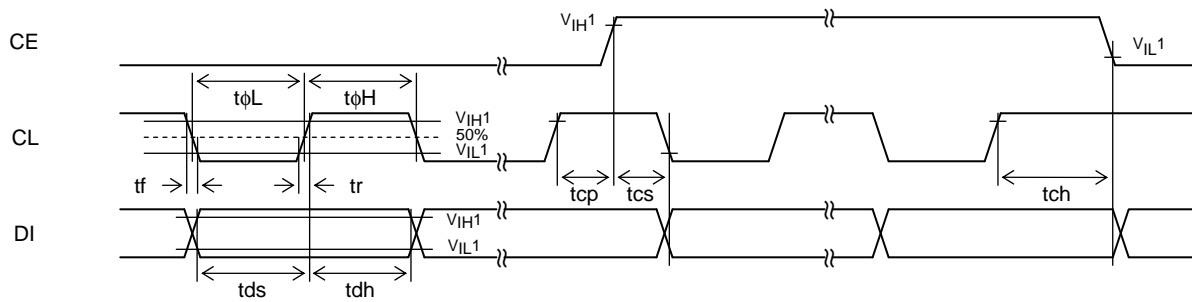
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1. When CL is stopped at the low level



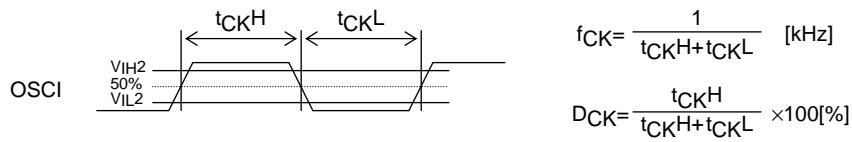
[Figure 2]

2. When CL is stopped at the high level



[Figure 3]

3. OSCI pin clock timing in external clock operating mode



[Figure 4]

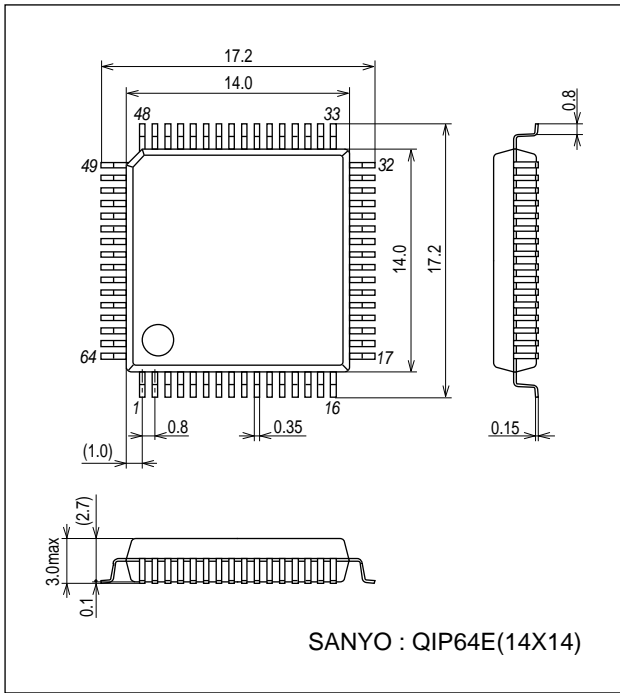
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Package Dimensions

unit : mm (typ)

3159A

[LC75829PE]

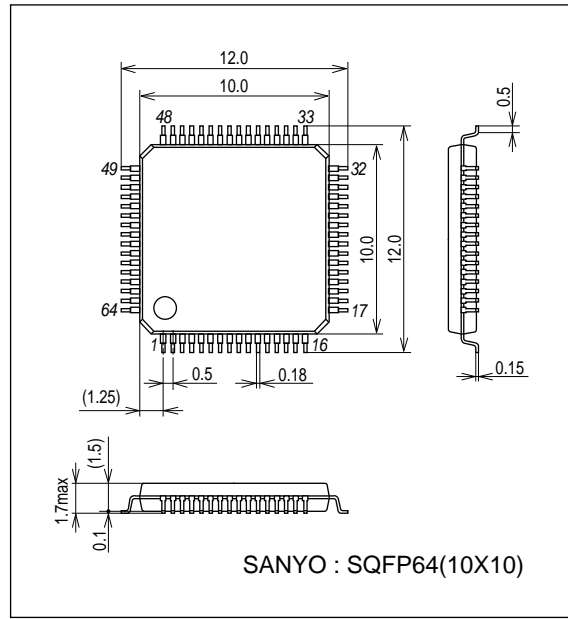


Package Dimensions

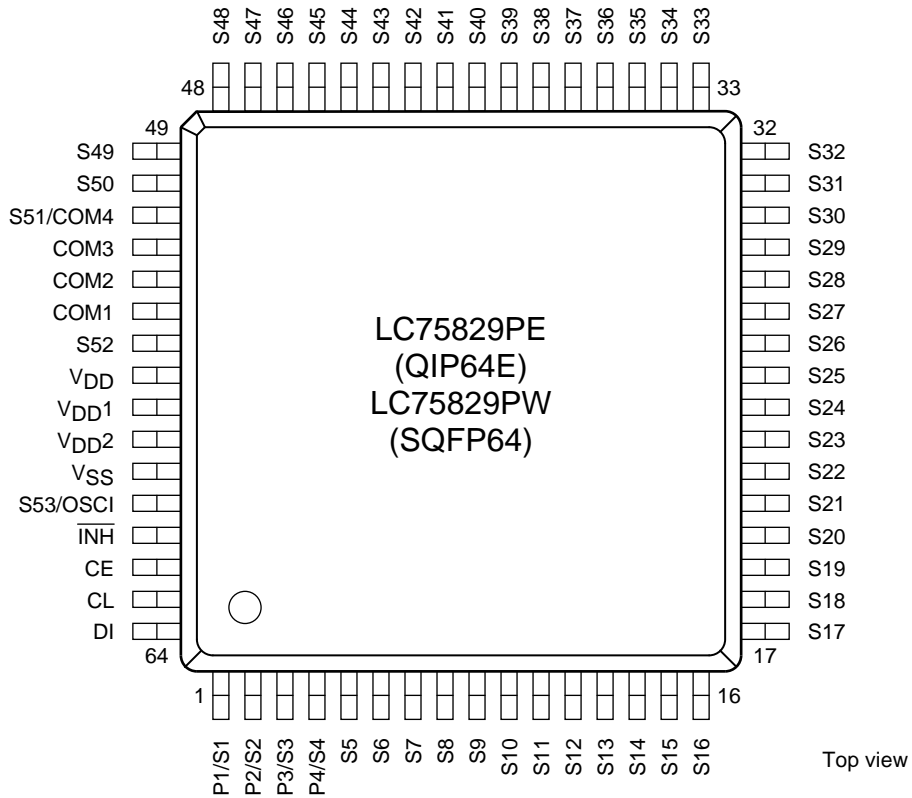
unit : mm (typ)

3190A

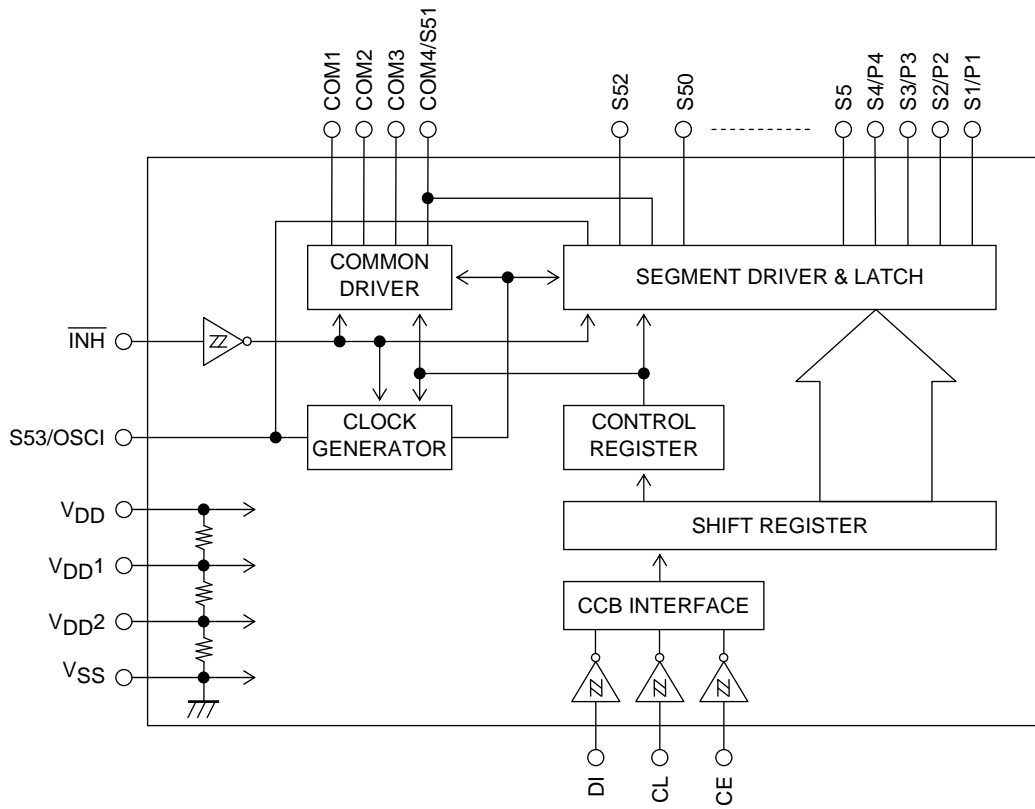
[LC75829PW]



Pin Assignment




Block Diagram



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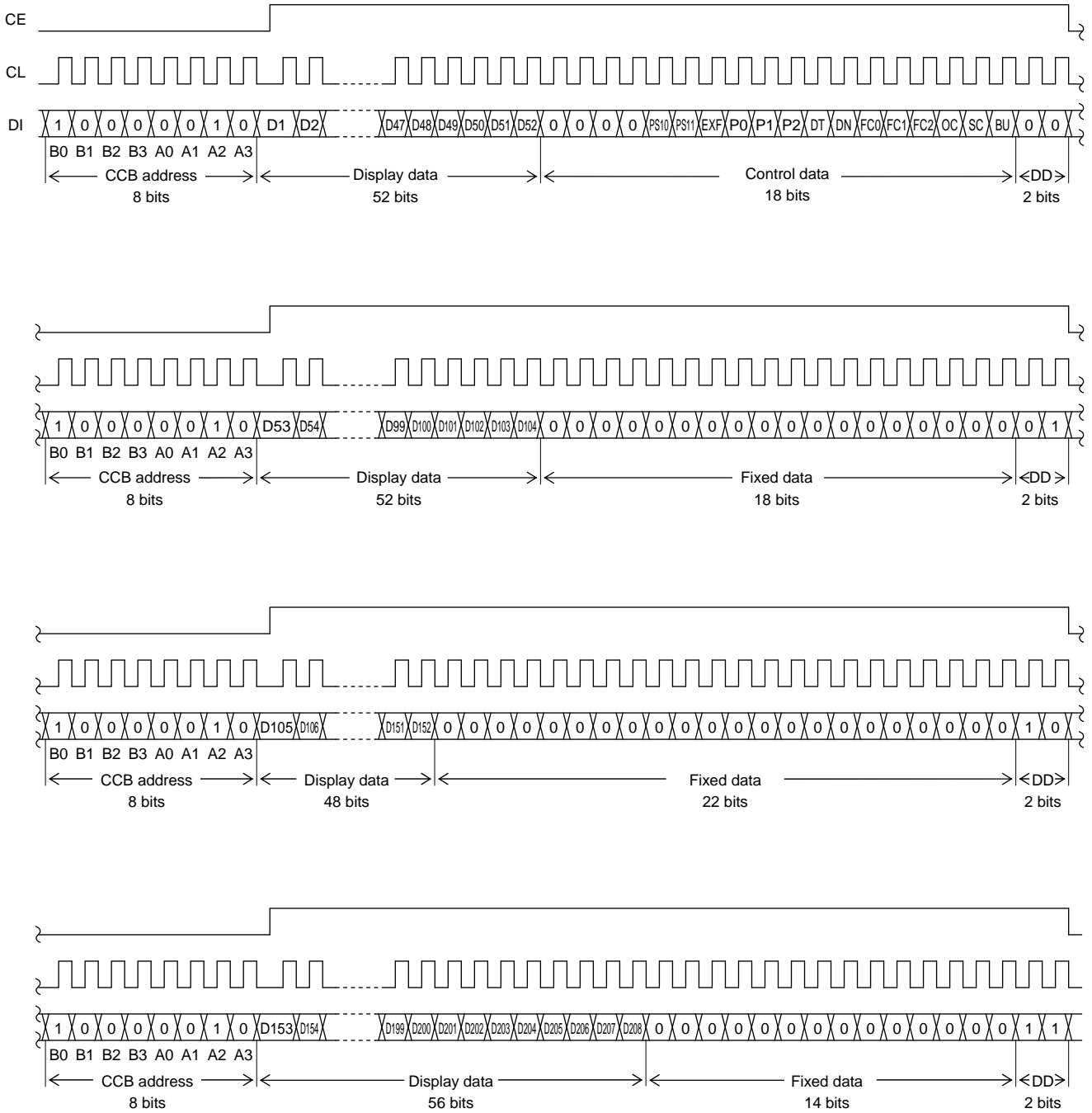
Pin Functions

| Symbol | Pin No. | Function | Active | I/O | Handling when unused |
|------------------------------------|-------------------------|--|---|-------------|----------------------|
| S1/P1 to S4/P4 S5 to S50 S52 | 1 to 4 5 to 50 55 | Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control. | - | O | OPEN |
| COM1 to COM3 COM4/S51 | 54 to 52 51 | Common driver outputs The frame frequency is f_0 [Hz]. The COM4/S51 pin can be used as a segment output in 1/3 duty. | - | O | OPEN |
| S53/OSCI | 60 | Segment output. This pin can also be used as the external clock input pin when the external clock operating mode is selected by control data. | - | I/O | OPEN |
| CE CL DI | 62 63 64 | Serial data transfer inputs. Must be connected to the controller. CE: Chip enable CL: Synchronization clock DI: Transfer data | H  - | I I I | GND |
| $\overline{\text{INH}}$ | 61 | Display off control input <ul style="list-style-type: none"> • $\overline{\text{INH}} = \text{low} (V_{SS})$...Display forced off S1/P1 to S4/P4 = low (V_{SS}) (These pins are forcibly set to the general-purpose output port function and held at the V_{SS} level.) S9 to S50, S52=low (V_{SS}) COM1 to COM3=low (V_{SS}) COM4/S51=low (V_{SS}) S53/OSCI=low (V_{SS}) (This pin is forcibly set to the segment output port function and held at the V_{SS} level.) Stops the internal oscillator. Inhibits external clock input. • $\overline{\text{INH}} = \text{high} (V_{DD})$...Display on Enables the internal oscillator circuit. (Internal oscillator operating mode) Enables external clock input. (External clock operating mode) However, serial data transfer is possible when the display is forced off. | L | I | GND |
| V_{DD1} | 57 | Used to apply the LCD drive 2/3 bias voltage externally. | - | I | OPEN |
| V_{DD2} | 58 | Used to apply the LCD drive 1/3 bias voltage externally. | - | I | OPEN |
| V_{DD} | 56 | Power supply pin. A power voltage of 4.5 to 6.0V must be applied to this pin. | - | - | - |
| V_{SS} | 59 | Ground pin. Must be connected to ground. | - | - | - |

Serial Data Input

1. 1/4 duty

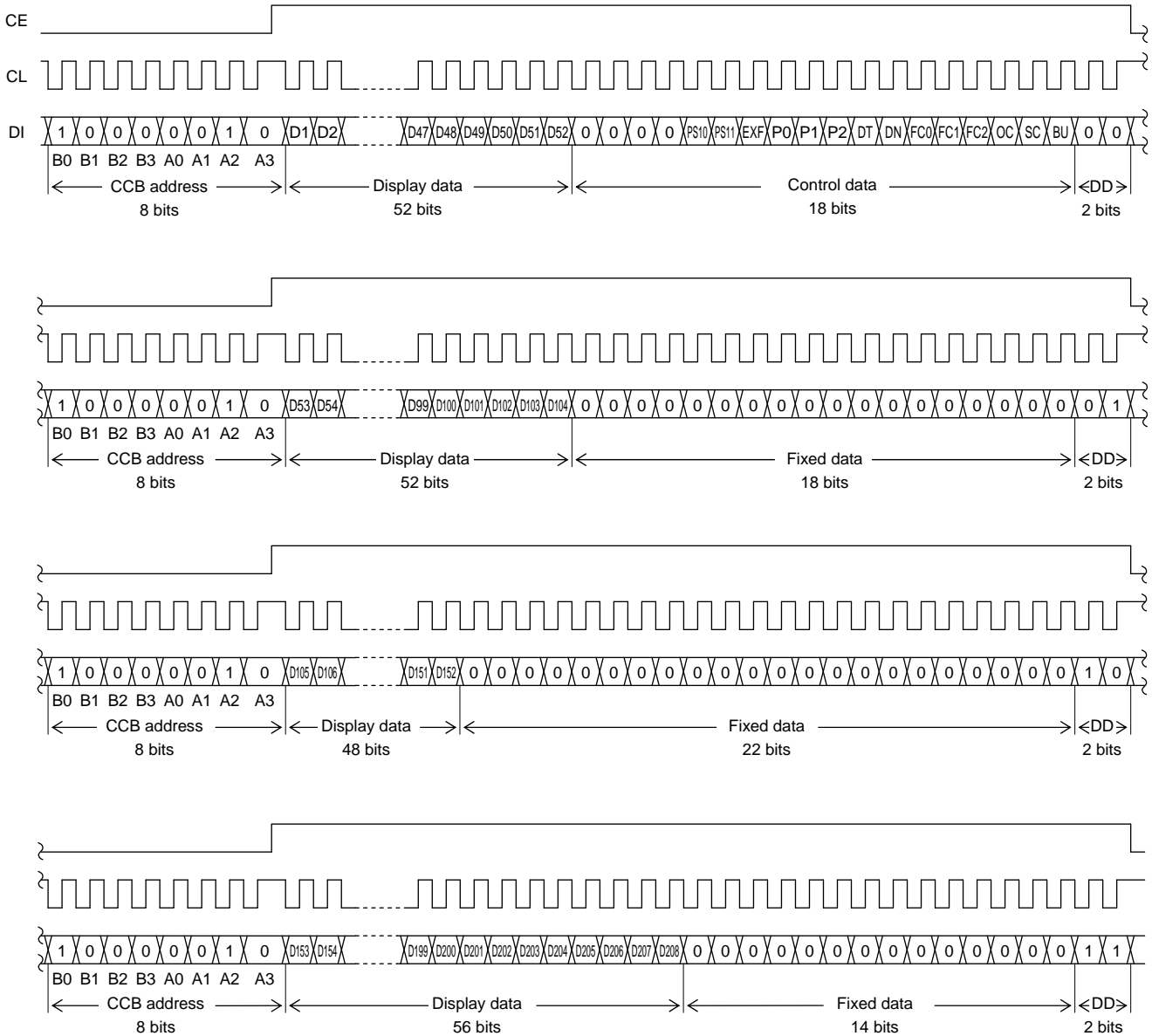
(1) When CL is stopped at the low level



Note: DD is the direction data.

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(2) When CL is stopped at the high level



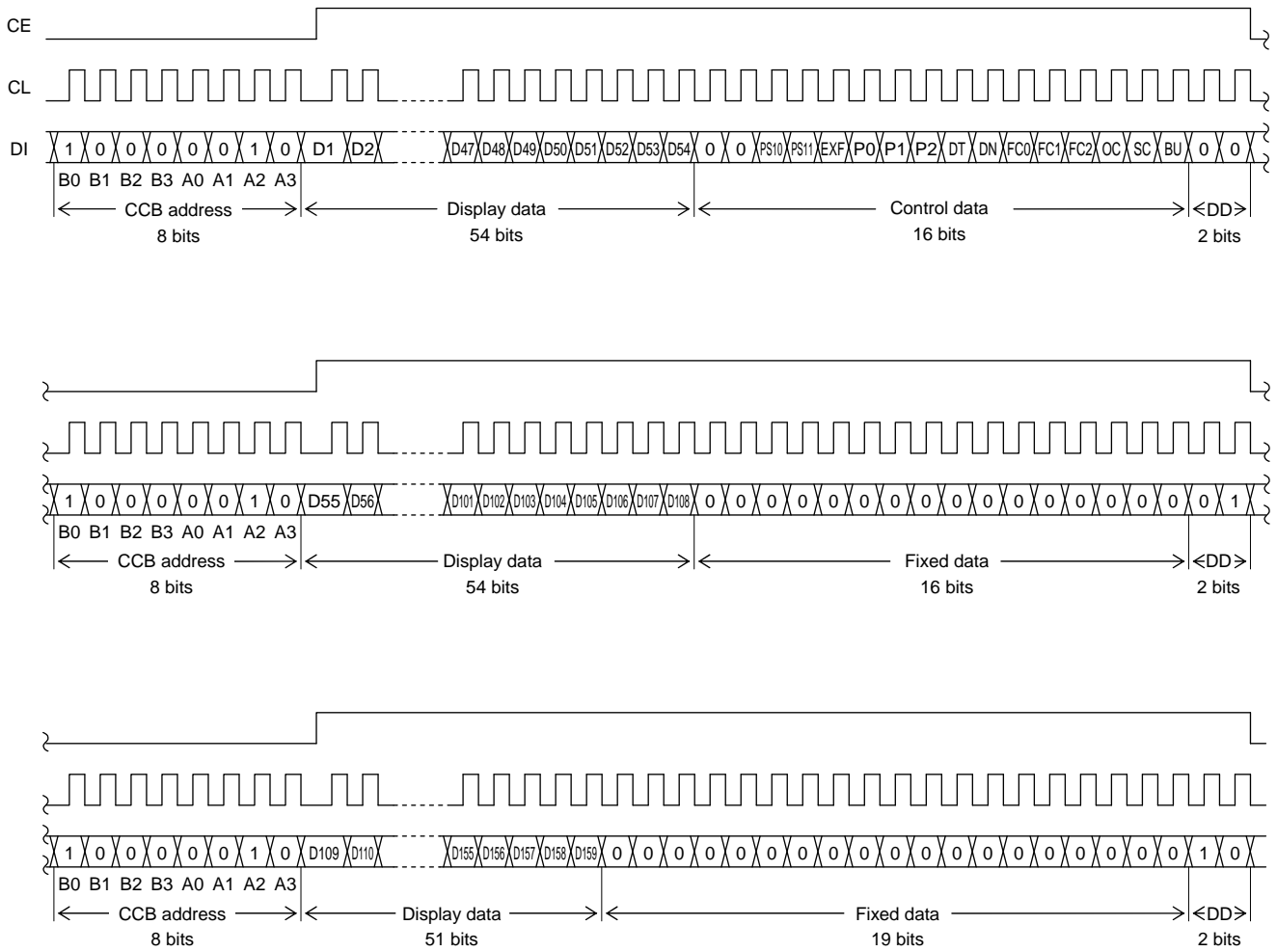
Note: DD is the direction data.

- CCB address "41H"
- D1 to D208 Display data
- PS10, PS11 General-purpose output port (P1) function setting control data
- EXF External clock operating frequency setting control data
- P0 to P2 Segment output port/general-purpose output port switching control data
- DT 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- DN S52 pin and S53/OSCI pin state setting control data
- FC0 to FC2 Common/segment output waveform frame frequency control data
- OC Internal oscillator operating mode/external clock operating mode switching control data
- SC Segment on/off control data
- BU Normal mode/power-saving mode control data

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2. 1/3 duty

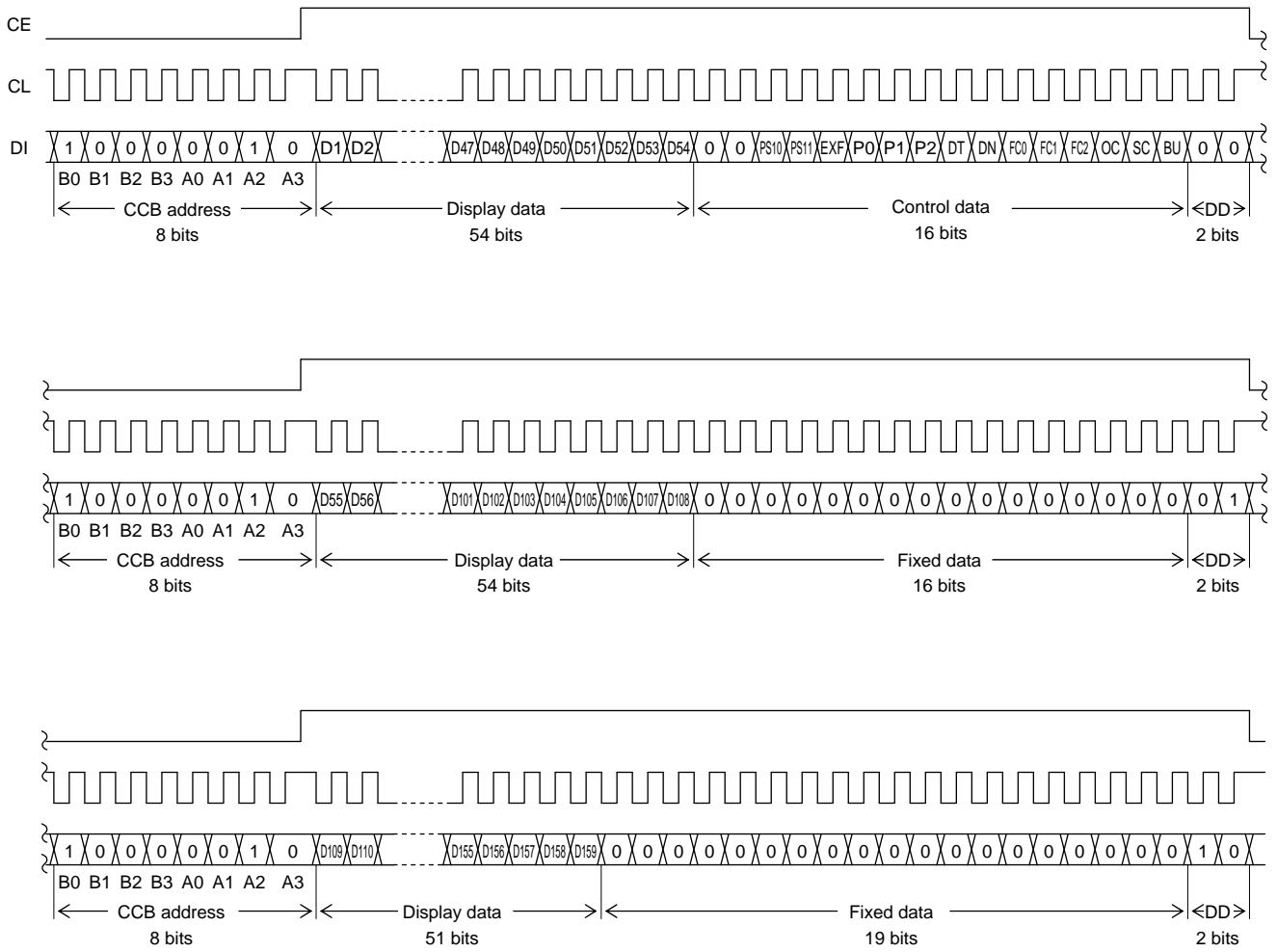
(1) When CL is stopped at the low level



Note: DD is the direction data.

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(2) When CL is stopped at the high level



Note: DD is the direction data.

- CCB address “41H”
- D1 to D159 Display data
- PS10, PS11 General-purpose output port (P1) function setting control data
- EXF External clock operating frequency setting control data
- P0 to P2 Segment output port/general-purpose output port switching control data
- DT 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- DN S52 pin and S53/OSCI pin state setting control data
- FC0 to FC2 Common/segment output waveform frame frequency control data
- OC Internal oscillator operating mode/external clock operating mode switching control data
- SC Segment on/off control data
- BU Normal mode/power-saving mode control data

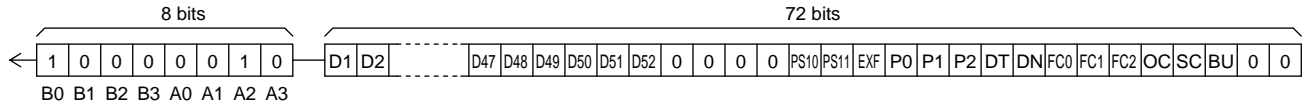
Serial Data Transfer Example

1. 1/4 duty

- When 153 or more segments are used
All 288 bits of serial data must be sent.

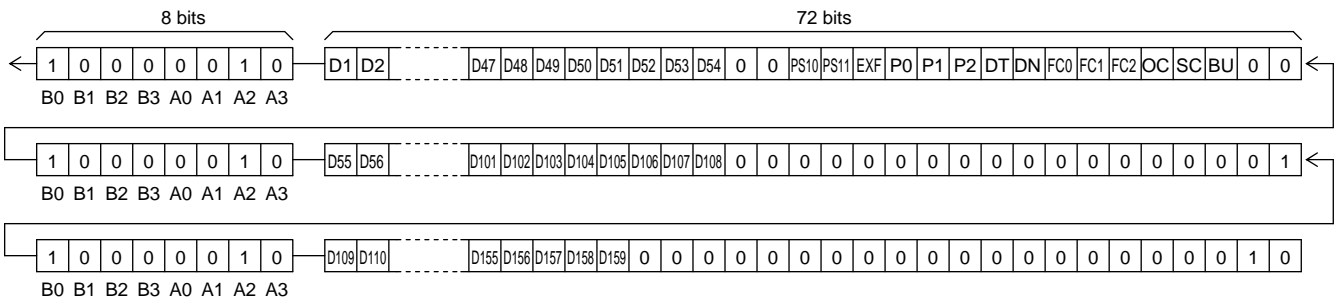


- When fewer than 153 segments are used
Either 72, 144, or 216 bits of serial data must be sent, depending on the number of segments to be used.
However, the serial data shown below (the D1 to D52 display data and the control data) must always be sent.

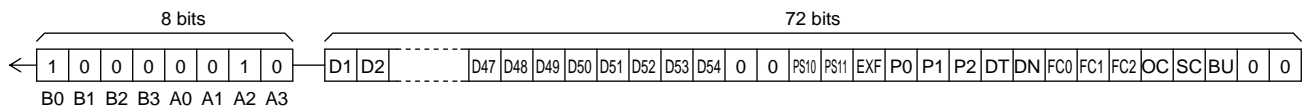


2. 1/3 duty

- When 109 or more segments are used
All 216 bits of serial data must be sent.



- When fewer than 109 segments are used
Either 72, or 144 bits of serial data must be sent, depending on the number of segments to be used.
However, the serial data shown below (the D1 to D54 display data and the control data) must always be sent.



Control Data Functions

(1) PS10 and PS11 ... General-purpose output port (P1) function setting control data

These control data bits set the clock output or general-purpose output function (High or low level output) of the P1 output pin.

| PS10 | PS11 | General-purpose output port (P1) function |
|------|------|---|
| 0 | 0 | General-purpose output function (High or low level output) |
| 1 | 0 | Clock output function (Clock frequency : $f_{osc}/2$, $f_{CK}/2$) |
| 0 | 1 | Clock output function (Clock frequency : $f_{osc}/8$, $f_{CK}/8$) |

Note: When is setting (PS10, PS11)=(1,1), the P1 output pin selects the general-purpose output function (High or low level output).

(2) EXF ... External clock operating frequency setting control data

This control data sets the operating frequency of the external clock which input into the OSCI pin, when the external clock operating mode (OC="1") is set. However, this data is effective only when external clock operating mode (OC="1") is set.

| EXF | External clock operating frequency f_{CK} [kHz] |
|-----|---|
| 0 | $f_{CK1}=300[\text{kHz}]_{\text{typ}}$ |
| 1 | $f_{CK2}=38[\text{kHz}]_{\text{typ}}$ |

(3) P0 to P2 ... Segment output port/general-purpose output port switching control data

These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S4/P4 output pins.

| Control data | | | Output pin state | | | |
|--------------|----|----|------------------|-------|-------|-------|
| P0 | P1 | P2 | S1/P1 | S2/P2 | S3/P3 | S4/P4 |
| 0 | 0 | 0 | S1 | S2 | S3 | S4 |
| 0 | 0 | 1 | P1 | S2 | S3 | S4 |
| 0 | 1 | 0 | P1 | P2 | S3 | S4 |
| 0 | 1 | 1 | P1 | P2 | P3 | S4 |
| 1 | 0 | 0 | P1 | P2 | P3 | P4 |

Note: Sn (n=1 to 4): Segment output ports
Pn (n=1 to 4): General-purpose output ports

Note: When are setting (P0,P1,P2)=(1,0,1), (1,1,0), and (1,1,1), the all P1/S1 to P4/S4 output pins selects the segment output port.

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports.

| Output pin | Correspondence display data | |
|------------|-----------------------------|----------|
| | 1/4 duty | 1/3 duty |
| S1/P1 | D1 | D1 |
| S2/P2 | D5 | D4 |
| S3/P3 | D9 | D7 |
| S4/P4 | D13 | D10 |

For example, if the circuit is operated in 1/4 duty and the S4/P4 output pin is selected to be a general-purpose output port, the S4/P4 output pin will output a high level (V_{DD}) when the display data D13 is 1, and will output a low level (V_{SS}) when D13 is 0.

(4) DT ... 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data

This control data bit selects either 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive.

| DT | Drive scheme | The COM4/S51 pin state |
|----|-------------------------|------------------------|
| 0 | 1/4-duty 1/3-bias drive | COM4 |
| 1 | 1/3-duty 1/3-bias drive | S51 |

Note: COM4: Common output
S51 : Segment output

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(5) DN ... S52 pin and S53/OSCI pin state setting control data

This control data bit sets state of the S52 pin and the S53/OSCI pin.

| DN | Number of display segments | | Pin state | |
|----|----------------------------|--------------------|------------------------|-----------------------------|
| | 1/4 duty | 1/3 duty | S52 | S53/OSCI |
| 0 | Up to 200 segments | Up to 153 segments | "L" (V _{SS}) | "L" (V _{SS})/OSCI |
| 1 | Up to 208 segments | Up to 159 segments | S52 | S53/OSCI |

Note: "L" (V_{SS}) : Low (V_{SS}) level output
 S52 : Segment output
 "L" (V_{SS})/OSCI : Low (V_{SS}) level output in internal oscillator operating mode (OC=0)
 : External clock input in external clock operating mode (OC=1)
 S53/OSCI : Segment output in internal oscillator operating mode (OC=0)
 External clock input in external clock operating mode (OC=1)

(6) FC0 to FC2 ... Common/segment output waveform frame frequency control data

These control data bits set the frame frequency of the common and segment output waveforms.

| Control data | | | Frame frequency fo[Hz] | | |
|--------------|-----|-----|--|--|---|
| FC0 | FC1 | FC2 | Internal oscillator operating mode | External clock operating mode | External clock operating mode |
| | | | (The control data OC is 0, fosc=300[kHz]typ) | (The control data OC is 1 and EXF is 0, f _{CK1} =300[kHz]typ) | (The control data OC is 1 and EXF is 1, f _{CK2} =38[kHz]typ) |
| 0 | 0 | 0 | fosc/6144 | f _{CK1} /6144 | f _{CK2} /768 |
| 0 | 0 | 1 | fosc/4608 | f _{CK1} /4608 | f _{CK2} /576 |
| 0 | 1 | 0 | fosc/3072 | f _{CK1} /3072 | f _{CK2} /384 |
| 0 | 1 | 1 | fosc/2304 | f _{CK1} /2304 | f _{CK2} /288 |
| 1 | 0 | 0 | fosc/1536 | f _{CK1} /1536 | f _{CK2} /192 |
| 1 | 0 | 1 | fosc/1152 | f _{CK1} /1152 | f _{CK2} /144 |
| 1 | 1 | 0 | fosc/768 | f _{CK1} /768 | f _{CK2} /96 |

Note: When is setting (FC0,FC1,FC2)=(1,1,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,1,0) setting (fosc/3072, f_{CK1}/3072, f_{CK2}/384).

(7) OC ... Internal oscillator operating mode/external clock operating mode switching control data

This control data bit selects either the internal oscillator operating mode or external clock operating mode.

| OC | Fundamental clock operating mode | I/O pin (S53/OSCI) state |
|----|------------------------------------|--------------------------|
| 0 | Internal oscillator operating mode | S53 |
| 1 | External clock operating mode | OSCI |

Note: S53: Segment output
 OSCI: External clock input

(8) SC ... Segment on/off control data

This control data bit controls the on/off state of the segments.

| SC | Display state |
|----|---------------|
| 0 | On |
| 1 | Off |

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

(9) BU ... Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

| BU | Mode |
|----|---|
| 0 | Normal mode |
| 1 | Power saving mode In this mode, the internal oscillator circuit stops oscillation (the S53/OSCI pin is configured for segment output) if the IC is in the internal oscillator operating mode (OC=0) and the IC stops receiving external clock signals (the S53/OSCI pin is configured for external clock input) if the IC is in the external clock operating mode (OC=1). The common and segment output pins go to the V _{SS} level. However, the S1/P1 to S4/P4 output pins can be used as general-purpose output ports under the control of the data bits P0 to P2. (The general-purpose output port P1 can not be used as clock output). |

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Display Data and Output Pin Correspondence (1/4 Duty)

| Output pin | COM1 | COM2 | COM3 | COM4 | Output pin | COM1 | COM2 | COM3 | COM4 |
|------------|------|------|------|------|------------|------|------|------|------|
| S1/P1 | D1 | D2 | D3 | D4 | S27 | D105 | D106 | D107 | D108 |
| S2/P2 | D5 | D6 | D7 | D8 | S28 | D109 | D110 | D111 | D112 |
| S3/P3 | D9 | D10 | D11 | D12 | S29 | D113 | D114 | D115 | D116 |
| S4/P4 | D13 | D14 | D15 | D16 | S30 | D117 | D118 | D119 | D120 |
| S5 | D17 | D18 | D19 | D20 | S31 | D121 | D122 | D123 | D124 |
| S6 | D21 | D22 | D23 | D24 | S32 | D125 | D126 | D127 | D128 |
| S7 | D25 | D26 | D27 | D28 | S33 | D129 | D130 | D131 | D132 |
| S8 | D29 | D30 | D31 | D32 | S34 | D133 | D134 | D135 | D136 |
| S9 | D33 | D34 | D35 | D36 | S35 | D137 | D138 | D139 | D140 |
| S10 | D37 | D38 | D39 | D40 | S36 | D141 | D142 | D143 | D144 |
| S11 | D41 | D42 | D43 | D44 | S37 | D145 | D146 | D147 | D148 |
| S12 | D45 | D46 | D47 | D48 | S38 | D149 | D150 | D151 | D152 |
| S13 | D49 | D50 | D51 | D52 | S39 | D153 | D154 | D155 | D156 |
| S14 | D53 | D54 | D55 | D56 | S40 | D157 | D158 | D159 | D160 |
| S15 | D57 | D58 | D59 | D60 | S41 | D161 | D162 | D163 | D164 |
| S16 | D61 | D62 | D63 | D64 | S42 | D165 | D166 | D167 | D168 |
| S17 | D65 | D66 | D67 | D68 | S43 | D169 | D170 | D171 | D172 |
| S18 | D69 | D70 | D71 | D72 | S44 | D173 | D174 | D175 | D176 |
| S19 | D73 | D74 | D75 | D76 | S45 | D177 | D178 | D179 | D180 |
| S20 | D77 | D78 | D79 | D80 | S46 | D181 | D182 | D183 | D184 |
| S21 | D81 | D82 | D83 | D84 | S47 | D185 | D186 | D187 | D188 |
| S22 | D85 | D86 | D87 | D88 | S48 | D189 | D190 | D191 | D192 |
| S23 | D89 | D90 | D91 | D92 | S49 | D193 | D194 | D195 | D196 |
| S24 | D93 | D94 | D95 | D96 | S50 | D197 | D198 | D199 | D200 |
| S25 | D97 | D98 | D99 | D100 | S52 | D201 | D202 | D203 | D204 |
| S26 | D101 | D102 | D103 | D104 | S53/OSCI | D205 | D206 | D207 | D208 |

Note: This table assumes that pins S1/P1 to S4/P4 and S53/OSCI are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

| Display data | | | | Output pin (S21) state |
|--------------|-----|-----|-----|---|
| D81 | D82 | D83 | D84 | |
| 0 | 0 | 0 | 0 | The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off. |
| 0 | 0 | 0 | 1 | The LCD segment corresponding to COM4 is on. |
| 0 | 0 | 1 | 0 | The LCD segment corresponding to COM3 is on. |
| 0 | 0 | 1 | 1 | The LCD segments corresponding to COM3 and COM4 are on. |
| 0 | 1 | 0 | 0 | The LCD segment corresponding to COM2 is on. |
| 0 | 1 | 0 | 1 | The LCD segments corresponding to COM2 and COM4 are on. |
| 0 | 1 | 1 | 0 | The LCD segments corresponding to COM2 and COM3 are on. |
| 0 | 1 | 1 | 1 | The LCD segments corresponding to COM2, COM3, and COM4 are on. |
| 1 | 0 | 0 | 0 | The LCD segment corresponding to COM1 is on. |
| 1 | 0 | 0 | 1 | The LCD segments corresponding to COM1 and COM4 are on. |
| 1 | 0 | 1 | 0 | The LCD segments corresponding to COM1 and COM3 are on. |
| 1 | 0 | 1 | 1 | The LCD segments corresponding to COM1, COM3, and COM4 are on. |
| 1 | 1 | 0 | 0 | The LCD segments corresponding to COM1 and COM2 are on. |
| 1 | 1 | 0 | 1 | The LCD segments corresponding to COM1, COM2, and COM4 are on. |
| 1 | 1 | 1 | 0 | The LCD segments corresponding to COM1, COM2, and COM3 are on. |
| 1 | 1 | 1 | 1 | The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on. |

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Display Data and Output Pin Correspondence (1/3 Duty)

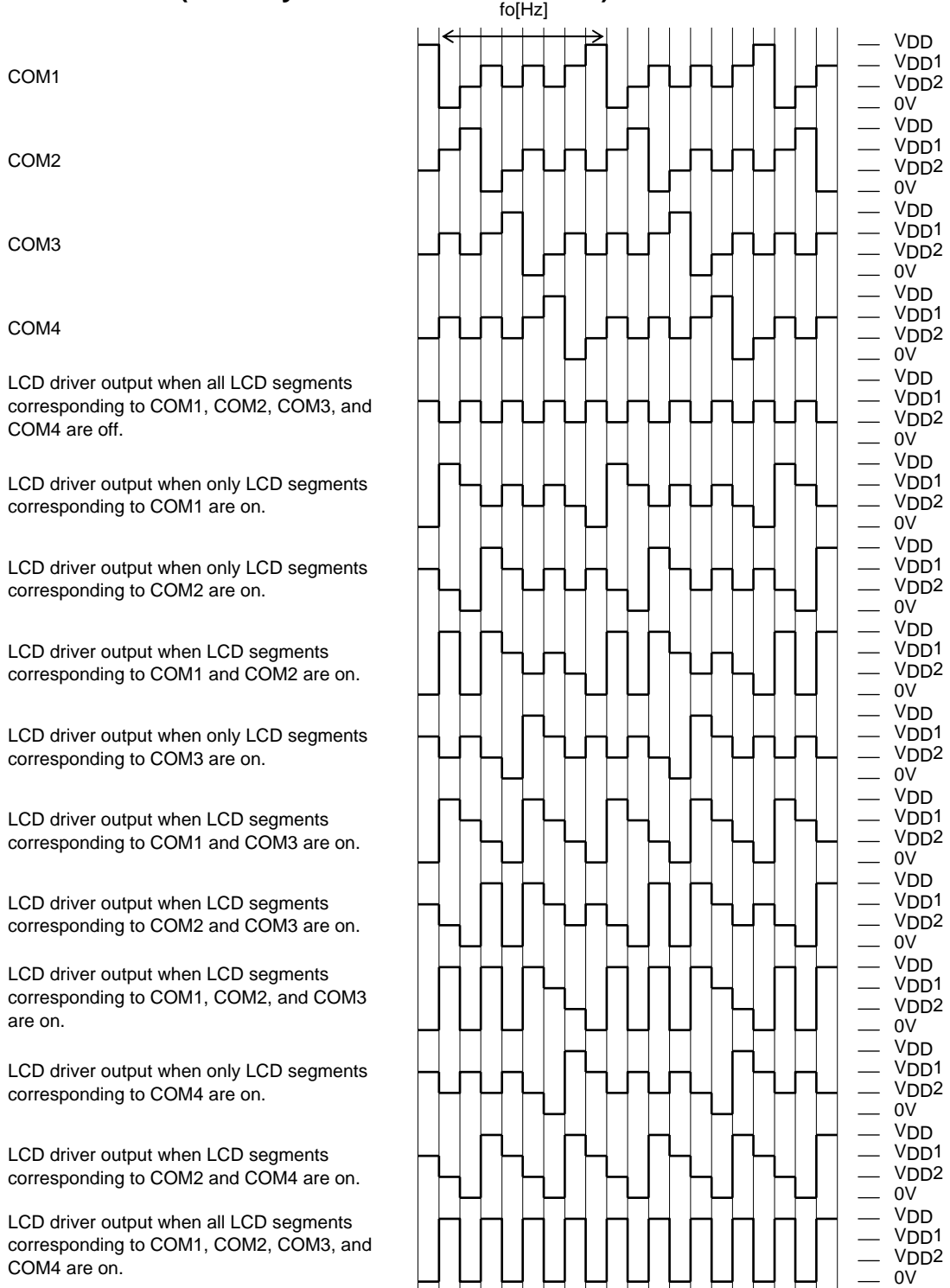
| Output pin | COM1 | COM2 | COM3 | Output pin | COM1 | COM2 | COM3 |
|------------|------|------|------|------------|------|------|------|
| S1/P1 | D1 | D2 | D3 | S28 | D82 | D83 | D84 |
| S2/P2 | D4 | D5 | D6 | S29 | D85 | D86 | D87 |
| S3/P3 | D7 | D8 | D9 | S30 | D88 | D89 | D90 |
| S4/P4 | D10 | D11 | D12 | S31 | D91 | D92 | D93 |
| S5 | D13 | D14 | D15 | S32 | D94 | D95 | D96 |
| S6 | D16 | D17 | D18 | S33 | D97 | D98 | D99 |
| S7 | D19 | D20 | D21 | S34 | D100 | D101 | D102 |
| S8 | D22 | D23 | D24 | S35 | D103 | D104 | D105 |
| S9 | D25 | D26 | D27 | S36 | D106 | D107 | D108 |
| S10 | D28 | D29 | D30 | S37 | D109 | D110 | D111 |
| S11 | D31 | D32 | D33 | S38 | D112 | D113 | D114 |
| S12 | D34 | D35 | D36 | S39 | D115 | D116 | D117 |
| S13 | D37 | D38 | D39 | S40 | D118 | D119 | D120 |
| S14 | D40 | D41 | D42 | S41 | D121 | D122 | D123 |
| S15 | D43 | D44 | D45 | S42 | D124 | D125 | D126 |
| S16 | D46 | D47 | D48 | S43 | D127 | D128 | D129 |
| S17 | D49 | D50 | D51 | S44 | D130 | D131 | D132 |
| S18 | D52 | D53 | D54 | S45 | D133 | D134 | D135 |
| S19 | D55 | D56 | D57 | S46 | D136 | D137 | D138 |
| S20 | D58 | D59 | D60 | S47 | D139 | D140 | D141 |
| S21 | D61 | D62 | D63 | S48 | D142 | D143 | D144 |
| S22 | D64 | D65 | D66 | S49 | D145 | D146 | D147 |
| S23 | D67 | D68 | D69 | S50 | D148 | D149 | D150 |
| S24 | D70 | D71 | D72 | S51/COM4 | D151 | D152 | D153 |
| S25 | D73 | D74 | D75 | S52 | D154 | D155 | D156 |
| S26 | D76 | D77 | D78 | S53/OSCI | D157 | D158 | D159 |
| S27 | D79 | D80 | D81 | | | | |

Note: This table assumes that pins S1/P1 to S4/P4, S51/COM4, and S53/OSCI are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

| Display data | | | Output pin (S21) state |
|--------------|-----|-----|---|
| D61 | D62 | D63 | |
| 0 | 0 | 0 | The LCD segments corresponding to COM1, COM2, and COM3 are off. |
| 0 | 0 | 1 | The LCD segment corresponding to COM3 is on. |
| 0 | 1 | 0 | The LCD segment corresponding to COM2 is on. |
| 0 | 1 | 1 | The LCD segments corresponding to COM2 and COM3 are on. |
| 1 | 0 | 0 | The LCD segment corresponding to COM1 is on. |
| 1 | 0 | 1 | The LCD segments corresponding to COM1 and COM3 are on. |
| 1 | 1 | 0 | The LCD segments corresponding to COM1 and COM2 are on. |
| 1 | 1 | 1 | The LCD segments corresponding to COM1, COM2, and COM3 are on. |

Output Waveforms (1/4-Duty 1/3-Bias Drive Scheme)

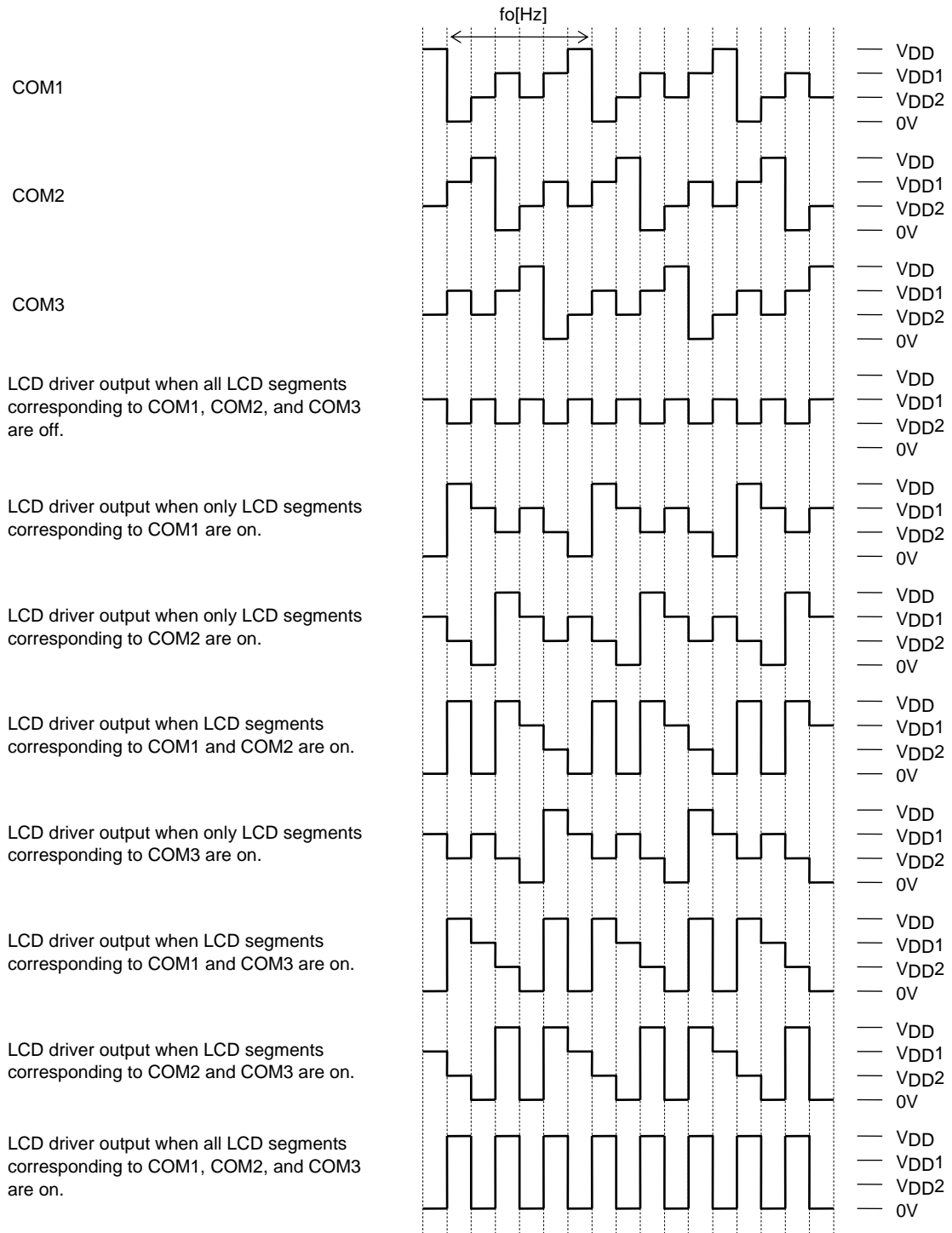


| Control data | | | Frame frequency f_o [Hz] | | |
|--------------|-----|-----|---|---|--|
| FC0 | FC1 | FC2 | Internal oscillator operating mode (The control data OC is 0, $f_{osc}=300$ [kHz]typ) | External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK1}=300$ [kHz]typ) | External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK2}=38$ [kHz]typ) |
| 0 | 0 | 0 | $f_{osc}/6144$ | $f_{CK1}/6144$ | $f_{CK2}/768$ |
| 0 | 0 | 1 | $f_{osc}/4608$ | $f_{CK1}/4608$ | $f_{CK2}/576$ |
| 0 | 1 | 0 | $f_{osc}/3072$ | $f_{CK1}/3072$ | $f_{CK2}/384$ |
| 0 | 1 | 1 | $f_{osc}/2304$ | $f_{CK1}/2304$ | $f_{CK2}/288$ |
| 1 | 0 | 0 | $f_{osc}/1536$ | $f_{CK1}/1536$ | $f_{CK2}/192$ |
| 1 | 0 | 1 | $f_{osc}/1152$ | $f_{CK1}/1152$ | $f_{CK2}/144$ |
| 1 | 1 | 0 | $f_{osc}/768$ | $f_{CK1}/768$ | $f_{CK2}/96$ |

Note: When is setting (FC0,FC1,FC2)=(1,1,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,1,0) setting ($f_{osc}/3072$, $f_{CK1}/3072$, $f_{CK2}/384$).

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Output waveforms (1/3-Duty 1/3-Bias Drive Scheme)



| Control data | | | Frame frequency f_o [Hz] | | |
|--------------|-----|-----|---|---|--|
| FC0 | FC1 | FC2 | Internal oscillator operating mode (The control data OC is 0, $f_{osc}=300$ [kHz]typ) | External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK1}=300$ [kHz]typ) | External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK2}=38$ [kHz]typ) |
| 0 | 0 | 0 | $f_{osc}/6144$ | $f_{CK1}/6144$ | $f_{CK2}/768$ |
| 0 | 0 | 1 | $f_{osc}/4608$ | $f_{CK1}/4608$ | $f_{CK2}/576$ |
| 0 | 1 | 0 | $f_{osc}/3072$ | $f_{CK1}/3072$ | $f_{CK2}/384$ |
| 0 | 1 | 1 | $f_{osc}/2304$ | $f_{CK1}/2304$ | $f_{CK2}/288$ |
| 1 | 0 | 0 | $f_{osc}/1536$ | $f_{CK1}/1536$ | $f_{CK2}/192$ |
| 1 | 0 | 1 | $f_{osc}/1152$ | $f_{CK1}/1152$ | $f_{CK2}/144$ |
| 1 | 1 | 0 | $f_{osc}/768$ | $f_{CK1}/768$ | $f_{CK2}/96$ |

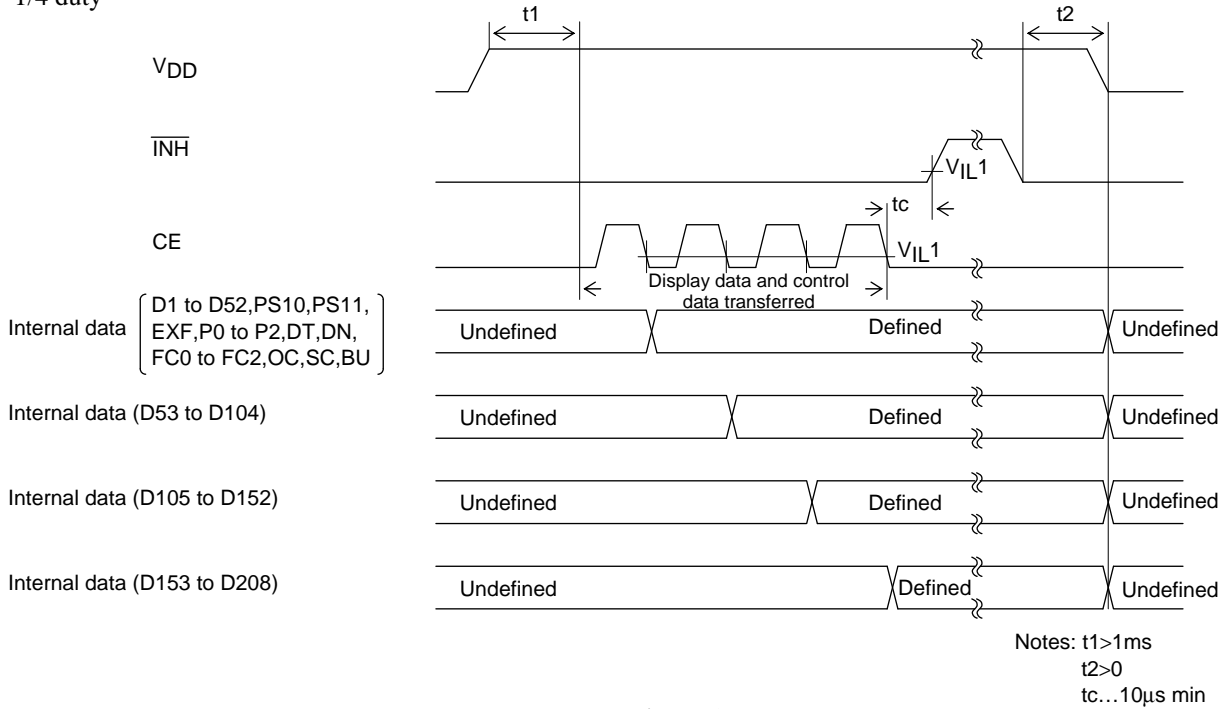
Note: When is setting (FC0,FC1,FC2)=(1,1,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,1,0) setting ($f_{osc}/3072$, $f_{CK1}/3072$, $f_{CK2}/384$).

Display Control and the $\overline{\text{INH}}$ Pin

Since the LSI internal data (1/4 duty : the display data D1 to D208 and the control data, 1/3 duty : the display data D1 to D159 and the control data) is undefined when power is first applied, applications should set the $\overline{\text{INH}}$ pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S4/P4, S5 to S50, COM1 to COM3, COM4/S51, S52, and S53/OSCI pins to the VSS level.) and during this period send serial data from the controller. The controller should then set the $\overline{\text{INH}}$ pin high after the data transfer has completed. This procedure prevents meaningless display at power on.

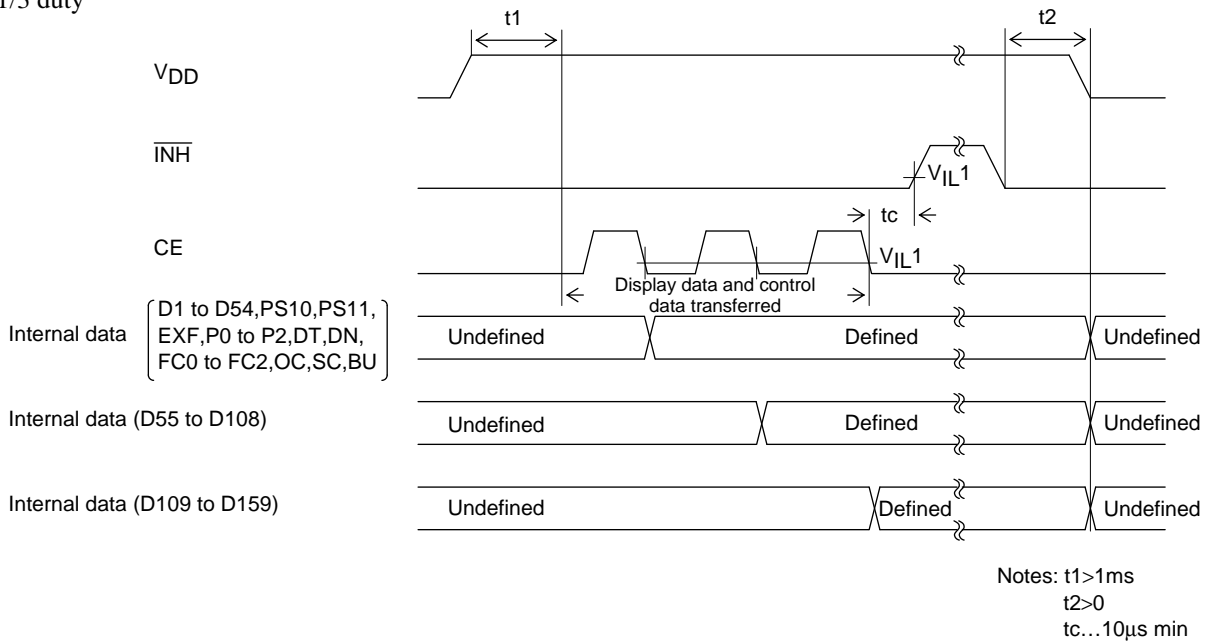
(See Figure 5 and Figure 6.)

• 1/4 duty



[Figure 5]

• 1/3 duty



[Figure 6]

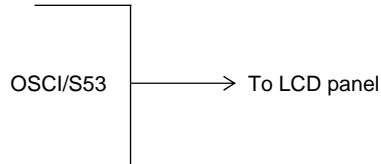
Notes on Controller Transfer of Display Data

When using the LC75829 in 1/4 duty, applications transfer the display data (D1 to D208) in four operations, and in 1/3 duty, they transfer the display data (D1 to D159) in three operations. In either case, applications should transfer all of the display data within 30 ms to maintain the quality of displayed image.

S53/OSCI Pin Peripheral Circuit

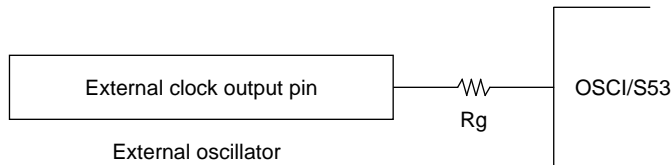
(1) Internal oscillator operating mode (control data OC=0)

Connect the S53/OSCI pin to the LCD panel when the internal oscillator operating mode is selected.



(2) External clock operating mode (control data OC=1)

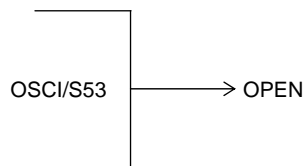
When the external clock operating mode is selected, insert a current protection resistor R_g (2.2 to 22k Ω) between the S53/OSCI pin and external clock output pin (external oscillator). Determine the value of the resistance according to the allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.



Note: Allowable current value at external clock output pin $> \frac{V_{DD}}{R_g}$

(3) Unused pin treatment

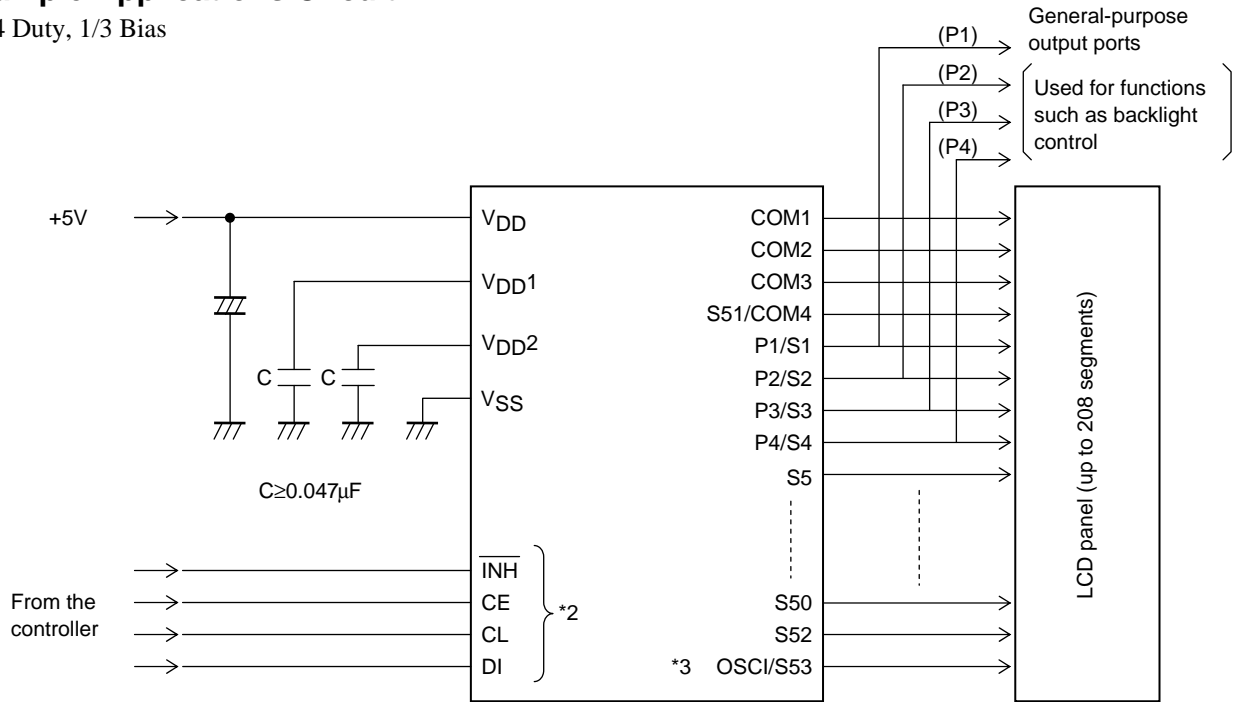
When the S53/OSCI pin is not to be used, select the internal oscillator operating mode (setting control data OC to 0) to keep the pin open.



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Sample Applications Circuit1

1/4 Duty, 1/3 Bias

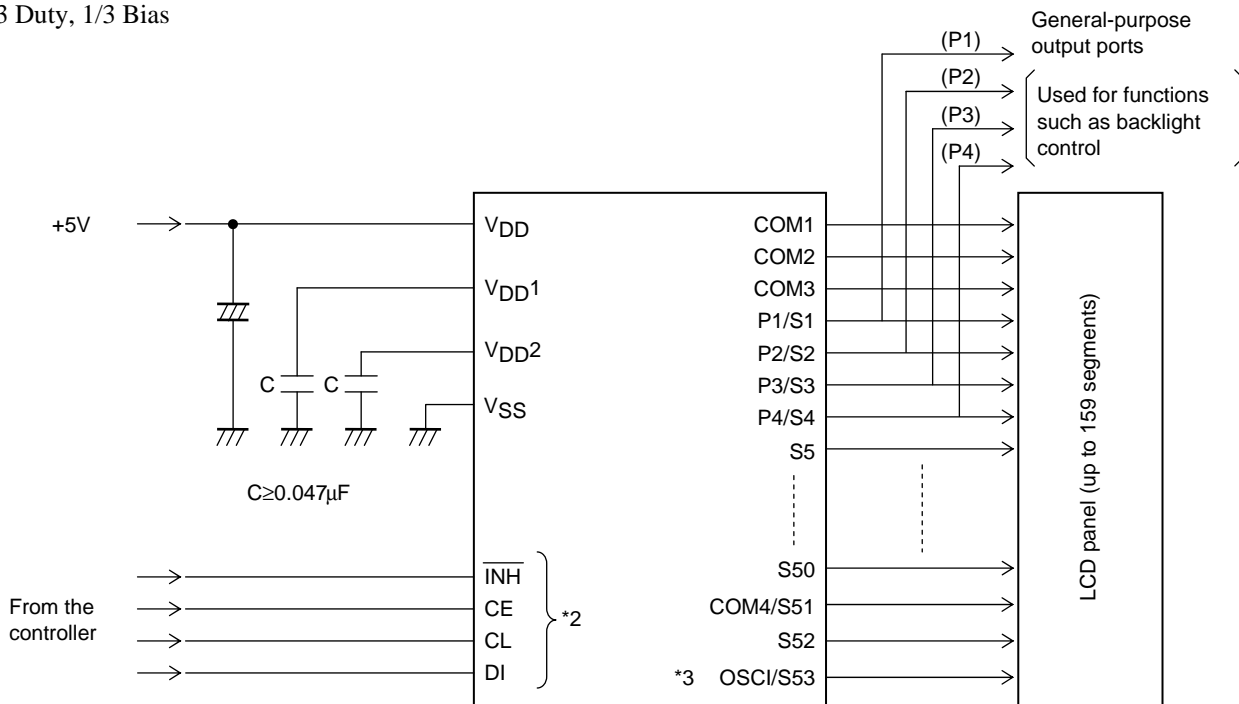


*2 The pins to be connected to the controller (CE, CL, DI, $\overline{\text{INH}}$) can handle 3.3V or 5V.

*3 Connect the S53/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor R_g (2.2 to 22kΩ) between the S53/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode (see "S53/OSCI Pin Peripheral Circuit").

Sample Application Circuit 2

1/3 Duty, 1/3 Bias



*2 The pins to be connected to the controller (CE, CL, DI, $\overline{\text{INH}}$) can handle 3.3V or 5V.

*3 Connect the S53/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor R_g (2.2 to 22kΩ) between the S53/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode (see "S53/OSCI Pin Peripheral Circuit").

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