

LC75873NE

LC75873NW

CMOS LSI

1/3-Duty General-Purpose LCD Display Driver

Overview

The LC75873NE and LC75873NW are 1/3-duty general-purpose microprocessor-controlled LCD driver that can be used in applications such as frequency display in products with electronic tuning. In addition to being able to drive up to 204 segments directly, the LC75873NE and LC75873NW can also control up to 4 general-purpose output ports.

Features

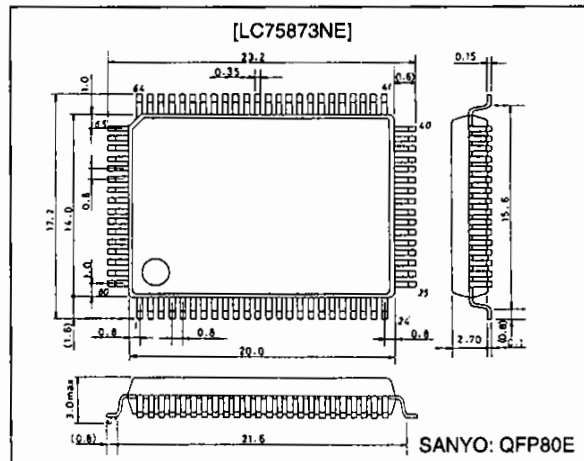
- Support for 1/3-duty 1/2-bias or 1/3-duty 1/3-bias drive techniques under serial data control (up to 204 segments)
- Serial data input supports CCB format communication with the system controller.
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port functions.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- The $\overline{\text{INH}}$ pin allows the display to be forced to the off state.
- RC oscillator circuit

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Package Dimensions

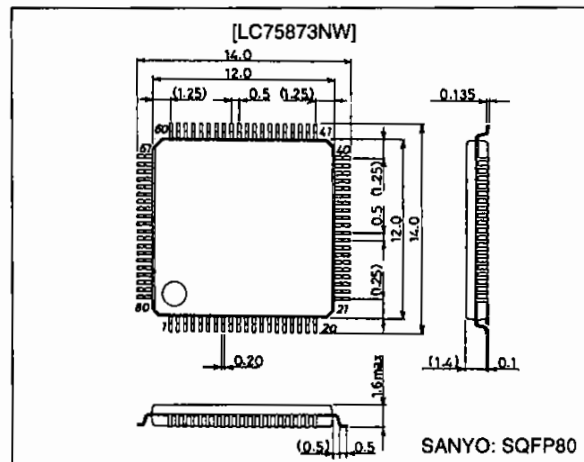
unit: mm

3174-QFP80E

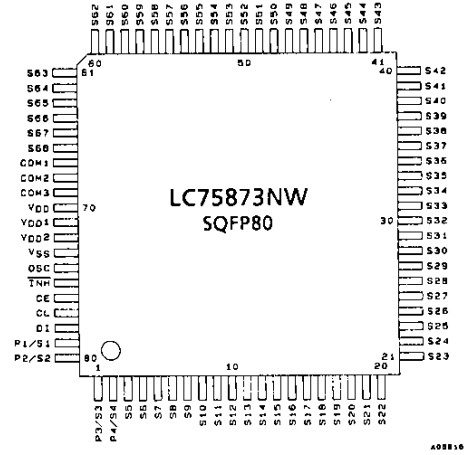
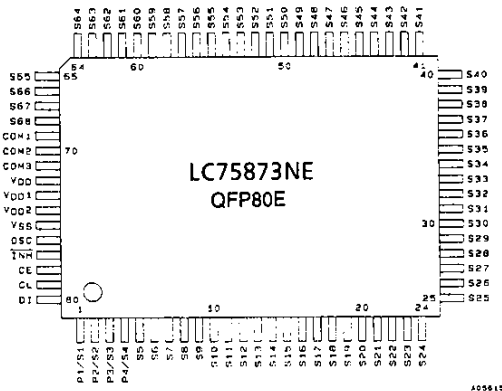


unit: mm

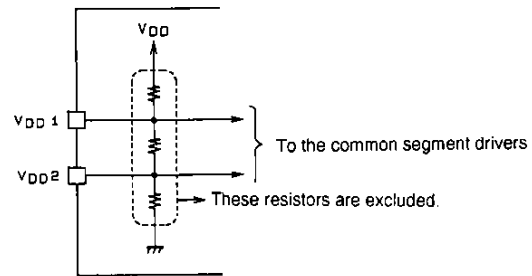
3220-SQFP80



Pin Assignments



Top view



A04171

Figure 1

Specifications

Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|--|-------------------------------|------|
| Maximum supply voltage | V _{DD max} | V _{DD} | -0.3 to +7.0 | V |
| Input voltage | V _{IN1} | CE, CL, DI, \overline{INH} | -0.3 to +7.0 | V |
| | V _{IN2} | OSC, V _{DD1} , V _{DD2} | -0.3 to V _{DD} + 0.3 | V |
| Output voltage | V _{OUT} | OSC, S1 to S68, COM1 to COM3, P1 or P4 | -0.3 to V _{DD} + 0.3 | V |
| Output current | I _{OUT1} | S1 to S68 | 300 | μA |
| | I _{OUT2} | COM1 to COM3 | 3 | mA |
| | I _{OUT3} | P1 to P4 | 5 | mA |
| Allowable power dissipation | P _{d max} | Ta = 85°C | 200 | mW |
| Operating temperature | T _{opr} | | -40 to +85 | °C |
| Storage temperature | T _{stg} | | -55 to +125 | °C |

LC75873NE, 75873NW

Allowable Operating Ranges at Ta = -40 to +85°C, VSS = 0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|----------------------------------|------------------|----------------------|---------------------|---------------------|---------------------|------|
| Supply voltage | V _{DD} | V _{DD} | 3.0 | | 6.0 | V |
| Input voltage | V _{DD1} | V _{DD1} | | 2/3 V _{DD} | V _{DD} | V |
| | V _{DD2} | V _{DD2} | | 1/3 V _{DD} | V _{DD} | V |
| Input high-level voltage | V _{IH} | CE, CL, DI, INH | 0.8 V _{DD} | | 6.0 | V |
| Input low-level voltage | V _{IL} | CE, CL, DI, INH | 0 | | 0.2 V _{DD} | V |
| Recommended external resistance | R _{OSC} | OSC | | 180 | | kΩ |
| Recommended external capacitance | C _{OSC} | OSC | | 220 | | pF |
| Guaranteed oscillation range | f _{OSC} | OSC | 19 | 38 | 76 | kHz |
| Data setup time | t _{ds} | CL, DI: Figure 2 | 160 | | | ns |
| Data hold time | t _{dh} | CL, DI: Figure 2 | 160 | | | ns |
| CE wait time | t _{cp} | CE, CL: Figure 2 | 160 | | | ns |
| CE setup time | t _{cs} | CE, CL: Figure 2 | 160 | | | ns |
| CE hold time | t _{ch} | CE, CL: Figure 2 | 160 | | | ns |
| High-level clock pulse width | t _{gH} | CL: Figure 2 | 160 | | | ns |
| Low-level clock pulse width | t _{gL} | CL: Figure 2 | 160 | | | ns |
| Rise time | t _r | CE, CL, DI: Figure 2 | | 160 | | ns |
| Fall time | t _f | CE, CL, DI: Figure 2 | | 160 | | ns |
| INH switching time | t _c | INH, CE: Figure 3 | 10 | | | μs |


Electrical Characteristics for the Allowable Operating Ranges

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|------------------------------|-------------------|--|---------------------------|---------------------|---------------------------|------|
| Hysteresis | V _H | CE, CL, DI, INH | | 0.1 V _{DD} | | V |
| Input high-level current | I _{IH} | CE, CL, DI, INH: V _I = 6.0 V | | | 5.0 | μA |
| Input low-level current | I _{IL} | CE, CL, DI, INH: V _I = 0 V | -5.0 | | | μA |
| Output high-level voltage | V _{OH1} | S1 to S68: I _O = -20 μA | V _{DD} - 1.0 | | | V |
| | V _{OH2} | COM1 to COM3: I _O = -100 μA | V _{DD} - 1.0 | | | V |
| | V _{OH3} | P1 to P4: I _O = -1 mA | V _{DD} - 1.0 | | | V |
| Output low-level voltage | V _{OL1} | S1 to S68: I _O = 20 μA | | | 1.0 | V |
| | V _{OL2} | COM1 to COM3: I _O = 100 μA | | | 1.0 | V |
| | V _{OL3} | P1 to P4: I _O = 1 mA | | | 1.0 | V |
| Output middle-level voltage* | V _{MID1} | COM1 to COM3: 1/2 bias, I _O = ±100 μA | 1/2 V _{DD} - 1.0 | | 1/2 V _{DD} + 1.0 | V |
| | V _{MID2} | S1 to S68: 1/3 bias, I _O = ±20 μA | 2/3 V _{DD} - 1.0 | | 2/3 V _{DD} + 1.0 | V |
| | V _{MID3} | S1 to S68: 1/3 bias, I _O = ±20 μA | 1/3 V _{DD} - 1.0 | | 1/3 V _{DD} + 1.0 | V |
| | V _{MID4} | COM1 to COM3: 1/3 bias, I _O = ±100 μA | 2/3 V _{DD} - 1.0 | | 2/3 V _{DD} + 1.0 | V |
| | V _{MID5} | COM1 to COM3: 1/3 bias, I _O = ±100 μA | 1/3 V _{DD} - 1.0 | | 1/3 V _{DD} + 1.0 | V |
| Oscillator frequency | f _{OSC} | OSC: R _{OSC} = 180 kΩ, C _{OSC} = 220 pF | 30.4 | 38 | 45.6 | kHz |
| Current drain | I _{DD1} | Power-saving mode | | | 5 | μA |
| | I _{DD2} | V _{DD} = 6.0 V, outputs open, 1/2 bias, f _{OSC} = 38 kHz | | 300 | 600 | μA |
| | I _{DD3} | V _{DD} = 6.0 V, outputs open, 1/3 bias, f _{OSC} = 38 kHz | | 250 | 500 | μA |

Note: * Excluding the bias voltage generation divider resistors built in the V_{DD1} and V_{DD2}. (See Figure 1.)

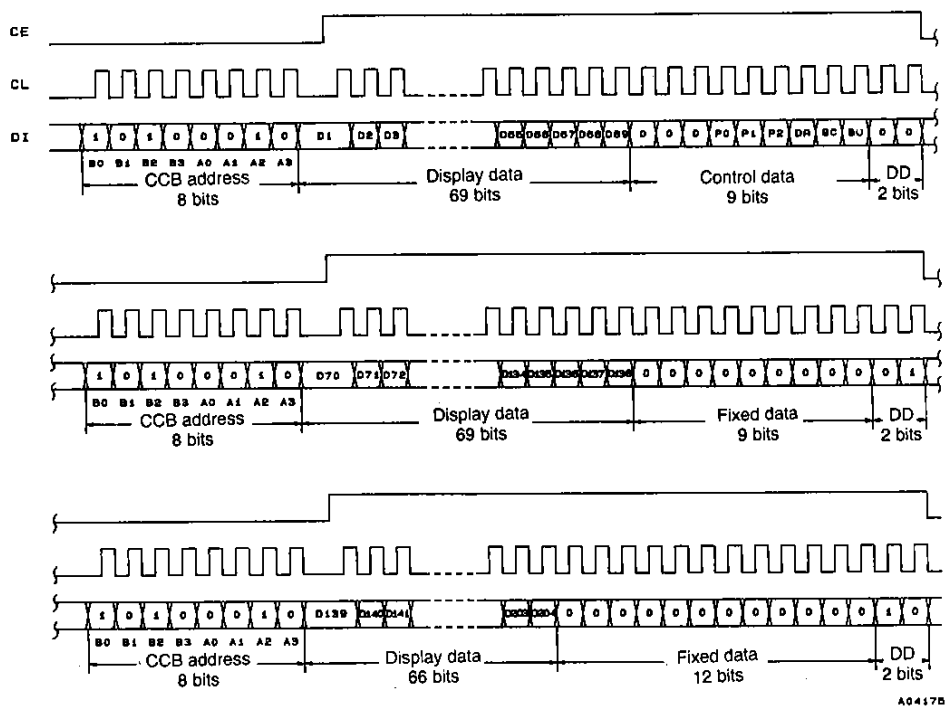
LC75873NE, 75873NW

Pin Functions

| Pin No. | | Symbol | Function | Active | I/O | Handling when unused |
|-------------------|----------------------------|-----------------------------|--|---|-------------|----------------------|
| LC75873NE | LC75873NW | | | | | |
| 1 to 4 5 to 6B | 79, 80, 1, 2 3 to 6B | S1/P1 to S4/P4 S5 to S6B | Segments outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control. | — | O | Open |
| 69 70 71 | 67 68 69 | COM1 COM2 COM3 | Common driver outputs. The frame frequency f_o is $f_{OSC}/384$ Hz. | — | O | Open |
| 76 | 74 | OSC | Oscillator connection. An oscillator circuit can be formed by connecting an external resistor and capacitor at this pin. | — | I/O | GND |
| 78 79 80 | 76 77 78 | CE CL DI | Serial data transfer inputs. Connected to the controller. CE: Chip enable CL: Synchronization clock DI: Transfer data | H  — | I I I | GND |
| 77 | 75 | \overline{INH} | Display off control input $\overline{INH} = \text{low } (V_{SS}) \dots \dots$ Display forced off S1/P1 to S4/P4 = low (These pins are forcibly set to the segment output port function and held at the low level.) S5 to S6B = low COM1 to COM3 = low $\overline{INH} = \text{high } (V_{DD}) \dots \dots$ Display on However, serial data transfer is possible when the display is forced off by this pin. | L | I | GND |
| 73 | 71 | V_{DD1} | Used to apply the LCD drive 2/3 bias voltage externally. Connect this pin to V_{DD2} when using a 1/2-bias drive scheme. | — | I | Open |
| 74 | 72 | V_{DD2} | Used to apply the LCD drive 1/3 bias voltage externally. Connect this pin to V_{DD1} when using a 1/2-bias drive scheme. | — | I | Open |
| 72 | 70 | V_{DD} | Power supply. Provide a voltage of between 3.0 and 6.0 V. | — | — | — |
| 75 | 73 | V_{SS} | Power supply. Connect to ground. | — | — | — |

Serial Data Input

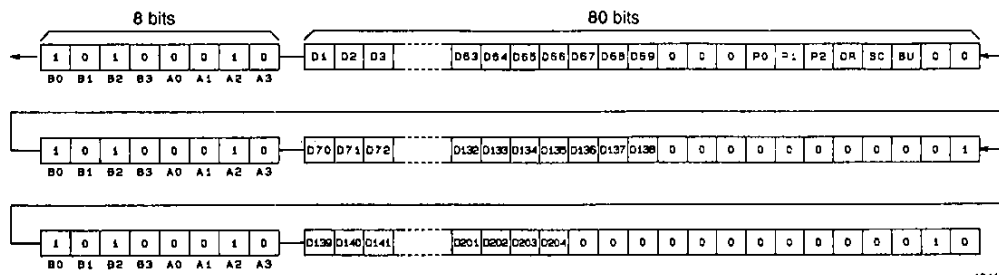
1. When CL is stopped at the low level



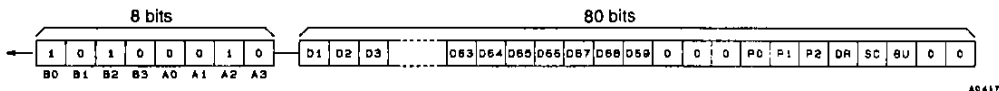
Note: DD is the direction data.

Serial Data Transfer Example

- When 139 or more segments are used
All 240 bits of serial data must be sent.



- When fewer than 139 segments are used
Either 80 or 160 bits of serial data may be sent, depending on the number of segments used. However, the serial data shown below (the D1 to D69 display data and the control data) must be sent.



Control Data Functions

- P0 to P2: Segment output port/general-purpose output port switching control data
These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S4/P4 output pins.

| Control data | | | Output pin state | | | |
|--------------|----|----|------------------|-------|-------|-------|
| P0 | P1 | P2 | S1/P1 | S2/P2 | S3/P3 | S4/P4 |
| 0 | 0 | 0 | S1 | S2 | S3 | S4 |
| 0 | 0 | 1 | P1 | S2 | S3 | S4 |
| 0 | 1 | 0 | P1 | P2 | S3 | S4 |
| 0 | 1 | 1 | P1 | P2 | P3 | S4 |
| 1 | 0 | 0 | P1 | P2 | P3 | P4 |

Note: Sn (n = 1 to 4): Segment output port function
Pn (n = 1 to 4): General-purpose output port function

Note that when the general-purpose output port function is selected, the correspondence between the output pins and the display data will be that shown in the table.

| Output pin | Corresponding display data |
|------------|----------------------------|
| S1/P1 | D1 |
| S2/P2 | D4 |
| S3/P3 | D7 |
| S4/P4 | D10 |

For example, if the general-purpose output port function is selected for the S4/P4 output pin, that output pin will output a high level when the display data D10 is 1, and a low level when the D10 is 0.

2. DR: 1/2-bias drive or 1/3-bias drive switching control data

This control data bit selects either 1/2-bias drive or 1/3-bias drive.

| DR | Drive scheme |
|----|----------------|
| 0 | 1/3-bias drive |
| 1 | 1/2-bias drive |

3. SC: Segment on/off control data

This control data controls the on/off state of the segments.

| SC | Display state |
|----|---------------|
| 0 | On |
| 1 | Off |

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

4. BU: Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

| BU | Mode |
|----|--|
| 0 | Normal mode |
| 1 | Power saving mode. In this mode, the OSC pin oscillator is stopped and the common and segment output pins go low. However, the S1/P1 to S4/P4 output pins can be used as general-purpose output ports under the control of the data bits P0 to P2. |

Display Data and Output Pin Correspondence

| Output pin | COM1 | COM2 | COM3 |
|------------|------|------|------|
| S1/P1 | D1 | D2 | D3 |
| S2/P2 | D4 | D5 | D6 |
| S3/P3 | D7 | D8 | D9 |
| S4/P4 | D10 | D11 | D12 |
| S5 | D13 | D14 | D15 |
| S6 | D16 | D17 | D18 |
| S7 | D19 | D20 | D21 |
| S8 | D22 | D23 | D24 |
| S9 | D25 | D26 | D27 |
| S10 | D28 | D29 | D30 |
| S11 | D31 | D32 | D33 |
| S12 | D34 | D35 | D36 |
| S13 | D37 | D38 | D39 |
| S14 | D40 | D41 | D42 |
| S15 | D43 | D44 | D45 |
| S16 | D46 | D47 | D48 |
| S17 | D49 | D50 | D51 |
| S18 | D52 | D53 | D54 |
| S19 | D55 | D56 | D57 |
| S20 | D58 | D59 | D60 |
| S21 | D61 | D62 | D63 |
| S22 | D64 | D65 | D66 |
| S23 | D67 | D68 | D69 |
| S24 | D70 | D71 | D72 |
| S25 | D73 | D74 | D75 |
| S26 | D76 | D77 | D78 |
| S27 | D79 | D80 | D81 |
| S28 | D82 | D83 | D84 |
| S29 | D85 | D86 | D87 |
| S30 | D88 | D89 | D90 |
| S31 | D91 | D92 | D93 |
| S32 | D94 | D95 | D96 |
| S33 | D97 | D98 | D99 |
| S34 | D100 | D101 | D102 |

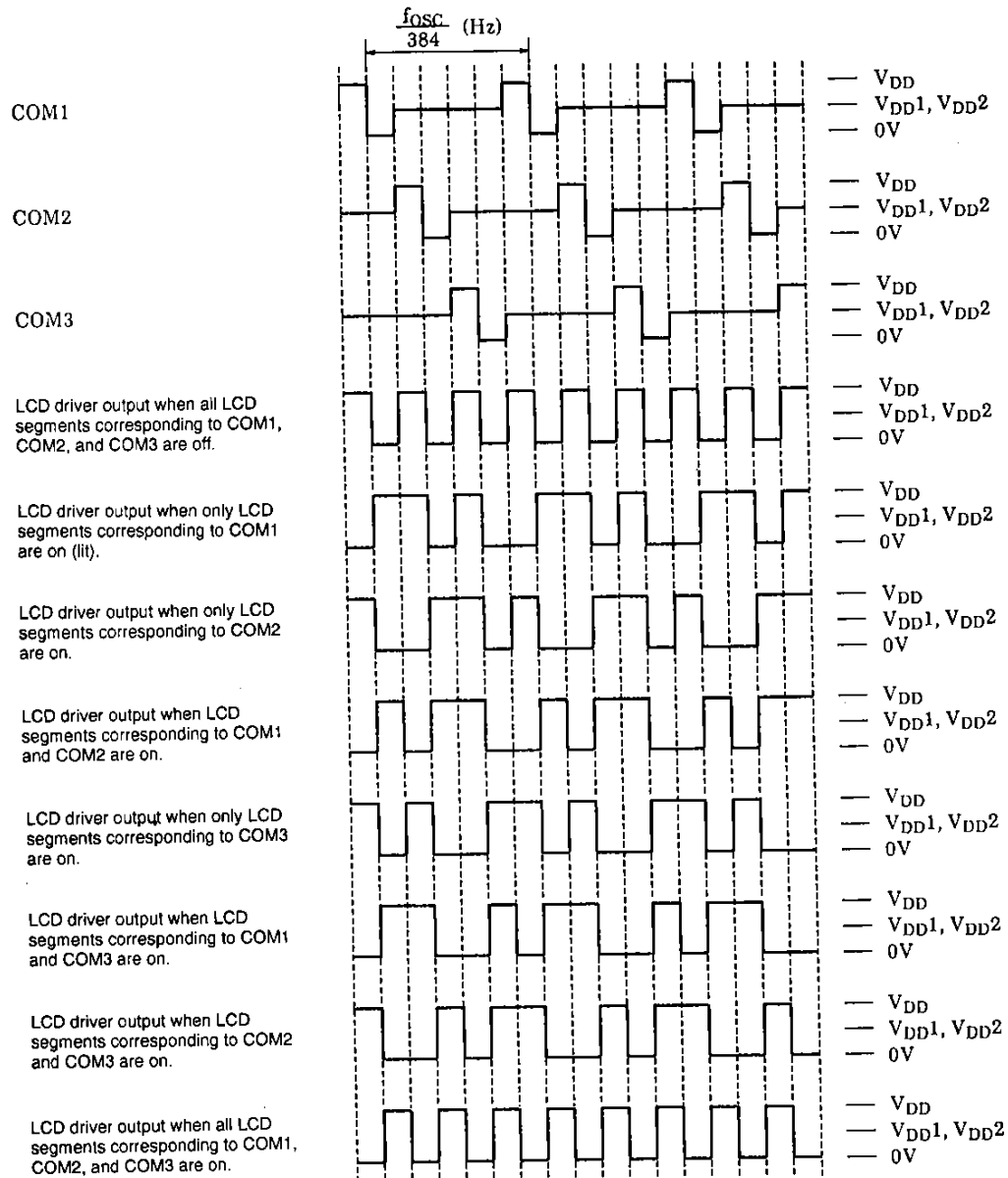
| Output pin | COM1 | COM2 | COM3 |
|------------|------|------|------|
| S35 | D103 | D104 | D105 |
| S36 | D106 | D107 | D108 |
| S37 | D109 | D110 | D111 |
| S38 | D112 | D113 | D114 |
| S39 | D115 | D116 | D117 |
| S40 | D118 | D119 | D120 |
| S41 | D121 | D122 | D123 |
| S42 | D124 | D125 | D126 |
| S43 | D127 | D128 | D129 |
| S44 | D130 | D131 | D132 |
| S45 | D133 | D134 | D135 |
| S46 | D136 | D137 | D138 |
| S47 | D139 | D140 | D141 |
| S48 | D142 | D143 | D144 |
| S49 | D145 | D146 | D147 |
| S50 | D148 | D149 | D150 |
| S51 | D151 | D152 | D153 |
| S52 | D154 | D155 | D156 |
| S53 | D157 | D158 | D159 |
| S54 | D160 | D161 | D162 |
| S55 | D163 | D164 | D165 |
| S56 | D166 | D167 | D168 |
| S57 | D169 | D170 | D171 |
| S58 | D172 | D173 | D174 |
| S59 | D175 | D176 | D177 |
| S60 | D178 | D179 | D180 |
| S61 | D181 | D182 | D183 |
| S62 | D184 | D185 | D186 |
| S63 | D187 | D188 | D189 |
| S64 | D190 | D191 | D192 |
| S65 | D193 | D194 | D195 |
| S66 | D196 | D197 | D198 |
| S67 | D199 | D200 | D201 |
| S68 | D202 | D203 | D204 |

Note: This table assumes that the segment output port function is selected for the S1/P1 to S4/P4 output pins.

For example, the table below lists the output states for the S11 output pin.

| Display data | | | Output pin (S11) state |
|--------------|-----|-----|---|
| D31 | D32 | D33 | |
| 0 | 0 | 0 | The LCD segments for COM1, COM2 and COM3 are off. |
| 0 | 0 | 1 | The LCD segment for COM3 is on (lit). |
| 0 | 1 | 0 | The LCD segment for COM2 is on. |
| 0 | 1 | 1 | The LCD segments for COM2 and COM3 are on. |
| 1 | 0 | 0 | The LCD segment for COM1 is on. |
| 1 | 0 | 1 | The LCD segments for COM1 and COM3 are on. |
| 1 | 1 | 0 | The LCD segments for COM1 and COM2 are on. |
| 1 | 1 | 1 | The LCD segments for COM1, COM2 and COM3 are on. |

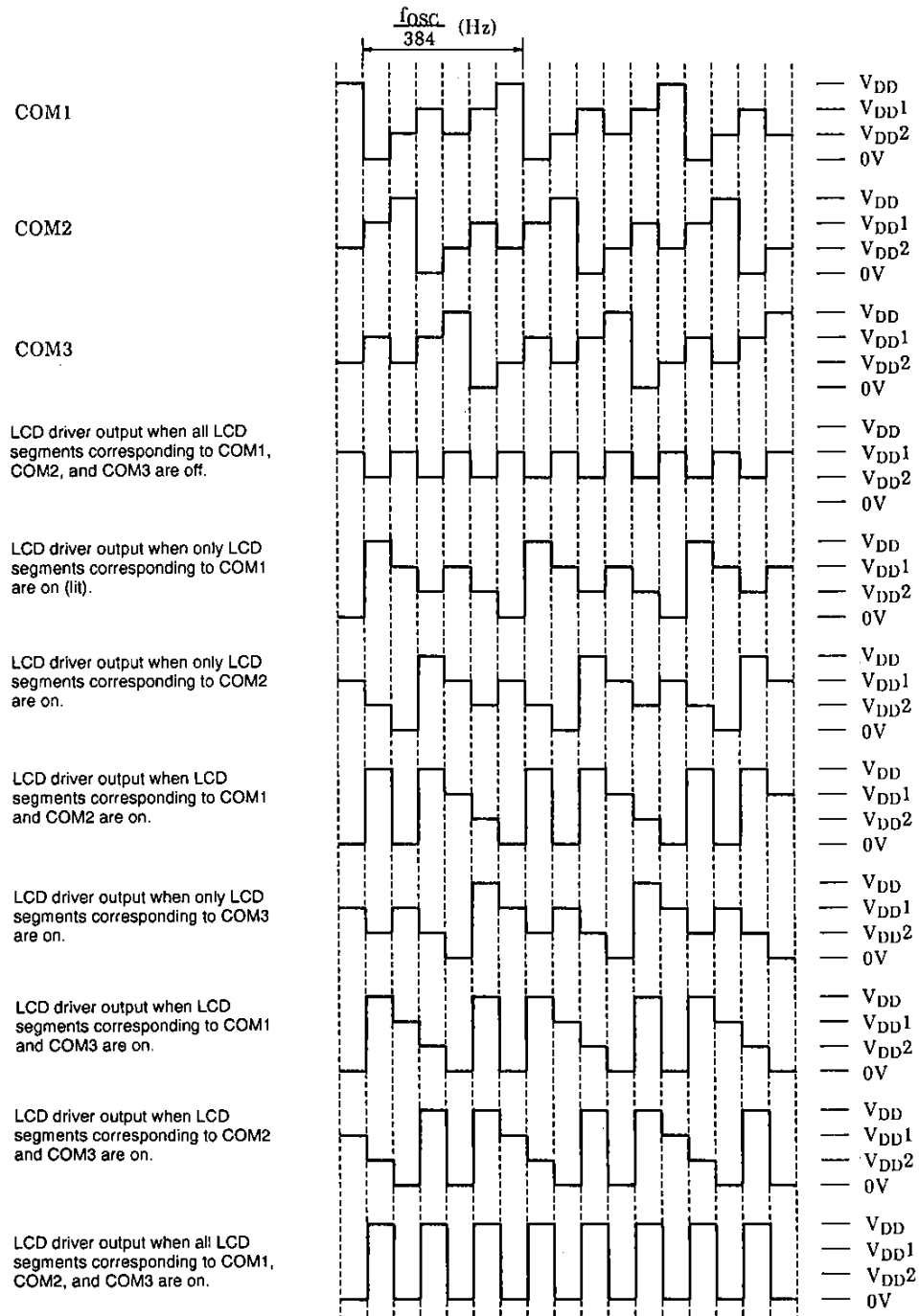
1/3-Duty 1/2-Bias Drive Scheme



A04179

1/3-Duty 1/2-Bias Waveforms

1/3-Duty 1/3-Bias Drive Scheme



A04180

Display Control and the $\overline{\text{INH}}$ Pin

Since the LSI internal data (the display data D1 to D204 and the control data) is undefined when power is first applied, applications should prevent meaningless displays with the following procedure. First, set the $\overline{\text{INH}}$ pin low at the same time as power is applied to turn off the display. This will set the S1/P1 to S4/P4, S5 to S68, and COM1 to COM3 pins low. While the $\overline{\text{INH}}$ pin is held low, the control microprocessor should send the serial data. Finally, the application can set the $\overline{\text{INH}}$ pin to high. (See Figure 3.)

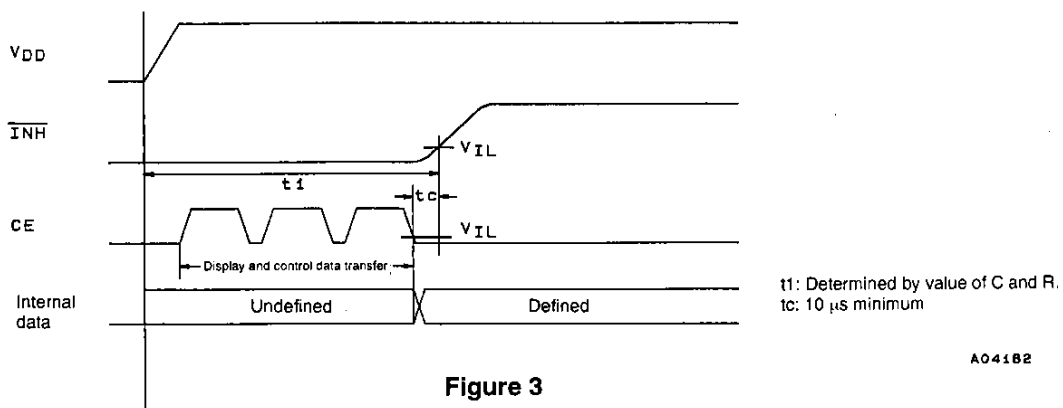
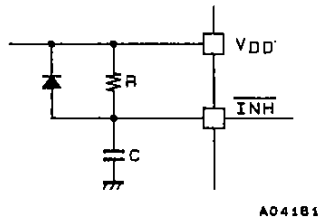


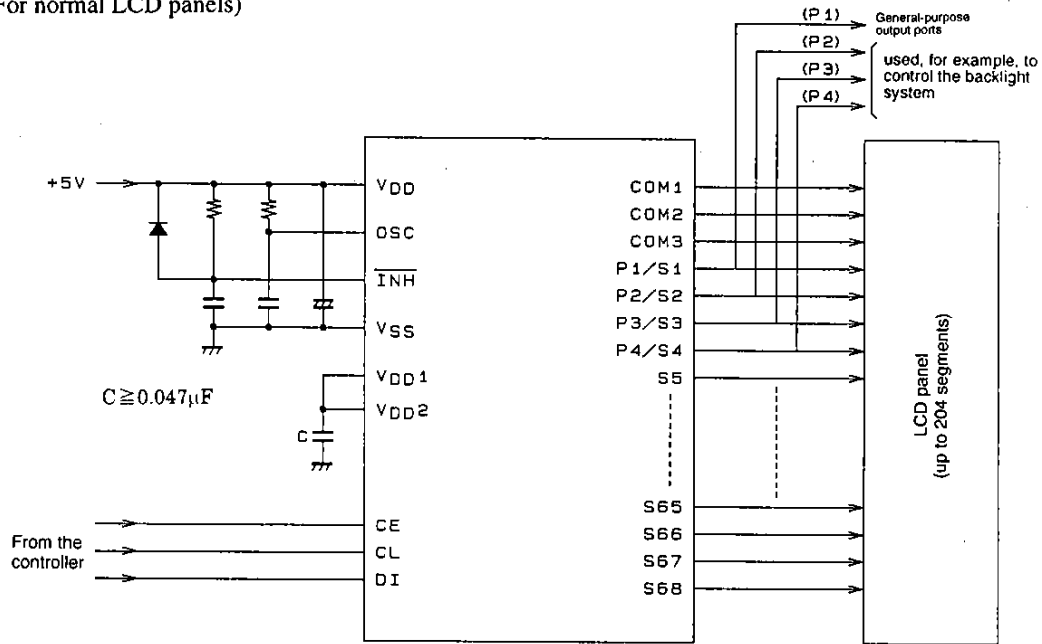
Figure 3

Notes on Controller Transfer of Display Data

Since the LC75873NE and LC75873NW accept the display data divided into four separate transfer operations, we recommend that applications make a point of completing all four data transfers within a period of no more than 30 ms to guarantee the quality of the displayed image.

Sample Application Circuit 1

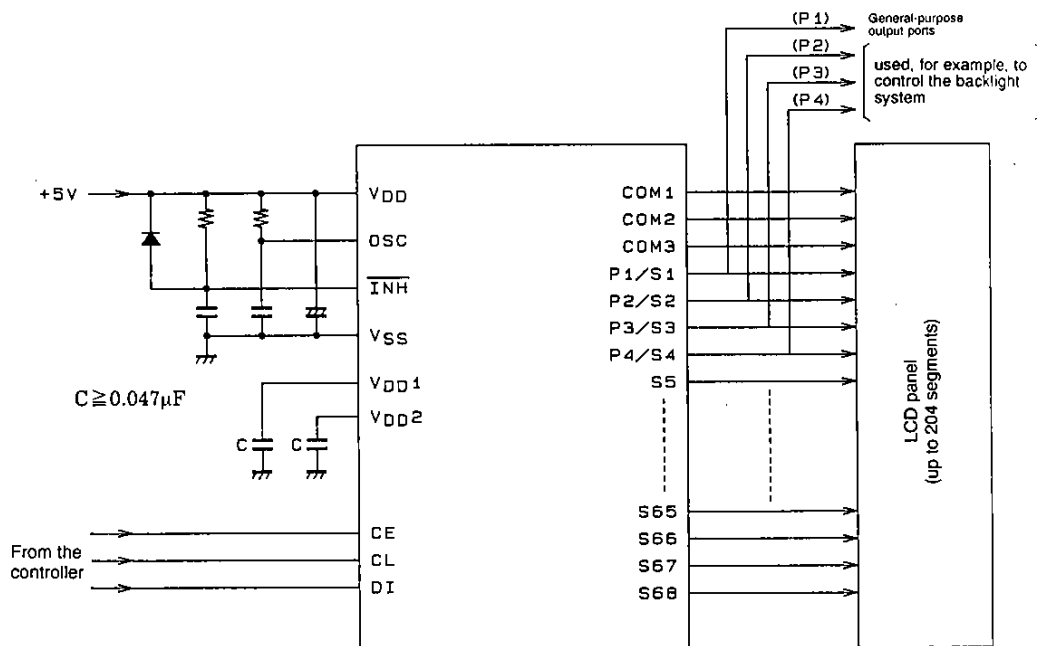
1/2 Bias (For normal LCD panels)



A05617

Sample Application Circuit 2

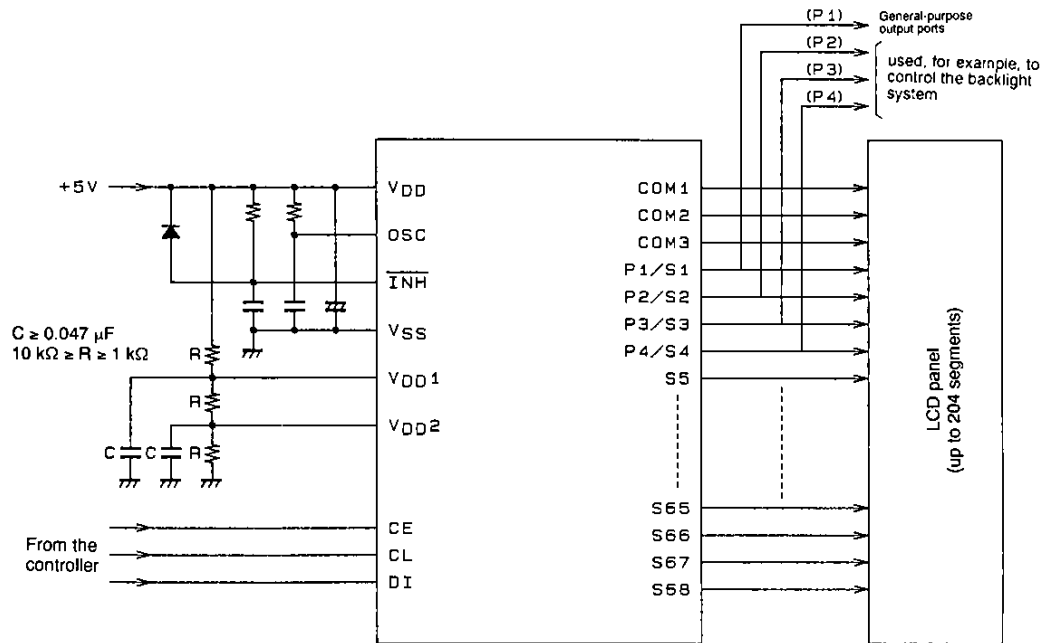
1/3 Bias (for normal LCD panels)



A05618

Sample Application Circuit 3

1/3 Bias (for large LCD panels)



A05619

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of June, 1996. Specifications and information herein are subject to change without notice.