Ordering number : EN※5214

CMOS LSI

No. ※ 5214

LC78010E

Video CD and CD-G Digital RGB Encoder LSI

Preliminary

Overview

The LC78010E is a CMOS LSI that integrates a digital RGB encoder and a synchronizing signal generation circuit on a single chip. A video CD or CD-G system can be implemented by combining the LC78010E with an MPEG video decoder or CD-G decoder.

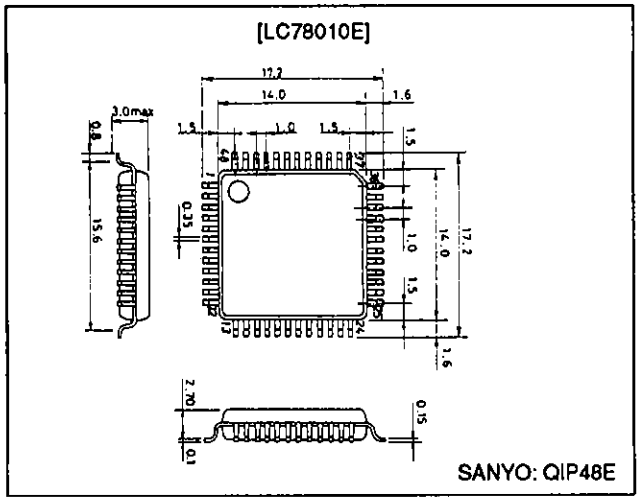
Features

- System structure: Systems can be implemented in 2 chips, the LC78010E plus an MPEG video decoder or CD-G decoder.
- Output D/A converter specifications: Two 8-bit D/A converters (for luminance signal output, chrominance signal output, and composite video output)
- Clock oscillator: External input: 4fsc
  (NTSC: 14.31818 MHz)
  (PAL: 17.734475 MHz)
  (PAL-M: 14.30244598 MHz)
- External input data types: RGB (24 bits)
  Y-U-V (24 bits)
  Y-UV (16 bits)
- Supports input of RGB OSD signal: R.G.B. + BLANK (4-line input)
- Supports CD-G decoder input
- External synchronizing signal input (HSYNC, CSYNC, and BLANK)
- External subcarrier signal input
- Supports the NTSC, PAL, and PAL-M formats
- Video signal output types: Y/C separate video signal outputs and composite video signal output

Package Dimensions

unit: mm

3156-QFP48E



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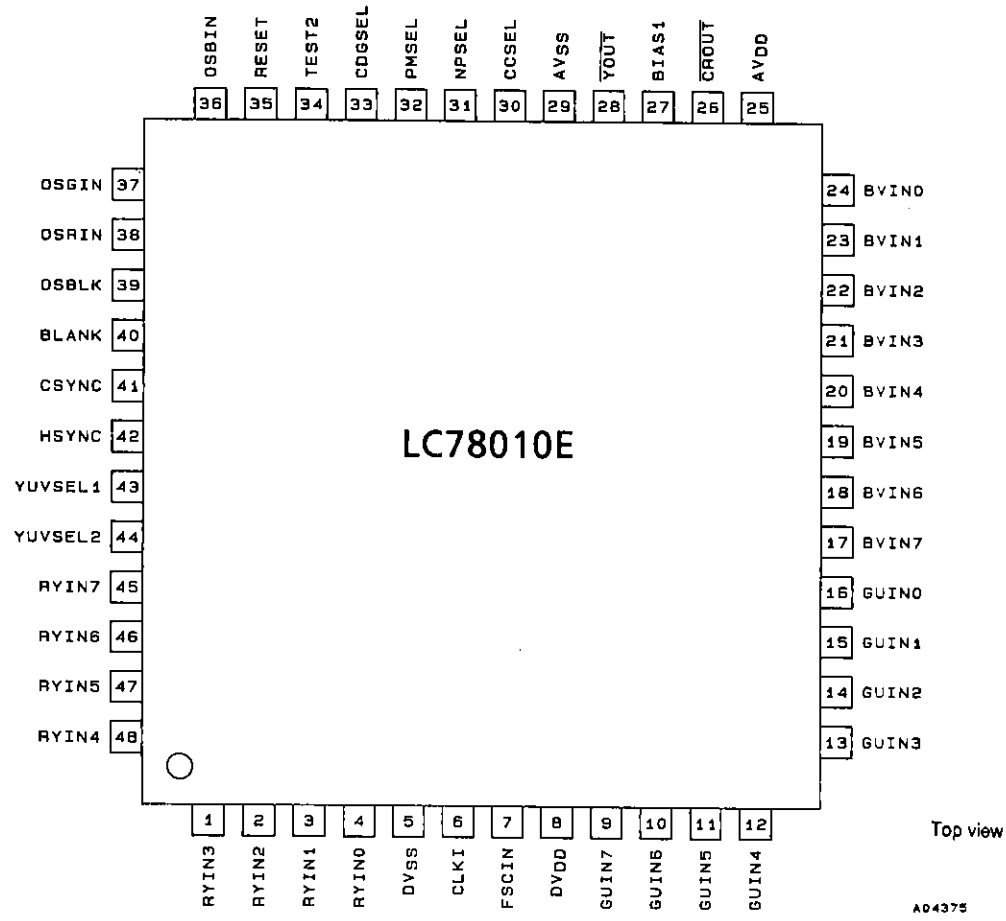
Pin Assignment



Pin Functions

Pin No.	Symbol	Function	I/O	Polarity	Description	
1	RYIN3	R/Y data input	I	Positive	R/Y data input, Pull-down resistor built in	
2	RYIN2	R/Y data input	I	Positive	R/Y data input, Pull-down resistor built in	
3	RYIN1	R/Y data input	I	Positive	R/Y data input, Pull-down resistor built in	
4	RYIN0	R/Y data input	I	Positive	R/Y data input (LSB), Pull-down resistor built in	
5	DV_{SS}	Ground	—	—	Digital system ground	
6	CLKI	Clock input	I	—	4fsc clock input. Feedback resistor built in	NTSC: 14.31818 MHz PAL: 17.734475 MHz PAL-M: 14.30244598 MHz
7	FSCIN	Clock input	I	—	External subcarrier clock input Feedback resistor built in	NTSC: 3.579545 MHz PAL: 4.43361875 MHz PAL-M: 3.57561149 MHz
8	DV_{DD}	Power supply (+5 V)	—	—	Digital system power supply	
9	GUIN7	G/U data input	I	Positive	G/U data input (MSB), Pull-down resistor built in	
10	GUIN6	G/U data input	I	Positive	G/U data input, Pull-down resistor built in	
11	GUIN5	G/U data input	I	Positive	G/U data input, Pull-down resistor built in	
12	GUIN4	G/U data input	I	Positive	G/U data input, Pull-down resistor built in	
13	GUIN3	G/U data input	I	Positive	G/U data input, Pull-down resistor built in	
14	GUIN2	G/U data input	I	Positive	G/U data input, Pull-down resistor built in	
15	GUIN1	G/U data input	I	Positive	G/U data input, Pull-down resistor built in	
16	GUIN0	G/U data input	I	Positive	G/U data input (LSB), Pull-down resistor built in	

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Pin No.	Symbol	Function	I/O	Polarity	Description
17	BVIN7	G/V/UV data input	I	Positive	G/V/UV data input (MSB), Pull-down resistor built in
18	BVIN6	G/V/UV data input	I	Positive	G/V/UV data input, Pull-down resistor built in
19	BVIN5	G/V/UV data input	I	Positive	G/V/UV data input, Pull-down resistor built in
20	BVIN4	G/V/UV data input	I	Positive	G/V/UV data input, Pull-down resistor built in
21	BVIN3	G/V/UV data input	I	Positive	G/V/UV data input, Pull-down resistor built in
22	BVIN2	G/V/UV data input	I	Positive	G/V/UV data input, Pull-down resistor built in
23	BVIN1	G/V/UV data input	I	Positive	G/V/UV data input, Pull-down resistor built in
24	BVIN0	G/V/UV data input	I	Positive	G/V/UV data input (LSB), Pull-down resistor built in
25	AV_{DD}	Power supply (+5 V)	—	—	Analog system power supply
26	$\overline{CROUT}$	Chrominance/ composite video signal output	O	Positive	Chrominance/composite video signal (analog) output (8-bit D/A converter output)
27	BIAS1	Capacitor connection	O	—	Ripple exclusion capacitor connection
28	$\overline{YOUT}$	Luminance signal output	O	Positive	Luminance signal (analog) output (8-bit D/A converter output)
29	AV_{SS}	Ground	—	—	Analog system ground
30	CCSEL	Output signal control	I	Positive	Output signal control (0: chrominance signal output, 1: composite video signal output)
31	NPSEL	Mode selection (NTSC, PAL, or PAL-M)	I	Positive	NPSEL / PMSEL / Mode 0 / 0 / NTSC mode 1 / 0 / PAL mode 0 / 1 / PAL-M mode 1 / 1
32	PMSEL	Mode selection (NTSC, PAL, or PAL-M)	I	Positive	
33	CDGSEL	Input signal control	I	Positive	Video input mode (Video CD or CD-G) control (Video CD:1, CD-G: 0)
34	TEST2	Test input	I	Positive	Test mode input. This input must be tied low during normal operation.
35	$\overline{RESET}$	Reset input	I	Negative	Reset signal input
36	OSBIN	OSD (B) input	I	Positive	OSD (B) signal input
37	OSGIN	OSD (G) input	I	Positive	OSD (G) signal input
38	OSRIN	OSD (R) input	I	Positive	OSD (R) signal input
39	OSBLK	OSD data input	I	Positive	OSD switching (OSD or BLANK) signal input
40	BLANK	Blanking signal input	I	Positive	Composite blanking (HBLANK and VBLANK) signal input
41	$\overline{CSYNC}$	Synchronizing signal input	I	Negative	CSYNC synchronizing signal input
42	$\overline{HSYNC}$	Synchronizing signal input	I	Negative	HSYNC synchronizing signal input
43	YUVSEL1	Input signal control	I	Positive	YUVSEL1 / YUVSEL2 / Mode 0 / 0 / RYIN: R, GUIN: G, BVIN: B 1 / 0 / RYIN: Y, GUIN: U, BVIN: V 0 / 1 / RYIN: Y, BVIN: UV
44	YUVSEL2	Input signal control	I	Positive	
45	RYIN7	R/Y data input	I	Positive	R/Y data input (MSB), Pull-down resistor built in
46	RYIN6	R/Y data input	I	Positive	R/Y data input, Pull-down resistor built in
47	RYIN5	R/Y data input	I	Positive	R/Y data input, Pull-down resistor built in
48	RYIN4	R/Y data input	I	Positive	R/Y data input, Pull-down resistor built in

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	AV_{DD}, DV_{DD}	V_{SS} – 0.3 to V_{SS} + 7.0	V
Maximum input voltage	V_{IN} max	RYIN7 to RYIN0, CLKI, FSCIN, GUIN7 to GUIN0, BVIN7 to BVIN0, CCSEL, NPSEL, PMSEL, CDGSEL, TEST2, $\overline{RESET}$, OSRIN, OSGIN, OSBIN, OSBLK, BLANK, $\overline{CSYNC}$, $\overline{HSYNC}$, YUVSEL1, YUVSEL2	V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max	CROUT, YOUT, BIAS1	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	250	mW
Operating temperature	Topr		–30 to +85	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions		min	typ	max	Unit
Supply voltage	AV_{DD}	AV_{DD}		4.5		5.5	V
	DV_{DD}	DV_{DD}		3.0		5.5	V
Input high-level voltage	$V_{IH}1$	CCSEL, NPSEL, PMSEL, CDGSEL, TEST2, OSRIN, OSGIN, OSBIN, OSBLK, YUVSEL1, YUVSEL2		0.7 DV_{DD}		DV_{DD} + 0.3	V
Input high-level voltage	$V_{IH}2$	RYIN7 to RYIN0, GUIN7 to GUIN0, BVIN7 to BVIN0, BLANK, $\overline{CSYNC}$, $\overline{HSYNC}$, $\overline{RESET}$		2.2		DV_{DD} + 0.3	V
Input low-level voltage	$V_{IL}1$	CCSEL, NPSEL, PMSEL, CDGSEL, TEST2, OSRIN, OSGIN, OSBIN, OSBLK, YUVSEL1, YUVSEL2		V_{SS} – 0.3		0.3 DV_{DD}	V
Input low-level voltage	$V_{IL}2$	RYIN7 to RYIN0, GUIN7 to GUIN0, BVIN7 to BVIN0, BLANK, $\overline{CSYNC}$, $\overline{HSYNC}$, $\overline{RESET}$		V_{SS} – 0.3		0.8	V
Input frequency	F_{SCKIN}	CLKI	NTSC		14.31818		MHz
			PAL		17.73447		MHz
			PAL-M		14.302444		MHz
Input frequency	F_{SCIN}	FSCIN	NTSC		3.579545		MHz
			PAL		4.433617		MHz
			PAL-M		3.57561		MHz
Input frequency	$V_{IN}1$	CLKI (sine wave, capacitor coupled)		2.0	4.0	$V_{DD}1$	Vp-p
	$V_{IN}2$	FSCIN (sine wave, capacitor coupled)		2.0	4.0	$V_{DD}1$	Vp-p
Reset pulse width	t_{WRES}	$\overline{RESET}$		400			ns

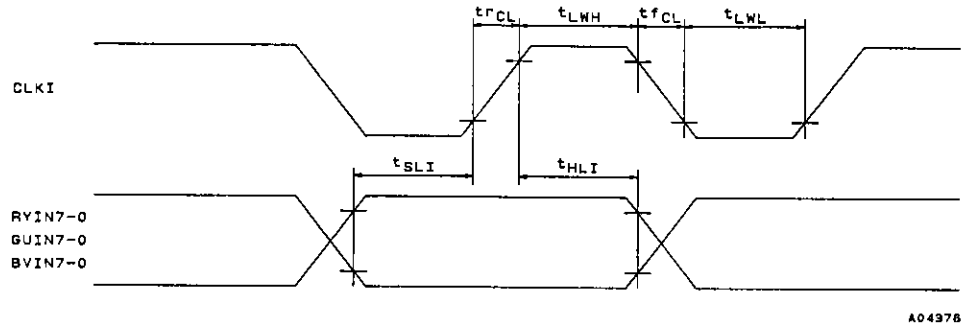
Electrical Characteristics at Ta = 25°C, DV_{DD} = AV_{DD} = 5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Output high-level voltage	$V_{OH}1$	CROUT, YOUT, BIAS1: I_{OH} = –1.0 mA	DV_{DD} – 1.0		DV_{DD}	V
Output low-level voltage	$V_{OL}1$	CROUT, YOUT, BIAS1: I_{OL} = 2.0 mA	V_{SS}		0.4	V
Input frequency	$I_{IH}1$	FSCIN, CCSEL, NPSEL, PMSEL, CDGSEL, TEST2, OSRIN, OSGIN, OSBIN, OSBLK, BLANK, $\overline{CSYNC}$, $\overline{HSYNC}$, YUVSEL1, $\overline{RESET}$, YUVSEL2: V_{IN} = DV_{DD}			5	µA
	$I_{IH}2$	RYIN7 to RYIN0, GUIN7 to GUIN0, BVIN7 to BVIN0: V_{IN} = DV_{DD}	25	50	75	µA
	$I_{IL}1$	FSCIN, CCSEL, NPSEL, PMSEL, CDGSEL, TEST2, OSRIN, OSGIN, OSBIN, OSBLK, BLANK, $\overline{CSYNC}$, $\overline{HSYNC}$, YUVSEL1, $\overline{RESET}$, YUVSEL2: V_{IN} = V_{SS}	–5			µA
Internal feedback resistance	R_{BIAS}	CLKI, FSCIN		1		MΩ
Operating current drain	$I_{DD}1$	AV_{DD}		21	40	mA
	$I_{DD}2$	DV_{DD}		34	56	mA
D/A converter resolution		YOUT, CROUT		8		Bit
D/A converter output resistance	R_{DA}	YOUT, CROUT	100	300	500	Ω
D/A converter reference voltage	V_{REF}	YOUT, CROUT (The voltage when the 8 bits of input data are all 0)	2.40	2.45	2.50	V

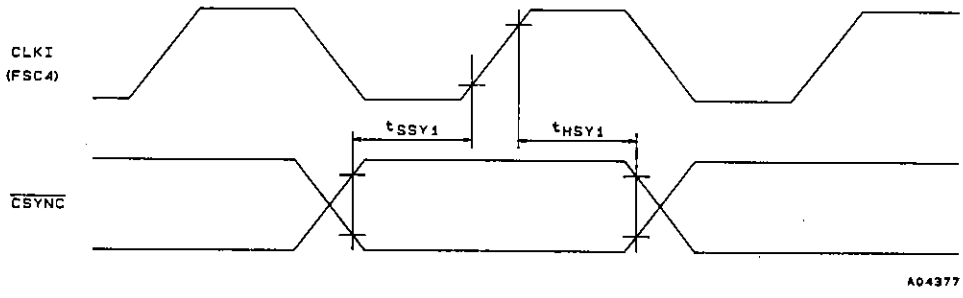
Timing Characteristics at Ta = 25°C, $V_{DD}1$ = 5 V, FSC4 = 14.31818 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input clock duty	V_{DUTY}	CLKI: sine wave	40		60	%
Clock rise time	t_{rCL}	CLKI: square wave			7.0	ns
Clock fall time	t_{fCL}	CLKI: square wave			7.0	ns
Minimum input pulse width	t_{LWH}	CLKI: High-level pulse width	23			ns
	t_{LWL}	CLKI: Low-level pulse width	23			ns
Data setup time	t_{SLI}	RYIN7 to RYIN0, GUIN7 to GUIN0, BVIN7 to BVIN0	10			ns
Data hold time	t_{HLI}	RYIN7 to RYIN0, GUIN7 to GUIN0, BVIN7 to BVIN0	10			ns
Data setup time	$t_{SSY}1$	$\overline{\text{CSYNC}}$ (FSC4)	10			ns
Data hold time	$t_{HSY}1$	$\overline{\text{CSYNC}}$ (FSC4)	10			ns
Data setup time	$t_{SSYB}2$	$\overline{\text{HSYNC}}$ (FSC4)	10			ns
Data hold time	$t_{HSYB}2$	$\overline{\text{HSYNC}}$ (FSC4)	10			ns
Data setup time	t_{SOSD}	OSBLK, OSRIN, OSGIN, OSBIN (FSC4)	10			ns
Data hold time	t_{HOSD}	OSBLK, OSRIN, OSGIN, OSBIN (FSC4)	10			ns

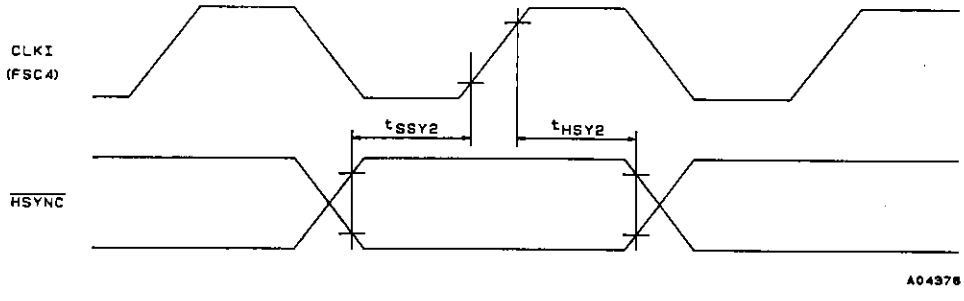
I/O Data Timing



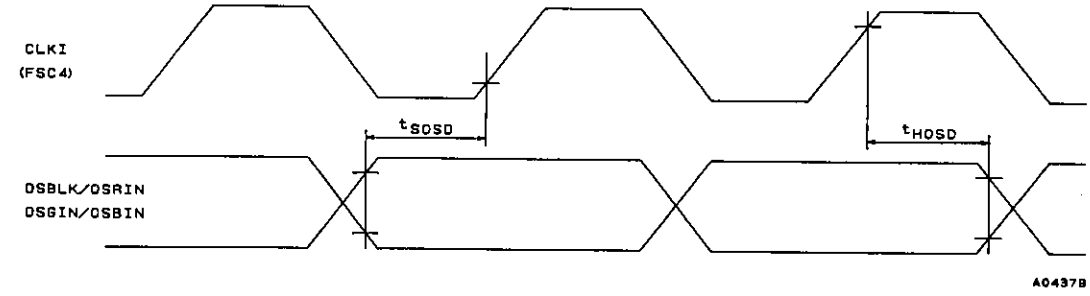
CSYNC Timing



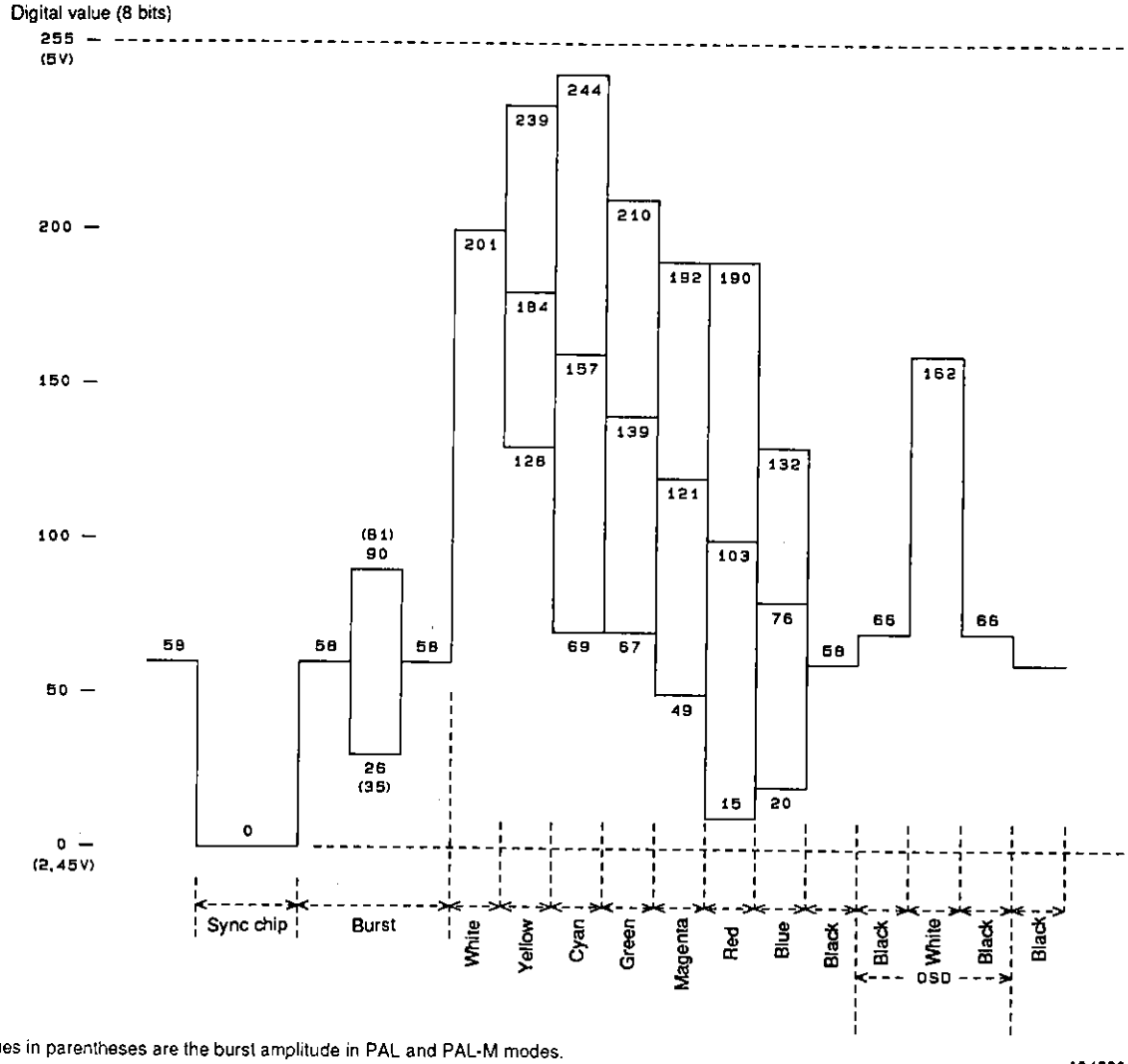
HSYNC Timing



OSBLK, OSRIN, OSGIN, and OSBIN Timing

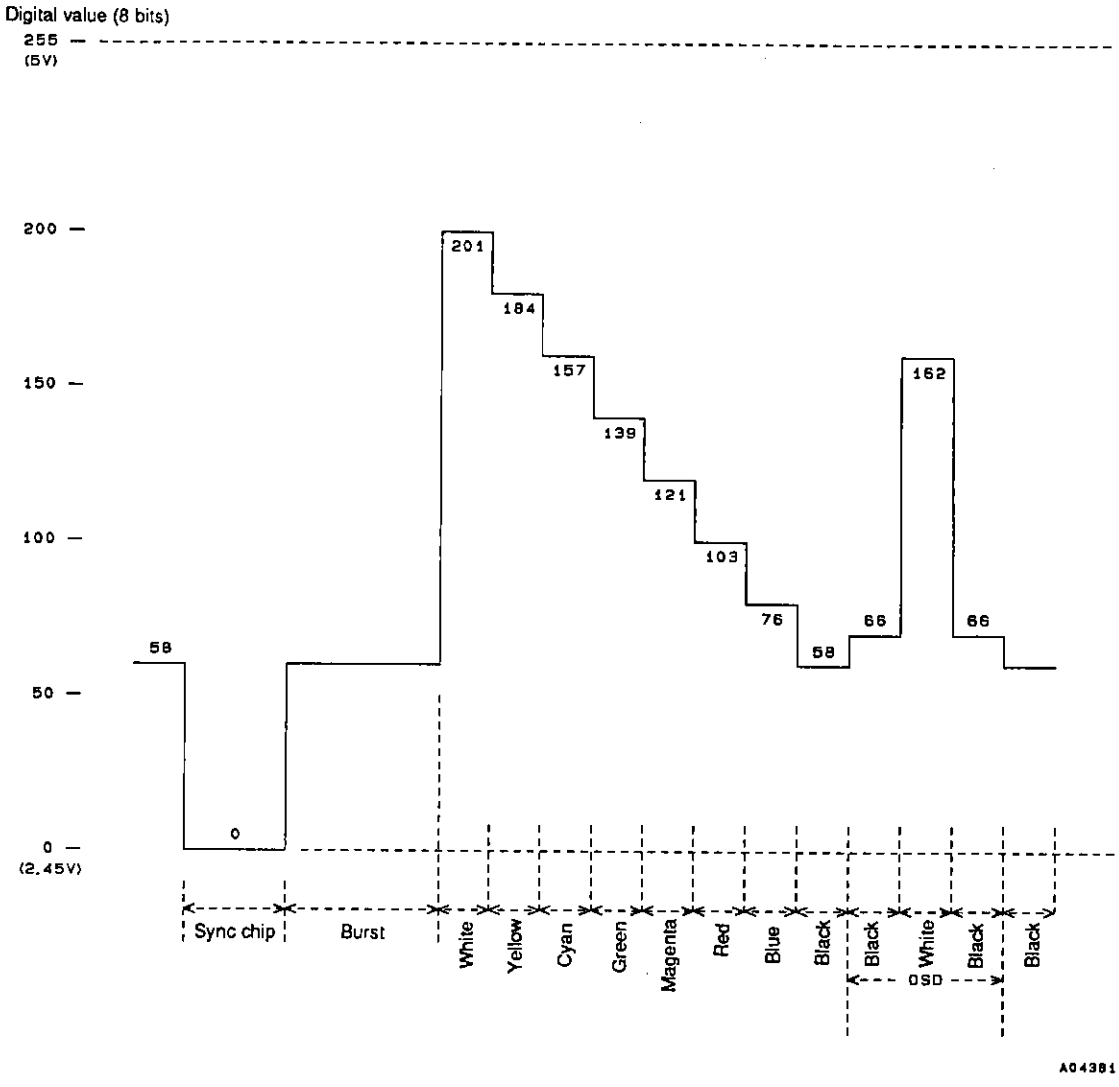


Composite Video Signal Output

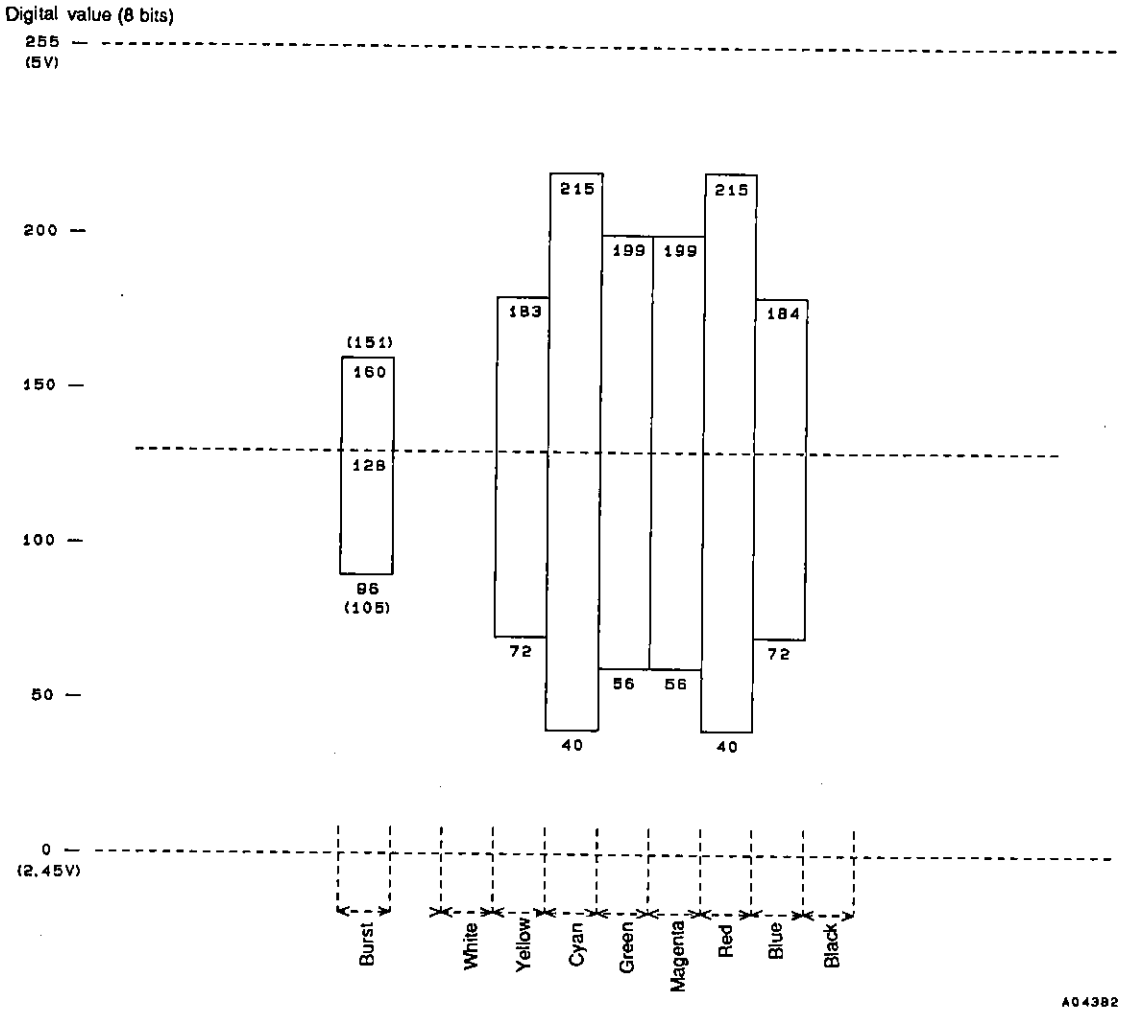


Note: Values in parentheses are the burst amplitude in PAL and PAL-M modes.

Luminance Signal Output

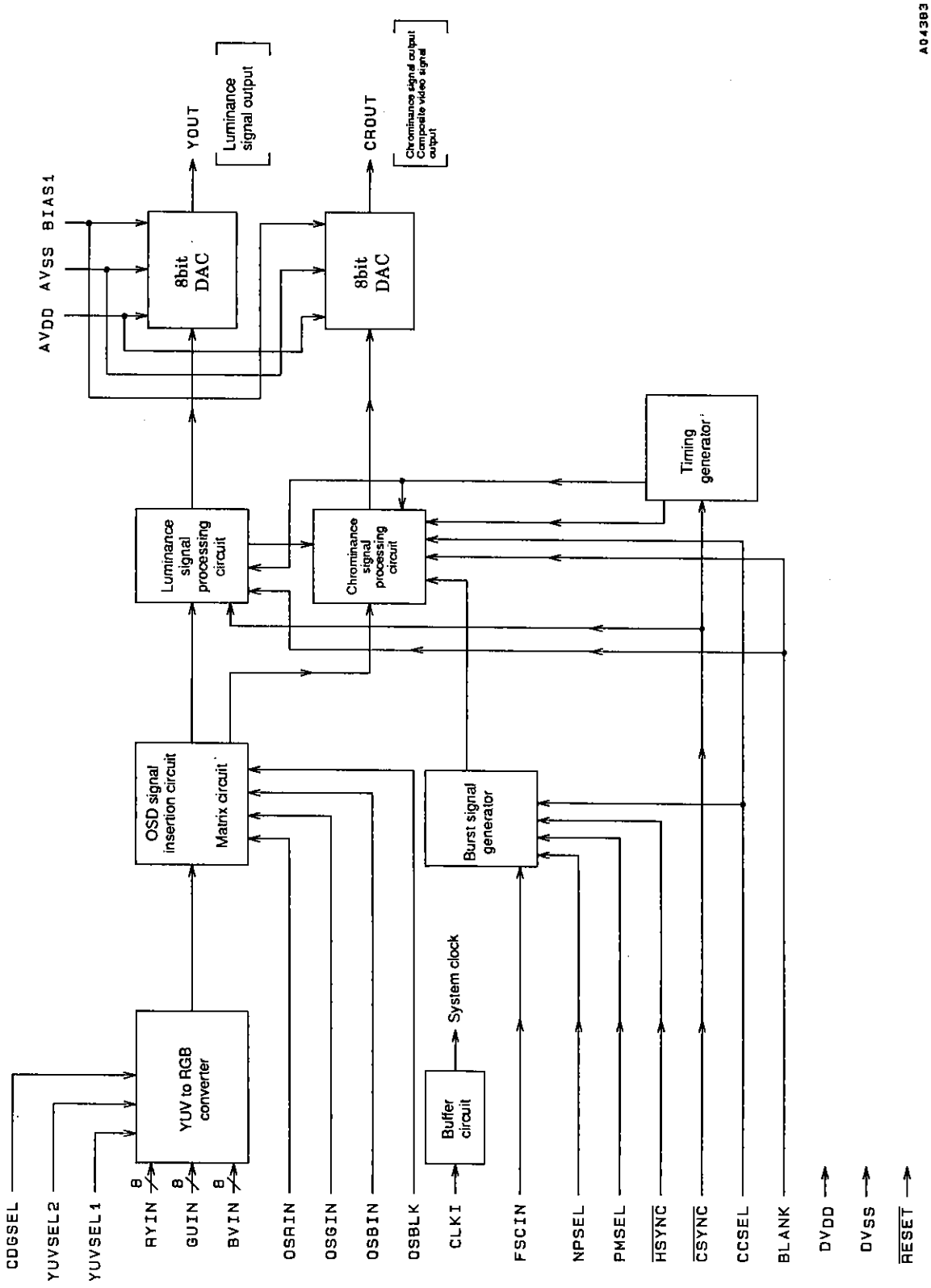


Chrominance Signal Output



Note: Values in parentheses are the burst amplitude in PAL and PAL-M modes.

Block Diagram



Functional Overview

1. Clock
   The LC78010E does not include an internal oscillator circuit. Therefore application systems must provide an external 4fsc clock from the MPEG decoder or the CD-G decoder.

2. Video signal output formats
   The LC78010E provides two types of video signal output: separate Y/C outputs (luminance and chrominance signals) and a composite video signal output. The CCSEL pin switches between separate Y/C output and composite video signal output. In particular, the CCSEL pin switches the chrominance signal output pin (CROUT) between chrominance signal output and composite video signal output. Note that when CCSEL is high and the chip is in composite video signal output mode, the luminance signal output pin (YOUT) will be fixed at the low level, since the luminance signal output 8-bit D/A converter is turned off in this mode.

CCSEL	High	Low
CROUT	Chrominance signal output	Composite video signal output

3. MPEG decoder/CD-G decoder switching
   The LC78010E supports the 24-bit (8 bits × 3 colors) and 12-bit (4 bits × 3 colors) data formats output by MPEG and CD-G decoders, respectively. The CDGSEL pin switches between these formats. Note that the 12 bits (4 bits × 3 colors) of RGB data output by the CD-G decoder must be connected to the RYIN4 to RYIN7, GUIN4 to GUIN7, and BUIN4 to BUIN7 pins. We recommend using the Sanyo LC7874E CG-D decoder, currently under development.

CDGSEL	High	Low
Decoder	V-CD	CD-G

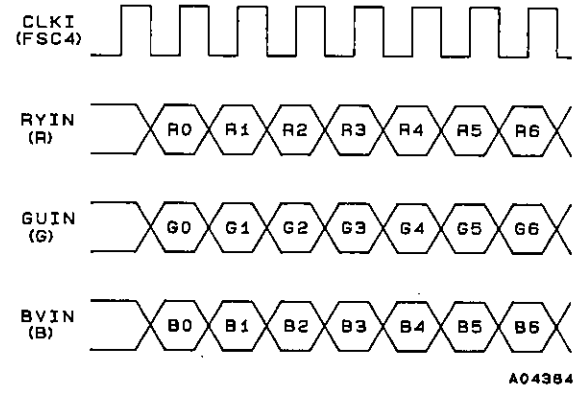
Connections between the LC78010E and the LC7874E

	LC78010E	LC7874E
R	RYIN7 RYIN6 RYIN5 RYIN4	ROUT3 ROUT2 ROUT1 ROUT0
G	GUIN7 GUIN6 GUIN5 GUIN4	GOUT3 GOUT2 GOUT1 GOUT0
B	BVIN7 BVIN6 BVIN5 BVIN4	BOUT3 BOUT2 BOUT1 BOUT0

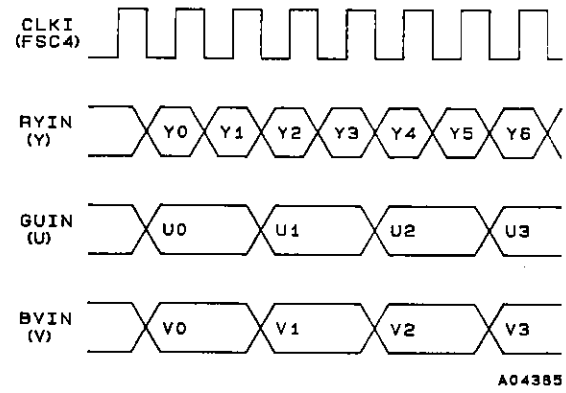
4. MPEG decoder input data format switching
   The LC78010E supports both RGB and YUV inputs. The YUVSEL1 and YUVSEL2 pins switch between the RGB and YUV input formats. When the YUV input format is used, a blanking signal is used as the reference signal. The YUV data input timing must be such that the YUV data is input when the blanking signal goes low. Note that for Y-UV input ③, the first data that is input must be the Cb (U) data input to the UV input pin.

YUVSEL1	YUVSEL2	
0	0	RGB input
1	0	Y-U-V input (24-bit)
0	1	Y-UV input (16-bit)

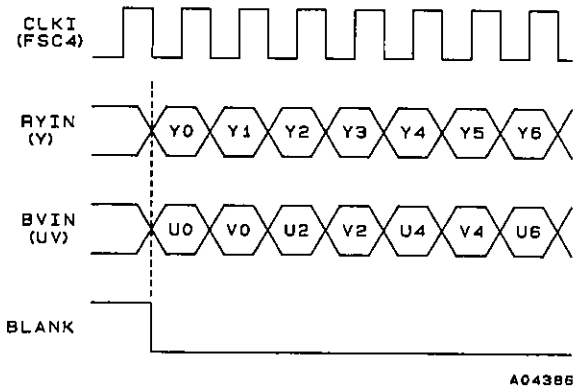
① RGB (24-bit) Input



② YCbCr (YUV) (24-bit) Input



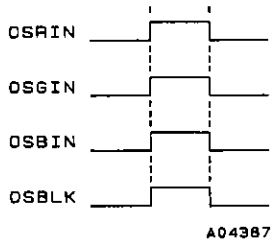
③ Y (8-bit) CbCr (8-bit) multiplexed



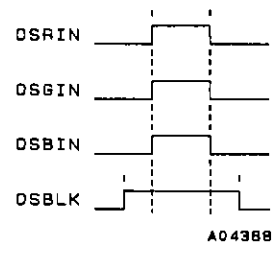
5. OSD (on-screen display) signal input

The LC78010E supports input of RGB OSD signals. The OSD input data must consist of 3-bit RGB data and a blanking signal. Eight color OSD data can be displayed on the screen by providing these four signals: OSRIN, OSGIN, OSBIN, and OSBLK. However, when converted to 8-bit (full scale: 255) values, the white luminance level will be 162, the black luminance level will be 66, and the green luminance level will be 66.

① No green



② Green present



OSRIN	OSGIN	OSBIN	OSBLK	Color
0	0	0	0	No OSD display
0	0	0	1	Black
1	0	0	1	Red
0	1	0	1	Green
0	0	1	1	Blue
1	0	1	1	Yellow
1	1	0	1	Cyan
0	1	1	1	Magenta
1	1	1	1	White

6. NTSC, PAL, and PAL-M modes

The LC78010E supports three video modes: NTSC, PAL, and PAL-M. The NPSEL and PMSEL pins switch between these modes.

NPSEL	PMSEL	Mode
0	0	NTSC
1	0	PAL
0	1	PAL-M