SANYO

LC78637E — CMOS IC for Compact Disc Player Applications

■ Overview

The LC78637E combines audio CD RF signal processing, servo control, EFM signal processing, audio signal processing, and a CDTEXT decoder in a single chip, enabling a system to be configured with very few peripheral components. The RF signal processing block performs such functions as EFM signal generation, error signal generation, and laser power control. The servo control block carries out A/D conversion of focus error and tracking error signals from the RF signal processing block, and digitally performs focus, tracking, sled, and spindle servo processing necessary for CD servo operation. The functions of the EFM signal processing block cover EFM signal demodulation and synchronization detection, protection, and interpolation, de-interleaving, and error detection and correction. The audio signal processing block handles data interpolation/mute processing based on the error correction situation, and incorporates an 8X over sampling filter, 1-bit DAC, and secondary LPF (differential amplifier). The status and characteristics of each function block can be set, or ascertained by data reads, via the microcomputer interface.

■ Playback functions

- — Playback speed: 1X speed, 2X speed
- — Jitter-free playback (VCEC)
- — CD-R/W: 1X speed, 2X speed
- — Simple CLV playback

■ RF processing block

- — RF system: AGC, CD-R, R/W playback supported, peak hold, bottom hold
- — Error system: Variable-balance TE signal generation, FE signal generation
- — Detection: Track counting signal, jitter, flaws (black, mirror)
- — Laser power control
- — DC offset voltage cancellation

■ Servo control block

- — Digital processing of tracking, focus, sled, and spindle servos
- — Automatic adjustment functions: Focus gain, focus bias, focus offset, tracking gain, tracking offset, tracking balance
- — Use of Sanyo's original high-performance servo control technology* to improve playability, covering external vibration and playback of warped or eccentric discs
- — Shock detection
- — Interruption detection

* Robust control technology developed by Sanyo, offering remarkable ability to suppress vibration and shocks, and to achieve tracking of warped or eccentric discs

■ EFM processing block

- — Error detection and correction (C1 = twofold, C2 = fourfold/twofold)
- — Jitter margin: ± 13 frames
- — DOUT output
- — Built-in text decoder
- — EFM signal synchronization detection, protection, interpolation

■ Audio processing block

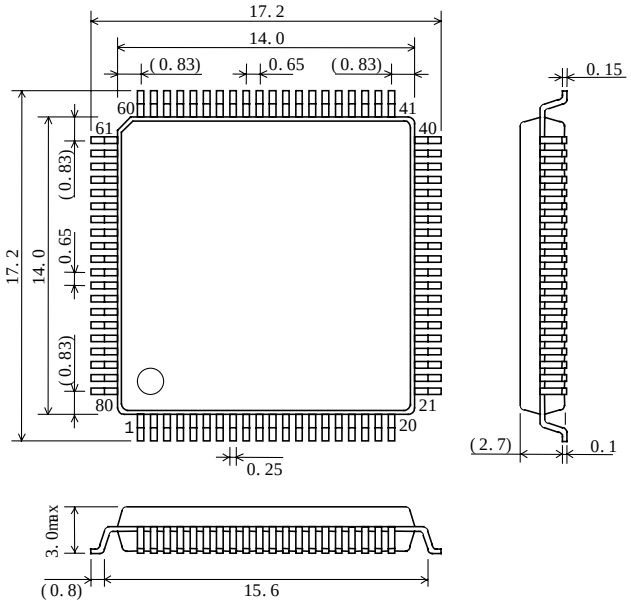
- — Interpolation (4 interpolations)
- — Digital attenuator
- — Built-in de-emphasis filter
- — 1-bit DAC (tertiary $\Delta\Sigma$ noise shaper system)
- — Built-in 8X oversampling digital filter
- — Fadeout function
- — Bilingual function
- — Built-in secondary LPF for audio output
- — DF and DAC clocks can be supplied externally

■ Power supply voltage and package

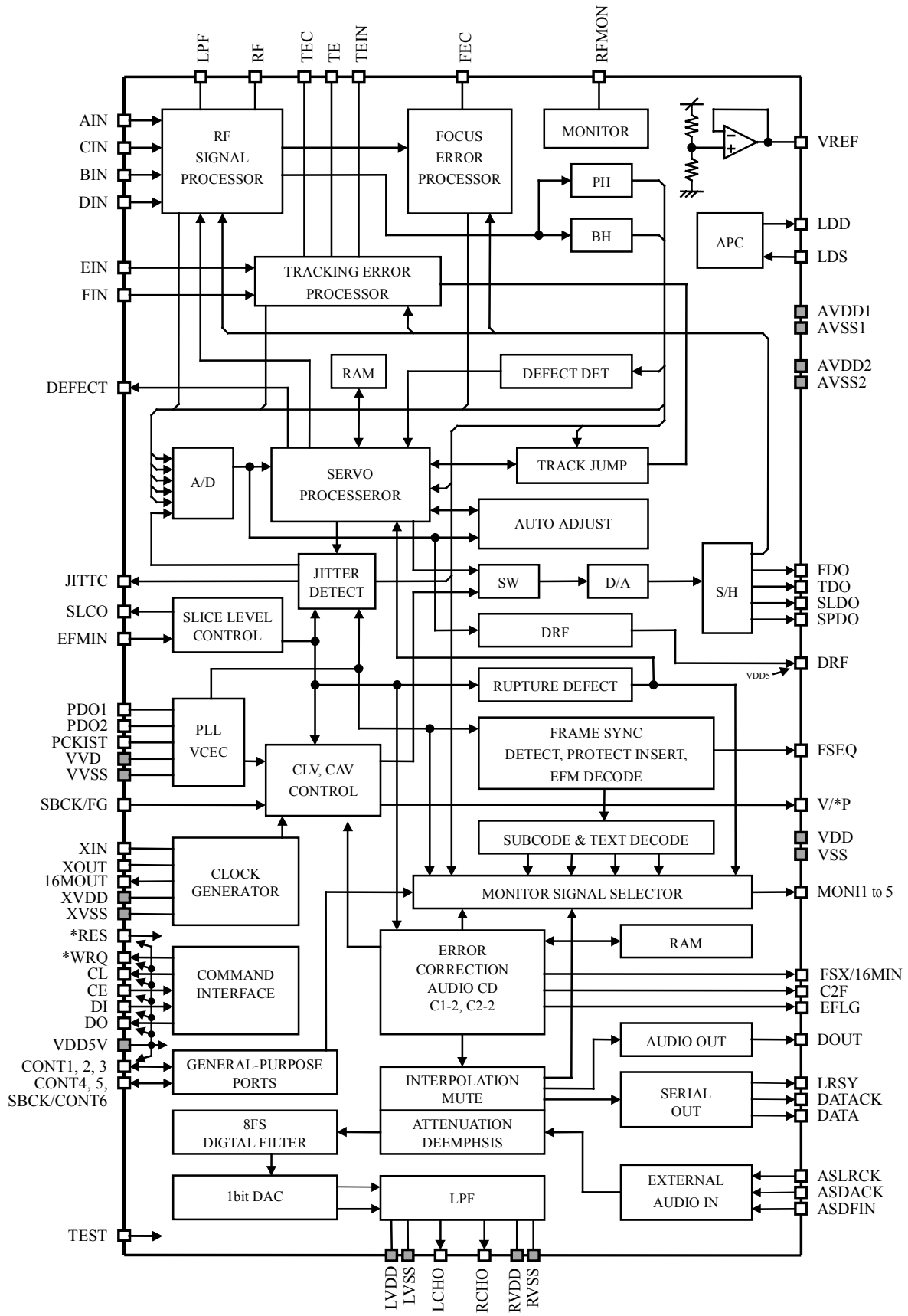
— Package
80-pin flat package

— Power supply voltage: 3.3 V
(5 V interface to microcomputer possible)

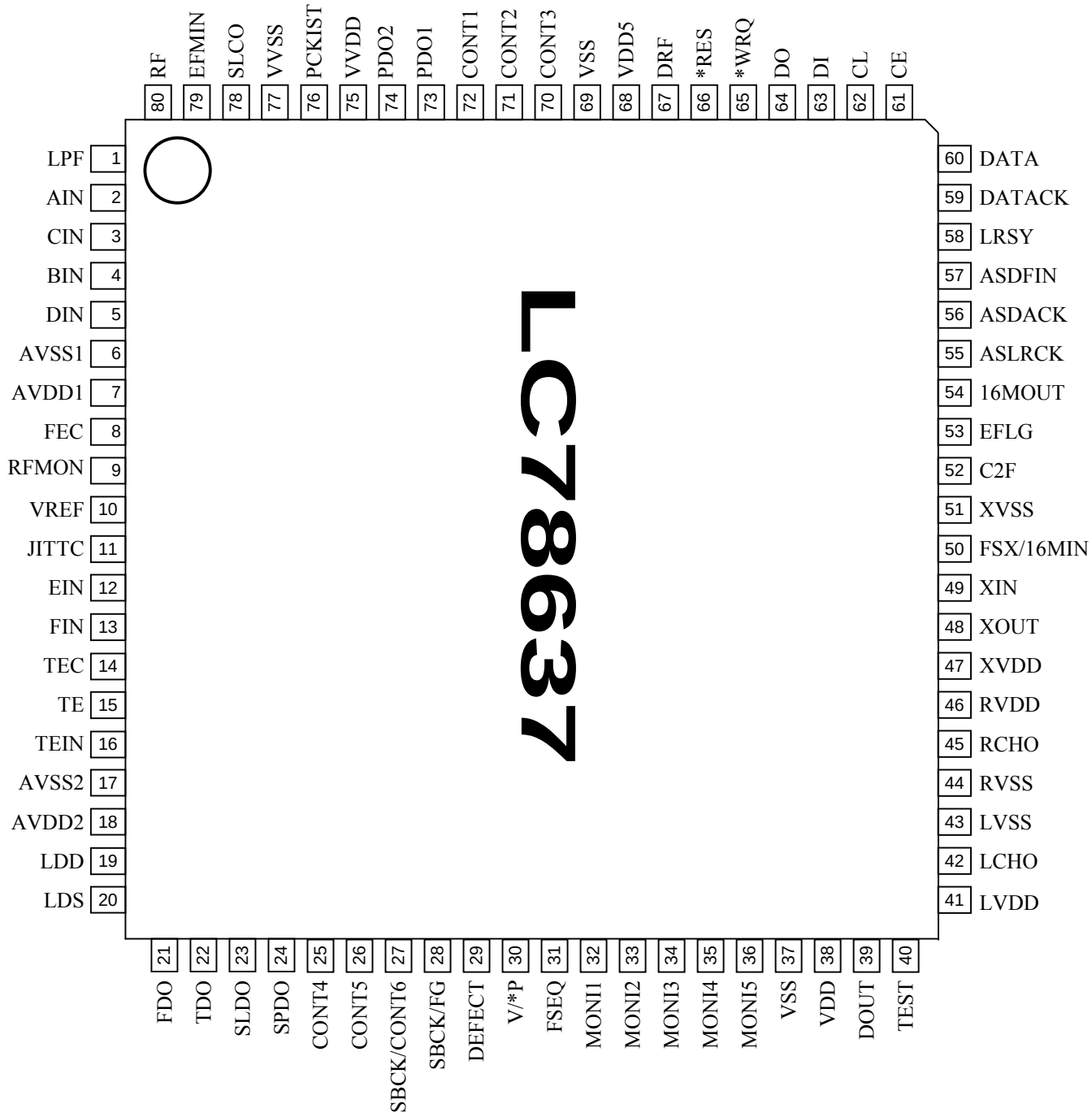
— Package Dimensions (unit: mm) SANYO: QFP80 (14×14)



■ Block Diagram



■ Pin Layout



■ Absolute Maximum Ratings/Ta = 25 °C, Vss = 0 V

Item	Symbol	Conditions	Rating	Unit
Maximum power supply voltage	V_{DD3max}		V_{SS}–0.3 to V_{SS}+4.0	V
	V_{DD5max}		V_{SS}–0.3 to V_{SS}+6.0	V
Input voltage	V_{IN3}		V_{SS}–0.3 to V_{DD3}+0.3	V
	V_{IN5}		V_{SS}–0.3 to V_{DD5}+0.3	V
Output voltage	V_{OUT3}		V_{SS}–0.3 to V_{DD3}+0.3	V
	V_{OUT5}		V_{SS}–0.3 to V_{DD5}+0.3	V
Allowable power dissipation	P_{dmax}		540	mW
Operating ambient temperature	T_{opg}		–20 to +75	°C
Storage ambient temperature	T_{stg}		–40 to +125	°C

■ Allowable Operating Ranges/Ta = 25 °C, Vss = 0 V

Item	Symbol	Pin Name	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD3}	V_{DD}, XV_{DD}, LV_{DD}, RV_{DD}, VV_{DD}, $AV_{DD}1$, $AV_{DD}2$		3.0	3.3	3.6	V
	V_{DD5}	$V_{DD}5$		3.0		5.5	V
"H" level input voltage	$V_{IH3}(1)$	SBCK/FG, CONT4 to 5, SBCK/CONT6, TEST, ASLRCK, ASDATA, ASDFIN		$0.7V_{DD3}$		V_{DD3}	V
	$V_{IH3}(2)$	EFMIN		$0.6V_{DD3}$		V_{DD3}	V
	$V_{IH5}(1)$	CE, CL, DI, *RES		$0.8V_{DD5}$		V_{DD5}	V
	$V_{IH5}(2)$	CONT1 to 3		$0.7V_{DD5}$		V_{DD5}	V
"L" level input voltage	$V_{IL3}(1)$	SBCK/FG, CONT4 to 5, SBCK/CONT6, TEST, ASLRCK, ASDATA, ASDFIN		0		$0.2V_{DD3}$	V
	$V_{IL3}(2)$	EFMIN		0		$0.4V_{DD3}$	V
	$V_{IL5}(1)$	CE, CL, DI, *RES		0		$0.2V_{DD5}$	V
	$V_{IL5}(2)$	CONT1 to 3		0		$0.3V_{DD5}$	V
Data/CE setup time	t_{SU}	CL, DI, CE	Fig. 1, 2	400			ns
Data/CE hold time	t_{HD}	CL, DI, CE	Fig. 1, 2	400			ns
"H" level clock pulse width	t_{WH}	SBCK/FG, SBCK/CONT6, CL	Fig. 1, 2, 3	400			ns
"L" level clock pulse width	t_{WL}	SBCK/FG, SBCK/CONT6, CL	Fig. 1, 2, 3	400			ns
Data read access time	t_{RAC}	DO, MONI5 (PW signal)	Fig. 1, 2, 3, 4	0		400	ns
Command sending time	t_{CE}	CE	Fig. 1, 2	1			µs
RAM read command sending time	t_{CERAM}	CE	Fig. 2	12			µs
Subcode read cycle time	t_{SC}	MONI3 (SFSY signal)	Fig. 3		136		µs
Subcode read enable time	t_{SE}	MONI3 (SFSY signal)	Fig. 3	400			ns
Port input data setup time	t_{CSU}	CONT1 to CONT5, SBCK/CONT6, CL	Fig. 4	400			ns
Port input data hold time	t_{CHD}	CONT1 to CONT5, SBCK/CONT6, CL	Fig. 4	400			ns
Port output data delay time	t_{CDD}	CONT1 to CONT5, SBCK/CONT6, CE	Fig. 5			1200	ns
Operating frequency range	f_{OP}	EFMIN				10	MHz
Crystal oscillation frequency	fX	X_{IN}, X_{OUT}			16.9344		MHz

■ Electrical Characteristics/Ta = 25 °C, V_{DD} = 3.3 V, Vss = 0 V

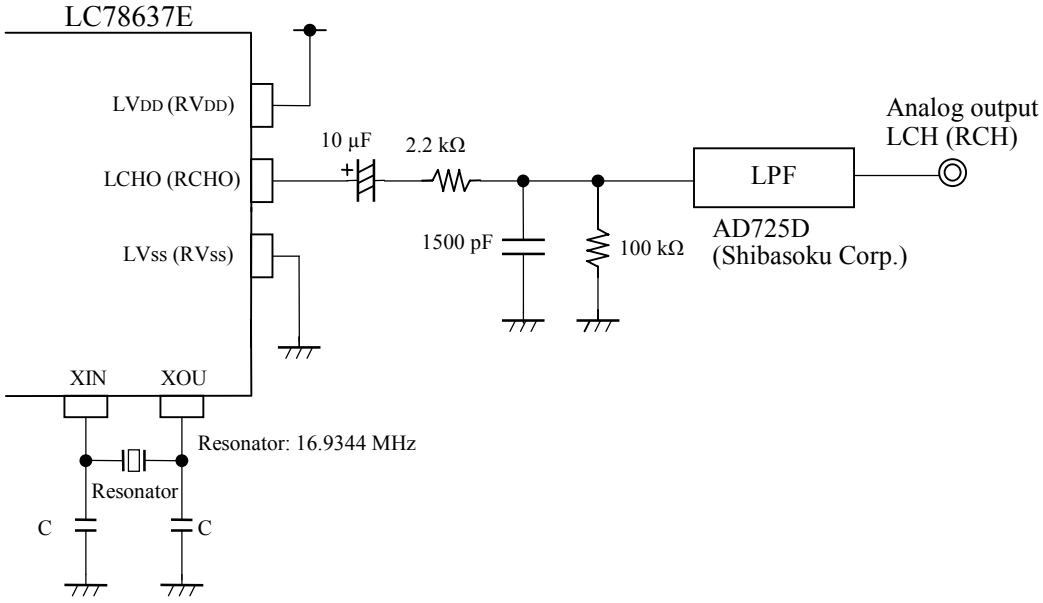
Item	Symbol	Pin Name	Conditions	Min.	Typ.	Max.	Unit
Current dissipation	I_{DD}	V_{DD}, XV_{DD}, LV_{DD}, RV_{DD}, VV_{DD}, $AV_{DD}1$, $RFV_{DD}2$			75	100	mA
"H" level input current	I_{IH3}	SBCK/FG, CONT4 to 5, SBCK/CONT6, TEST, ASLRCK, ASDATA, ASDFIN	V_{IN} = 3.6 V			10	µA
	I_{IH5}	CE, CL, DI, *RES, CONT1 to 3	V_{IN} = V_{DD5V} = 5.5 V			10	µA
"L" level input current	I_{IL3}	SBCK/FG, CONT4 to 5, SBCK/CONT6, TEST, ASLRCK, ASDATA, ASDFIN	V_{IN} = 0 V	–10			µA
	V_{IL5}	CE, CL, DI, *RES, CONT1 to 3	V_{IN} = 0 V	–10			µA
"H" level output voltage	V_{OH3a}	CONT4 to 5, SBCK/CONT6, C2F, EFLG, FSX/16MIN, MONI1 to 5, LRSY, DATA, DATACK, 16MOUT, V/*P, FSEQ, DEFECT,	I_{OH} = –2 mA	V_{DD3} – 0.4			V
	V_{OH3b}	DOUT	I_{OH} = – 4 mA	V_{DD3} – 0.4			V
	V_{OH5}	DO, *WRQ, DRF, CONT1 to 3	I_{OH} = –1.5 mA	V_{DD5} – 0.4			V
"L" level output voltage	V_{OL3a}	CONT4 to 5, SBCK/CONT6, C2F, EFLG, FSX/16MIN, MONI1 to 5, LRSY, DATA, DATACK, 16MOUT, V/*P, FSEQ, DEFECT,	I_{OL} = 2 mA			0.4	V
	V_{OL3b}	DOUT	I_{OL} = 4 mA			0.4	V
	V_{OL5}	DO, *WRQ, DRF, CONT1 to 3	I_{OL} = 1.5 mA			0.4	V
Output leakage current	I_{OFF3}	CONT4 to 5, SBCK/CONT6	High-impedance output	–10		10	µA
	I_{OFF5}	CONT1 to 3	High-impedance output	–10		10	µA
Charge pump output current	I_{PDOH}	PDO1, 2	R_{ISET} = 120 kΩ	48	60	72	µA
	I_{PDOL}	Charge pump current setting = 1×		–72	–60	–48	µA

■ 1-Bit DAC Block Analog Characteristics/Ta = 25 °C, V_{DD} = LV_{DD} = RV_{DD} = 3.3 V, V_{SS} = LV_{SS} = RV_{SS} = 0 V

Item	Symbol	Pin Name	Conditions	Min.	Typ.	Max.	Unit
Output level	LEVEL	LCHO, RCHO	1 kHz: 0 dB data input		0.63		Vrms
Total harmonic distortion factor	THD+N	LCHO, RCHO	1 kHz: 0 dB data input, 20 kHz-LPF used (incorporated in AD725D)		0.012	0.015	%
D range	DR	LCHO, RCHO	1 kHz: –60 dB data input, 20 kHz-LPF, A filter used (incorporated in AD725D)	92	96		dB
Signal-to-noise ratio	S/N	LCHO, RCHO	1 kHz: 0 dB data input, 20 kHz-LPF, A filter used (incorporated in AD725D)	95	98		dB
Crosstalk	CT	LCHO, RCHO	1 kHz: 0 dB data input, 20 kHz-LPF used (incorporated in AD725D)	82	85		dB

* Measurements in normal-speed playback mode in Sanyo 1-bit DAC block reference circuit

1-Bit DAC Block Reference Circuit



■ Data Transmission/Reception

Figure 1 Command Input / Data Output

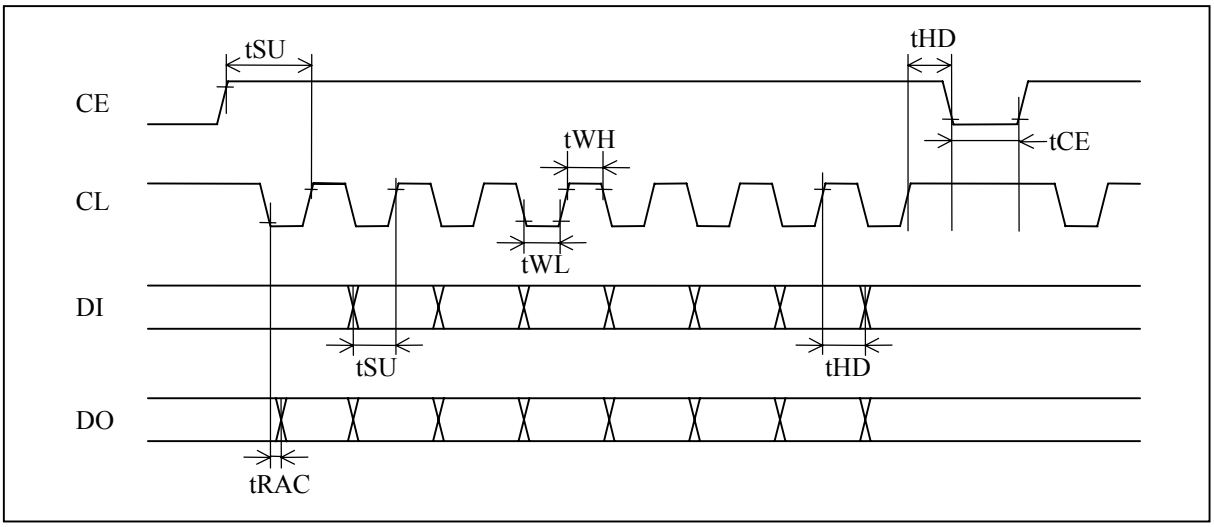


Figure 2 RAM Read Command Input / Data Output

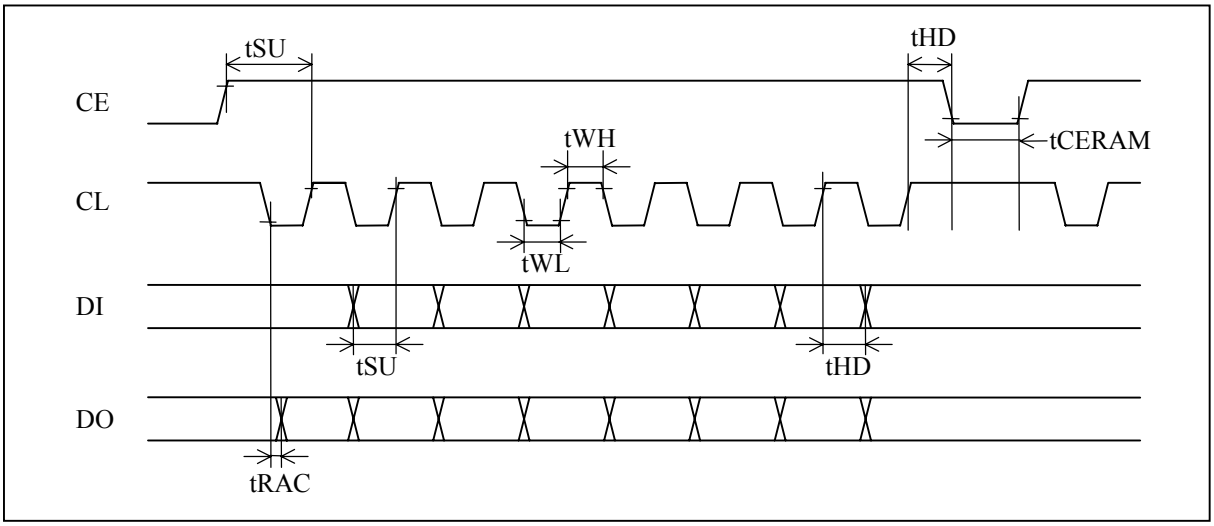


Figure 3 Subcode Output

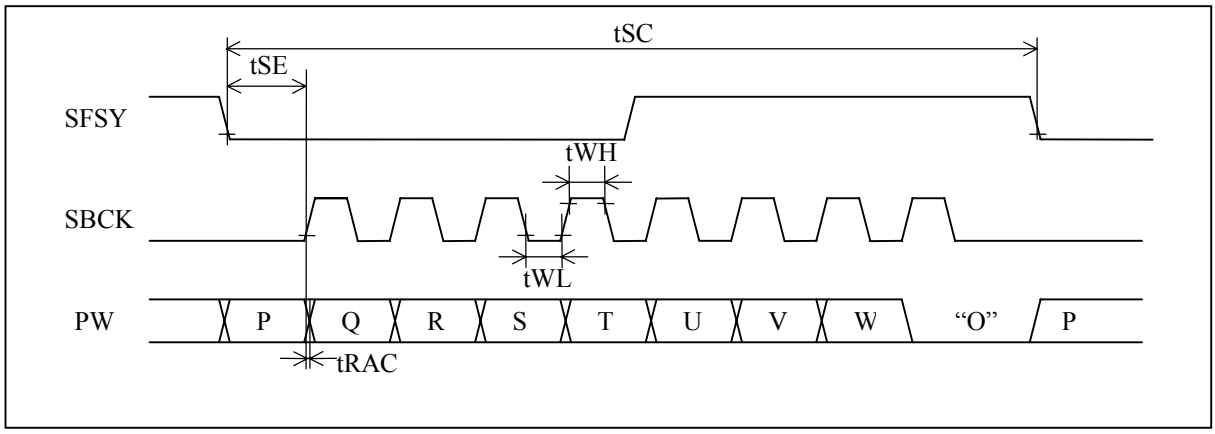


Figure 4 General-Purpose Port Input Timing

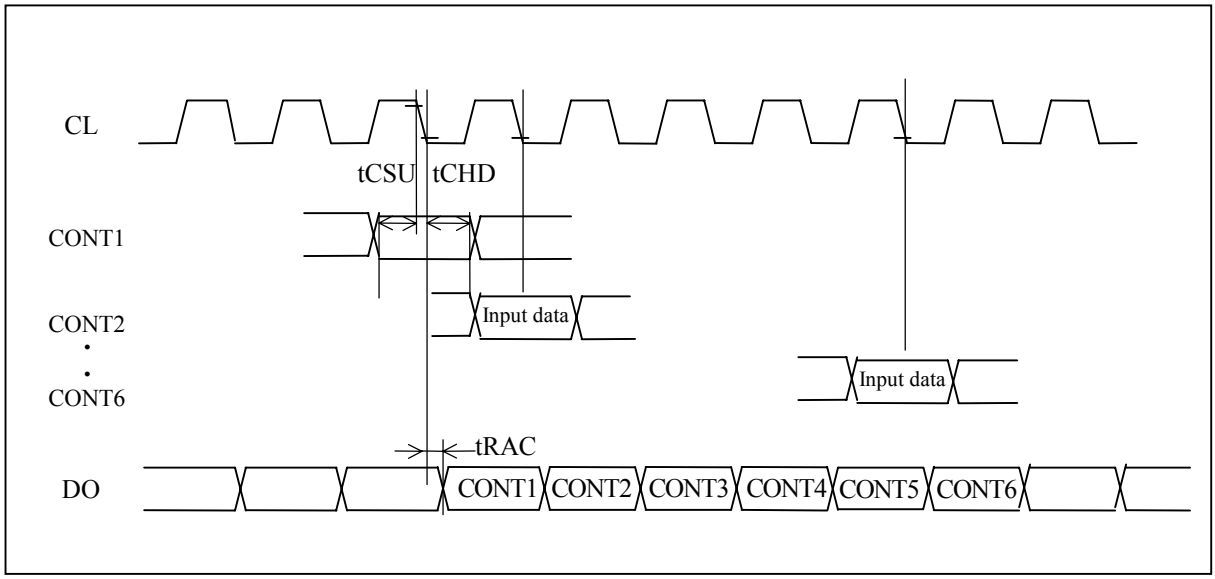
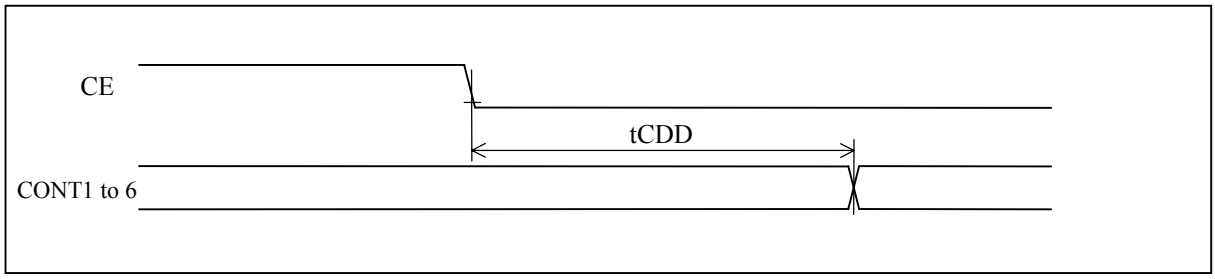


Figure 5 General-Purpose Port Output Timing



■ Pin Function Table

Pin No.	Pin Name	I/O	State after Reset	Function	
1	LPF	AO	—	RF signal DC level detection LPF capacitor connection pin	
2	AIN	AI	—	A signal input pin	
3	CIN	AI	—	C signal input pin	
4	BIN	AI	—	B signal input pin	
5	DIN	AI	—	D signal input pin	
6	AVSS1	—	—	Analog ground pin 1. Must be connected to 0V.	
7	AVDD1	—	—	Analog power supply pin 1	
8	FEC	AO	—	FE signal LPF capacitor connection pin	
9	RFMON	AO	ZHI	IC internal analog signal monitor pin	
10	VREF	AO	RFVDD /2	VREF voltage output pin	
11	JITTC	AI	—	Jitter detection capacitor connection pin	
12	EIN	AI	—	E signal input pin	
13	FIN	AI	—	F signal input pin	
14	TEC	AO	—	TE signal LPF capacitor connection pin	
15	TE	AO	—	TE signal output pin	
16	TEIN	AI	—	TES signal generation TE signal input pin	
17	AVSS2	—	—	Analog ground pin 2. Must be connected to 0V.	
18	AVDD2	—	—	Analog power supply pin 2	
19	LDD	AO	ADAVDD	Laser power control signal output pin	
20	LDS	AI	—	Laser power detection signal input pin	
21	FDO	AO	ADAVDD /2	Focus control signal output pin. D/A output	
22	TDO	AO	ADAVDD /2	Tracking control signal output pin. D/A output	
23	SLDO	AO	ADAVDD /2	Thread control signal output pin. D/A output	
24	SPDO	AO	ADAVDD /2	Spindle control signal output pin. D/A output	
25	CONT4	I/O	Input	General-purpose I/O pin 4	Controlled by command from microcomputer. When not used, set as input pin and connect to 0V or set as output pin and leave open.
26	CONT5	I/O	Input	General-purpose I/O pin 5	
27	SBCK/ CONT6	I/O	Input	General-purpose I/O pin 6, or subcode read clock input pin	
28	SBCK/FG	I	—	Subcode read clock input pin / FG signal input pin / external emphasis setting pin Set pin function with a command. When not used, connect to 0V.	
29	DEFECT	O	L	Defect pin	
30	V/∗P	O	H	Rough servo/phase control automatic switching monitor output pin. “H”: Rough servo, “L”: Phase servo	
31	FSEQ	O	L	Detected synchronization signal output pin “H” when synchronization signal detected from EFM signal and internally generated synchronization signal match.	
32	MONI1	O	L	Internal signal monitor pin 1	
33	MONI2	O	L	Internal signal monitor pin 2	
34	MONI3	O	L	Internal signal monitor pin 3	
35	MONI4	O	L	Internal signal monitor pin 4	
36	MONI5	O	L	Internal signal monitor pin 5	
37	VSS	—	—	Digital ground pin. Must be connected to 0V.	
38	VDD	—	—	Digital power supply pin	
39	DOUT	O	L	Digital OUT output pin. EIAJ format	
40	TEST	I	L	Test input pin. Must be connected to 0V.	

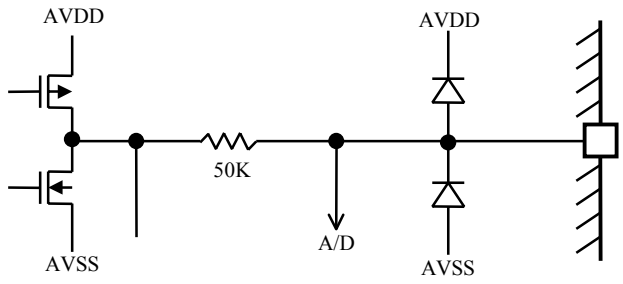
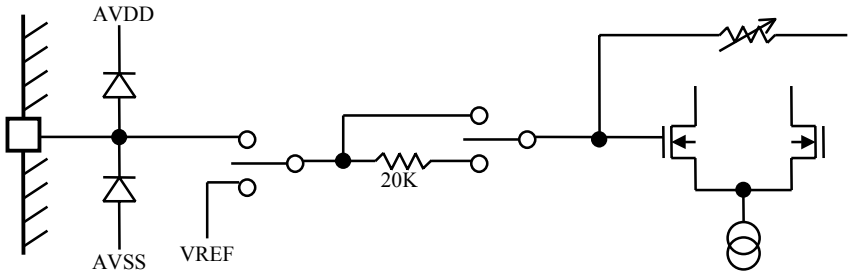
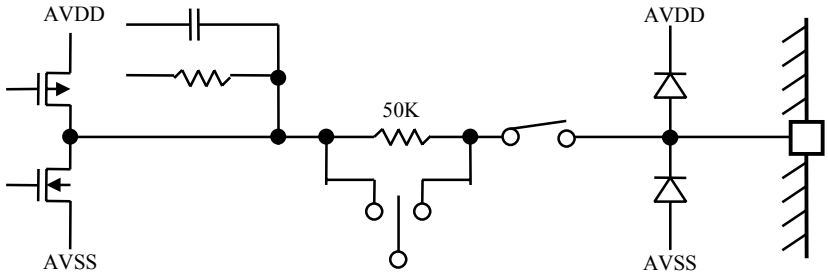
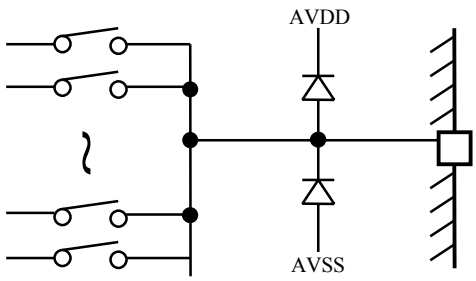
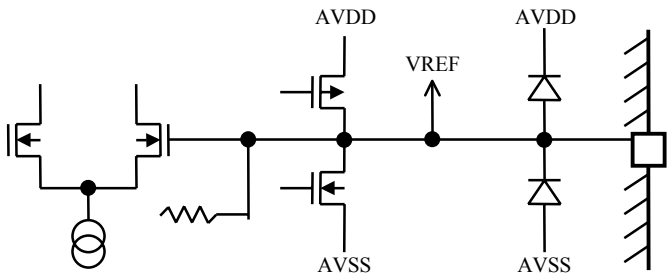
Pin No.	Pin Name	I/O	State after Reset	Function	
41	LVDD	—	—	L channel D/A converter	L channel power supply pin
42	LCHO	AO	LVDD /2		L channel output pin
43	LVSS	—	—		L channel ground pin. Must be connected to 0V.
44	RVSS	—	—	R channel D/A converter	R channel ground pin. Must be connected to 0V.
45	RCHO	AO	LVDD /2		R channel output pin
46	RVDD	—	—		R channel power supply pin
47	XVDD	—	—	For crystal oscillation	Crystal oscillation power supply pin
48	XOUT	O	Oscillation		16.9344 MHz resonator connection pins
49	XIN	I	Oscillation		
50	FSX/16MIN	I/O	Input mode	7.35 kHz synchronization signal output pin, or DF/DAC external clock input pin	
51	XVSS	—	—	For crystal oscillation	Crystal oscillation ground pin. Must be connected to 0V.
52	C2F	O	H	C2 flag output pin	
53	EFLG	O	L	C1, C2 correction monitor pin	
54	16MOUT	O	CLK output	16.9344 MHz output pin	
55	ASLRCK	I	—	For anti-shock mode	L/R clock input pin. (Connect to 0 V when not used.)
56	ASDACK	I	—		Bit clock input pin. (Connect to 0 V when not used.)
57	ASDFIN	I	—		L/R channel data input pin. (Connect to 0 V when not used.)
58	LRSY	O	L	For digital data output	L/R clock output pin
59	DATACK	O	L		Bit clock output pin
60	DATA	O	L		L/R channel data output pin
61	CE	I	—	For microcomputer interface	Chip enable signal input pin
62	CL	I	—		Data transfer clock input pin
63	DI	I	—		Data input pin
64	DO	O	(H)		Data output pin (Nch open-drain output)
65	∗WRQ	O	H		Interrupt signal output pin
66	∗RES	I	—	LC78637E IC reset input pin. Drive to “L” level at power-on.	
67	DRF	O	L	Focus ON detection pin	
68	VDD5	—	—	Microcomputer interface power supply pin	
69	VSS	—	—	Digital ground pin. Must be connected to 0 V.	
70	CONT3	I/O	Input mode	General-purpose I/O pin 3	Controlled by command from microcomputer. When not used, set as input pin and connect to 0V or set as output pin and leave open.
71	CONT2	I/O	Input mode	General-purpose I/O pin 2	
72	CONT1	I/O	Input mode	General-purpose I/O pin 1	
73	PDO1	O	—	For PLL	Built-in VCO control phase comparator output pin 1
74	PDO2	O	—		Built-in VCO control phase comparator output pin 2
75	VVDD	—	—		Built-in VCO power supply pin
76	PCKIST	AI	—		PDO1, PDO2 output current setting resistor connection pin
77	VVSS	—	—		Built-in VCO ground pin. Must be connected to 0V.
78	SLCO	AO	—	For slice level control	Slice level control output pin
79	EFMIN	AI	—		RF signal input pin
80	RF	AO	—	RF signal output pin	

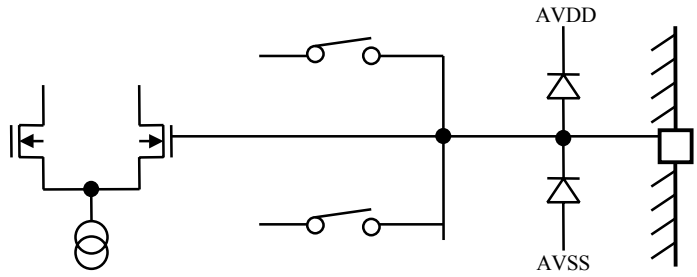
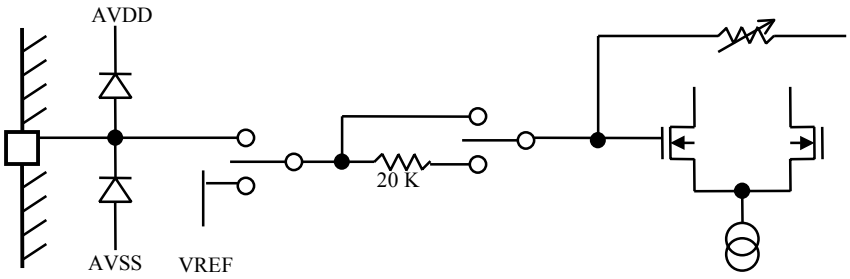
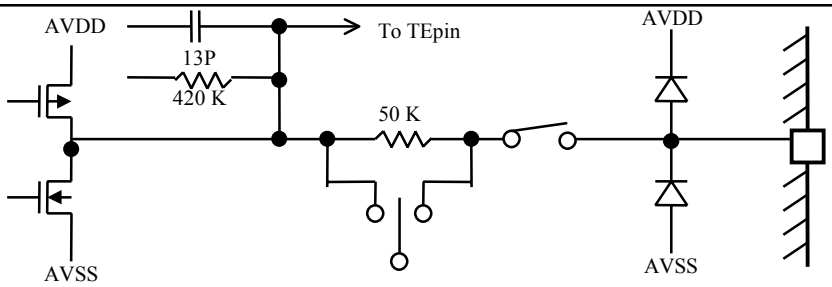
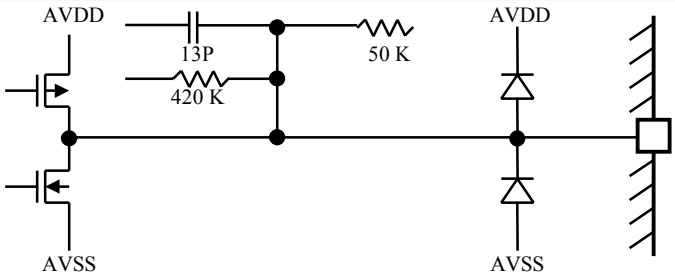
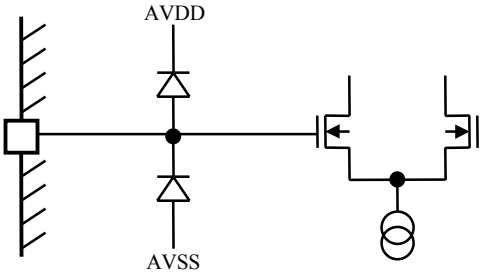
Note: The same potential must be applied to all power supply pins ($AV_{DD}1$, $AV_{DD}2$, VV_{DD}, V_{DD}, LV_{DD}, RV_{DD}, XV_{DD}).

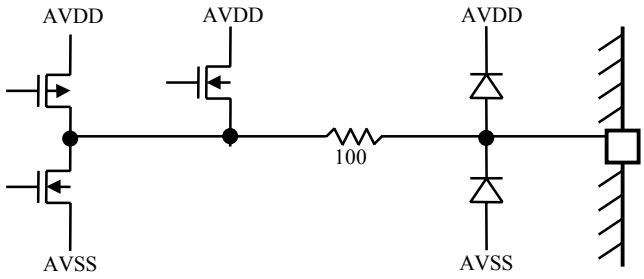
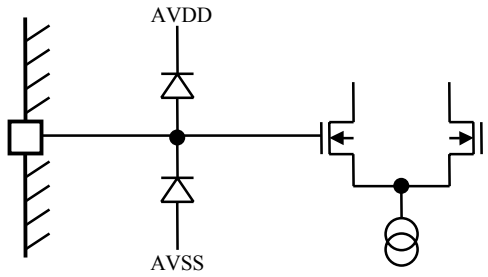
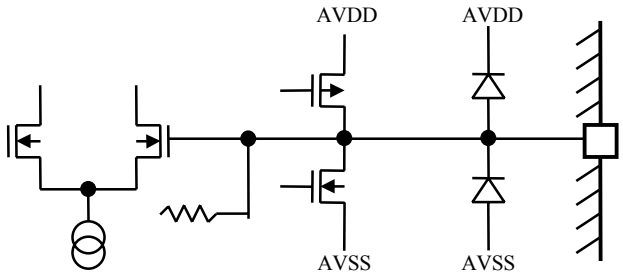
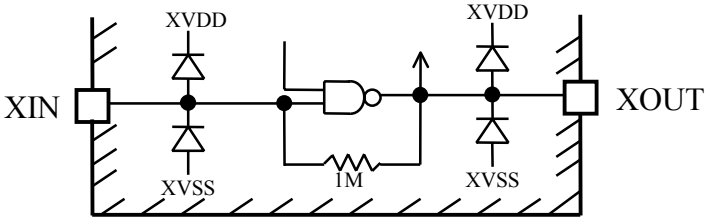
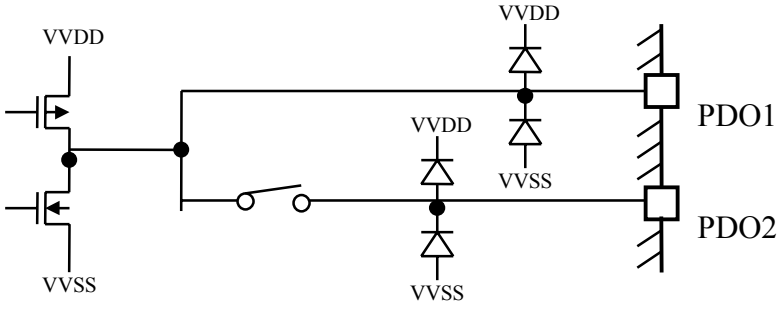
Pins operating on microcomputer interface power supply pin ($V_{DD}5V$):

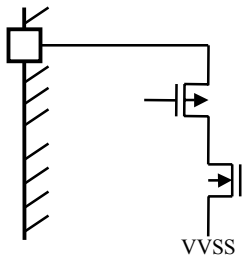
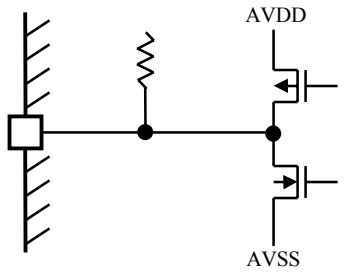
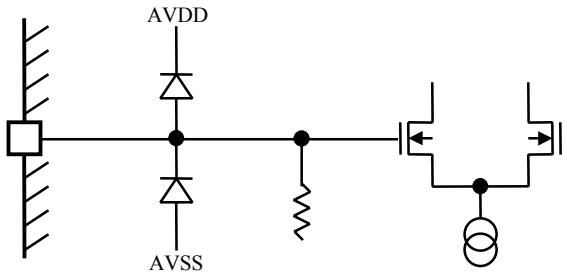
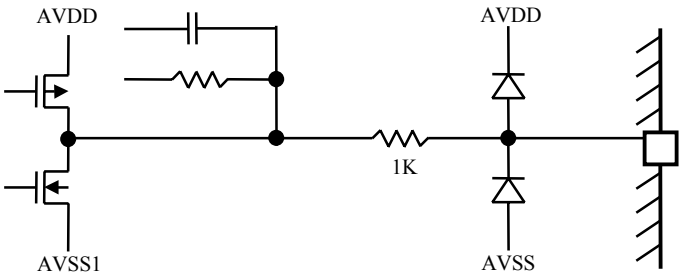
CE (pin 61), CL (pin 62), DI (pin 63), DO (pin 64), *WRQ (pin 65), *RES (pin 66), DRF (pin 67), CONT1 (pin 72), CONT2 (pin 71), CONT3 (pin 70)

■ Analog Pin Internal Equivalent Circuits

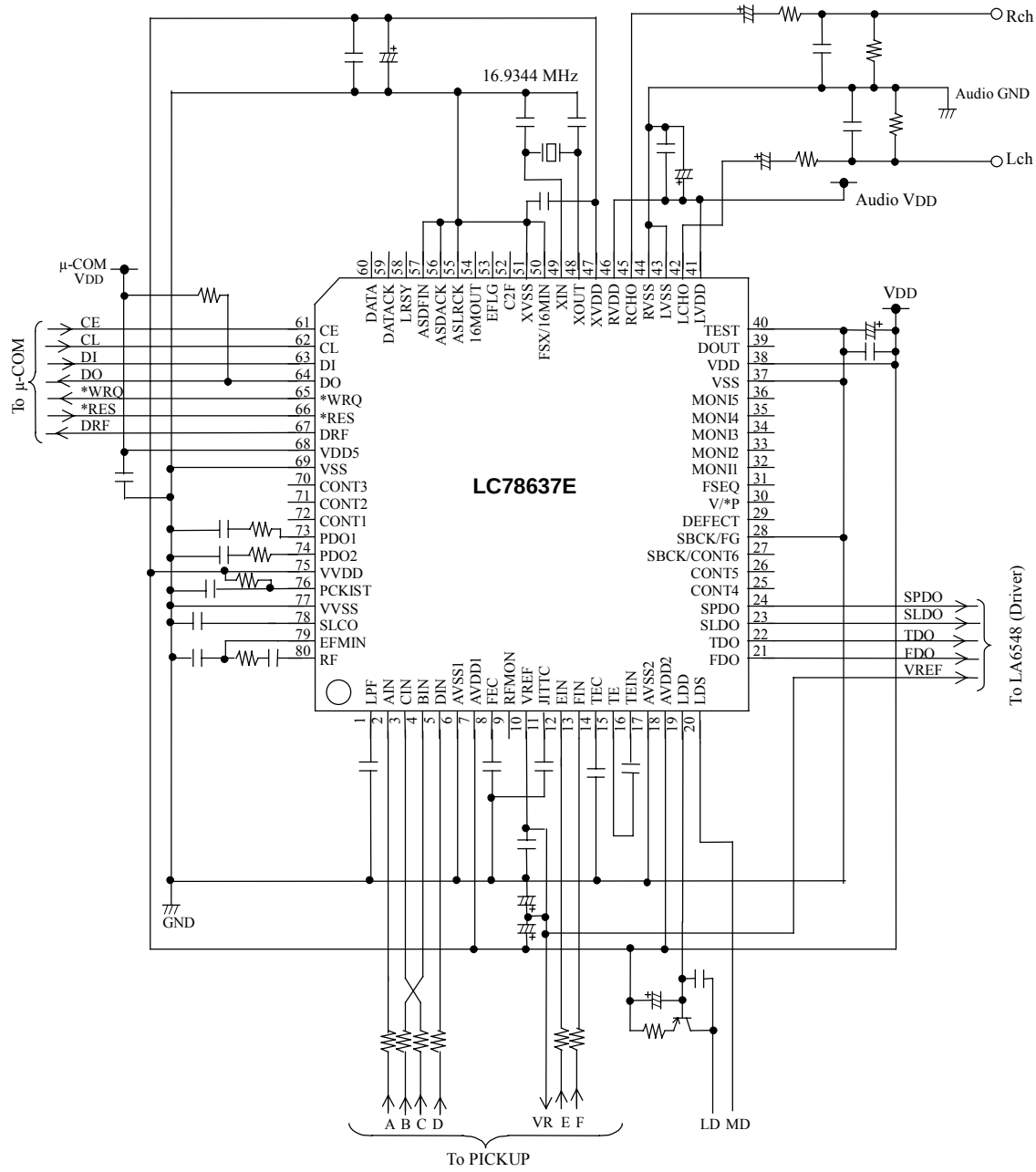
Pin Name (Pin No.)	Internal Equivalent Circuit
LPF (1)	
AIN (2) CIN (3) BIN (4) DIN (5)	
FEC (8)	
RFMON (9)	
VREF (10)	

Pin Name (Pin No.)	Internal Equivalent Circuit
JITTC (11)	
EIN (12) FIN (13)	
TEC (14)	
TE (15)	
TEIN (16)	

Pin Name (Pin No.)	Internal Equivalent Circuit
LDD (19)	
LDS (20)	
FDO (21) TDO (22) SLDO (23) SPDO (24)	
XOUT (48) XIN (49)	
PDO1 (73) PDO2 (74)	

Pin Name (Pin No.)	Internal Equivalent Circuit
PCKIST (76)	
SLCO (78)	
EFMIN (79)	
RF (80)	

■ Application Circuit Example



■ CD-DSP Function Comparison

Model / Function	LC78637E	LC78646E	LC78641NE	LC78636E	LC78626E (LC78626KE)	LC78622E	LC78622NE	LC78628E
Servo	D servo	D servo	D servo	D servo	A servo	A servo		A servo
RF amp/ASP	On-chip	On-chip	LA9235M	LA9235M	LA9241/50M	LA9241/50M		LA9241/50M
EFM-PLL	VCO on-chip	VCO on-chip	VCO on-chip	VCO on-chip	VCO on-chip	VCO on-chip		VCO on-chip
RAM	20 K	20 K	18 K	18 K	16 K	16 K		16 K
Error correction	C1 = twofold C2 = twofold/ fourfold	C1 = twofold C2 = twofold	C1 = twofold C2 = twofold	C1 = twofold C2 = fourfold	C1 = twofold C2 = twofold	C1 = twofold C2 = twofold		C1 = twofold C2 = twofold
Playback speed	2×	2×	4×	4×	2×	2×		2×
Digital OUT	○	○	○	○	○	○		○
Inter-polation	4	4	4	4	2	2		4
Zero-cross mute	○ –12dB, –∞	○ –12dB, –∞	○ –12dB, –∞	○ –12dB, –∞	○ –∞	○ –∞		○ –12dB, –∞
Digital attenuator	○	○	○	○	○	○		○
Digital filter	8fs	8fs	8fs	8fs	4fs (8fs)	4fs	8fs	8fs
Digital de-emphasis	○	○	○	○	○	○		○
General-purpose ports: Output	×	×	×	×	×	×	(3)	×
General-purpose ports: Input/ output	6	6	7	7	1 + (3)	5		5
VCD support	○	○	○	○	×	×		○
Anti-shock I/F	○	○	○	○	Not necessary	×		○
Anti-shock controller	×	×	×	×	○ max 4-M DRAM (max 16-M DRAM)	×		×
HDCD	×	×	×	×	×	×		○
CD text	○	×	×	×	×	×		○
CD-ROM I/F	○	○	○	○	×	×		○
1-bit DAC	○	○	○	○	○	○		○
L.P.F	○	○	○	○	○	○		×
Power supply voltage	3.0 to 3.6 (I/F: 3.0 to 5.5 V	3.0 to 3.6 (I/F: 3.0 to 5.5 V)	3.0 to 3.6 (I/F: 3.0 to 5.5 V)	3.0 to 3.6 (I/F: 3.0 to 5.5 V)	3.0 to 5.5 V (3.0 to 3.6 V)	3.0 to 5.5 V	3.6 to 5.5 V	3.0 to 3.6 V (External: 4.5 to 5.5 V)
Package	QFP80	QFP80	QIP80E	QIP80E	QIP100E	QIP64E		QIP80E

■ Notes on Application Design

It goes without saying that applications must strictly observe the absolute maximum ratings and allowable operating ranges (recommended operating conditions) stipulated for this IC to achieve reliability as a system. However, we also strongly recommend that designers carefully consider both the mounting conditions and the actual usage environment, including ambient temperatures and static electricity, when designing applications.

This section provides additional notes concerning design, mounting, and certain other points that require care during application design.

1. Handling of Unused Pins

   — If any unused pins on this IC are left in the open state, certain internal states may become undefined. Unused pins for which the handling is specified in the documentation must be handled as specified. Also be sure that no output pins contact any power supply or ground lines or any other output pin.

   — If an input/output pin is not used, either set it as an output pin or fix the input level by pull-up or pull-down with an input setting.

2. Latch-Up Prevention

   — The same potential must be applied to all power supply pins on this IC (except power supply pins that are completely isolated within the IC).

   — The IC may latch up if timing discrepancies appear between the rise times for different power supply pins. Design applications so that no such discrepancies appear.

   — Ensure that pin voltage levels are within the absolute maximum ratings and allowable operating ranges. This point requires special care when power is first applied.

   — Do not allow overvoltages or abnormal signal noise levels to be applied to this IC.

   — In general, latch-up can be prevented by tying unused pins to VDD or VSS. However, the directions for unused pin handling in the documentation for this IC must be followed.

   — Do not short the outputs.

3. Interface

   When different devices are connected, incorrect operation may result if the input VIL and VIH and the output VOL and VOH levels do not match. Insert level shifters so that the IC is not destroyed if it is connected to a device that uses a different power supply voltage, such as in a dual power supply system application.

4. Load Capacitance and Output Current

   — If a load with a large capacitance is connected, the wiring may fuse since such a load can result in the equivalent of an output short for an extended period. Also, excessive charge and discharge currents can cause noise and degrade application performance or lead to incorrect operation. Use loads of the recommended capacitance.

   — Excessive output sink or source currents can lead to problems similar to those described above. Use this IC within the recommended current levels while also taking the maximum allowable power dissipation into consideration.

5. Notes on Power Application and Resets

   — There are cases where care is required at power on, during a reset, and when the reset state is cleared. Refer to the specification sheet for the product and observe the notes concerning power on and IC resets.

   — Output pin states, pin I/O direction settings, and register contents are undefined when power is first applied to this IC. Items that are defined by the reset operation and when the mode is set are guaranteed after that operation. Applications must first apply a reset to this IC after power is applied. Since pin states and register contents that are not defined by the reset operation may change over time from the states in early versions due to long term variations across lots, applications should not depend on these values.

   — General-purpose I/O pins function as input pins after a reset. When the level is fixed high or low with an input setting, pull-up or pull-down via a resistance is valid individually from the failsafe point.

6. Notes on Thermal Design

   The failure rate of semiconductor devices is accelerated by higher ambient temperatures and power dissipation levels. We strongly recommend taking changes in ambient conditions into account and providing as large a margin as possible in thermal design to assure high reliability.

7. Notes on Printed Circuit Board Design Patterns

   — Ideally, the influence of shared impedances should be minimized by separating the VDD and ground lines for each system.

   — Design VDD and ground lines to be as short and wide as possible, and to have the lowest high-frequency impedance possible. Ideally, decoupling capacitors (0.01 to 1 μF) should be inserted in each VDD/ground pair. These capacitors should be placed as close to the corresponding VDD pin as possible. It is also appropriate to insert capacitors of about 100 to 220 μF between each VDD and ground as low-frequency filters. However, be careful not to use values that are too large for these capacitors, since this can result in latch-up.

     - In the servo system, the reference voltage line (VREF) and the driver VCC and ground lines are handled in the same way. The driver ground should be made especially wide. If at all possible, use the recommended driver pattern, which, being directly under the device, was also designed to provide a heat dissipation effect as well.

     - If a current output pickup is used, locate the optimal pickup element and the connector and the AIN, BIN, CIN and DIN pins as close together as possible. Even if a voltage output type pickup is used, the I/V conversion resistor connected to the AIN, BIN, CIN and DIN pins should be located near these pins.

   — The EFM signal line should be made as short as possible, and should either be located away from adjacent lines or should be shielded from adjacent lines by VSS or VDD shield lines.

   — Noise on the microcomputer interface can cause incorrect operation. In general, interface lines should be kept short to minimize inductance and capacitance. However, care must be taken concerning crosstalk. When interface lines are long or when there is a large amount of external noise, insertion of a noise cancellation circuit is effective. A filter should be used that takes interface timing into consideration.

   — Cover the area around the crystal with the ground pattern.

8. Notes on Software Design

   — Any prohibitions or recommendations concerning the software design phase given in the documentation should be observed.

   — When using digital OUT, if UBIT OFF is set initially, this is effective for DIR unlocking prevention and prevention of subcode misidentification. Set UBIT ON only for playback.

9. Other Notes

   If you have any questions during the application design phase, do not hesitate to contact your Sanyo sales representative or the nearest Sanyo semiconductor sales office.

   This IC is specifically designed for use in CD players, and as such its specifications differ from those of general-purpose product standard logic ICs. We recommend system debugging using the end product system itself and adopting failsafe system design if required by the application.

- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

- SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.

- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.

- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.