# LC7860KA, 7863KA

SANYO SEMICONDUCTOR CORP

3044B

CMOS LSI

©3158A

# Digital Signal Processor for Compact Disc Players

## Overview

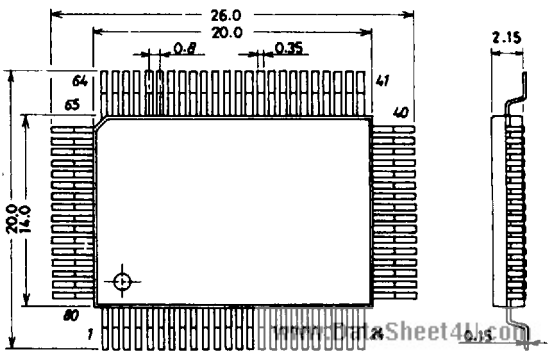
The Sanyo LC7860KA and LC7863KA CMOS Digital Signal Processing LSIs provide servo control and signal processing for the digital audio sections of compact disk and laser disk players. Available in surface-mount 80-pin plastic flat package, the LC7860KA and LC7863KA integrate several Compact Disk player functions into a single chip for reduced system costs. Both devices perform several signal processing functions, including demodulation of the EFM signal from the optical pickup, de-interleave, detection and correction of error signals, and digital filtering for sound quality improvement. In addition, they can process control commands from a microprocessor for the servo system. Both the LC7860KA and LC7863KA can be direct interfaced to the Sanyo LC7880 Serial I/O Digital-to Analog Converter LSI. The difference between LC7860KA and LC7863KA lies in the conditions for reading subcode Q as well as track jumping and the LRCLK timing. For further details, see Notes 1 and 2 (page 9, 10).

## Functions

- When an HF signal is input, it is sliced at the proper level and converted to an EFM signal. Phase comparison with VCO is carried out and a 4.3218MHz (average) phase-locked loop playback clock signal is generated.
- A 4.3218MHz standard clock and necessary internal timing can be generated by connecting an external crystal oscillator.
- Disk motor rotation speed is controlled by the frame phase differential signal generated using the playback and standard clocks.
- Detection, protection, and interpolation of the frame sync signal ensures stable data reading.
- The EFM signal is demodulated and converted to 8-bit symbol data.
- Subcodes are separated from the EFM modulation signal and output to an external microprocessor.
- The subcode Q signal is output to the microprocessor using serial I/O after cyclical redundancy checking. (SLB first out order can be selected.)
- Using external RAM, the EFM modulated signal is buffered to absorb jitter (up to ±4 frames) caused by fluctuations in the disk rotation speed.

Continued on next page.

**Case Outline** 3044B
(unit : mm)




SANYO: QIP80A

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- Unscrambling and de-interleaving is performed by arranging EFM demodulated signal in required order.
- Detection, correction and flag processing for error signals using C1, two-level C2, two-level correction method.
- C2 flag is set by reference to C1 flag and C2 ckeck results, and signal interpolation and previous value hold is performed by C2 flag.
- DAC signal with improved output data continuity is obtained by over-sampling (2×) and digital filtering.
- Functions such as track jump, focus start, disk motor start/stop and muting ON/OFF can be performed using commands from a microprocessor (8-bit serial input).

**Features**

- Compact surface-mount 80-pin plastic flat pack
- Low-power silicon-gate CMOS technology
- Single +5V power supply
- Easily calibrated using DEMO pin

**Absolute Maximum Ratings** at Ta = 25°C, $V_{SS}$ = 0V

| | | | unit |
|---|---|---|---|
| Maximum Supply Voltage | $V_{DD}$ max | $V_{SS}-0.3$ to 7 | V |
| Input Voltage | $V_{IN}$ | $V_{SS}-0.3$ to $V_{DD}+0.3$ | V |
| Output Voltage | $V_{OUT}$ | $V_{SS}-0.3$ to $V_{DD}+0.3$ | V |
| Allowable Power Dissipation | Pd max | 300 | mW |
| Operating Temperature | Topg | −30 to +75 | °C |
| Storage Temperature | Tstg | −40 to +125 | °C |

**Allowable Operating Conditions** at Ta = 25°C, $V_{SS}$ = 0V

| | | | min | typ | max | unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | $V_{DD}$ | 4.5 | | 5.5 | V |
| Input 'H'-Level Voltage | $V_{IH}(1)$ | (TEST1 to 5)AI,$\overline{FZD}$,HFL, DEMO,IOFF,DFOFF, DSPOFF,M/L,MSBF,$\overline{RES}$ | $0.7V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH}(2)$ | DFIN,DB0 to 7,SBCK,RWC, COIN,$\overline{CQCK}$ | 2.2 | | $V_{DD}$ | V |
| | $V_{IH}(3)$ | EFMIN | $0.6V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH}(4)$ | TES | $0.8V_{DD}$ | | $V_{DD}$ | V |
| Input 'L'-Level Voltage | $V_{IL}(1)$ | (TEST1 to 5)AI,$\overline{FZD}$,HFL, DEMO,IOFF,DFOFF, DSPOFF,M/L,MSBF,$\overline{RES}$ | $V_{SS}$ | | $0.3V_{DD}$ | V |
| | $V_{IL}(2)$ | DFIN,DB0 to 7,SBCK,RWC, COIN,$\overline{CQCK}$ | $V_{SS}$ | | 0.8 | V |
| | $V_{IL}(3)$ | EFMIN | $V_{SS}$ | | $0.4V_{DD}$ | V |
| | $V_{IL}(4)$ | TES | $V_{SS}$ | | $0.2V_{DD}$ | V |
| Data Setup Time | $t_{set\ up}$ | COIN,RWC,Fig.1 | 400 | | | ns |
| Data Hold Time | $t_{hold}$ | RWC,Fig.1 | 400 | | | ns |
| 'H'-Level Clock Pulse Width | $t_{w\phi H}$ | SBCK,$\overline{CQCK}$,RWC,Figs.1,2,3 | 400 | | | ns |
| 'L'-Level Clock Pulse Width | $t_{w\phi L}$ | $\overline{CQCK}$,SBCK,Figs.1,2,3 | 400 | | | ns |
| Data Read Access Time | $t_{RAC}$ | Figs.2,3 | 0 | | 400 | ns |
| Subcode Q Signal Read Enable Time | $t_{SQE}$ | Fig.2,without RWC signal | | 11.2 | | ms |
| Subcode Read Cycle | $t_{SC}$ | Fig.3 | | 136 | | μs |
| Subcode Read Enable | $t_{SE}$ | Fig.3 | 400 | | | ns |
| Reset Pulse Width | $t_{WRES}$ | $\overline{RES}$ | 400 | | | ns |
| X'tal OSC Frequency | $f_{x'tal}$ | $X_{IN}$,$X_{OUT}$ | | 8.6436 | | MHz |
| Operating Frequency Range | fop (1) | AI | 2.0 | 8.6436 | 10 | MHz |
| | fop (2) | EFMIN, $V_{IN} \geqq 1$Vp-p | | | 10 | MHz |

| Electrical Characteristics at Ta = 25°C, $V_{SS}$ = 0V, $V_{DD}$ = 5V | | | min | typ | max | unit |
|---|---|---|---|---|---|---|
| Current Dissipation | $I_{DD}$ | | | 15 | 30 | mA |
| Input 'H'-Level Current | $I_{IH}(1)$ | AI,EFMIN,$\overline{FZD}$,TES,MSBF, SBCK,COIN,$\overline{CQCK}$,$\overline{RES}$,HFL, RWC,M/L : $V_{IN} = V_{DD}$ | | | 5 | μA |
| | $I_{IH}(2)$ | (TEST1 to 5)DEMO,DFOFF, DSPOFF,IOFF : $V_{IN} = V_{DD} = 5.5V$ | 20 | | 75 | μA |
| Input 'L'-Level Current | $I_{IL}(1)$ | AI,EFMIN,$\overline{FZD}$,TES,MSBF, SBCK,COIN,$\overline{CQCK}$,$\overline{RES}$,HFL, RWC,M/L : $V_{IN} = V_{SS}$ | −5 | | | μA |
| Output 'H'-Level Voltage | $V_{OH}(1)$ | AO,PDO,EFMO,$\overline{EFMO}$,CLV+, CLV−,FOCS,FSEQ/PCK,TOFF, TGL,THLD,JP+,JP−,EMPH, EFLG : $I_{OH} = -1mA$ | $V_{DD}-1$ | | | V |
| | $V_{OH}(2)$ | SMP1,2,3,LRCLK,DFOUT, DACLK,DFIN,LRSY,CK2,$\overline{OE}$, $\overline{WE}$,AD0 to 10,DB0 to 7,PW,PWSY, FSX,WRQ,SQOUT : $I_{OH} = -0.5mA$ | $V_{DD}-1$ | | | V |
| Output 'L'-Level Voltage | $V_{OL}(1)$ | AO,PDO,EFMO,EFMO,CLV+, CLV−,FOCS,FSEQ/PCK,TOFF, TGL,THLD,JP+,JP−,EMPH, EFLG : $I_{OL} = 1mA$ | | | 1 | V |
| | $V_{OL}(2)$ | SMP1,2,3,LRCLK,DFOUT,DACLK, DFIN,LRSY,CK2,$\overline{OE}$,$\overline{WE}$,AD0 to 10, DB0 to 7,PW,PWSY,FSX,WRQ, SQOUT : $I_{OL} = 2mA$ | | | 0.4 | V |
| | $V_{OL}(3)$ | FST : $I_{OL} = 5mA$ | | | 0.75 | V |
| Output OFF-Leak Current | $I_{OFF}(1)$ | PDO,FST,DFIN,AD0 to 6, DB0 to 7 : $V_{OH} = V_{DD}$ | | | 5 | μA |
| | $I_{OFF}(2)$ | PDO,FST,DFIN,AD0 to 6, DB0 to 7 : $V_{OL} = V_{SS}$ | −5 | | | μA |
| Write Cycle Time | $t_{WC}$ | Fig.4 | | 462.8 | | ns |
| Read Cycle Time | $t_{RC}$ | Fig.4 | | 462.8 | | ns |
| Address Setup Time | $t_{AS}$ | Fig.4 | 80 | | 150 | ns |
| Write Pulse Width | $t_{WP}$ | Fig.4 | | 231.4 | | ns |
| Read Pulse Width | $t_{RP}$ | Fig.4 | | 347.1 | | ns |
| Address Access Time | $t_{AA}$ | Fig.4 | 80 | | 170 | ns |
| Output Hold Time | $t_{OH}$ | Fig.4 | −10 | | 80 | ns |
| Read/Write Setup Time | $t_{WS}$ | Fig.4 | 0 | | 20 | ns |

Fig.1 Command Input

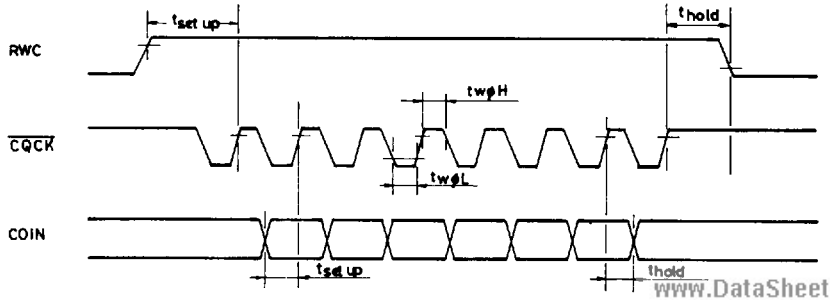


Fig.2 Subcode Q Output



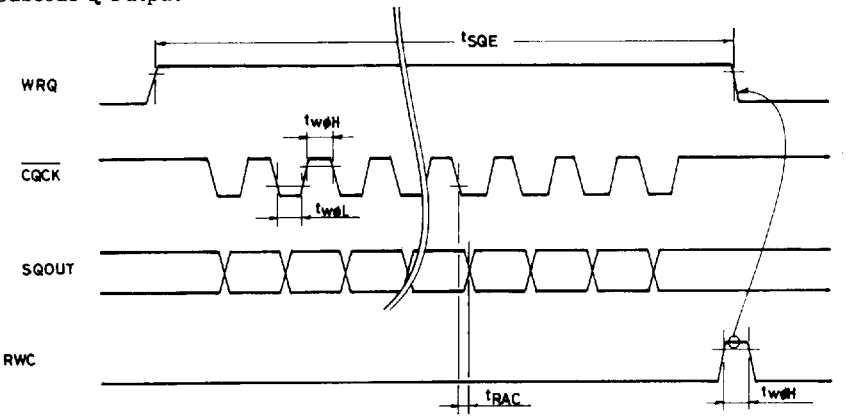



Fig.3 Subcode Output

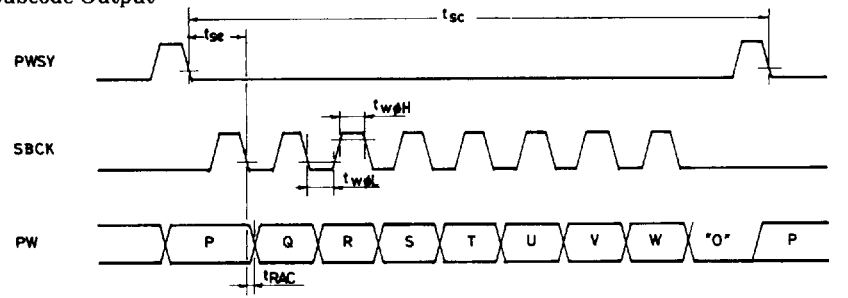
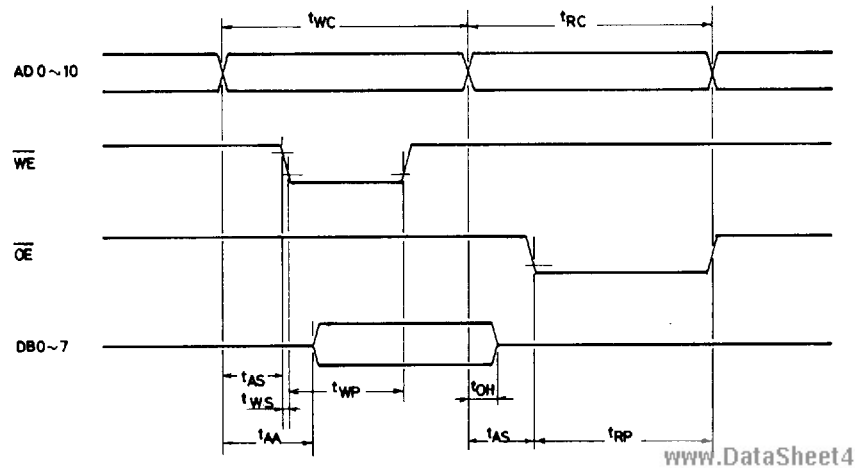
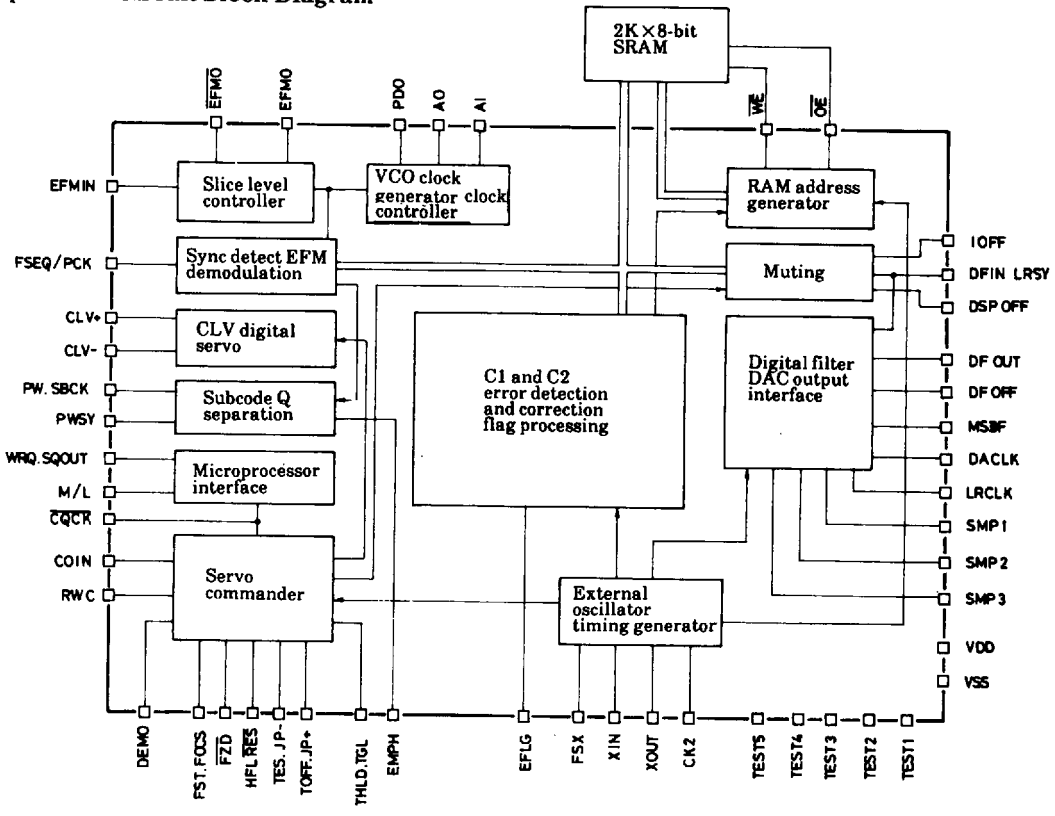


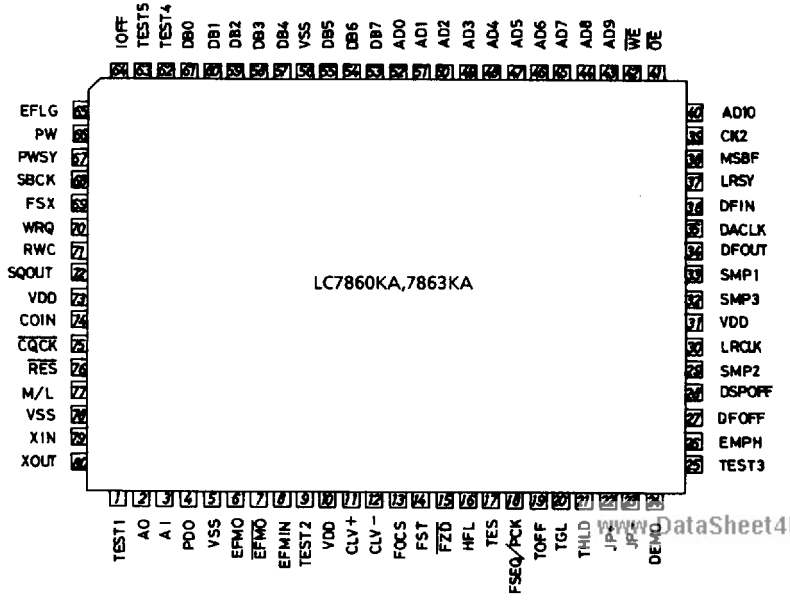

Fig.4 RAM Access



## Equivalent Circuit Block Diagram




## Pin Assignment



**Pin Description**



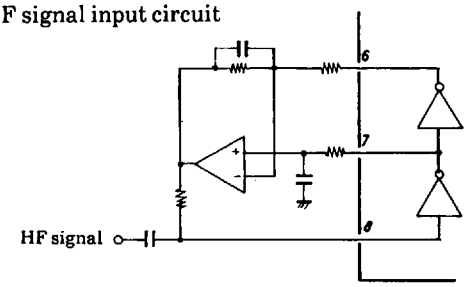
| Pin No. | Pin Name | I/O | | Functions |
|---|---|---|---|---|
| 1 | TEST1 | I | - | Test pin. Normally not connected. |
| 2 | AO | O | - | VCO is generated by connecting resonance circuit between AI and AO. (8.6436MHz) is phase output with EFM signal, and is set to increase frequency when +. |
| 3 | AI | I | - | |
| 4 | PDO | O | - | |
| 5 | $V_{SS}$ | - | - | GND |
| 6 | EFMO | O | - | 1 to 2Vpp HF signal is input to EFMIN. Output from $\overline{EFMO}$ and BFMO passes through amplitude limiter and reverse phase EFM signal is obtained from both. This performs slice level control. |
| 7 | $\overline{EFMO}$ | O | - | |
| 8 | EFMIN | I | - | |
| 9 | TEST2 | I | - | Test pin. Normally not connected. |
| 10 | $V_{DD}$ | - | - | +5V |
| 11 | CLV+ | O | - | Disk motor control output |
| 12 | CLV− | O | - | |
| 13 | FOCS | O | - | Focus servo is off when FOCS is HIGH. The lens is lowered by FST and then FST is HIGH, the lens is gradually pulled up. FOCS is reset when $\overline{FZD}$ is generated. For focus-in. |
| 14 | FST | O | - | |
| 15 | $\overline{FZD}$ | I | - | |
| 16 | HFL | I | *1 | *1 Kick pulses, JP+ and JP−, are generated according to track jump command. A jump of the prescribed number of tracks is (1,4,16,64).<br>*2 When 4.3218MHz PCK monitor terminal/DEMO is HIGH both SYNC detected from EFM signal and SYNC of counter are the same at HIGH. |
| 17 | TES | I | *1 | |
| 18 | FSEQ/PCK | O | *2 | |
| 19 | TOFF | O | *1 | |
| 20 | TGL | O | *1 | |
| 21 | THLD | O | *1 | |
| 22 | JP+ | O | *1 | |
| 23 | JP− | O | *1 | |
| 24 | DEMO | I | - | Set and sound output adjustment pin function. |
| 25 | TEST3 | I | - | Test pin. Normally not connected. |
| 26 | EMPH | O | - | De-emphasis is necessary when HIGH. |
| 27 | DFOFF | I | - | ON/OFF switch for digital filter. No filtering when HIGH. |
| 28 | DSPOFF | I | - | Test pin. Normally not connected. |
| 29 | SMP2 | O | *3 | *3 Signal output to DAC and signal for L/R switching and sample hold.<br>*4 +5V<br>*5 Signal output for CD ROM<br>*6 CD ROM sync signal |
| 30 | LRCLK | O | *3 | |
| 31 | $V_{DD}$ | - | *4 | |
| 32 | SMP3 | O | *3 | |
| 33 | SMP1 | O | *3 | |
| 34 | DFOUT | O | *3 | |
| 35 | DACLK | O | *3 | |
| 36 | DFIN | I/O | *5 | |
| 37 | LRSY | O | *6 | |
| 38 | MSBF | I | *3 | |
| 39 | CK2 | O | - | 2.1609MHz |
| 40 | AD10 | O | *7 | *7 RAM address output<br>*8 Output state when $\overline{WE}$ = L and input state when $\overline{WE}$ = H. $\overline{OE}$ is for input/output control. |
| 41 | $\overline{OE}$ | O | *8 | |
| 42 | $\overline{WE}$ | O | *8 | |
| 43 | AD9 | O | *7 | |
| 44 | AD8 | O | *7 | |
| 45 | AD7 | O | *7 | |
| 46 | AD6 | O | *7 | |
| 47 | AD5 | O | *7 | |
| 48 | AD4 | O | *7 | |
| 49 | AD3 | O | *7 | |
| 50 | AD2 | O | *7 | |
| 51 | AD1 | O | *7 | |
| 52 | AD0 | O | *7 | |

| Pin No. | Pin Name | I/O | | Functions |
|---|---|---|---|---|
| 53 | DB7 | I/O | *9 | *9 DB7 to DB0 : connected to RAM data pins. |
| 54 | DB6 | I/O | *9 | *10 GND |
| 55 | DB5 | I/O | *9 | SANYO SEMICONDUCTOR CORP |
| 56 | $V_{SS}$ | - | *10 | |
| 57 | DB4 | I/O | *9 | |
| 58 | DB3 | I/O | *9 | |
| 59 | DB2 | I/O | *9 | |
| 60 | DB1 | I/O | *9 | |
| 61 | DB0 | I/O | *9 | |
| 62 | TEST4 | I | - | Test pin. Normally not connected. |
| 63 | TEST5 | I | - | |
| 64 | IOFF | I | - | For CD ROM. HIGH time interpolation and holding of previous value not performed. |
| 65 | EFLG | O | - | C1,C2 1-level and 2-level error correction |
| 66 | PW | O | - | PWSY is SYNC combining main and sub and change from HIGH to LOW is taken externally. The P,Q,R,S,T,U,V and W subcodes are read by sending 8 clock pulses to SBCK. |
| 67 | PWSY | O | - | |
| 68 | SBCK | I | - | |
| 69 | FSX | O | - | 7.35kHz sync signal output |
| 70 | WRQ | O | *11 | *11 WRQ goes HIGH when data of subcode Q passes CRC check. This is taken externally and the data from SQOUT isread by sending $\overline{CQCK}$. When data is required with LSB first, M/L is driven LOW. After the microprocessor sets RWC to HIGH, the command is given by output synchronized with the $\overline{CQCK}$ command data. |
| 71 | RWC | I | *11 | |
| 72 | SQOUT | O | *11 | |
| 73 | $V_{DD}$ | - | *11 | |
| 74 | $\overline{COIN}$ | I | *11 | |
| 75 | $\overline{CQCK}$ | I | *11 | |
| 76 | $\overline{RES}$ | I | *12 | *12 Goes LOW once when power is turned on. |
| 77 | M/L | I | *11 | |
| 78 | $V_{SS}$ | - | - | GND |
| 79 | $X_{IN}$ | I | - | Pin for connection to 8.6436MHz crystal oscillator |
| 80 | $X_{OUT}$ | O | - | |

## Pin Applications

8 EFMIN, 7 $\overline{EFMO}$, 6 EFMO

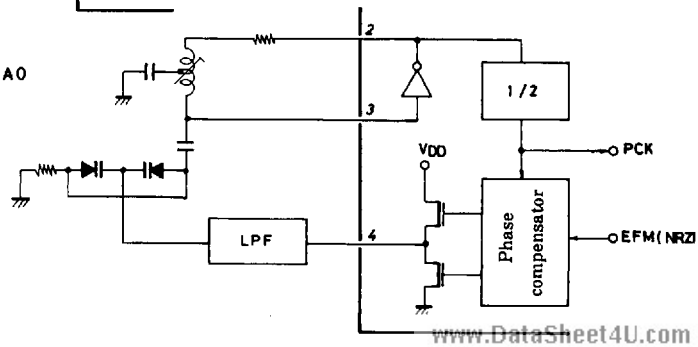
1) HF signal input circuit




A sliced EFM signal (NRZ) at the optimum level can be obtained inputting of the HF signal to EFMIN.

2) PLL clock generator

4 PDO, 3 AI, 2 AO






A VCO is configured by connecting a resonance circuit between AO and AI. As the PDO pin output is deflected to + when the VCO phase is delayed, control voltage is supplied to the variable capacitor by raising the VCO frequency.

3) Synchronization detection monitor 18 FSEQ/PCK

When 24 DEMO is LOW the average 4.3218MHz PCK signal obtained by dividing the VCO by two is monitored. When DEMO is HIGH, the level will be HIGH when the frame sync of the EFM signal read by PCK is the same as the timing generated by the counter, allowing for synchronization monitoring.

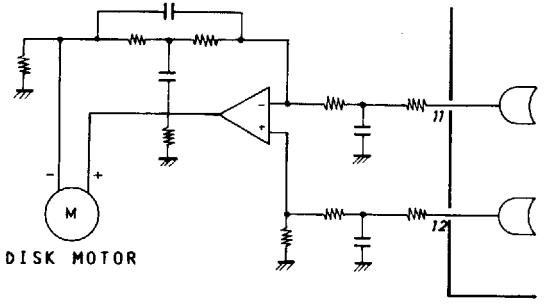
4) CLV servo circuit 11 CLV+, 12 CLV−

CLV+ is a signal for accelerating the disk in the forward direction and CLV− is a deceleration signal. One of the four modes, acceleration, deceleration, CLV, and stop, is selected by a command from the microprocessor. The CLV+ and CLV− output in each of these modes is shown in the table below.

| MODE | CLV+ | CLV− |
|---|---|---|
| Acceleration | H | L |
| Deceleration | L | H |
| CLV | ※ | ※ |
| Stop | L | L |

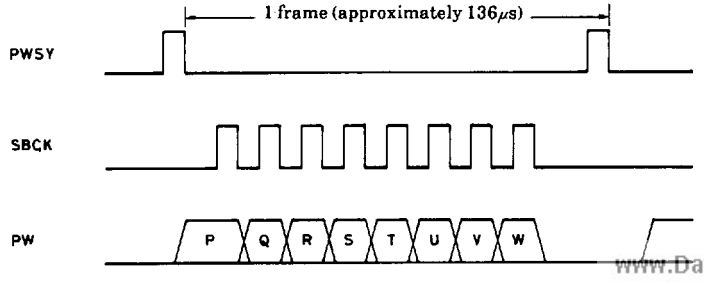
※ : In CLV mode, the disk rotation is detected from the HF signal, the DSP internal mode is changed to, and normal linear linear speed rotation is adopted by control of each signal. The cycle of PWM is 7.35kHz and the 1/64 duty cycle is 1.114s.

| Internal Mode | CLV+ | CLV− |
|---|---|---|
| Rough Servo (judged as low speed rotation) | H | L |
| Rough Servo (judged as high speed rotation) | L | H |
| Phase Control (PCK is locked) | PWM | PWM |
| Low Speed Rotation (when no HF signal) | 1/64 Duty | L |




5) Output circuit for subcodes P,Q,R to W 67 PWSY, 66 PW, 68 SBCK

PW is the output pin for the subcode signal, and all codes from P to W can be read by sending 8 clock pulses to SBCK within 136$\mu$s from the trailing edge of PWSY. The signal emerging at PW is altered by the trailing edge of RCK. When clock pulses are not sent to SBCK, only the P code is output from PW.

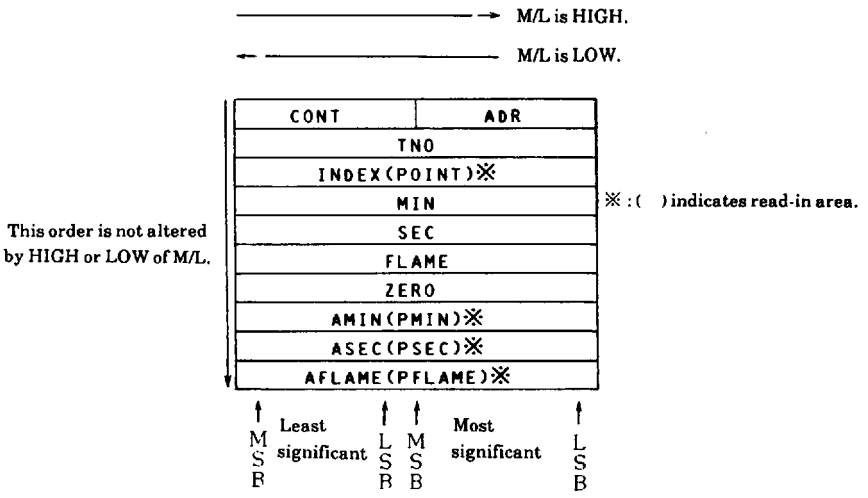


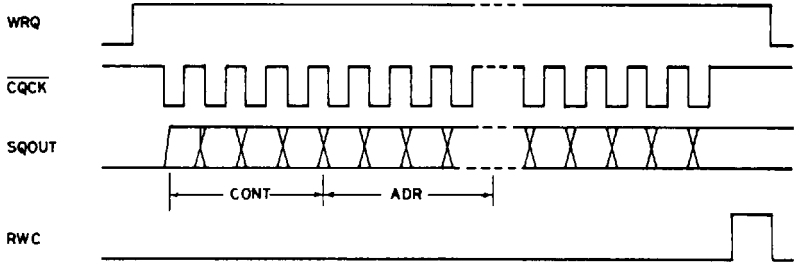

In the subcode, SO, and SI frames, PWSY does not drop to LOW, instead it remains HIGH.

6) Subcode "Q" output circuit 70 WRQ, 71 RWC, 72 SQOUT, 75 $\overline{CQCK}$, 77 M/L

Of the 8 bits of the subcode, the "Q" signal is useful for accessing selections and indication, etc. WRQ goes HIGH when the CRC check is passed and in addition only when at address 1 (See Note 1 below). The data from SQOUT can be read in the order if the microprocessor detects this HIGH state and sends $\overline{CQCK}$. When $\overline{CQCK}$ output starts, the updating of data in the registers of the DSP is prohibited. When the microprocessor completes reading of the data, RWC is driven once to HIGH and permission to update data is given. At this time, WRQ drops to LOW. As WRQ drops to LOW 11.2ms after going to "H", transmission of $\overline{CQCK}$ starts while it is "H". The data can be read with in the LSB first out order by setting M/L to LOW.

**Note 1 : LC7863KA lacks this address 1 condition.**



7) Servo command functions 71 RWC, 74 COIN, 75 $\overline{CQCK}$

Four types of commands (focus start, disk motor, track jump, and mute) can be input by setting RWC to HIGH and sending an 8-bit/1-word command synchronized to $\overline{CQCK}$ clock from COIN.

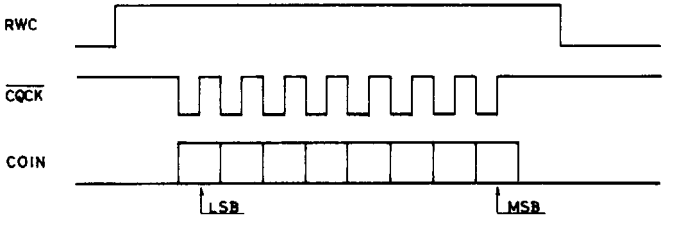
| MSB CODE LSB | COMMAND | | | | |
|---|---|---|---|---|---|
| 00000000 | | | NOTHING | | |
| 00010001 | 1 | TRACK | JUMP | IN | #1 |
| 00010010 | 1 | TRACK | JUMP | IN | #2 |
| 00010011 | 4 | TRACK | JUMP | IN | |
| 00010100 | 16 | TRACK | JUMP | IN | |
| 00010101 (Note 2) | 64 | TRACK | JUMP | IN | |
| 00011001 | 1 | TRACK | JUMP | OUT | #1 |
| 00011010 | 1 | TRACK | JUMP | OUT | #2 |
| 00011011 | 4 | TRACK | JUMP | OUT | |
| 00011100 | 16 | TRACK | JUMP | OUT | |
| 00011101 (Note 2) | 64 | TRACK | JUMP | OUT | |
| 00010110 | 256 | TRACK | CHECK | | |
| 00000001 | MUTE | | | 0dB | |
| 00000010 | MUTE | | | -12DB | |
| 00000011 | MUTE | | | -∞DB | |
| 00000100 | DISK | MOTOR | | START | |
| 00000101 | DISK | MOTOR | | CLV | |
| 00000110 | DISK | MOTOR | | BRAKE | |
| 00000111 | DISK | MOTOR | | STOP | |
| 00001000 | FOCUS | | START | | |

LSB first out

#1 : JP pulse width 233$\mu$s + 233$\mu$s

#2 : Switching from acceleration pulse to deceleration pulse is made by detecting the intermedeate point of the track.

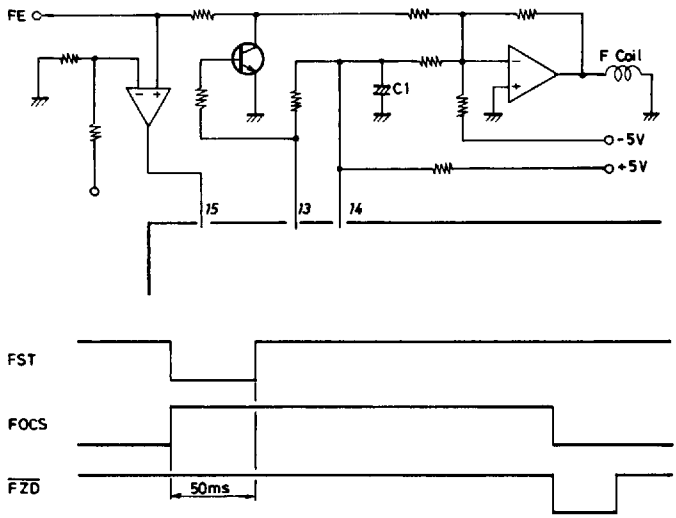
**Note 2 : This command is 32 track JUMP in the case of the LC7863KA.**




The command is executed from trailing edge of RWC. As mute and disk motor commands are latched to the registers, the command type varies according to the other commands. When reset by $\overline{RES}$, mute is $-\infty$dB and disk motor is STOP. Although approximately 25ms is needed for execution of the track JUMP command, the next track JUMP command can be given during execution of the previous. The focus START command requires even more time, but other commands cannot be input during execution of this command. Thus when more than one commands are to be input, the mute or disk motor command is input first followed by input of the focus START or track JUMP command.

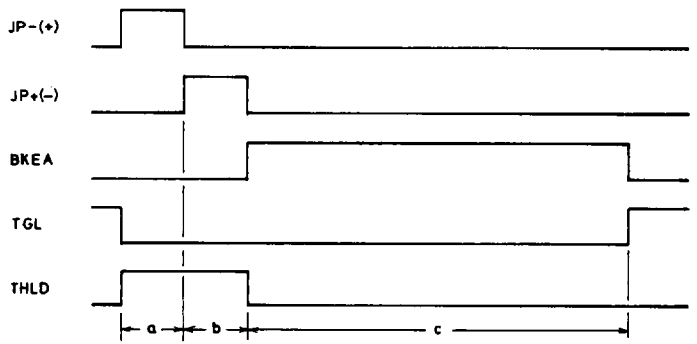
8) Focus servo circuit 13 FOCS, 14 FST, 15 $\overline{\text{FZD}}$

When the focus START command is input to the servo commander, first the charge of C1 is discharged by FST and the lens is slowly raised. When the focal point is reached, $\overline{\text{FZD}}$ drops and at the same time, FOCS is reset to turn on the servo.



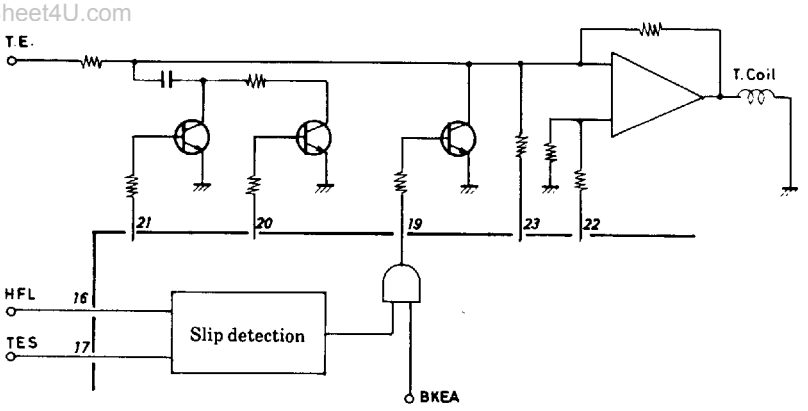

After the command is set, the microprocessor checks DRF, confirms the focus, and proceeds to the next flow. If the focus is not attained though C1 has been charged, the focus START command is sent again and the focus servo operation is repeated.

9) Track jump circuit 16 HFL, 17 TES, 19 TOFF, 20 TGL, 21THLD, 22 JP+, 23 JP−



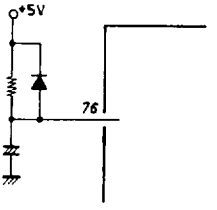

| COMMAND | a | b | c |
|---|---|---|---|
| 1 TRACK JUMP IN (OUT) #1 | 233$\mu$s | 233$\mu$s | 17ms |
| 1 TRACK JUMP IN (OUT) #2 | 0.5 TRACK JUMP period | 233$\mu$s | 17ms |
| 4 TRACK JUMP IN (OUT) | 2 TRACK JUMP period | 466$\mu$s | 17ms |
| 16 TRACK JUMP IN (OUT) | 9 TRACK JUMP period | 2 TRACK JUMP period | 17ms |
| 64 TRACK JUMP IN (OUT) | 36 TRACK JUMP period | 28 TRACK JUMP period | 17ms |
| 256 TRACK CHECK | When 256 tracks elapse, only THLD goes HIGH. | | 17ms |

When the track JUMP command is input to the servo commander, acceleration pulses are issued followed by deceleration pulses, the braking period elapses, the prescribed jump is completed. The brake period is determined by TSE and HFL. The beam is detected in the slit direction, the section in the TE signal enhancing the slit is cut by TOFF, and the track destination after jumping is determined by raising the servo gain by TGL. The TOFF pin goes HIGH when the CLV servo command is STOP.



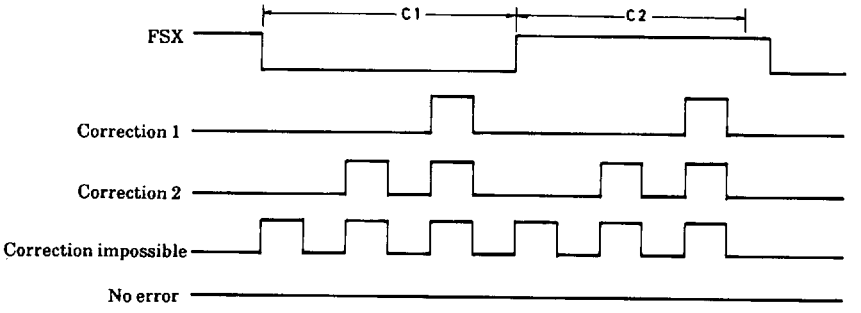

10) Sound output function for adjustment 24 DEMO
Even if no command is sent from the microprocessor, setting this pin to HIGH will set muting to 0dB, the disk motor to CLV, and will perform the focus start operation. In addition, the 18FSEQ /PCK function is switched.

11) Reset circuit 76 $\overline{RES}$
When this power is turned on, this pin goes LOW and then to HIGH muting is set to $-\infty$ dB and the disk motor to STOP.



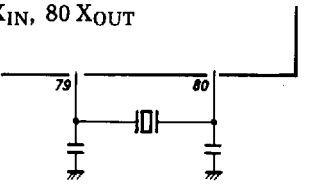

12) Deemphasis ON/OFF 26 EMPH
The pre-emphasis ON/OFF bit of the control information of subcode Q is output from the EMPH pin. Deemphasis is performed when the level is HIGH.

13) Error flag output 65 EFLG, 69 $\overline{FSX}$




FSX is created by dividing the crystal oscillator clock and is a 7.35kHz frame synchronization signal. The error correction status for each frame is output from EFLG. The HIGH level shown here allows for easy evaluation of the playback status.

14) Crystal clock oscillation 79 $X_{IN}$, 80 $X_{OUT}$





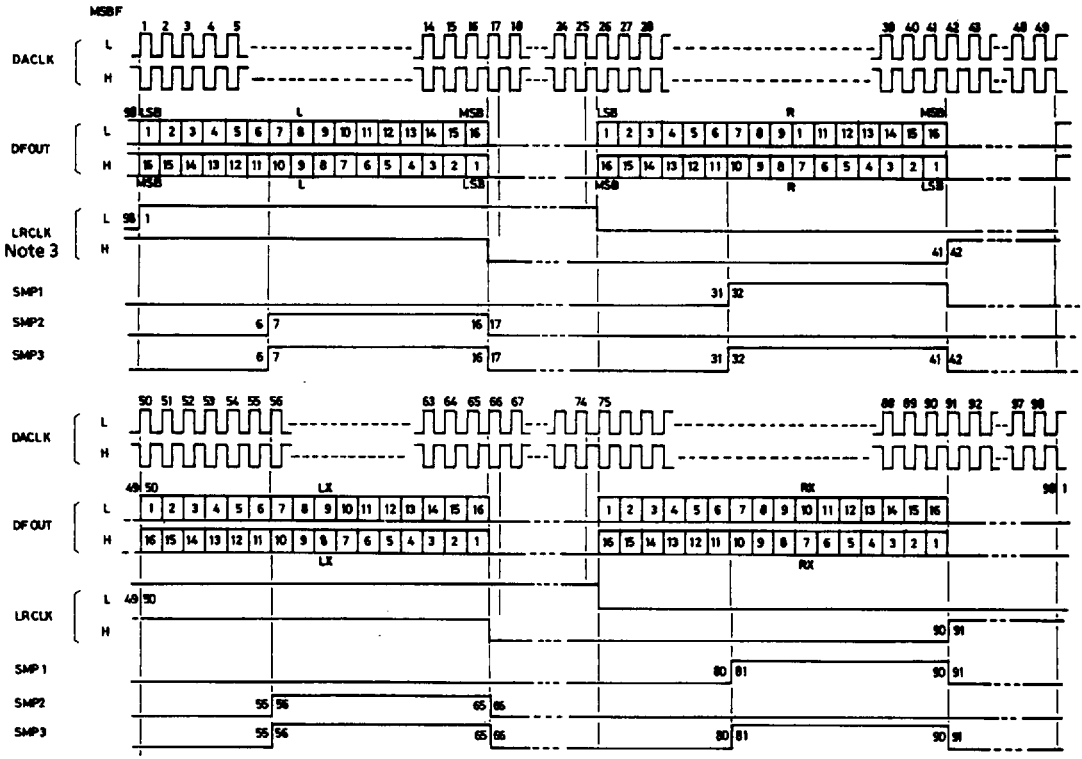

The clock which forms the time base oscillates by connecting a 8.6436MHz crystal oscillator to these pins.

15) DAC interface 27 DFOFF, 29 SMP2, 30 LRCLK, 32 SMP3, 33 SMP1, 34 DFOUT, 35 DACLK, 38 MSBF

When MSBF is LOW, the data for the DAC is output in LSB first out order from DFOUT synchronized with the leading edge of DACLK. When MSBF is HIGH, the data is output in MSB first out order from synchronized with the trailing edge of DACLK.

**LC7860KA, 7863KA digital filter output data format (DFOFF = "L")**

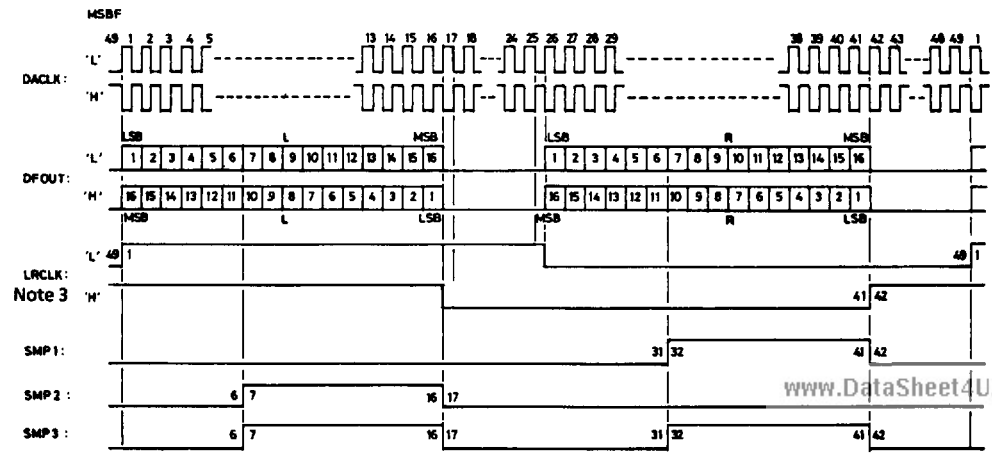
※ The DACLK rate is the same as CK4 (4.3218MHz)




**LC7860KA, 7863KA digital filter output data format (DFOFF = "H")**

※ In this mode, the input data passes through without changing. The timing signal for DAC and MSB first out mode are effective.

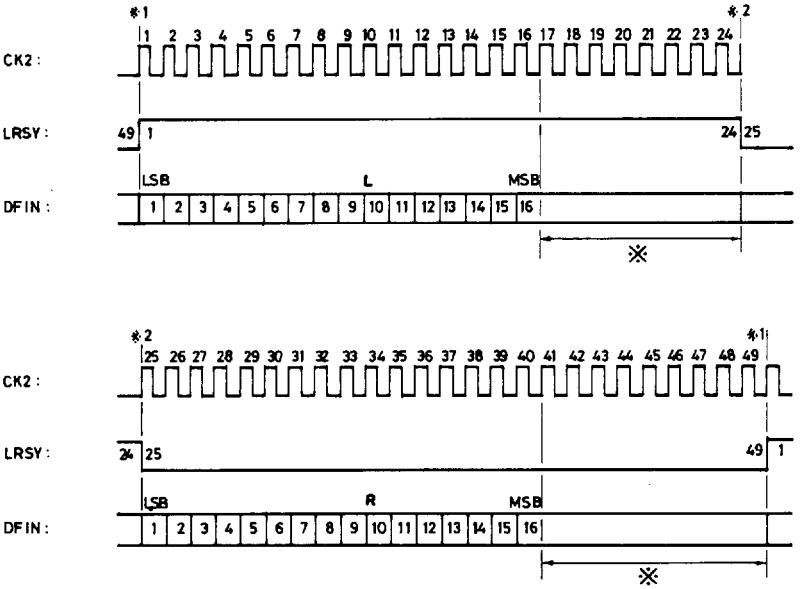
※ The DACLK rate is the same as CK2 (2.1609MHz)



16) Output for CD ROM 39 CK2, 37 LRSY, 36 DFIN, 28 DSP OFF, 64 IOFF

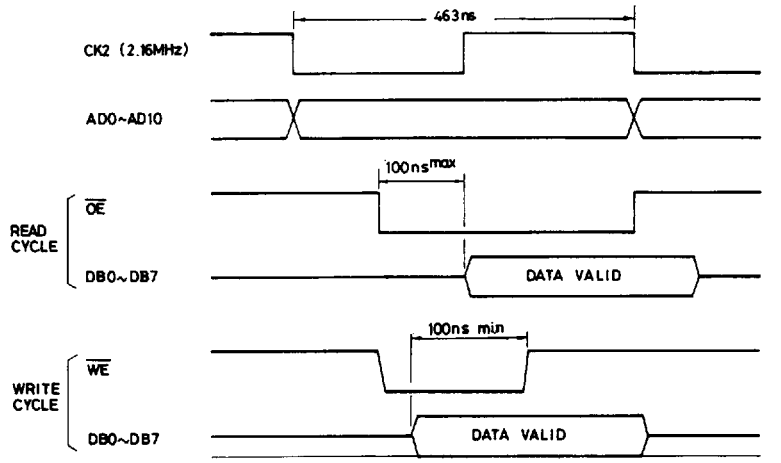
When DSPOFF is LOW, the input signal to the digital filter can be obtained from DFIN. The data is obtained in LSB first out data as the LCH data synchronized to CK2 from the leading edge of LRSY or the RCH data synchronized to CK2 from the leading edge of LRSY. CK2 is a 2.1609MHz clock and when DSPOFF is HIGH, an externla signal can be input to the digital filter from DFIN. This function is used primarily for testing the LSI.

LC7860KA, 7863KA digital filter section input data format




※ When DSPOFF = LOW, the DSP signal is output and the period data is the same as MSB. When DSPOFF = HIGH, an external signal is applied and the periad data is meaningless (don't care).

17) RAM interface 41 $\overline{OE}$, 43 $\overline{WE}$, 40 to 52 AD10 to AD0, 53 to 61 DB7 to DB0




There are the address signals, data signals, and control signals connected to 2K byte RAM.

## Block Operation Description

1) RAM address control

LC7860KA, 7863KA perform de-interleave processing of EFM demodulated data by address control of 8 bits/2K words of external RAM. The jitter absorption capabilities of the input data is ±4 frames as the buffer memory capability. The remaining buffer space is constantly checked and the data write addres is controlled to the center of the buffer by fine-tuning the division ratio on the CLV servo circuit PCK side. If the ±4 frame buffer capabity is exceeded, the write address is forcibly set to ±0. this means that the errors occurring cannot be processed by flags and muting is applied for a 128 frame period.

| Position | Division Ratio or Action |
|---|---|
| −4 or less | Forcibly moved to ±0 |
| −3 | 589 ┐ |
| −2 | 589 ├ Advance division |
| −1 | 589 ┘ |
| ±0 | 588 Standard division |
| +1 | 587 ┐ |
| +2 | 587 ├ Retard division |
| +3 | 587 ┘ |
| +4 or greater | Forcibly moved to ±0 |

2) C1, C2 correction

The EFM demodulated data is written to the external RAM, jitter absorption is made, and the following processing is made at fixed timing set by the XTAL clock. First, error checking and correction is made for the C1 block, and the C1 flag is determined and written to the C1 flag register. Next, error checking and correction is made for the C2 block, and the C2 flag is determined and written to the external RAM.

| C1 Check | Correction and Flag Processing | |
|---|---|---|
| No Errors | Correction unnecessary | Flag reset |
| 1 Error | Correction made | Flag reset |
| 2 Errors | Correction made | Flag set |
| 3 Errors or more | Correction impossible | Flag set |

| C2 Check | Correction and Flag Processing | |
|---|---|---|
| No Errors | Correction unnecessary | Flag reset |
| 1 Error | Correction made | Flag reset |
| 2 Errors | Reference to C1 flag | ※1 |
| 3 Errors or more | Reference to C1 flag | ※2 |

※1 When the error position determined by C2 check and C1 flag are the same, correction is made and the flag is reset. However when the number of C1 flags is 3 or more, the possibility of improper correction exists and correction is not made. The C1 flag remains as it is and the C2 flag is set. When one of the error positions is the same and the other does not match, correction is not possible. furthermore, when the number of C1 flags is less than 5, the C1 check results are thought to be suspect and the flag is set. 6 or more errors is handled in the same manner as correction impossible; the C1 flag remains as it is and the C2 flag is set. Correction is of course not possible if noe of the error positions match. When the number of C1 flags is less than 2, the data evaluated as OK by the C1 check is probably incorrect and the flag is set. In all other cases, the C1 flag remains as it is and C2 flag is set.

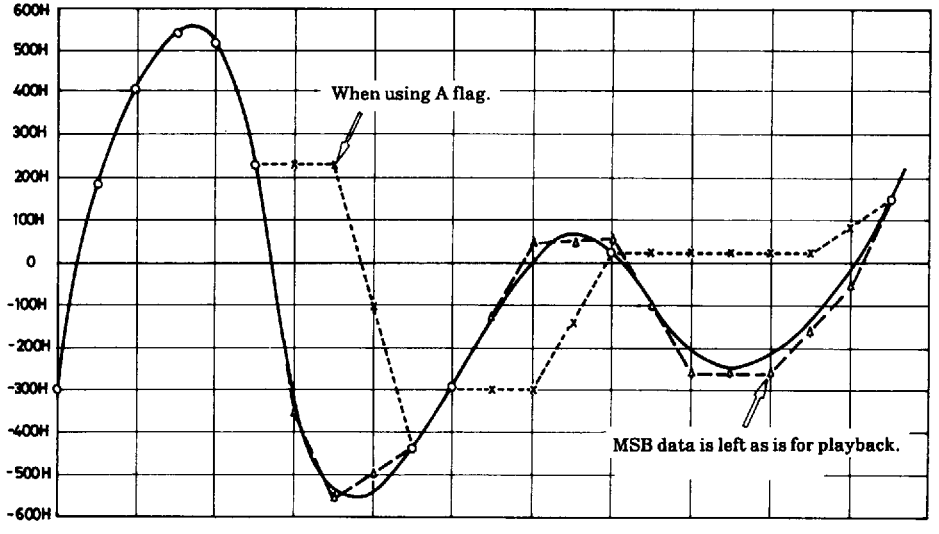
※2 When correction impossible is evaluated with 3 or more errors, correction is of course not possible. Whe the number of C1 flags is less than 2, the data evaluated as OK by the C1 check is probably incorrect and the flag is set. In all other cases, the C1 flag remains as it is and C2 flag is set.

3) Playback flag determination and interpolation

| C2 Flag | | Playback Flag |
|---|---|---|
| Upper | Lower | |
| 0 | 0 | Reset |
| 0 | 1 | ※ |
| 1 | 0 | Set |
| 1 | 1 | Set |

※ Reset performed if amplitude of previous 8 samples is 200H or greater, set performed if not.

The data up to the C2 block is treated as symbols in 9-bit units with each sample of an upper and lower symbol for a total of 16 bits. Thus, each sample has two C2 flags. Data mainpulation such as average value interpolation and previous value hold, etc., can be made by attempting to infer a value as close to the true value as possible from the surrounding samples and substituting this for the error sample. The error in this is low when the signal level is low, but becomes large when the amplitude becomes larger. For a sample in which the upper symbol is no-error and only the lower sample contains an error, adopting a procedure of substituting 80H for the lower symbol will limit the error to 80H, a relatively low level. Thus in this case, the playback flag is reset if the amplitude of the previous 8 samples is 200H or greater. Average value interpolation occurs when there is an error in only one sample and previous value hold occurs when there are consecutive errors in two or more samples.




| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

A : OR obtained from upper and lower C2 flags to obtain playback flag.

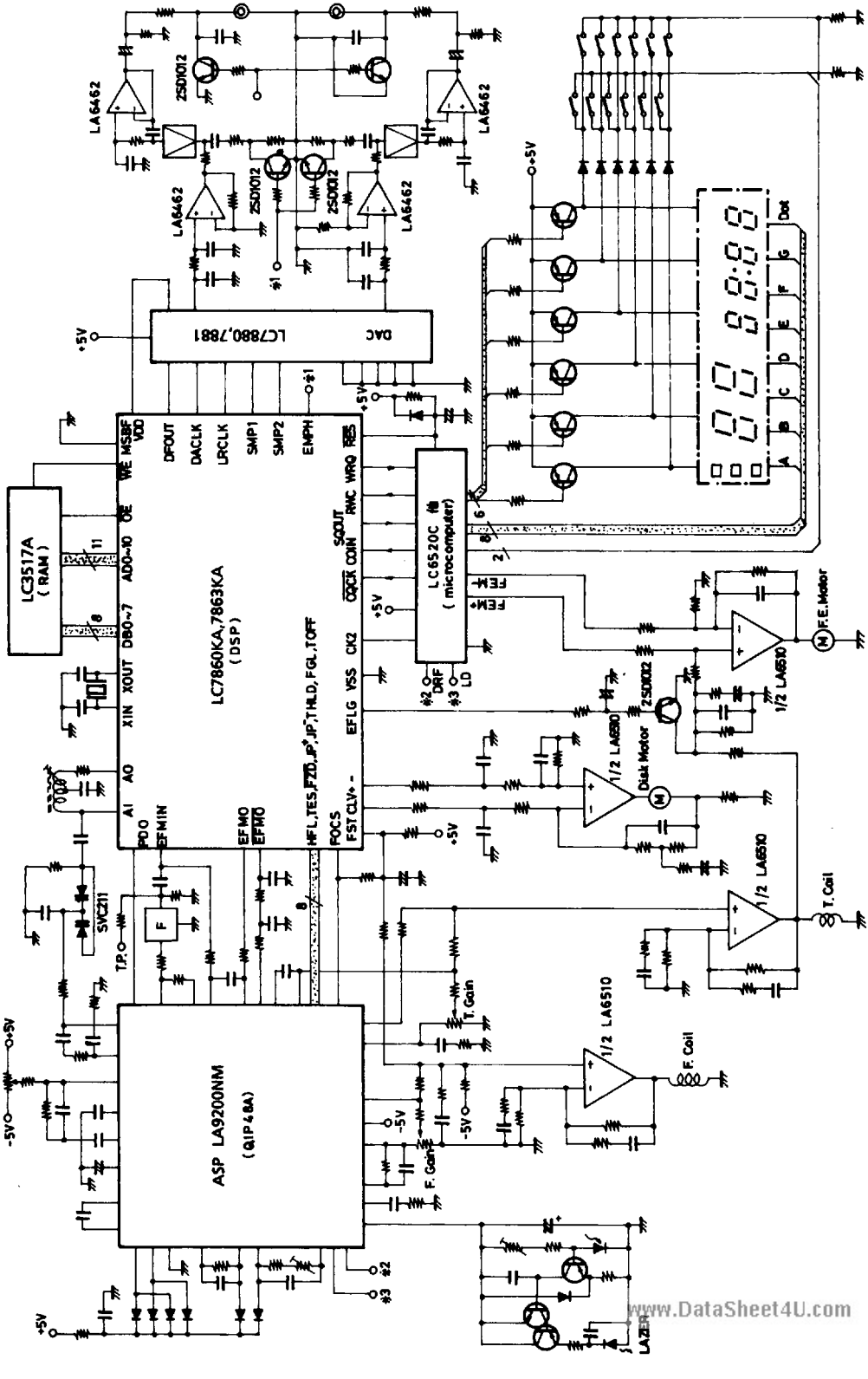
B : C2 flag of upper symbol used as playback flag (LC7860KA, 7863KA).

4) Muting

There is −12dB and −∞dB muting. Both limit popping at power ON/OFF and move through 4 steps.

| | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| −∞dB | 1 | 3/4 | 1/4 | 0 |
| −12dB | 1 | 3/4 | 2/4 | 1/4 |

## Sample Application Circuit



**Differences between LC7860N/7863 and LC7860KA/7863KA**

The LC7860N/7863 is basically compatible with the LC7860KA/7863KA in software and pin layout. The differences between them are as follows :

(1) The LC7860KA/7863KA is an enhanged version of the conventional products in playability.
The LC7860KA/7863KA performs the C2, 2 error correction if the number of C1 flags is in the range from 2 to 6 while the LC7860N/7863 is based on the condition that the number of C1 flags is greater than 2.

(2) The LC7860KA/7863KA uses the same DAC interface signal LRCLK as that of the LC7863.

(3) "H" level input current $I_{IH(2)}$ : 25$\mu$A min to 20$\mu$A min

| Enhancements | LC7860N | LC7863 | LC7860KA | LC7863KA |
|---|---|---|---|---|
| C2, 2 error correction conditions | Number of C1 flags : 2 | Number of C1 flags : 2 | Number of C1 flags : 2 to 6 | Number of C1 flags : 2 to 6 |
| Sub code Q register change condition | Address "1" | Unconditionally | Address "1" | Unconditionally |
| Track jump command 15H | Track count : 64 | Track count : 32 | Track count : 64 | Track count : 32 |
| LRCLK | "H" level period : 24.5DACLK<br>"L" level period : 24.5DACLK | "H" level period : 25DACLK<br>"L" level period : 25DACLK | "H" level period : 25DACLK<br>"L" level period : 25DACLK | "H" level period : 25DACLK<br>"L" level period : 25DACLK |
| "H" level input current $I_{IH(2)}$ | 25$\mu$A min | 25$\mu$A min | 20$\mu$A min | 20$\mu$A min |