Ordering number : ENA2081

SANYO Semiconductors
DATA SHEET

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LC786961W — CMOS LSI Compact Disc Player IC

Overview

The LC786961W integrates ARM7TDMI-S™, CD servo control, CD signal processing, compressed audio decode processing, audio signal processing, USB host processing, SD memory card host processing and a flash memory to store the program for ARM7TDMI-S™ and various data in a package. Furthermore, various kinds of interface functions such as SIO, UART etc. reduce the external main controller's processing load and make high performance and much functional CD player system, using with less components.

Features

- RF signal processing for CD-DA/R/RW, servo control, EFM signal processing, and anti-shock processing
- MP3*, WMA*, AAC* decoder processing
- Sampling rate convertor, High frequency compensation filter and other various audio signal processing
- USB host function (Full speed as 12Mbps), SD memory card host function
- ARM7TDMI-S™ as internal CPU core, flash memory for program and various data storage
- Operating voltage: 3.3V typical
- Operating temperature: -40°C to +85°C
- Packages: SQFP144 (20 × 20)

* MP3(MPEG Layer-3 Audio Coding)
MPEG Layer-3 audio coding technology licensed from Fraunhofer IIS and Thomson.
Supply of this product does not convey license under the relevant intellectual property of Thomson and/or Fraunhofer Gesellschaft nor imply any right to use this product in any finished end user or ready-to-use final product. An independent license for such use is required.
For details, please visit http://mp3licensing.com/.

* Windows Media Audio
Windows Media™ is a trademark and a registered trademark in the United States and other countries of United States Microsoft Corporation.

* AAC
Advanced Audio Coding

* This product incorporates technology licensed from Silicon Storage Technology Inc.

Detail of Functions

[CD DSP functions]

<Playback functions>

- Playback mode: CLV playback/Jitter free playback (VCEC)
- Playback speed: Normal speed, double speed , Quadruple speed

<RF Processing block>

- RF system:AGC, CD-R and CD-R/W playback support, peak hold, bottom hold
- Error system: TE signal generation, FE signal generation
- Detection: Track count signal, Jitter, Defect (black, mirror)
- LASER power controller (APC)
- DC offset voltage cancellation

<Servo control block>

- All servo systems as tracking, focus, sled and spindle are implemented with digital processing.
- Automatic adjustment functions: focus gain, focus bias, focus offset, tracking gain, tracking offset and tracking balance
- Shock detection / Interruption detection

<CD signal processing block>

- EFM signal synchronization detection, protection and interpolation
- Error detection, correction (C1=double, C2=quadruple/double)
- Jitter margin ±19 frames

<CD TEXT processing block>

- Buffers CD-TEXT data to the desired area of SDRAM
- Starts buffering desired ID3/ID4 of CD-TEXT data.

<CD-DA Anti-shock processing block>

- Anti-shock processing using with SDRAM
  Maximum about 10 seconds with 16M bit SDRAM and about 40 seconds with 64M bit SDRAM

<CD-ROM processing block>

- CD-ROM decoding (Mode1, Mode2 <form1, form2>)
- Outputs CD-ROM decoded data

[Compressed audio decode functions]

- MP3 decode (ISO/IEC 11172-3, ISO/IEC 13818-3)
  - Sampling rate support: MPEG1-Layer1/2/3 (32kHz, 44.1kHz, 48kHz)
    MPEG2-Layer1/2/3 (16kHz, 22.05kHz, 24kHz)
    MPEG2.5-Layer3 (8kHz, 11.025kHz, 12kHz)
  - Bit rate support: All Bit Rate (Variable Bit Rate support)
  - MPEG header read support
- WMA decode (Version 9 standard)
  - Sampling rate support: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz, 48kHz
  - Bit rate support: 5kbps to 384kbps (Variable Bit Rate support)
- AAC decode (ISO/IEC 14496-3, ISO/IEC 13818-7)
  - Profile: MPEG4-AAC-LowComplexity
  - Sampling rate support: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
  - Bit rate support: Monaural 8kbps to 160kbps (Variable bit rate support)
    Stereo 16kbps to 320kbps (Variable bit rate support)
- Decodes both the compressed data read from the disc and input from outside through the interface pins

[Audio processing functions]

<Audio processing block>

- Sampling rate converter (SRC) for compressed audio data playback
- High frequency compensation filter for compressed audio data playback
- Interpolation (CD-DA only)
- Digital attenuator
- Bilingual function
- Mute function (-12dB, -∞)
- De-emphasis filter
- Bass / Treble filter

<Digital filter and D/A convertor processing block>

- Eight-fold over-sampling digital filter (24bit)
- One bit DAC (tertiary ΔΣ noise shaper type)
- Secondary LPF for audio output

<Interface block>

- Allows external audio data supply to the digital filter and D/A converter (Uses four signals)
- Various external audio data output format
  IIS (48fs/64fs), MSB first right justified (32fs/48fs/64fs), 16 bit data length

[External interface functions]

<USB host control block>

- Open Host Controller Interface 1.0a
- Universal Serial Bus Specification 1.1
  Supports up to Full speed (12MHz)for USB2.0
- Supports four kinds of transfer type (Control/Bulk/Interrupt/Isochronous)

<SD memory card host control block>

- Multimedia Card Specification v2.11
- Secure Digital Memory Card Physical Layer Specification v0.96

* Individual contract is necessary to use SD memory card controller. For detail, please contact to us.

[Internal Microcontroller functions]

<Sequencer control>

- CD, USB, SD memory card playback control
  Servo control, CD anti-shock playback control, CD-ROM/USB/SD file analysis, etc.

<Communication control between main controller>

- Communication format: SIO

<Peripheral interface block>

- GPIO port 30ports maximum (Shared with other functions. Several pins are 5V tolerant.)
- External interrupt pins 4pins maximum (Shared with other functions.)
- Serial interface

SIO	clock synchronized full duplex (3 lines)	2 channel
UART	full duplex	2 channel
IIC	master function	1 channel

<Program memory block>

- Flash memory
  Program version up from the external media (CD-ROM/USB)or main controller is available.

<Others>

- Watch Dog Timer
  Notify to outside from the pin or reset internally.
- Power management
  2 kinds of sleep mode
  (1) Only CPU core operates at slow clock and clocks for other blocks are stopping.
  (2) All clocks are stopping.

[Others]

<External memory>

- External SDRAM Memory size : 16Mbit or 64Mbit
  Data width : 16bit
  CAS latency : 2
  Burst length : Full

Used for CD-DA anti-shock control, CD-ROM decoding, USB data temporary storage, etc.

<Internal power supply>

- 1.5V regulator for internal blocks

Specifications

Absolute Maximum Ratings at Ta = 25°C, DV_{SS} = AV_{SS} = LRV_{SS} = $XV_{SS}1$ = $XV_{SS}2$ = $VV_{SS}1$ = $VV_{SS}2$ = 0V

Parameter	Symbol	Pin names	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	DV_{DD}, AV_{DD}, LRV_{DD}, $XV_{DD}1$, $XV_{DD}2$, UV_{DD}, $VV_{DD}1$, $VV_{DD}2$, $VV_{DD}3$		-0.3 to +3.95	V
Input voltage 1	$V_{IN}1$	Input pins other than $V_{IN}2$		-0.3 to DV_{DD}+0.3	V
Input voltage 2	$V_{IN}2$	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP14, GP15, GP16, GP26, GP27, JTRSTB, JTCK, JTDI, JTMS		-0.3 to +5.6	V
Output voltage	V_{OUT}			-0.3 to DV_{DD}+0.3	V
Allowable power dissipation	Pd max		Ta ≤ 85°C Mounted reference PCB (*)	540	mW
Operating temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-40 to +125	°C

(*)Reference PCB: 114.3mm×76.1mm×1.6mm, glass epoxy resin

Allowable Operating Ranges at Ta = -40 to +85°C, DV_{SS} = AV_{SS} = LRV_{SS} = $XV_{SS}1$ = $XV_{SS}2$ = $VV_{SS}1$ = $VV_{SS}2$ = 0V

Parameter	Symbol	Pin names	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}1$	DV_{DD}, AV_{DD}, LRV_{DD}, $XV_{DD}1$, $XV_{DD}2$, UV_{DD}, $VV_{DD}1$, $VV_{DD}2$, $VV_{DD}3$		3.00		3.60	V
High-level input voltage	V_{IH}(1)	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP14, GP15, GP16, GP26, GP27, JTMS, JTRSTB, JTCK, JTDI	Schmitt	2.00		5.50	V
	V_{IH}(2)	GP13, GP17, GP20, GP21, GP22, GP23, GP24, GP25, GP60, GP61, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15, PMODE0, PMODE1	Schmitt	2.00		$V_{DD}1$	V
Low-level input voltage	V_{IL}(1)	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP14, GP15, GP16, GP26, GP27, JTMS, JTRSTB, JTCK, JTDI	Schmitt	0		0.80	V
	V_{IL}(2)	GP13, GP17, GP20, GP21, GP22, GP23, GP24, GP25, GP60, GP61, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15, MODE0, MODE1, MODE2	Schmitt	0		0.80	V
Crystal oscillator frequency	FX1	XIN XOUT	Oscillator circuit		12.0		MHz
	FX2	X16IN X16OUT	Oscillator circuit		16.9344		MHz

Electrical Characteristics at Ta = -40 to +85°C, $V_{DD}1$ = 3.0V to 3.6V,
DV_{SS} = AV_{SS} = LRV_{SS} = $XV_{SS}1$ = $XV_{SS}2$ = $VV_{SS}1$ = $VV_{SS}2$ = 0V

Parameter	Symbol	Pin names	Conditions	min	typ	max	Unit
Current drain	$I_{DD}1$	DV_{DD}, AV_{DD}, LRV_{DD}, $XV_{DD}1$, $XV_{DD}2$, UV_{DD}, $VV_{DD}1$, $VV_{DD}2$, $VV_{DD}3$			125	150	mA
High-level input current	I_{IH}(1)	RESB, SIFCK, SIFDI, JTMS, JTRSTB, JTCK, JTDI, PMODE0, PMODE1, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP14, GP15, GP16, GP26, GP27	Schmitt, V_{IN} = 5.50V Built-in Pull-down resistor OFF			10.00	µA
	I_{IH}(2)	GP13, GP17, GP20, GP21, GP22, GP23, GP24, GP25, GP60, GP61, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15	Schmitt, V_{IN} = $V_{DD}1$ Built-in Pull-down resistor OFF			10.00	µA
Low-level input current	I_{IL}(1)	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP24, GP25, GP26, GP27, GP60, GP61, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15, JTMS, JTRSTB, JTCK, JTDI, MODE0, MODE1, MODE2	Schmitt, V_{IN} = 0V	-10.00			µA
High-level output voltage	V_{OH}(1)	GP04, GP05, GP06, GP07, GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP24, GP25, GP26, GP27, GP60, GP61, GP62, GP63, GP64, GP65, SDBA, SDDAT00 to SDDAT15, SDADRS00 to SDADRS12, SDCSB, SDRASB, SDCASB, SDWEB, SDCKE, SDDQM	CMOS, I_{OH} = -2mA	$V_{DD}1$-0.6			V
	V_{OH}(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP10, GP11, SDCLK, JTDO, JTRTCK	CMOS, I_{OH} = -4mA	$V_{DD}1$-0.6			V
Low-level output voltage	V_{OL}(1)	GP04, GP05, GP06, GP07, GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP24, GP25, GP26, GP27, GP60, GP61, GP62, GP63, GP64, GP65, SDBA, SDDAT00 to SDDAT15, SDADRS00 to SDADRS12, SDCSB, SDRASB, SDCASB, SDWEB, SDCKE, SDDQM	CMOS, I_{OL} = 2mA			0.40	V
	V_{OL}(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP10, GP11, SDCLK, JTDO, JTRTCK	CMOS, I_{OL} = 4mA			0.40	V
Output off-leakage current	IOFF(1)	PDOUT0, PDOUT1, AFILT	Hi-Z Out	-10.00		10.00	µA
	IOFF(2)	SIFDO	Hi-Z Out	-10.00		10.00	µA

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Parameter	Symbol	Pin names	Conditions	min	typ	max	Unit
Built-in pull down resistor	RPD	SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP24, GP25, GP26, GP27, GP60, GP61, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15		50	100	200	kΩ
Charge pump output current	IPDOH	PDOUT1, PDOUT0	PCKIST = 100kΩ Current value setting: 1x	42.50	50.00	57.50	µA
	IPDOL	PDOUT1, PDOUT0		-57.50	-50.00	-42.50	µA
	IAFILH	AFILT			15.0		µA
	IAFILL	AFILT			15.0		µA

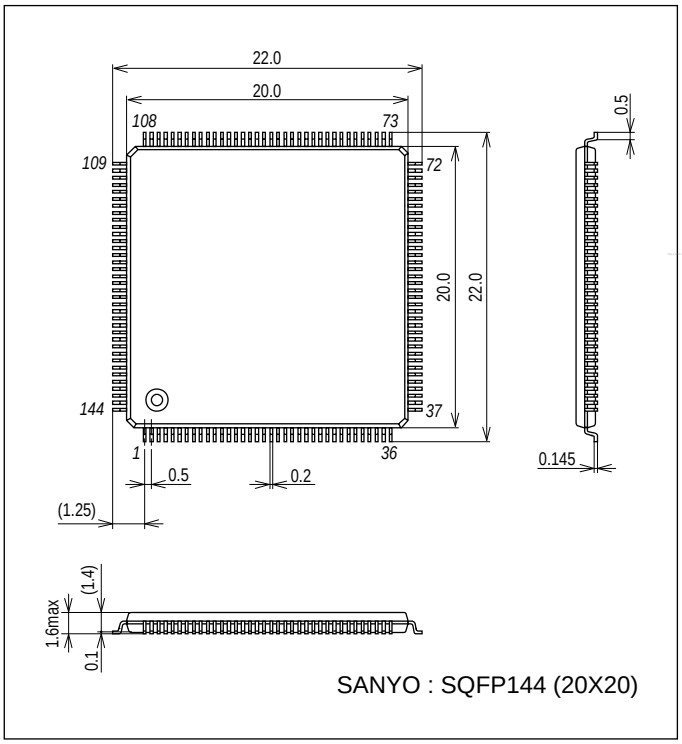
<Note>

- Put a internal pull down resistor or external pull down resistor or external pull up resistor to the SIFDO pin if its output condition is set to 3-State mode.

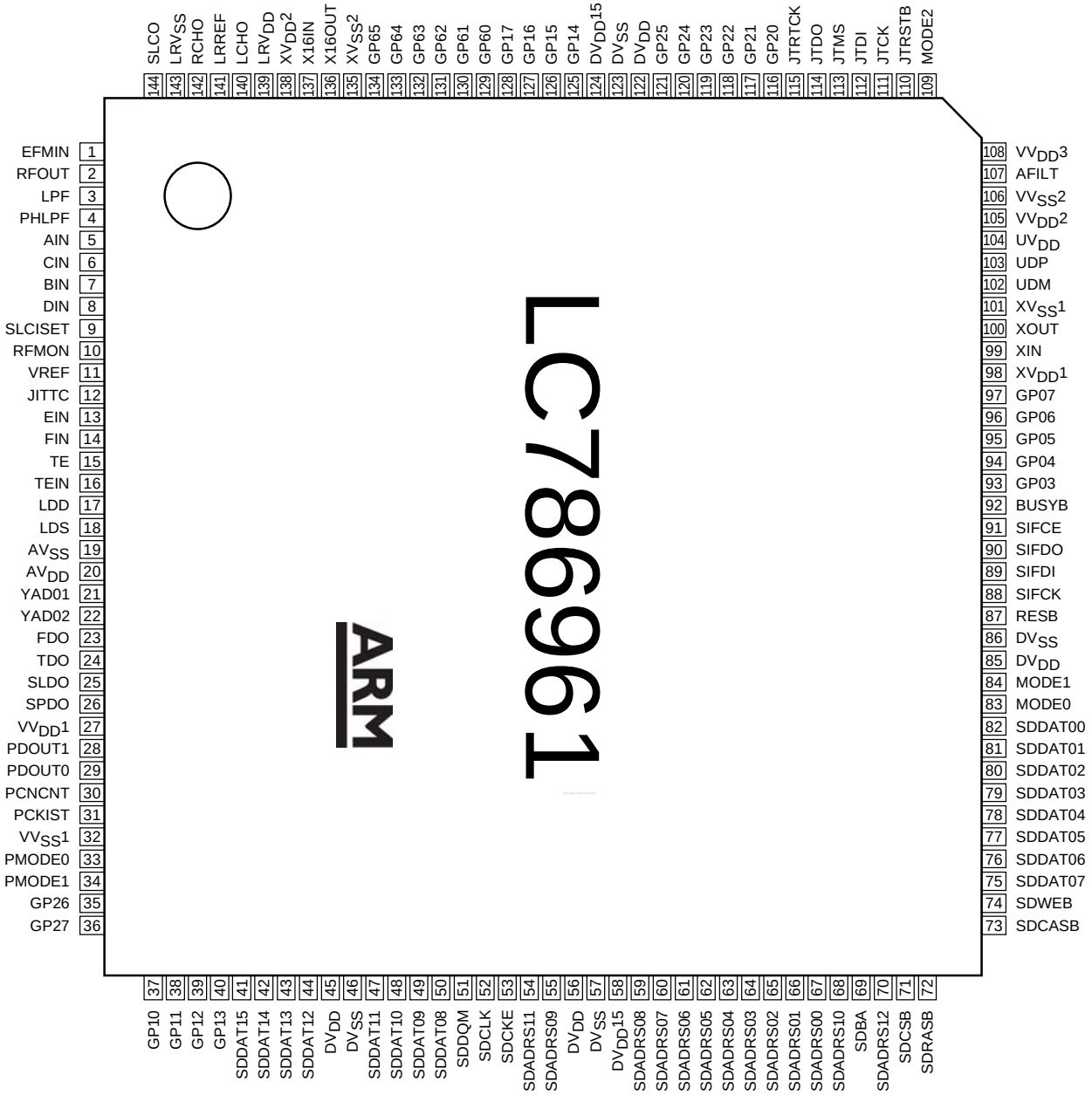
Package Dimensions

unit : mm (typ)

3214A



Pin Assignment



Top view

Pin Description

Pin No.	Pin name	I/O	State when "Reset"	Function
1	EFMIN	AI	Input	RF signal input
2	RFOUT	AO	Undefined	RF signal output
3	LPF	AO	Undefined	RF signal DC level detection low-pass filter capacitor connection
4	PHLPF	AO	Undefined	Defect detection low-pass filter capacitor connection
5	AIN	AI	Input	A signal input
6	CIN	AI	Input	C signal input
7	BIN	AI	Input	B signal input
8	DIN	AI	Input	D signal input
9	SLCISET	AI	Input	SLCO output current setting resistor connection
10	RFMON	AO	Undefined	IC internal analog signal monitor 1
11	VREF	AO	$AV_{DD}/2$	VREF voltage output
12	JITTC	AO	Undefined	Jitter detection capacitor connection
13	EIN	AI	Input	E signal input
14	FIN	AI	Input	F signal input
15	TE	AO	Undefined	TE signal output
16	TEIN	AI	Input	TE signal input used for TES signal generation
17	LDD	AO	Undefined	Laser power control signal output
18	LDS	AI	Input	Laser power detection signal input
19	AV_{SS}	-	-	Analog system ground. This pin must be connected to the 0V level.
20	AV_{DD}	-	-	Analog system power supply
21	YADO1	AI/AO	Input	AD input 1/FE signal monitor output
22	YADO2	AI/AO	Input	AD input 2/IC internal analog signal monitor 2
23	FDO	AO	$AV_{DD}/2$	Focus control signal output
24	TDO	AO	$AV_{DD}/2$	Tracking control signal output
25	SLDO	AO	$AV_{DD}/2$	Sled control signal output
26	SPDO	AO	$AV_{DD}/2$	Spindle control signal output
27	$VV_{DD}1$	-	-	EFMPLL power supply
28	PDOUT1	AO	Undefined	EFMPLL charge pump output 1
29	PDOUT0	AO	Undefined	EFMPLL charge pump output 0
30	PCNCNT	AI	Input	EFMPLL charge pump control voltage input
31	PCKIST	AI	Input	EFMPLL charge pump current setting resistor connection pin
32	$VV_{SS}1$	-	-	EFMPLL ground. This pin must be connected to the 0V level.
33	PMODE0	I	Input	Must be connected to the DV_{DD}.
34	PMODE1	I	Input	Must be connected to the DV_{DD}.
35	GP26	I/O	Input (L)	General purpose I/O port with pull down resistor
36	GP27	I/O	Input (L)	General purpose I/O port with pull down resistor
37	GP10	I/O	Input (L)	General purpose I/O port with pull down resistor UART1 data transmit
38	GP11	I/O	Input (L)	General purpose I/O port with pull down resistor UART1 data receive
39	GP12	I/O	Input (L)	General purpose I/O port with pull down resistor Clock control input 1
40	GP13	I/O	Input (L)	General purpose I/O port with pull down resistor Clock control input 2 Watch Dog Timer state monitor output SDRAM lower byte data mask control output SDRAM-DQML (LDQM) pin should be connected for 64Mbit-SDRAM (Only when “byte access” is enabled.)
41	SDDAT15	I/O	Input (L)	SDRAM data input/output 15 (pull down resistor)
42	SDDAT14	I/O	Input (L)	SDRAM data input/output 14 (pull down resistor)
43	SDDAT13	I/O	Input (L)	SDRAM data input/output 13 (pull down resistor)
44	SDDAT12	I/O	Input (L)	SDRAM data input/output 12 (pull down resistor)
45	DV_{DD}	-	-	Digital system power supply
46	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.

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Pin No.	Pin name	I/O	State when "Reset"	Function
47	SDDAT11	I/O	Input (L)	SDRAM data input/output 11 (pull down resistor)
48	SDDAT10	I/O	Input (L)	SDRAM data input/output 10 (pull down resistor)
49	SDDAT09	I/O	Input (L)	SDRAM data input/output 9 (pull down resistor)
50	SDDAT08	I/O	Input (L)	SDRAM data input/output 8 (pull down resistor)
51	SDDQM	O	Low	SDRAM data mask control output SDRAM-DQMH(UDQM) pin should be connected both for 16M and 64Mbit-SDRAM.
52	SDCLK	O	Low	SDRAM clock output
53	SDCKE	O	Low	SDRAM clock enable output
54	SDADRS11	O	Low	SDRAM address output 11 No use (NC) for 16Mbit-SDRAM SDRAM-ADRS11 pin connection for 64Mbit-SDRAM
55	SDADRS09	O	Low	SDRAM address output 9
56	DV_{DD}	-	-	Digital system power supply
57	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
58	$DV_{DD}15$	AO	High	Capacitor connection pin for internal regulator
59	SDADRS08	O	Low	SDRAM address output 8
60	SDADRS07	O	Low	SDRAM address output 7
61	SDADRS06	O	Low	SDRAM address output 6
62	SDADRS05	O	Low	SDRAM address output 5
63	SDADRS04	O	Low	SDRAM address output 4
64	SDADRS03	O	Low	SDRAM address output 3
65	SDADRS02	O	Low	SDRAM address output 2
66	SDADRS01	O	Low	SDRAM address output 1
67	SDADRS00	O	Low	SDRAM address output 0
68	SDADRS10	O	Low	SDRAM address output 10
69	SDBA	O	Low	SDRAM bank select address output SDRAM-BANK pin connection for 16Mbit-SDRAM SDRAM-BANK1 pin connection for 64Mbit-SDRAM
70	SDADRS12	O	Low	SDRAM address output 12 SDRAM-DQML (LDQM) pin connection for 16Mbit-SDRAM. SDRAM-BANK0 pin connection for 64Mbit-SDRAM
71	SDCSB	O	Low	SDRAM Chip Select output
72	SDRASB	O	Low	SDRAM Row Address Strobe output
73	SDCASB	O	Low	SDRAM Column Address Strobe output
74	SDWEB	O	Low	SDRAM Write Enable output
75	SDDAT07	I/O	Input (L)	SDRAM data input/output 7 (pull down resistor)
76	SDDAT06	I/O	Input (L)	SDRAM data input/output 6 (pull down resistor)
77	SDDAT05	I/O	Input (L)	SDRAM data input/output 5 (pull down resistor)
78	SDDAT04	I/O	Input (L)	SDRAM data input/output 4 (pull down resistor)
79	SDDAT03	I/O	Input (L)	SDRAM data input/output 3 (pull down resistor)
80	SDDAT02	I/O	Input (L)	SDRAM data input/output 2 (pull down resistor)
81	SDDAT01	I/O	Input (L)	SDRAM data input/output 1 (pull down resistor)
82	SDDAT00	I/O	Input (L)	SDRAM data input/output 0 (pull down resistor)
83	MODE0	I	Input	LSI mode set pin 0 This pin must be connected to the 0V level.
84	MODE1	I	Input	LSI mode set pin 1 This pin must be connected to the 0V level.
85	DV_{DD}	-	-	Digital system power supply
86	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
87	RESB	I	-	IC reset input ("L"-active) This pin must be set low once after power is first applied.
88	SIFCK	I	Input	Host-I/F Data transmit clock input for serial communication 1
89	SIFDI	I/O	Input	Host-I/F Data input for serial communication 1

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Pin No.	Pin name	I/O	State when "Reset"	Function
90	SIFDO	I/O	Input	Host-I/F Data output for serial communication 1 (CMOS or 3-State output)
91	SIFCE	I/O	Input	Host -I/F Enable signal input for serial communication 1 ("H"-active)
92	BUSYB	I/O	Input (L)	Host -I/F System busy signal output ("L"-active)
93	GP03	I/O	Input (L)	General purpose I/O port with pull down resistor USB device detection flag output
94	GP04	I/O	Input (L)	General purpose I/O port with pull down resistor IIC (master) clock output
95	GP05	I/O	Input (L)	General purpose I/O port with pull down resistor IIC (master) data input/output
96	GP06	I/O	Input (L)	General purpose I/O port with pull down resistor
97	GP07	I/O	Input (L)	General purpose I/O port with pull down resistor
98	$XV_{DD}1$	-	-	Oscillator power supply
99	XIN	I	Oscillation	12MHz oscillator connection
100	XOUT	O	Oscillation	12MHz oscillator connection
101	$XV_{SS}1$	-	-	Oscillator ground. This pin must be connected to the 0V level.
102	UDM	I/O	-	USB data input/output D- signal connection
103	UDP	I/O	-	USB data input/output D+ signal connection
104	UV_{DD}	-	-	USB power supply
105	$VV_{DD}2$	-	-	System PLL power supply
106	$VV_{SS}2$	-	-	System PLL ground. This pin must be connected to the 0V level.
107	AFILT	AO	Undefined	Audio PLL charge pump output
108	$VV_{DD}3$	-	-	Audio PLL power supply
109	MODE2	I	Input	LSI mode set pin 2 This pin must be connected to the 0V level.
110	JTRSTB	I	Input	JTAG reset input (Connect to pll-down resister or 0V level in normal mode.)
111	JTCK	I	Input	JTAG clock input (Connect to pll-down resister or 0V level in normal mode.)
112	JTDI	I	Input	JTAG data input (Connect to pll-down resister or 0V level in normal mode.)
113	JTMS	I	Input	JTAG mode input (Connect to pll-up resister or DV_{DD} level in normal mode.)
114	JTDO	O	Low	JTAG data output (Leave open in normal mode.)
115	JTRTCK	O	Low	JTAG return clock output (Leave open in normal mode.)
116	GP20	I/O	Input (L)	General purpose I/O port with pull down resistor Data 1 input/output for SD memory card
117	GP21	I/O	Input (L)	General purpose I/O port with pull down resistor Data 0 input/output for SD memory card
118	GP22	I/O	Input (L)	General purpose I/O port with pull down resistor Clock output for SD memory card
119	GP23	I/O	Input (L)	General purpose I/O port with pull down resistor Command input/output for SD memory card
120	GP24	I/O	Input (L)	General purpose I/O port with pull down resistor Data 3 input/output for SD memory card
121	GP25	I/O	Input (L)	General purpose I/O port with pull down resistor Data 2 input/output for SD memory card
122	DV_{DD}	-	-	Digital system power supply
123	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
124	$DV_{DD}15$	AO	High	Capacitor connection pin for internal regulator
125	GP14	I/O	Input (L)	General purpose I/O port with pull down resistor
126	GP15	I/O	Input (L)	General purpose I/O port with pull down resistor
127	GP16	I/O	Input (L)	General purpose I/O port with pull down resistor
128	GP17	I/O	Input (L)	General purpose I/O port with pull down resistor
129	GP60	I/O	Input (L)	General purpose I/O port with pull down resistor
130	GP61	I/O	Input (L)	General purpose I/O port with pull down resistor

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Pin No.	Pin name	I/O	State when "Reset"	Function
131	GP62	I/O	Input (L)	General purpose I/O port with pull down resistor
132	GP63	I/O	Input (L)	General purpose I/O port with pull down resistor
133	GP64	I/O	Input (L)	General purpose I/O port with pull down resistor
134	GP65	I/O	Input (L)	General purpose I/O port with pull down resistor
135	$XV_{SS}2$	-	-	Oscillator ground. This pin must be connected to the 0V level.
136	X16OUT	O	Oscillation	16.9344MHz oscillator connection
137	X16IN	I	Oscillation	16.9344MHz oscillator connection
138	$XV_{DD}2$	-	-	Oscillator power supply
139	LRV_{DD}	-	-	Audio LPF power supply
140	LCHO	AO	$LRV_{DD}/2$	Audio Lch data output
141	LRREF	AO	$LRV_{DD}/2$	Reference voltage for audio LPF
142	RCHO	AO	$LRV_{DD}/2$	Audio Rch data output
143	LRV_{SS}	-	-	Audio LPF ground. This pin must be connected to the 0V level.
144	SLCO	AO	Undefined	Slice Level Control output

<Note>

(1) For unused pins:

- The unused input pins must be connected to the GND (0V) level if there is no individual note in the above table.
- The unused output pins must be left open (No connection) if there is no individual note in the above table.
- The unused input/output pins must be connected to the GND (0V) or power supply pin for I/O block with internal pull down resistor OFF or be left open with internal pull down resistor ON when input pin mode or must be left open (No connection) when output pin mode if there is no individual note in the above table.
  When you connect an I/O pin which is an input pin without internal pull-down resistor at reset mode to the GND or power supply level, we recommend you to use pull-down resistor or pull-up resistor individually as fail-safe.

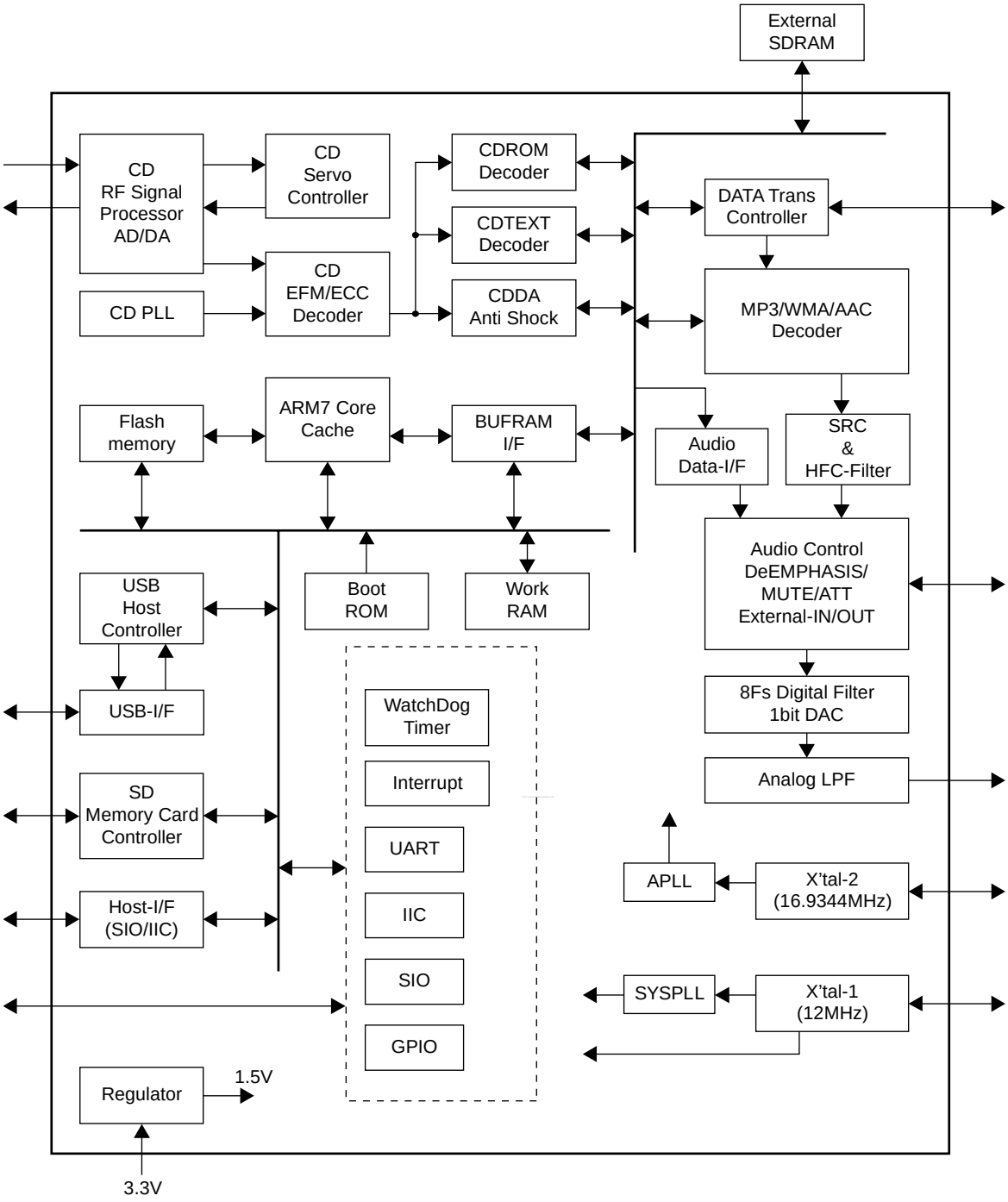
(2) For power supply pins:

- Same voltage level must be supplied to DV_{DD}, AV_{DD}, $XV_{DD}1$, $XV_{DD}2$, $VV_{DD}1$, $VV_{DD}2$, $VV_{DD}3$, UV_{DD} and LRV_{DD} power supply pins.
  (Refer to“Allowable operating ranges”.)

(3) For “Reset” condition:

- This LSI is not reset only by making the RESB pin “Low”.
  Refer to “Power on and Reset control” for detail of “Reset” condition.

Block Diagram

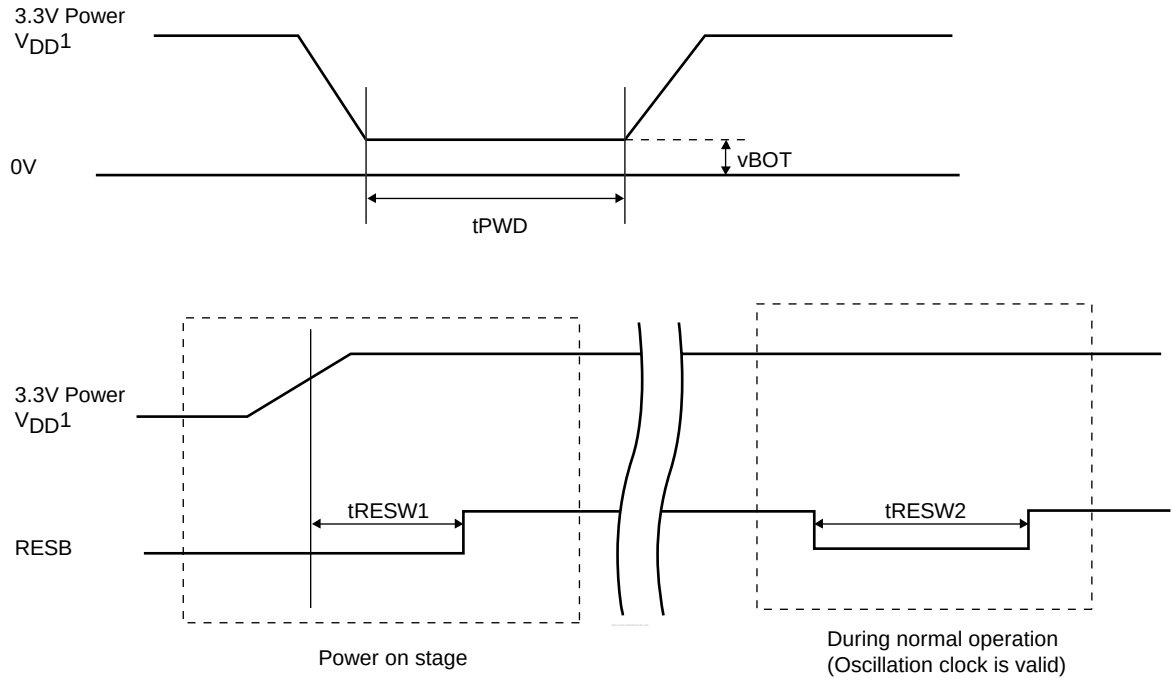


Power on and Reset control

- Attention when power on

  The RESB pin must be set to “Low” level to initialize the operating state of internal flash memory.
  If the power is on during the RESB pin is “High” level, this LSI may operate incorrectly because the internal flash memory is not initialized. In this case, this LSI is not initialized even if a low level supplied to RESB pin.
  Therefore, the RESB pin must be set to “Low” level when power is first supplied.
  You may input the voltage of 3.6V or less to each input pin when the power supply is off. However, it is necessary to supply a regulated voltage to the power supply pin beforehand when more than 3.6V voltage is input to the 5V tolerant input pins.

Power ON/Power Down/Reset timing



Parameter	Symbol	min	typ	max	unit
Power down time	tPWD	10			ms
Power down voltage	vBOT	0		0.2	V
Reset time (Power on)	tRESW1	20			ms
Reset time (Normal) (*1)	tRESW2	1			ms

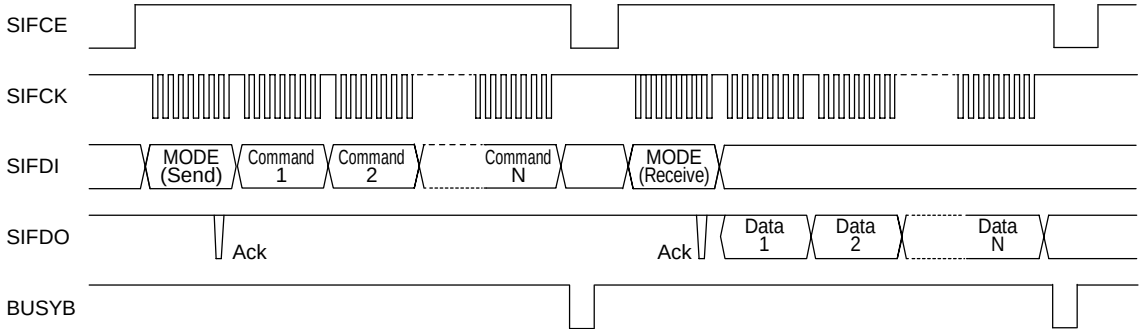
*1: The specification of tRESW2 above is the time defined while steady the X16 clock and having oscillated.
When the X16 clock has been stopped by the command etc. , the specification of tRESW2 could be larger than the value shown above, because it takes time that the X16 oscillator becomes stable.

Host interface

The data transmission between this LSI and Host controller is performed with SPI type synchronous SIO protocol. The transmission procedure is as follows.

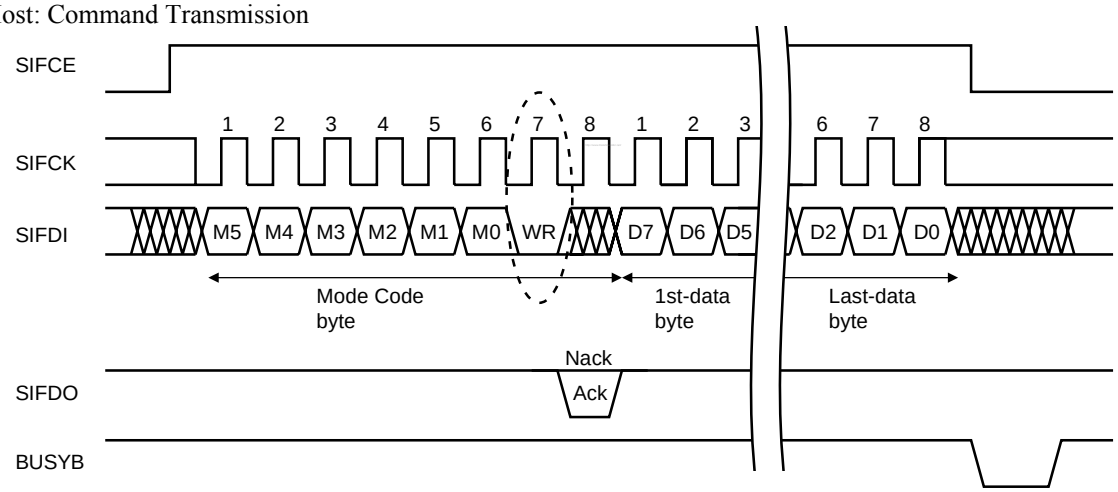
- Refer to the internal software specification of this LSI about M5 to M0 code in Mode code transmission. When the input data of M5 to M0 coincide to the data in the internal register, the SIFDO pin becomes to “Low” level (Ack) then the transmission is enabled. When not coincide, the SIFDO pin keeps “High” level (Nack) then the transmission is not enabled.
- The seventh data in Mode code transmission shows whether the following procedure is the Command transmission or the Data reception. When the seventh data is “Low”, the following procedure is Command transmission. When the seventh data is “High”, the following procedure is Data reception.
- Attention because the specifications of transmission timings are different depending on the internal CPU’s operating speed modes (Low speed or Normal speed). Refer to the table in next page.

Communication Interface format between Host controller

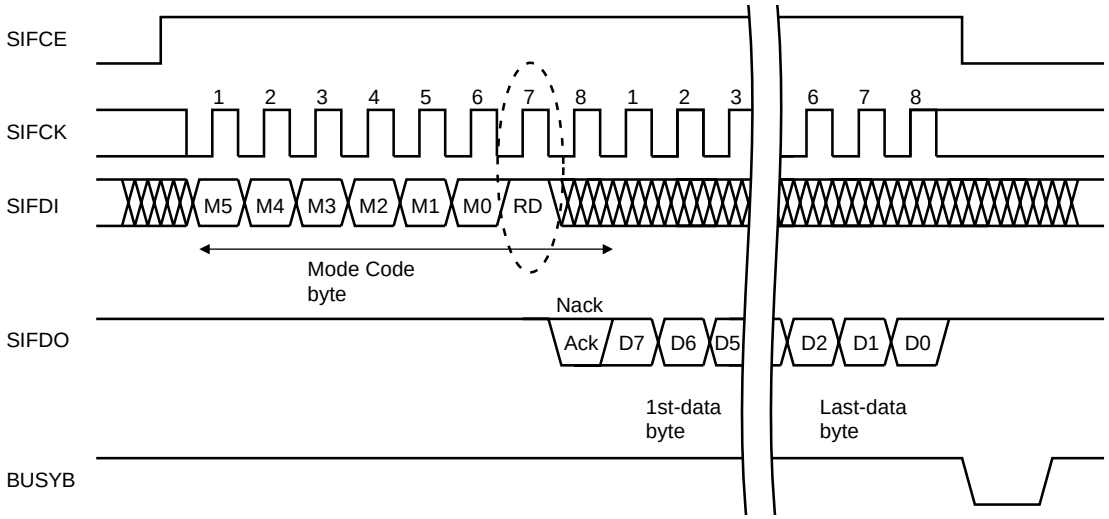


Transmission/Reception format between Host controller

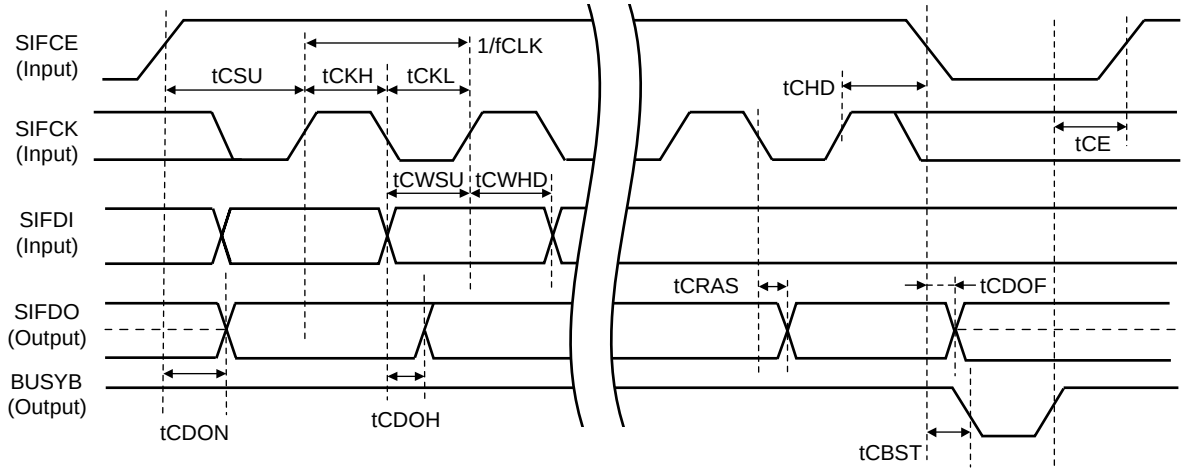
(1) Host: Command Transmission



(2) Host: Data Reception



Communication Timing specification between Host controller



Parameter	Symbol	Pin names	min	typ	max	unit
SIFCK clock frequency	fCLK	SIFCK			3.3 0.725	MHz
SIFCK clock "H" level width	tCKH	SIFCK	150 690			ns
SIFCK clock "L" level width	tCKL	SIFCK	150 690			ns
Transfer start enable time	tCE	BUSYB, SIFCE	0 0			ns
Setup time for transfer start	tCSU	SIFCE, SIFCK	100 200			ns
Hold time for transfer end	tCHD	SIFCE, SIFCK	100 200			ns
Setup time for SIFDI	tCWSU	SIFDI, SIFCK	75 75			ns
Hold time for SIFDI	tCWHD	SIFDI, SIFCK	75 200			ns
Output delay time for SIFDO “H”	tCDOH	SIFDO, SIFCK			100 350	ns
Output delay time for SIFDO	tCRAS	SIFDO, SIFCK			100 350	ns
Turn on time for SIFDO *1	tCDON	SIFDO, SIFCE			100 100	ns
Turn off time for SIFDO *1	tCDOF	SIFDO, SIFCE			150 150	ns
BUSYB "L" level output delay time	tCBST	BUSYB			150 350	ns

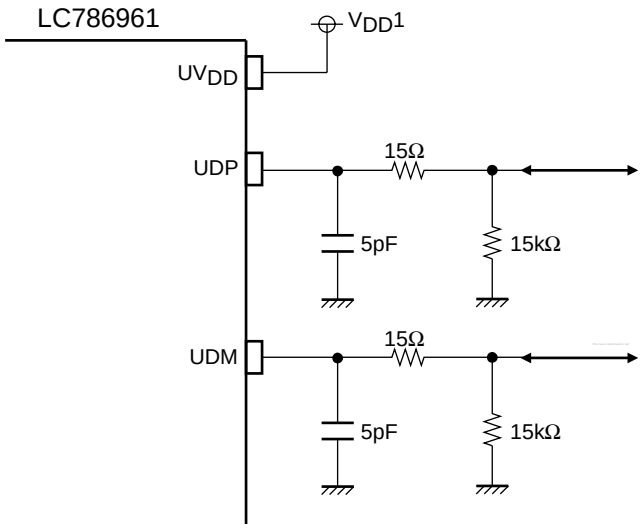
Internal CPU operating speed mode Upper step : Normal speed
Lower step : Low speed

*1: The tCDON and tCDOF specifications are for when the SIFDO pin is set to the 3-State mode.

USB Specification at Ta = -40°C to +85°C, $V_{DD}1$ = 3.0V to 3.6V,
$DV_{SS} = AV_{SS} = LRV_{SS} = XV_{SS}1 = XV_{SS}2 = VV_{SS}1 = VV_{SS}2 = 0V$

Parameter	Symbol	Pin names	Conditions	min	typ	max	unit
High-level input voltage	V_{IH} (USB)	UDM, UDP		2.0			V
Low-level input voltage	V_{IL} (USB)					0.8	
Input leakage current	ILI		Output driver: OFF	-10.0		10.0	µA
Differential input sensitivity	VDI		|(UDP) - (UDM)|	0.2			V
Common mode voltage range	VCM		Includes VDI range	0.8		2.5	V
High-level output voltage	V_{OH} (USB)		Connect 15kΩ ±5% pull-down resistor to GND (0V).	2.8		3.6	V
Low-level output voltage	V_{OL} (USB)		Connect 1.5kΩ ±5% pull-up resistor to $V_{DD}1$.	0		0.3	V
Crossover voltage	VCR			1.3		2.0	V
USB data rising time	TUR		CL = 50pF	4.0		20.0	ns
USB data falling time	TUF			4.0		20.0	

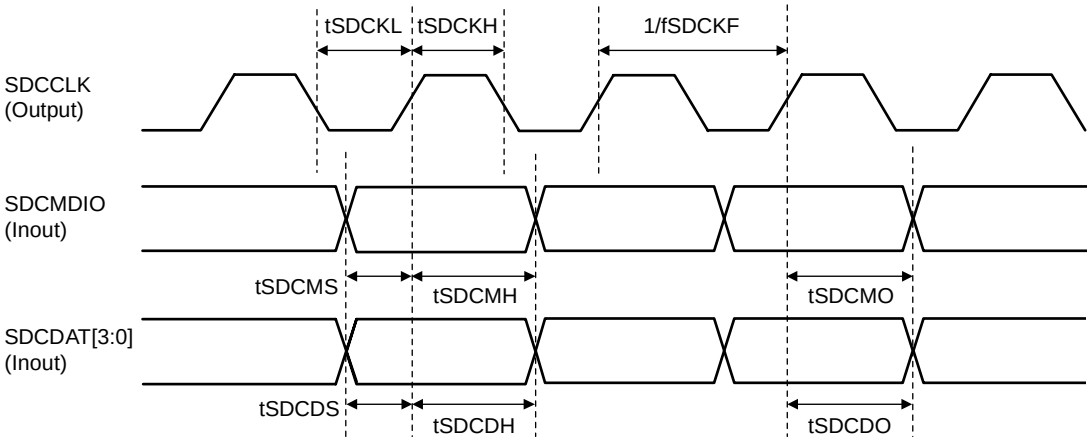
Example circuit for USB application



* The value of resistors and capacitors in this circuit might be needed to be adjusted for each application.

SD Memory Card Interface

SD Memory Card Input/Output Timing specification



* Relationship between signal name and pin name

SDCCLK : GP22 SDCMDIO : GP23 SDCDAT [3] : GP24
SDCDAT [2] : GP25 SDCDAT [1] : GP20 SDCDAT [0] : GP21

Parameter	Symbol	Pin names	min	typ	max	unit
SDCCLK clock frequency	fSDCKF	SDCCLK		6.0		MHz
SDCCLK clock "H" level width	tSDCKH	SDCCLK		83.3		ns
SDCCLK clock "L" level width	tSDCKL	SDCCLK		83.3		ns
Setup time for command input	tSDCMS	SDCMDIO, SDCCLK	30.0			ns
Hold time for command input	tSDCMH	SDCMDIO, SDCCLK	30.0			ns
Command output valid time	tSDCMO	SDCMDIO, SDCCLK			30.0	ns
Setup time for data input	tSDCDS	SDCDAT [3:0], SDCCLK	30.0			ns
Hold time for data input	tSDCDH	SDCDAT [3:0], SDCCLK	30.0			ns
Data output valid time	tSDCDO	SDCDAT [3:0], SDCCLK			30.0	ns

Note: Internal CPU (ARM7) must be set to normal mode. Never use the SD Memory Card interface at the internal CPU's Low speed mode.

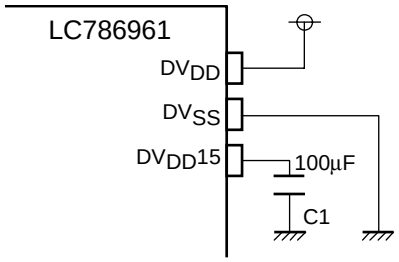
Internal Voltage Regulator at Ta = -40°C to +85°C,

$DV_{SS} = AV_{SS} = LRV_{SS} = XV_{SS}1 = XV_{SS}2 = VV_{SS}1 = VV_{SS}2 = 0V$

Parameter	Symbol	Condition	min	typ	max	unit
Output voltage	$DV_{DD}15$	$V_{DD}1$ = 3.0V to 3.6V	1.35	1.50	1.65	V
Load current	Iope	$V_{DD}1$ = 3.3V			200	mA

Note : The spec. of "load current" above is sum of the load current of two internal voltage regulator.

Example circuit for Regulator



* Same circuit need to be mounted both for two regulator pins. (No.58 and No.124)
* The capacitor C1 must be greater than 50µF and low Secure 50µF or more for low ESR and the capacity value in the range of the operating temperature so that there is a possibility of the oscillation when the capacity value changes by the temperature change etc.
(The recommended value is 100µF.)

A/D, D/A converter Characteristics for servo

at Ta = -40°C to +85°C, $V_{DD}1$ = 3.3V, $DV_{SS} = AV_{SS} = LRV_{SS} = XV_{SS}1 = XV_{SS}2 = VV_{SS}1 = VV_{SS}2 = 0V$

Parameter	Symbol	Condition	min	typ	max	unit
Resolution	Res			8		bit
Maximum input/output range	Vaio1			$4/5 \times V_{DD}1$		V
Minimum input/output range	Vaio2			$1/5 \times V_{DD}1$		V

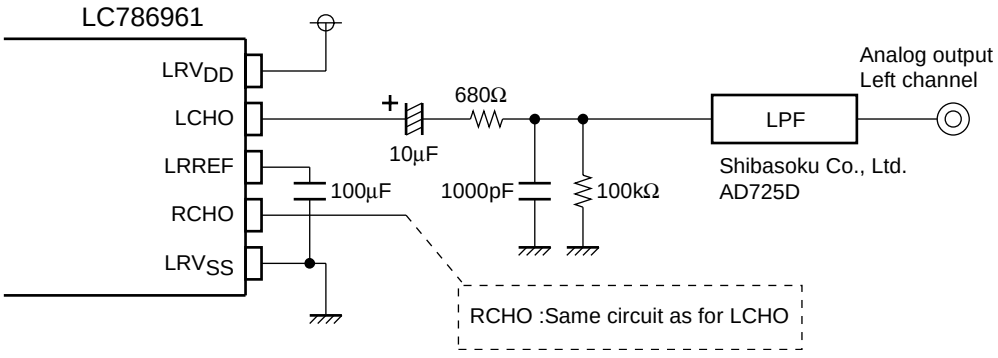
1-Bit D/A converter Characteristics

at Ta = 25°C, $V_{DD}1$ = 3.3V, $DV_{SS} = AV_{SS} = LRV_{SS} = XV_{SS}1 = XV_{SS}2 = VV_{SS}1 = VV_{SS}2 = 0V$

Parameter	Symbol	Pin names	Conditions	min	typ	max	unit
Output level	LEVEL	LCHO, RCHO	With a 1kHz, 0dB data signal		0.63		Vrms
Total harmonics distortion	THD+N	LCHO, RCHO	With a 1kHz, 0dB data signal, Using the 20kHz Low-pass filter (built-in AD725D)		0.008	0.012	%
Dynamic range	DR	LCHO, RCHO	With a 1kHz, -60dB data signal, Using the 20kHz Low-pass filter and A-filter (built-in AD725D)	92	96		dB
Signal to noise ratio	S/N	LCHO, RCHO	With a 1kHz, 0dB data signal, Using the 20kHz Low-pass filter and A-filter (built-in AD725D)	95	98		dB
Cross talk	CT	LCHO, RCHO	With a 1kHz, 0dB data signal, Using the 20kHz Low-pass filter (built-in AD725D)	82	85		dB

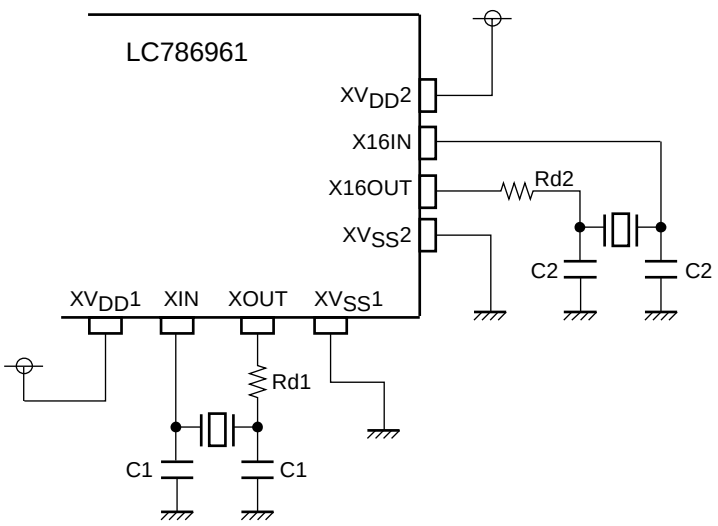
Note : Measured in normal speed playback mode in SANYO's 1-bit D/A converter block reference circuit.

1-Bit D/A converter output reference circuit



Oscillator

Example circuit for Oscillator



(1) XIN/XOUT: 12.0000MHz

- For System Main clock, USB control
- Recommended Oscillator

Nihon Dempa Kogyo Co., Ltd.

Type	Recommended value
NX5032GA	Rd1 = 0Ω, C1 = 4pF
NX8045GB	Rd1 = 0Ω, C1 = 4pF

(2) X16IN/X16OUT: 16.9344MHz

- For CD control, Audio control
- Recommended Oscillator

Murata Manufacturing Co., Ltd.

Type	Recommended value
CSTCE16M9V53-R0	Rd2 = 0Ω, C2 = open
CSTCW16M9X51008-R0	Rd2 = 0Ω, C2 = open
CSTLS16M9X53-B0	Rd2 = 0Ω, C2 = open

Nihon Dempa Kogyo Co., Ltd.

Type	Recommended value
AT51-CD2	Rd2 = 0Ω, C2 = 8pF

<Notes>

- Because the characteristics of oscillator could be changed according to the circuit board, ask evaluation with the individual original circuit board to the oscillator maker.
- The accuracy of 12MHz oscillator (XIN/XOUT) must be in ±500ppm when this oscillator clock is used for USB Host function.
- Concerning about internal circuit for XIN/XOUT and X16IN/X16OUT, refer to the “Analog Pin Internal Equivalent Circuits” section.

SDRAM Interface

(1) Required specification for external SDRAM

Memory size :16Mbit or 64Mbit
Data width :16bit
CAS latency :2
Burst length :Full

(2) Interface pins to external SDRAM

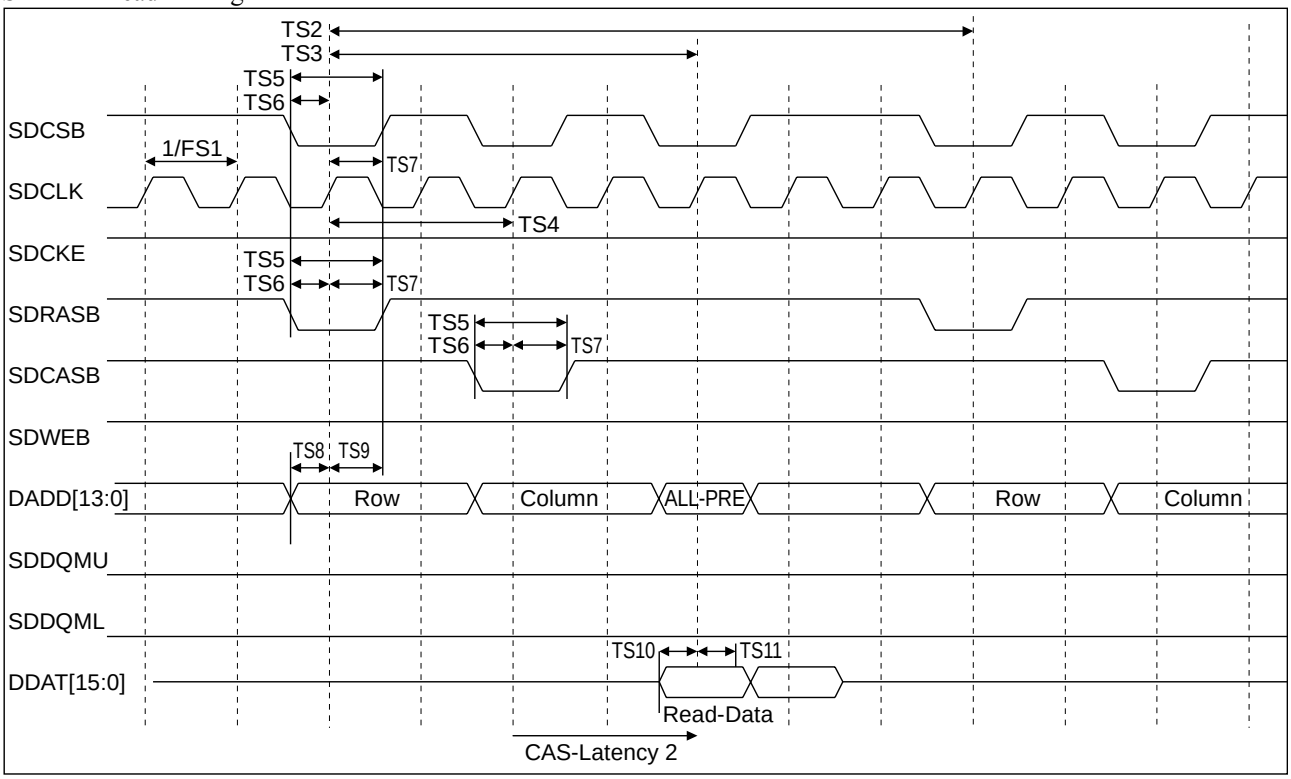
Pin Name	Function at 16Mbit-SDRAM	Function at 64Mbit-SDRAM	Signal name in Cf. P24, P25
SDDAT15 to SDDAT00	Data input/output (16bit)	Data input/output (16bit)	DDAT[15:0] DDAT[15:0]
SDADRS10 to SDADRS00	Address output (11bit)	Address output (11bit)	DADD[10:0] DADD[10:0]
SDADRS11	Not used	Address (A11) output	- DADD[11]
SDADRS12	DQML (LDQM) output Lower byte data mask control	Address (A12) or bank0 output	SDDQML DADD[12]
SDBA	Bank output	Bank or bank1 output	DADD[11] DADD[13]
SDDQM	DQMH (UDQM) output Upper byte data mask control	DQMH (UDQM) output Upper byte data mask control	SDDQMU SDDQMU
GP13	Not used	DQML (LDQM) output Lower byte data mask control	- SDDQML
SDCSB	CSB output	CSB output	SDCSB SDCSB
SDRASB	RASB output	RASB output	SDRASB SDRASB
SDCASB	CASB output	CASB output	SDCASB SDCASB
SDWEB	WEB output	WEB output	SDWEB SDWEB
SDCKE	Clock enable output	Clock enable output	SDCKE SDCKE
SDCLK	Clock output	Clock output	SDCLK SDCLK

Notes

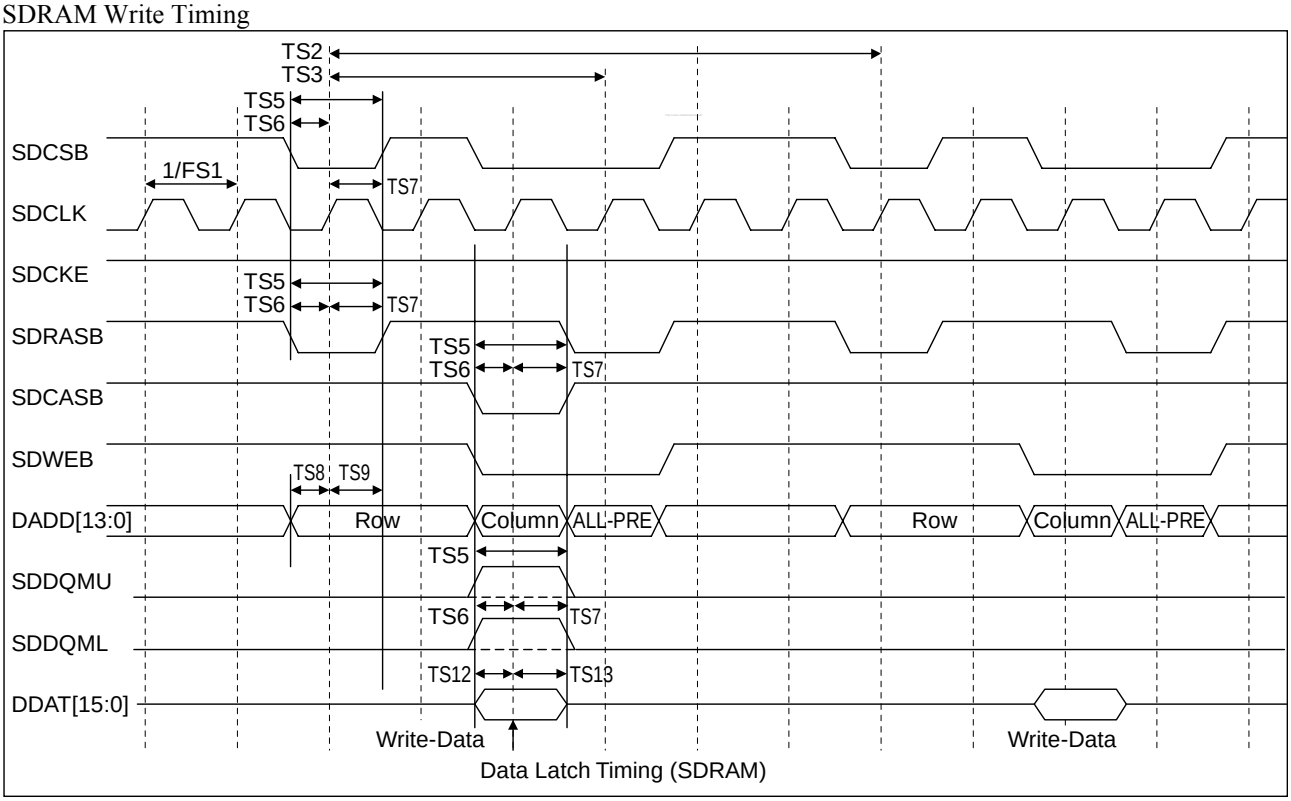
- SDADRS11 and GP13 in 16Mbit-SDRAM using mode should be treated as described below.
  SDADRS11 : Open (No connect)
  GP13 : Use as other function or Open
- SDDAT00 to SDDAT15 pins can have internal pull down resistor optionally. Those pull down resistors are set to ON mode in initialization.
  When setting the SDRAM using mode, those pull down resistors will be set to OFF mode.
- Some signals named in P22 to P23 use different pins according to the using SDRAM. The signal name in P22 to P23 for the actual pin is shown at the most right column in above table.
  Upper step : Signal name in 16Mbit-SDRAM using mode
  Lower step : Signal name in 64Mbit-SDRAM using mode

(3) SDRAM Access Timing

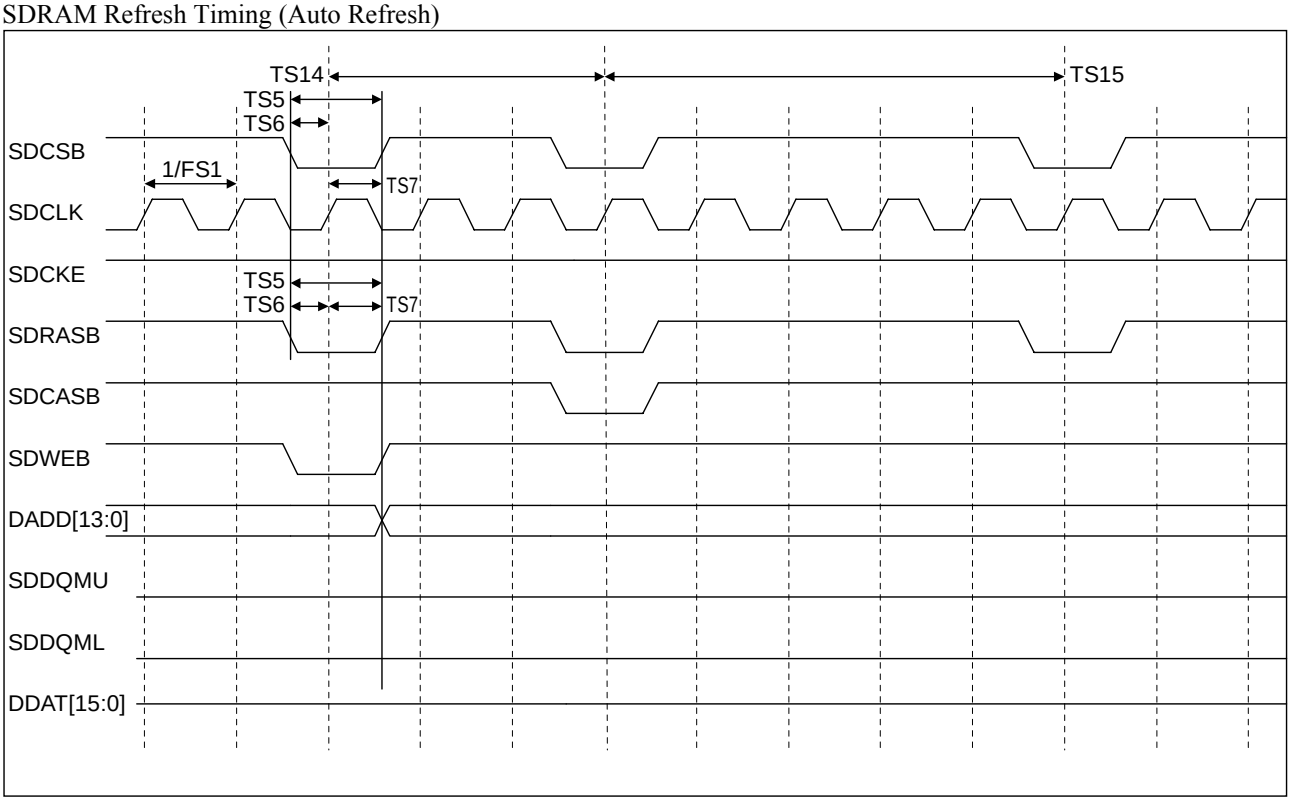
SDRAM Read Timing



SDRAM Write Timing



SDRAM Refresh Timing (Auto Refresh)

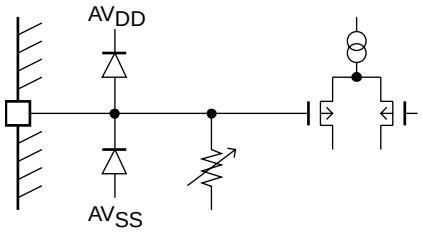
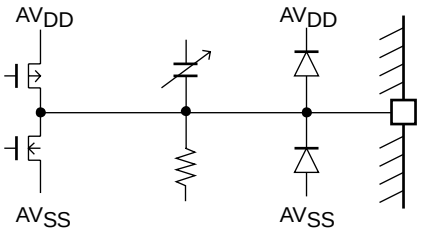
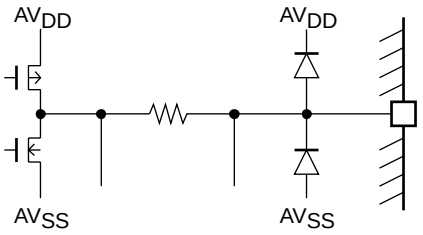
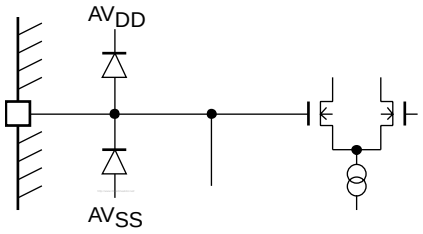
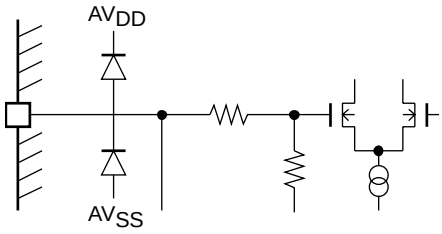
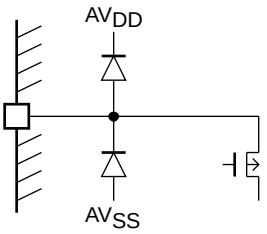
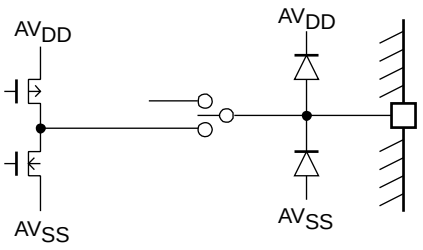


Symbol	Parameter	min	typ	max	unit
FS1	SDRAM clock (SDCLK) frequency		16.9344		MHz
TS2	Row (SDRASB) cycle time	(1/FS1)×5			ns
TS3	Row (SDRASB) active time	(1/FS1)×3			ns
TS4	RASB-CASB delay time (SDRASB-SDCASB)	(1/FS1)×2			ns
TS5	Command "L" level width (SDCSB, SDCKE, SDRASB, SDCASB, SDWEB)	40			ns
TS6	Command setup time (SDCSB, SDCKE, SDRASB, SDCASB, SDWEB, SDDQMU, SDDQML)	10			ns
TS7	Command hold time (SDCSB, SDCKE, SDRASB, SDCASB, SDWEB, SDDQMU, SDDQML)	10			ns
TS8	Address (DADD) setup time	10			ns
TS9	Address (DADD) hold time	10			ns
TS10	SDRAM read data setup time (Data read from SDRAM)	20			ns
TS11	SDRAM read data hold time (Data read from SDRAM)	0			ns
TS12	SDRAM write data hold time before rising edge of SDCLK (Data write to SDRAM)	10			ns
TS13	SDRAM write data hold time after rising edge of SDCLK (Data write to SDRAM)	10			ns
TS14	Row (SDRASB) pre-charge time	(1/FS1)×3			ns
TS15	Row (SDRASB) active time after refresh	(1/FS1)×5			ns

Notes

- Setup time and Hold time specifications in above table are measured from the rising edge of SDCLK signal.
- All the specifications in above table are applied to Read mode, Write mode and Refresh mode.

Analog Pin Internal Equivalent Circuits

Pin Name (Pin No.)	Equivalent circuit
EFMIN (1)	
RFOUT (2)	
LPF (3)	
PHLPF (4)	
AIN (5) CIN (6) BIN (7) DIN (8)	
SLCISET (9)	
RFMON (10)	

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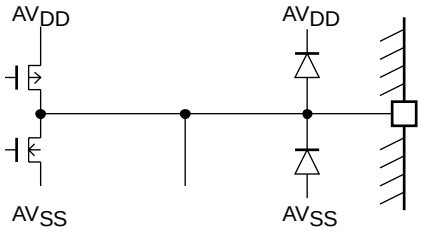
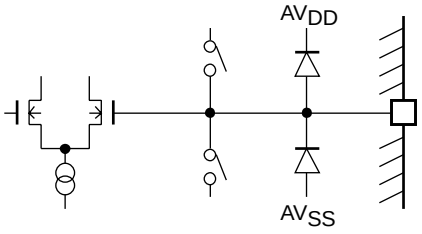
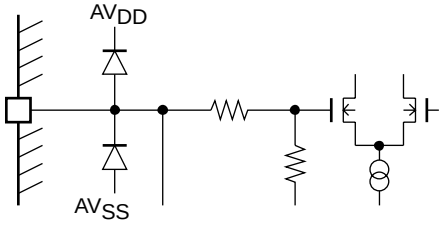
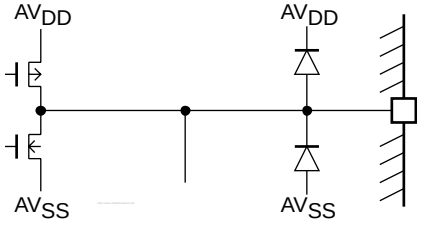
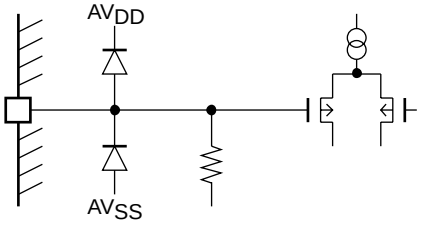
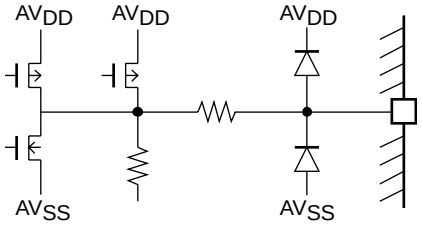
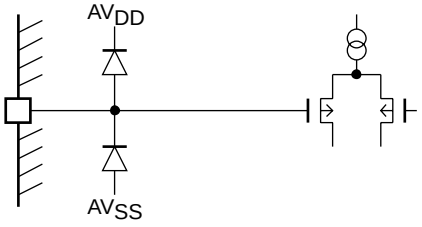
Pin Name (Pin No.)	Equivalent circuit
VREF (11)	
JITTC (12)	
EIN (13) FIN (14)	
TE (15)	
TEIN (16)	
LDD (17)	
LDS (18)	

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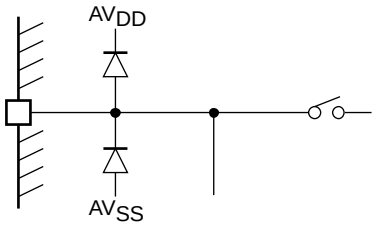
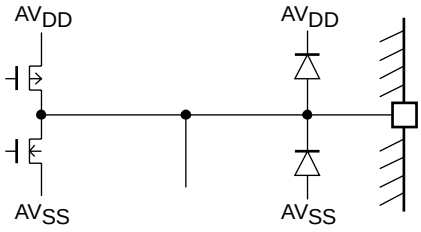
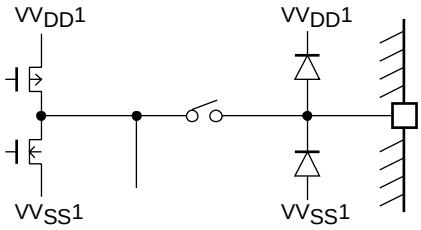
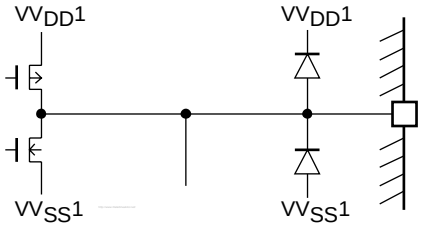
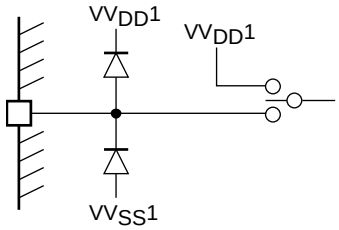
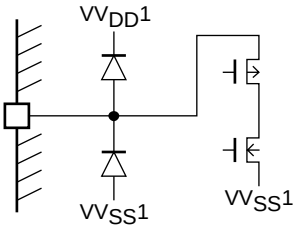
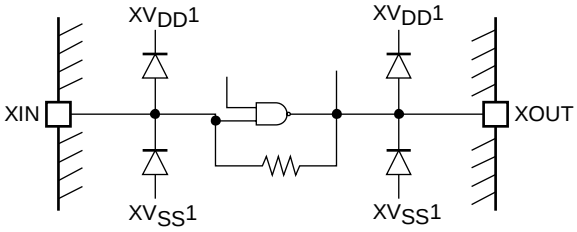
Pin Name (Pin No.)	Equivalent circuit
YADO1 (21) YADO2 (22)	
FDO (23) TDO (24) SLDO (25) SPDO (26)	
PDOUT1 (28)	
PDOUT0 (29)	
PCNCNT (30)	
PCKIST (31)	
XIN (99) XOUT (100)	

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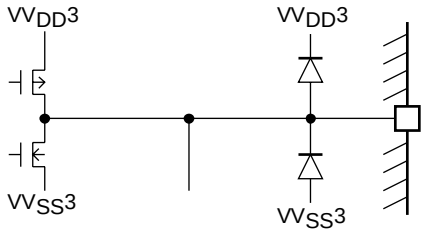
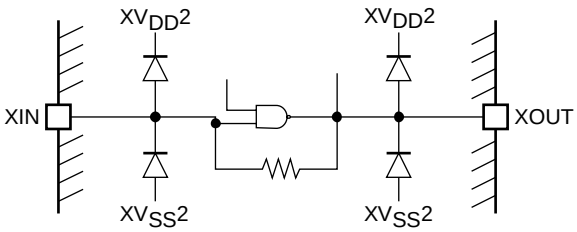
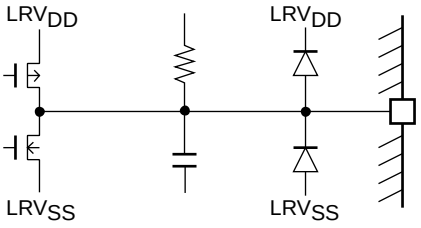
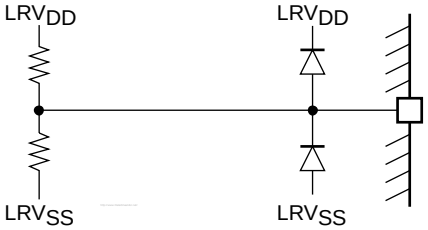
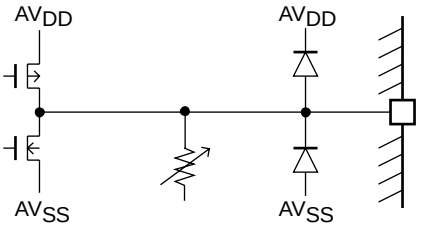
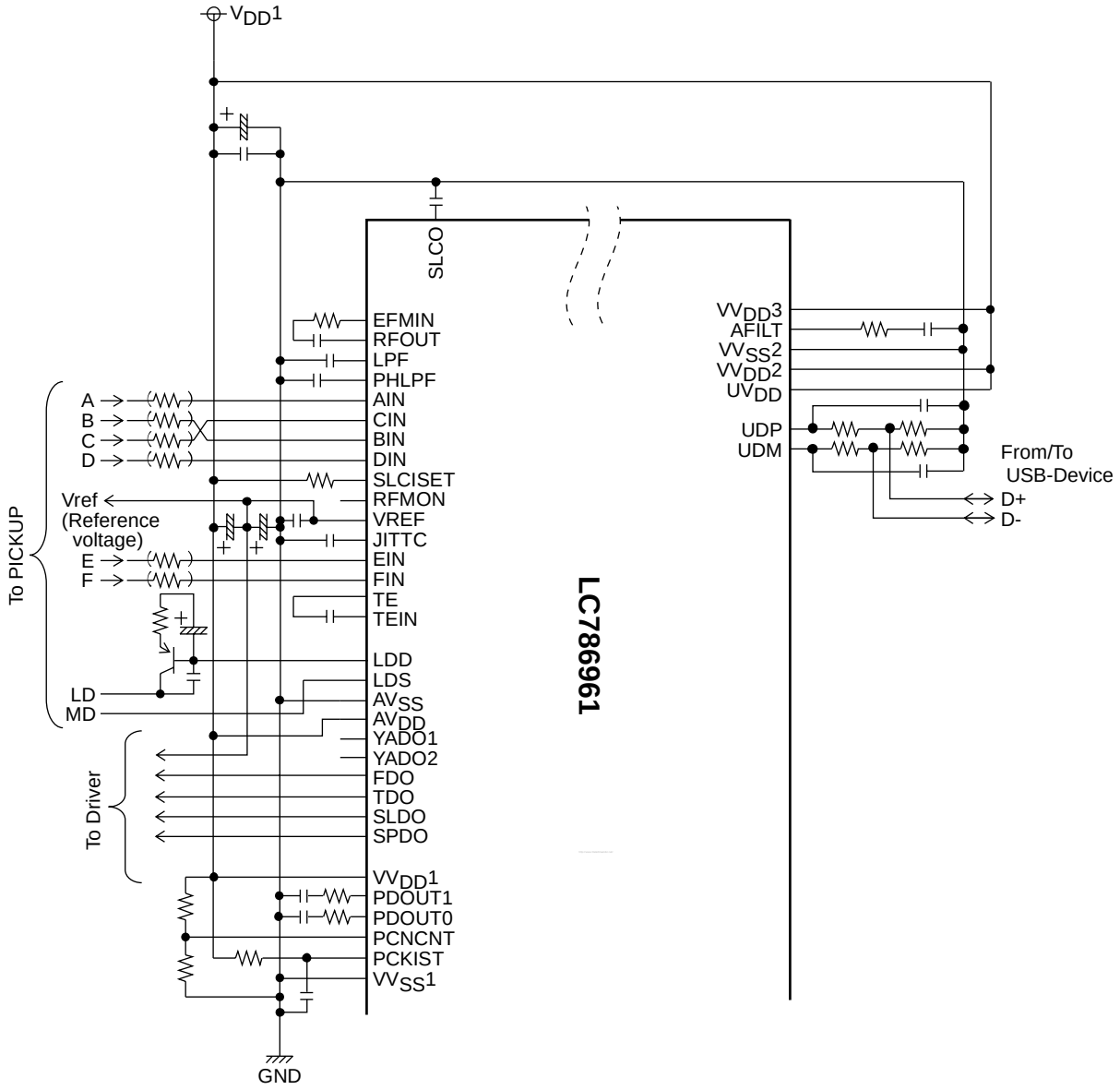
Pin Name (Pin No.)	Equivalent circuit
AFILT (107)	
X16OUT (136) X16IN (137)	
LHCO (140) RCHO (142)	
LRREF (141)	
SLCO (144)	

Sample Application Circuit



* This sample circuit is only for CD servo block, each PLL block and USB block.
The value of each component needs to be adjusted under the target conditions.
The circuit for CD servo shown above could be changed depending on the CD mechanism used.

Concerning to the application circuit for Regulator, Audio DAC and Oscillator, refer to the page 19 and 20 respectively.