# SANYO LC7883

Dual 16 bit D/A Converter with Digital Filter for Audio System

TENTATIVE

## 1. Summary

LC7883 is 16 bit D/A converter with eight-times over sampling digital filter.

## 2. Features

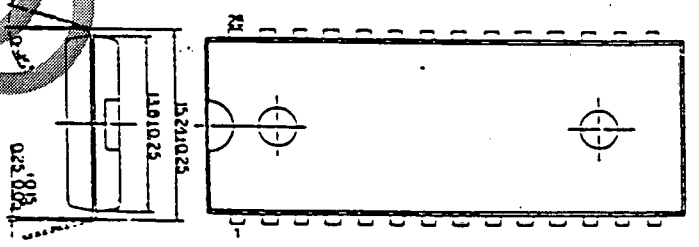
- ★ Eight-times over sampling digital filter
- ★ Digital de-emphasis
- ★ Digital attenuation
- ★ Double speed operation
- ★ 48CLK-384Fs, 49CLK-392Fs, 56CLK-448Fs, 64CLK-512Fs operations
- ★ Dynamic level shift conversion method
- ★ Independent dual channel D/A converter (in-phase output)
- ★ Single 5v power supply

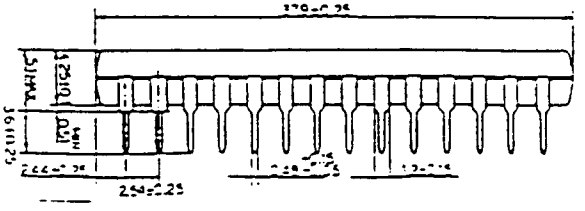
## 3. Absolute Maximum Rating/Ta=25°C ( $V_{SS}$ = 0 V )

| item | symbol | rating | unit |
|---|---|---|---|
| max. power supply voltage | $V_{DD}$ | −0.3 ~ +7.0 | V |
| input voltage | $V_{IN}$ | −0.3 ~ $V_{DD}$ + 0.3 | V |
| output voltage | $V_{OUT}$ | −0.3 ~ $V_{DD}$ + 0.3 | V |
| operating temp. | Topg | −30 ~ +75 | °C |
| storage temp. | Tstg | −40 ~ +125 | °C |

## 4. Physical Configuration Diagrams

DIP-28
(600mil)





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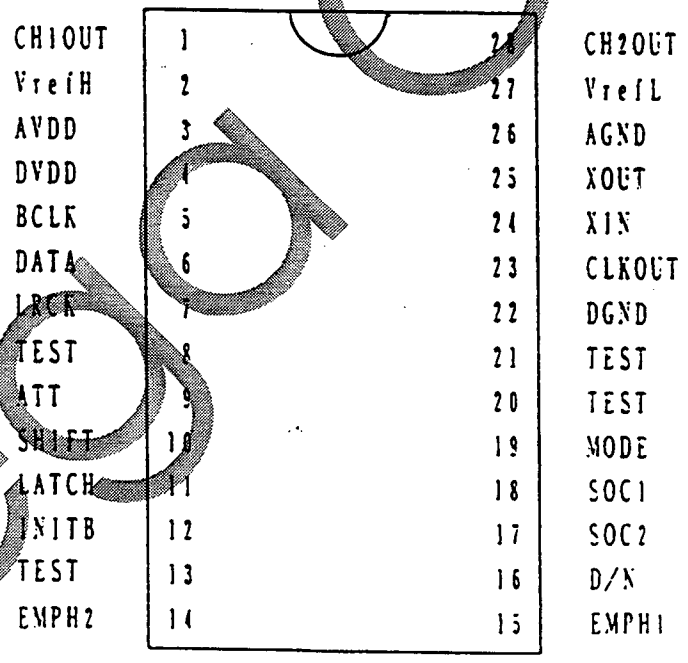
5. Recommended Operating Conditions

| item | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| power supply voltage | $V_{DD}$ | 4.5 | 5.0 | 5.5 | V |
| reference voltage "H" | VrefH | $V_{DD}$-0.5 | | $V_{DD}$ | V |
| reference voltage "L" | VrefL | 0 | | 0.5 | V |
| input voltage "H" | $V_{IH}$ | 2.2 | | $V_{DD}$+0.3 | V |
| input voltage "L" | $V_{IL}$ | -0.3 | | 0.8 | V |
| operating ambient temp. | Ta | -30 | | 75 | °C |

6. Pin Layout

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7. Pin Description

| PIN No | PIN name | I/O | FUNCTION |
|---|---|---|---|
| 1 | CH1OUT | O | DAC CH-1 output pin |
| 2 | VrefH | R | reference voltage "H" input pin |
| 3 | AVDD | P | analog system power supply pin |
| 4 | DVDD | P | digital system power supply pin |
| 5 | BCLK | I | bit CLK pin |
| 6 | DATA | I | digital audio data input pin<br>input in bit serial from MSB |
| 7 | LRCK | I | LR CLK input pin<br>LRCK= "H" CH1<br>LRCK= "L" CH2 |
| 8 | TEST | I | test pin (normally "L" ) |
| 9 | ATT | I | attenuation data input pin<br>input in bit serial from LSB |
| 10 | SHIFT | I | attenuation data shift CLK input pin |
| 11 | LATCH | I | attenuation data latch CLK input pin |
| 12 | INITB | I | initializing signal input pin(normally "H" ) |

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| PIN No | PIN name | I/O | FUNCTION |
|---|---|---|---|
| 13 | TEST | I | test pin (normally "L" ) |
| 14 | EMPH2 | I | de-emphasis set pin |
| 15 | EMPH1 | I | |
| 16 | D/N | I | normal/double speed switch pin |
| 17 | SOC2 | I | input source select pin (PULL DOWN) |
| 18 | SOC1 | I | |
| 19 | MODE | I | operation mode set pin (PULL DOWN) |
| 20 | TEST | I | test pin (normally "L" ) (PULL DOWN) |
| 21 | TEST | I | |
| 22 | DGND | P | digital system GND pin |
| 23 | CLKOUT | O | CLK output pin<br>At 392Fs :1/2 XOUT<br>At 384FS, 448Fs, 512Fs :1/4 XOUT |
| 24 | XIN | I | crystal oscillation input pin |
| 25 | XOUT | O | crystal oscillation output pin |
| 26 | AGND | P | analog system GND pin |
| 27 | VrefL | R | reference voltage "L" input pin |
| 28 | CH2OUT | O | D A C C H − 2 output pin |

I :INPUT PIN
O :OUTPUT PIN
P :POWER PIN
R :REFERENCE VOLTAGE PIN

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8. Electric Characteristics

(Ta=25°C. VDD=5.0V. VrefH=5.0V VrefL=0.0V unless it is specified)

| item | symbol | condition | MIN. | TYP. | MAX. | unit |
|---|---|---|---|---|---|---|
| D A C resolution | RES | | | 16 | | bit |
| total harmonic distortion | THD1 | 1KHz. 0dB | | | 0.08 | % |
| cross talk | C·T | 1KHz. 0dB | | -85 | -79 | dB |
| signal/noise ratio | S/N | 1KHz. 0dB | 85 | 92 | | dB |
| power consumption | Pd | ※1 | | 250 | 300 | mW |
| oscillating frequency | fx | | | 16.9344 | 25 | MHz |
| amplitudo of clkout(pin23) | $A_{CLK}$ | ※2 | 1 | | | VPP |
| PULL DOWN resistance (PIN 17.18.19.20.21) | $R_{DOWN}$ | | 10 | | 80 | KΩ |
| input BCLK frequency | $f_{BCK}$ | | | | 3.1 | MHz |
| input BCLK pulse width | $t_{WB}$ | | 100 | | | nS |
| input DATA setup time | $t_{DS}$ | | 20 | | | |
| input DATA hold time | $t_{DH}$ | | 20 | | | |
| input LRCK setup time | $t_{LRS}$ | | 50 | | | |
| input LRCK hold time | $t_{LRH}$ | | 50 | | | |
| program input basic time | $t_{PR}$ | fx= | 250 | | | |
| latch input pulse width | $t_{WLT}$ | 16.9344MHz | 50 | | | |
| SHIFT.LATCH.rise time | tr | | | | 200 | |
| SHIFT.LATCH.fall time | tf | | | | 200 | |
| A T T setup time | $t_{SET}$ | | 500 | | | |
| A T T hold time | $t_{HOLD}$ | | 500 | | | |
| interval | $t_{INT}$ | | 1000 | | | |

※1 X I N amp. 1.5~3.5V, fx=16.9344MHz
※2 fx=16.9344MHz CL=20pF
Measuring circuits accord with application circuit examples.

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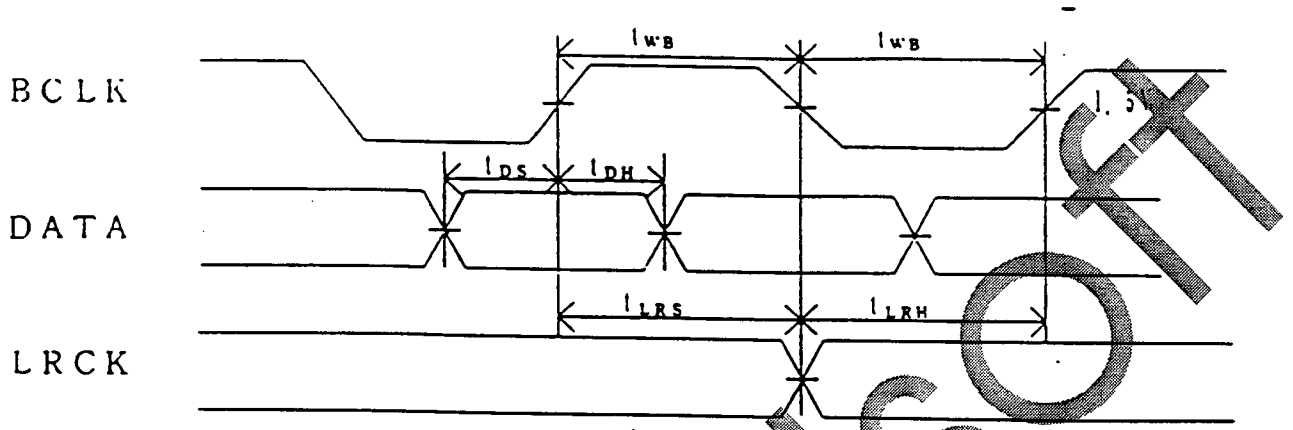
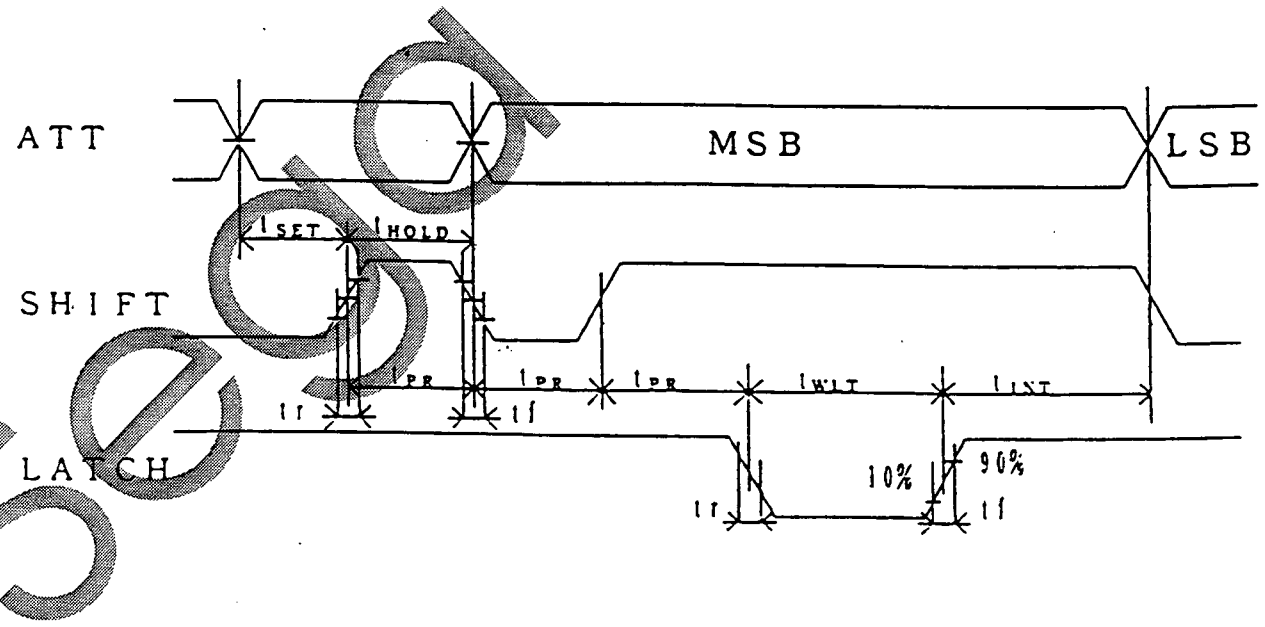
[ Audio Input ]




[ Program Input ]

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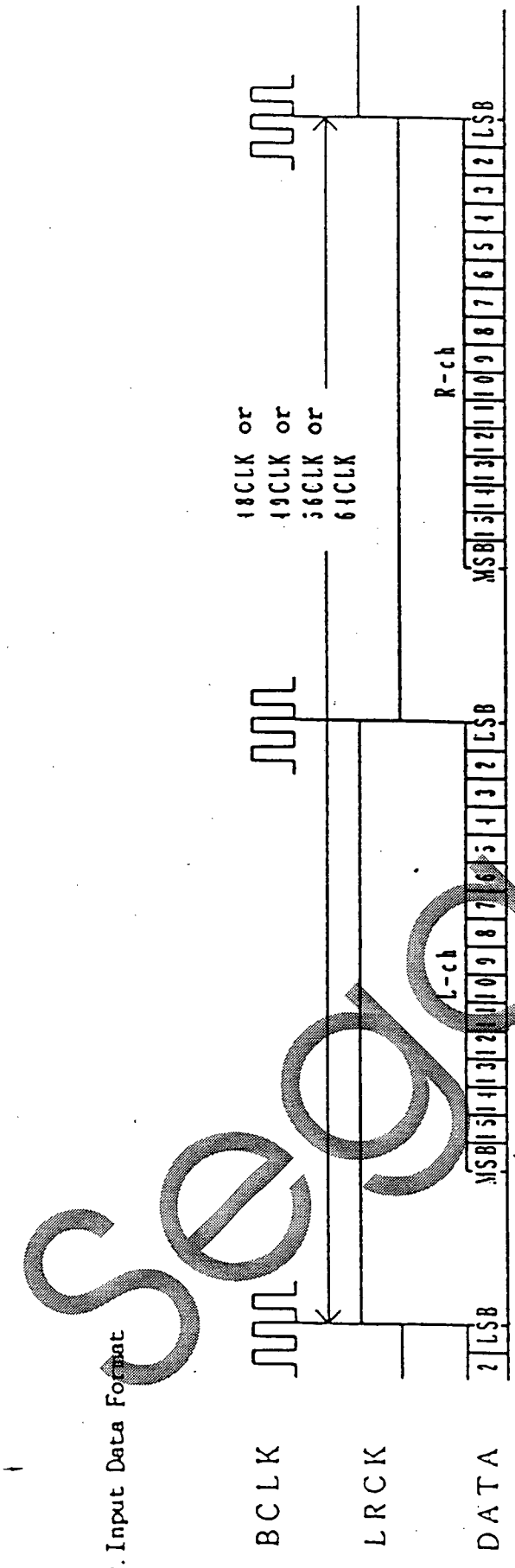
9. Input Data Format

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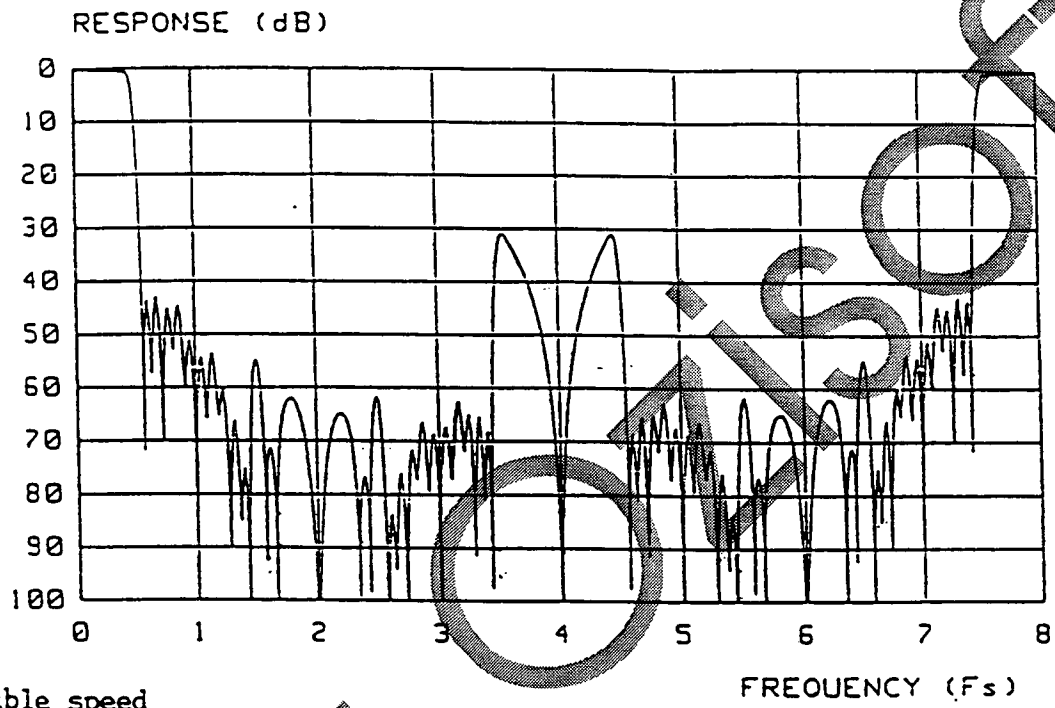
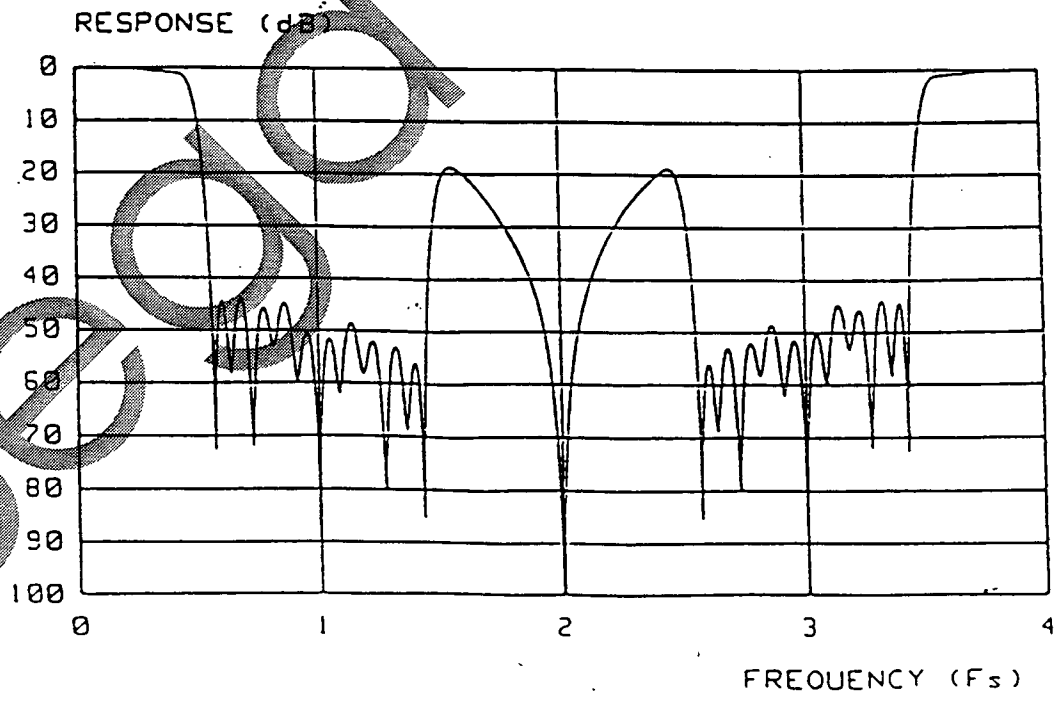
10. Filter Characteristics (Theoretical value)

At normal speed: 8 times over sampling
At double speed: 4 times over sampling
Ripple: within ±0.05dB
Stop-band attenuation: under -40dB

·Normal speed




·Double speed

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11. Operation Description

LC7883M consists of 8-times over sampling digital filter and 16bit D/A converter.

·8-times over sampling digital filter

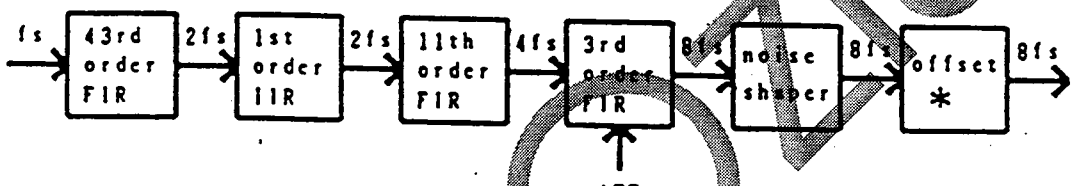
The digital filter process functions are shown in block diagram below. During the process. 18-bit data transfer are performed and 16-bit data are output to DAC after noise shaping of lower 6 bit of 22 bit data.

The digital filter has normal and double speed modes.

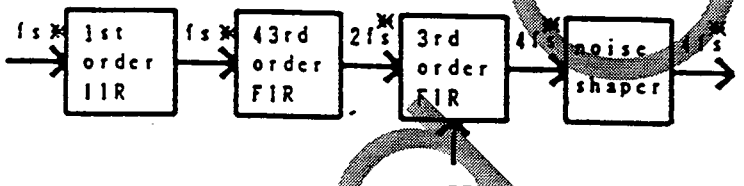
The normal speed mode does 2-times over sampling at each stage 43rd order FIR. 11th order FIR and 3rd order FIR. finally composes 8-times over sampling digital filter. 1st order IIR does de-emphasis.

The double speed mode is way to copy CD to cassette tape at double the speed. On this mode. BCLK. DATA and LRCK are input at double the speed, but XIN is input at the normal speed. This mode does 2-times over sampling at each stage 43rd order FIR and 3rd order FIR. finally composes 4-times over sampling digital filter.

·Normal speed




·Double spped




*offset : "02AAH"

fs* : double speed input

·16bit D/A Converter

DAC is same as Sanyo LC7881 basically and has dynamic level shift conversion method using CH1. CH2. independent D/A converters. D/A conversion by resistance string (R-string DAC). D/A conversion by pulse width modulation (PWMDAC) and D/A conversion by level shift (Level Shift DAC).

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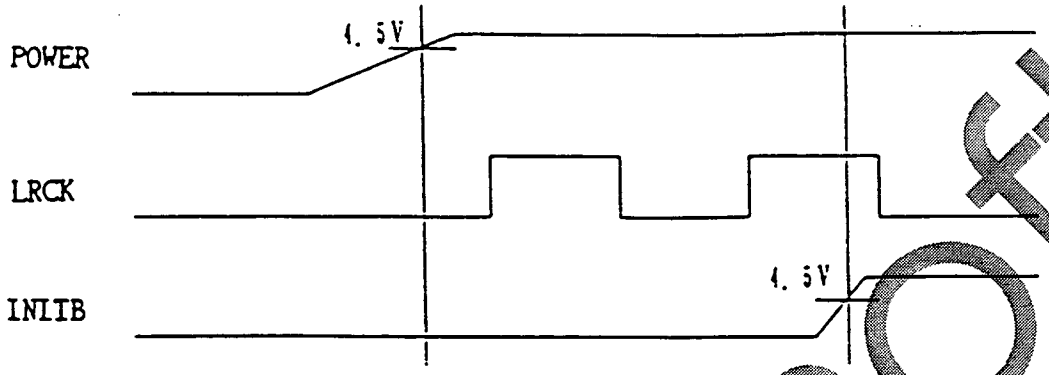
12. Initiation

The IC needs to be initialized when power supply is on and when input source is changed. "L" level is longer than on period of LRCK shown below should be input to INITB when XIN, BCKL and LRCK are supplied and when power supply is stable for the initialization.




13. Input Source Setting

SOC1 and SOC2 pins are set according to frequency of oscillator as shown below.

| frequency | SOC1 | SOC2 |
|---|---|---|
| 384Fs | L | L |
| 392Fs | L | H |
| 448Fs | H | L |
| 512Fs | H | H |

14. Mode Setting

When MODE pin is high level, de-emphasis ON/OFF and normal/double speed are set by EMPH1, EMPH2 and D/N pins.
When MODE pin is low level, the mode is serial data transfer mode using ATT, SHIFT and LATCH pins.

At MODE pin "H" (PINs setting mode)

| EMPH1 | EMPH2 | de-emphsis |
|---|---|---|
| L | L | O F F |
| L | H | Fs=32KHz |
| H | L | Fs=44.1KHz |
| H | H | Fs=48KHz |

D/N pin "H" double speed mode.
"L" normal speed mode.

ATT, SHIFT, LATCH pins should be fixed to "H" or "L".

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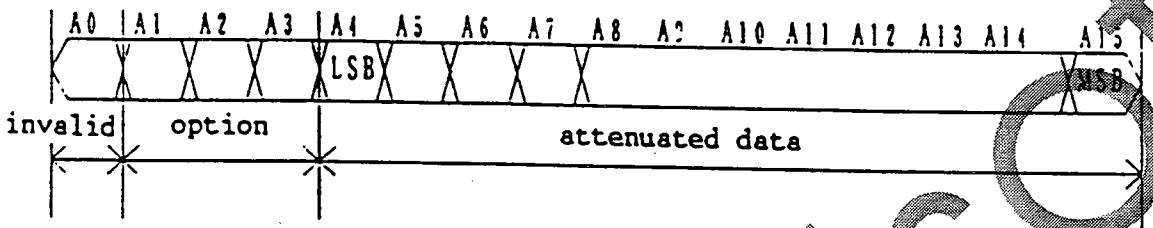
At MODE pin "L" (serial data transfer mode)

EMPH1. EMPH2 and D/N pins should be fixed to "H" or "L" for serial data transfer mode.

15. ATT Data Format In Use Of Serial Data Transter Mode

Normal & double speed. de-emphasis and attenuation can be manipulated by input of the following data by timing described in electric characteristics section.




A 1 : speed flag. "L" normal speed , "H" double speed

A 2. A 3 : de-emphasis flag

| A 2 | A 3 | de-emphasis |
|---|---|---|
| L | L | O F F |
| L | H | Fs=32KHz |
| H | L | Fs=44.1KHz |
| H | H | Fs=48KHz |

ATT data should be set 4000H ("1" only for A14) when initializing.

·ATTenuation

Since coefficient bit length of internal multiplier is 10 bit. normally upper 10 bit (A15 -A6) of attenuated data are valid.

And the attenuation : $-20\log\left\{\frac{\text{upper 10bit}}{256}\right\}$ dB

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When upper 10bit of attenuated data become all "0", lower 2bit (A5 & A4) become valid and there will be attenuation by barrel sifter.

| attenuation | | | | | | | | | | | | - attenuation level [dB] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | LSB A4 | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | −0.034 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | −0.034 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | −0.034 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | −0.034 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | −0.068 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | −0.068 |
| . | . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . | . |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | −48.16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | −50.66 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | −54.19 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | −60.21 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | −∞ |

Softmute after attenuation data change from 400H to 000H
Softmute time : 1/Fs × 1.024
Attenuation varying period is also on the linear of varying period of the softmute.

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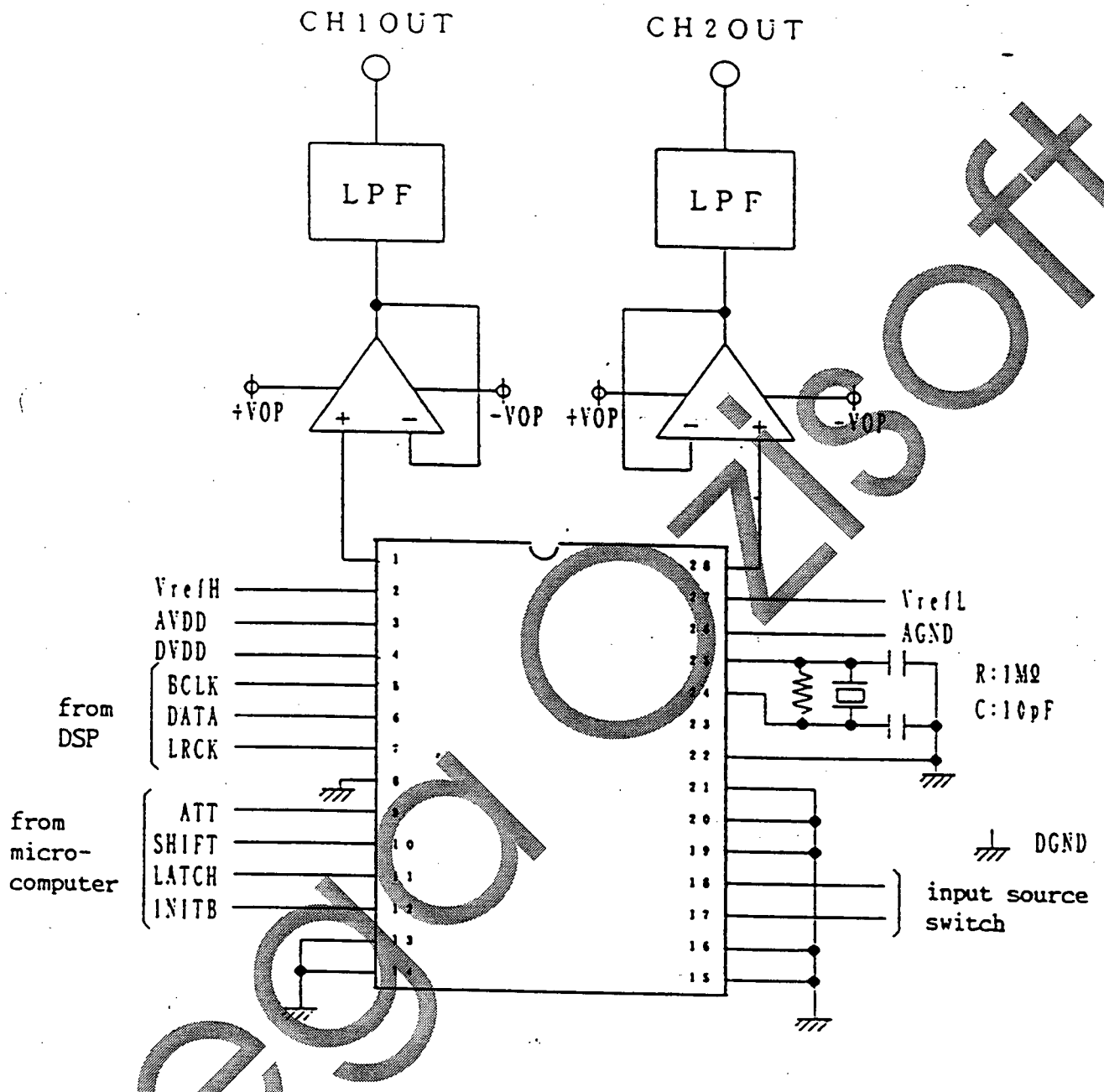
16. Application Circuit Examples




Since output impedance is high at pins. 1 and 28. voltage follower should be used for opeamp. for buffer.

AVDD and DVDD should be turned on simultaneously.

LPF:LOW PASS FILTER(Fc=20000Hz)
±VOP ≥ 6.0V
DVDD = 5.0V
AVDD = 5.0V
VrefH = 5.0V
AGND = 0.0V
VerfL = 0.0V

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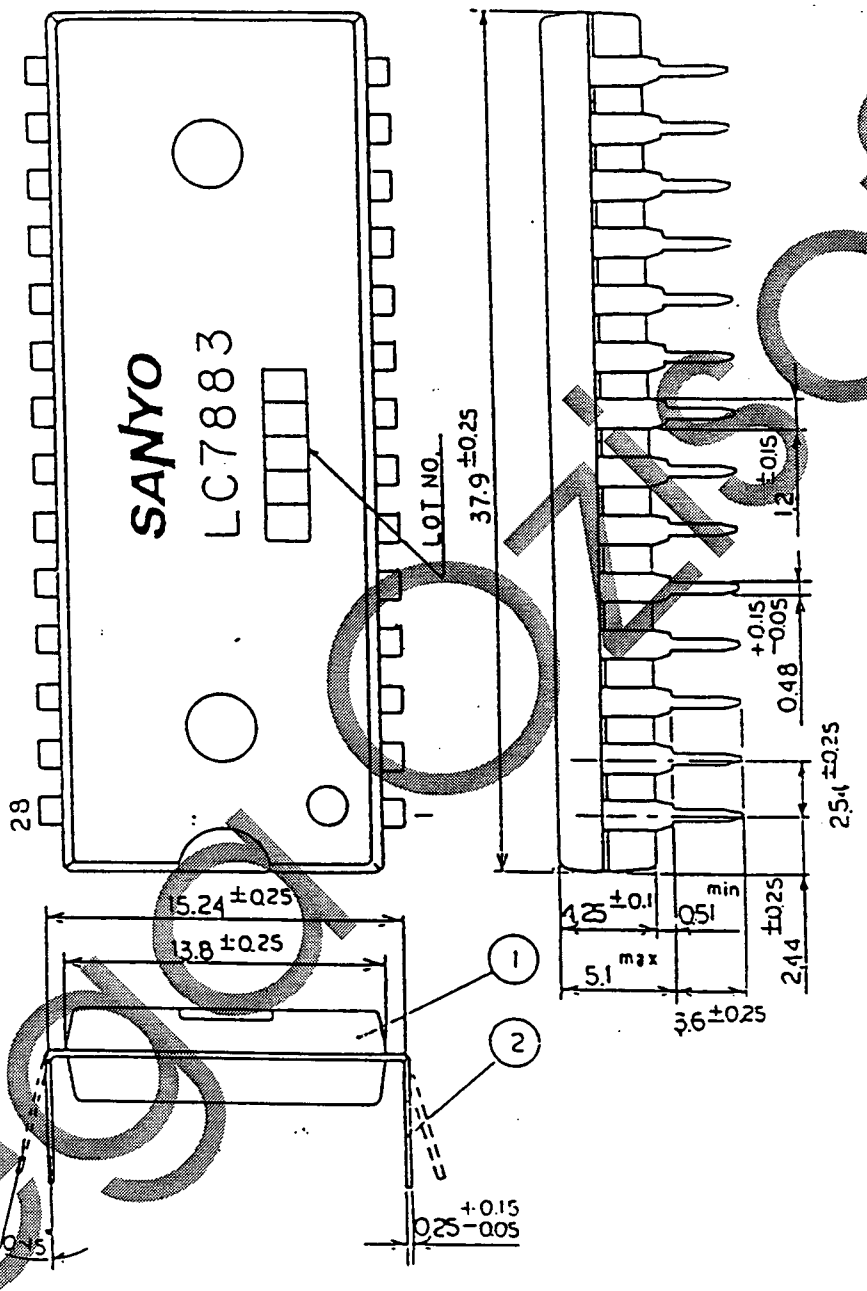
# PHYSICAL DIMENSIONS

| SCALE | 3/1 |
|---|---|
| DIMENSIONS | mm |

MODEL LC7883




| APPROVED BY |
|---|
| |
| CHECKED BY |
| '90. 11. 13. T. Akiyama |
| DRAWN BY |
| '90. 11. 9 |

| | MATERIAL | FINISH |
|---|---|---|
| ① | Epoxy Resins | ——— |
| ② | 42-ALLOY | Solder Plated |

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