Ordering number : EN*4450

CMOS LSI

LC78866V

16-Bit A/D Converter

Overview

The LC78866V is a 16-bit CMOS A/D converter with a built-in 4-channel input multiplexer. The LC78866V is optimal for use in low band digital sampling and uses a charge redistribution successive approximation method as its conversion technique.

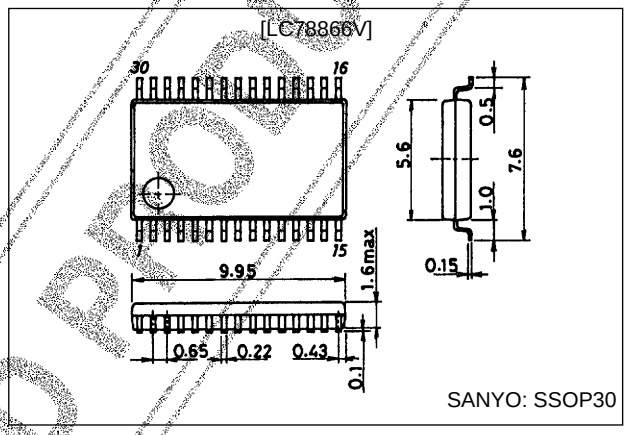
Features

- A/D converter for use with 16-bit interface microprocessors
- Charge redistribution successive approximation conversion
- Built-in 4-channel input multiplexer
- LSB first, offset binary code output
- Built-in sample and hold circuit
- +5 V single voltage power supply
- Low power mode
- Miniature package (SSOP30)

Package Dimensions

unit: mm

3191-SSOP30



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Maximum input voltage	V_{IN} max		–0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max		–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Reference voltage (high level)	V_H		3.3		V_{DD}	V
Reference voltage (low level)	V_L		0		1.2	V
Analog input voltage	V_{AIN}		V_L		V_H	V
Operating temperature	Topr		–20		+75	°C

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DC Electrical Characteristics at Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

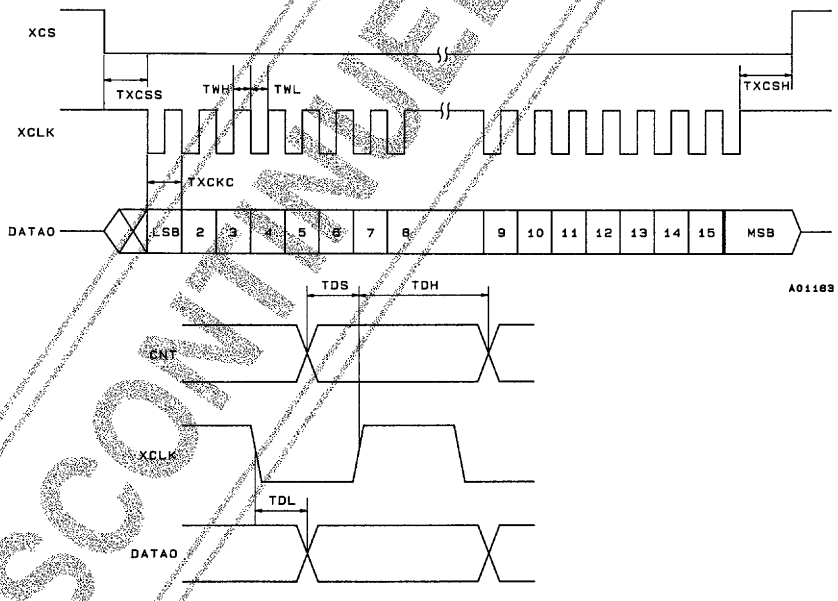
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage		(note)	2.2			V
Input low level voltage		(note)			0.8	V
Output high level voltage		I_{OH} = –1 µA	V_{DD} – 0.05			V
Output low level voltage		I_{OL} = 1 µA			V_{SS} + 0.05	V
Clock input amplitude		SCK pin	0.5			V_{P-P}

Note: Digital input pins other than SCK.

AC Electrical Characteristics at Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
XCS setup time	T_{XCSS}		1.5			µs
XCS hold time	T_{XCSH}		1.5			µs
XCLK cycle time	T_{XCKC}		1.0			µs
XCLK pulse width	T_{WH}		300			ns
XCLK pulse width	T_{WL}		300			ns
CNT setup time	T_{DS}		50			ns
CNT hold time	T_{DH}		50			ns
DATAO delay time	T_{DL}		0		150	ns
SCK clock frequency	F_{SCK}		5	14.32	16	MHz

Timing Diagram



Analog Characteristics at Ta = 25°C, AV_{DD} = DV_{DD} = 5.0 V, V_L = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
A/D conversion frequency	fs	(note)	17.4	49.7	55.6	kHz
Linearity error	LE	(note)			0.025	%
Power dissipation	Pd	Normal mode		50	80	mW
		Standby mode		15	30	mW

Note: The A/D converter performs one conversion every F_{SCK}/288 period and loads the converted data into the output register in a single operation. Therefore, when XCS is high, the output register is continually updated every 288 SCK clock cycles, and at the point XCS goes low, data update is stopped and data output preparation is performed.

Input Impedance at AV_{DD} = DV_{DD} = 5.0 V, V_H = 5.0 V, V_L = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input impedance	A_{DIN}	DC input*	5 M			Ω
		AC 1 kHz input*	250 k			Ω

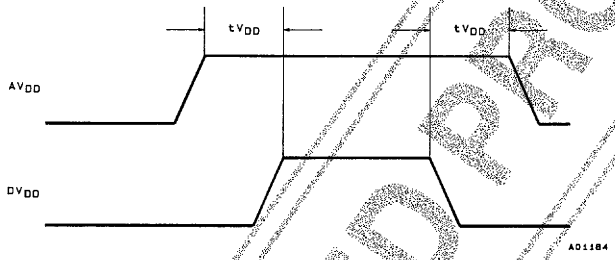
Note: * Sampling frequency: 49.7 kHz

Power On Timing

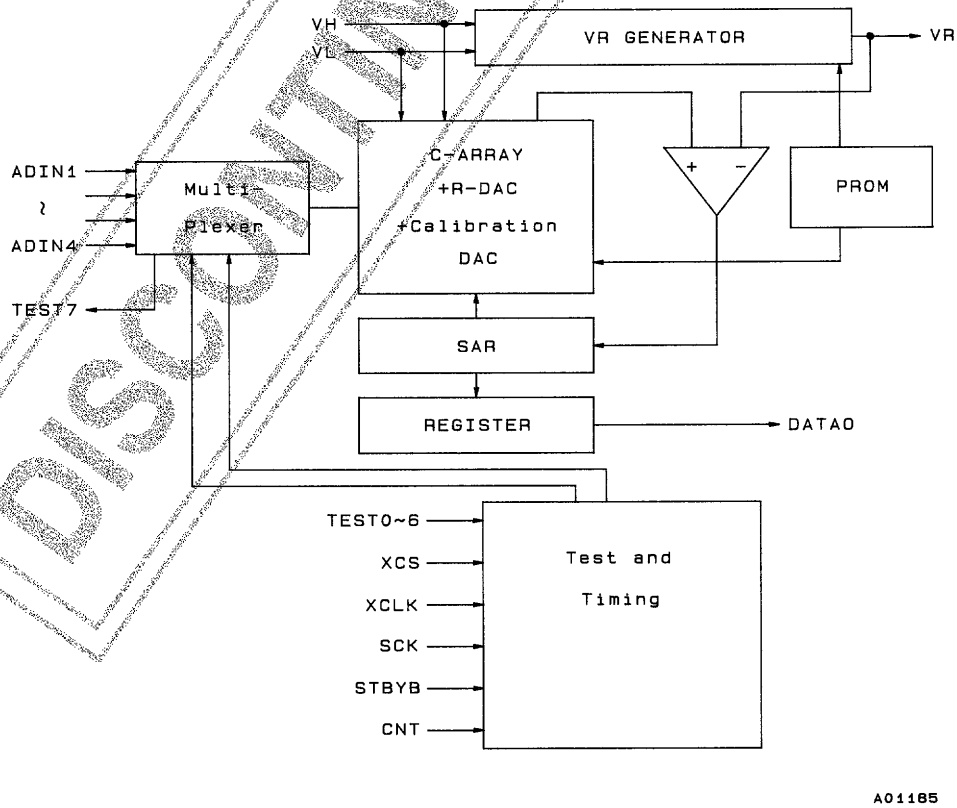
AV_{DD} and DV_{DD} are completely independent.

AGND and DGND are connected through the IC substrate.

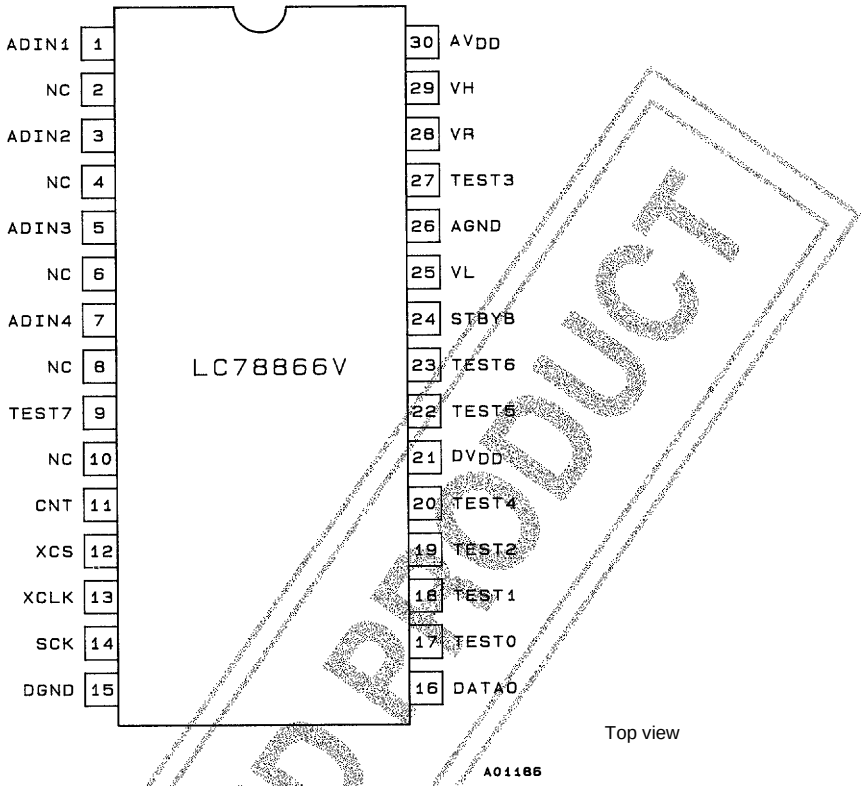
The optimal power on/off timing is to bring up (or down) the analog power supply (AV_{DD}) and the digital power supply (DV_{DD}) voltages at the same time. If a time difference must be used, apply power first to the analog system and then to the digital system, with a time difference (tV_{DD}) of 2 to 3 ms or less. Power down the chip in the opposite order.



Block Diagram



Pin Assignment

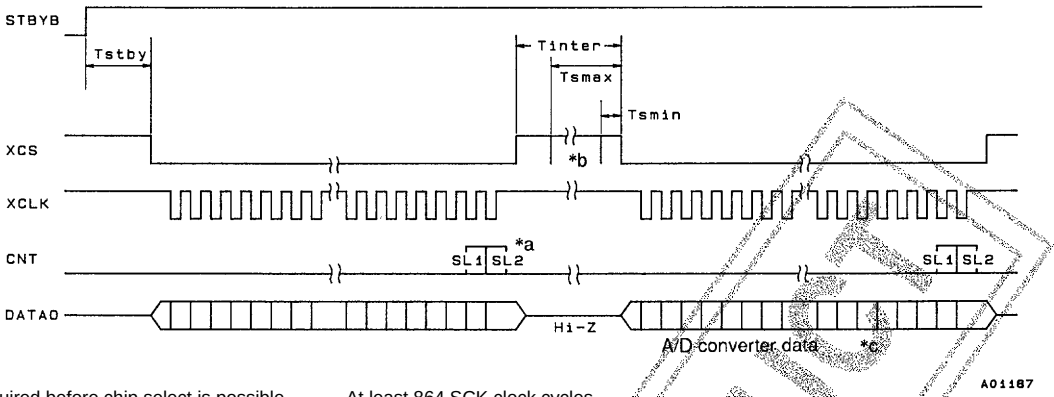


Top view

Pin Functions

Pin No.	Pin	Function and operating description
1	ADIN1	Analog input 1
2	NC	No connection
3	ADIN2	Analog input 2
4	NC	No connection
5	ADIN3	Analog input 3
6	NC	No connection
7	ADIN4	Analog input 4
8	NC	No connection
9	TEST7	Test output. Normally left open.
10	NC	No connection
11	CNT	Input multiplexer control serial input
12	XCS	Microprocessor control input Data is transferred to the microprocessor when XCS is low.
13	XCLK	Data transfer clock input
14	SCK	System clock input
15	DGND	Digital system ground
16	DATAO	Digital data output LSB first, offset binary code output. When XCS is high, output goes to high impedance.
17	TEST0	Test input. Connect to digital ground during normal operation.
18	TEST1	Test input. Connect to digital ground during normal operation.
19	TEST2	Test input. Connect to digital ground during normal operation.
20	TEST4	Test input. Connect to digital ground during normal operation.
21	DV_{DD}	Digital system power supply
22	TEST5	Test input. Since this pin is pulled up to V_{DD} internally, it should be left open during normal operation.
23	TEST6	Test input. Connect to digital ground during normal operation.
24	STBYB	Standby mode control input STBYB = high: Normal A/D converter operation STBYB = low: Low power mode Note that the A/D converter does not operate when the LC78866V is in low power mode.
25	VL	Low level reference voltage input
26	AGND	Analog system ground
27	TEST3	Test output. Leave this pin open during normal operation.
28	VR	Reference voltage output (VH + VL)/2: Normally left open.
29	VH	High level reference voltage input
30	AV_{DD}	Analog system power supply

Interface



Tstby:	The time required before chip select is possible following the clearing of standby mode:	At least 864 SCK clock cycles
Tinter:	The chip select interval time:	At least 576 SCK clock cycles
Tsmax:	Analog sampling timing:	480 SCK clock cycles (max)
Tsmin:	Analog sampling timing:	204 SCK clock cycles (min)

Note that the analog sampling time is the interval that precedes chip select bordered by Tsmax (maximum) and Tsmin (minimum).

Multiplexer Control Timing

The analog input pin signal specified at the point marked "*a" is sampled at the point marked "*b" and output as digital data at the point marked "*c" in the figure above.

Four Input Multiplexer Control Conditions

Valid input pin	SL1	SL2
ADIN1	L	L
ADIN2	H	L
ADIN3	L	H
ADIN4	H	H

Operating Principles

The LC78866V uses a charge redistribution successive approximation method for A/D conversion. The major components of this circuit are a binary weighted capacitor array used for the upper 12 bits, a resistor string used for the lower 4 bits, and a resistor string D/A converter used for compensation. This method charges the capacitor array with charges based on the analog weights, and determines the code by successive comparisons between the capacitor array potential and the reference voltage. The capacitor array also implements the sample and hold function. Also, to allow the circuit to function with only a single power supply voltage, an internal reference potential Vr (with the value (VH + VL)/2) is generated internally from the external reference potentials VH and VL. Internal operation is a sign/magnitude type operation centered on Vr. (See figure 1.)

The precision of this circuit depends on the precision of the internal reference voltage Vr and the capacitor array. The manufacturing variations in these parameters are tested at shipment, and their deviations are written to an internal PROM. Then, this PROM data is used for compensation during actual A/D conversion.

Sample Application Circuit

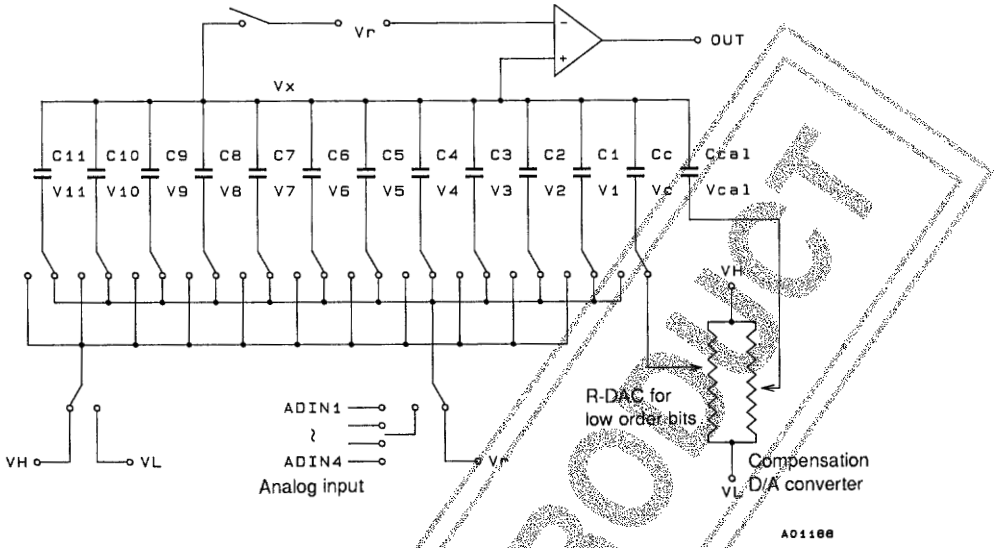
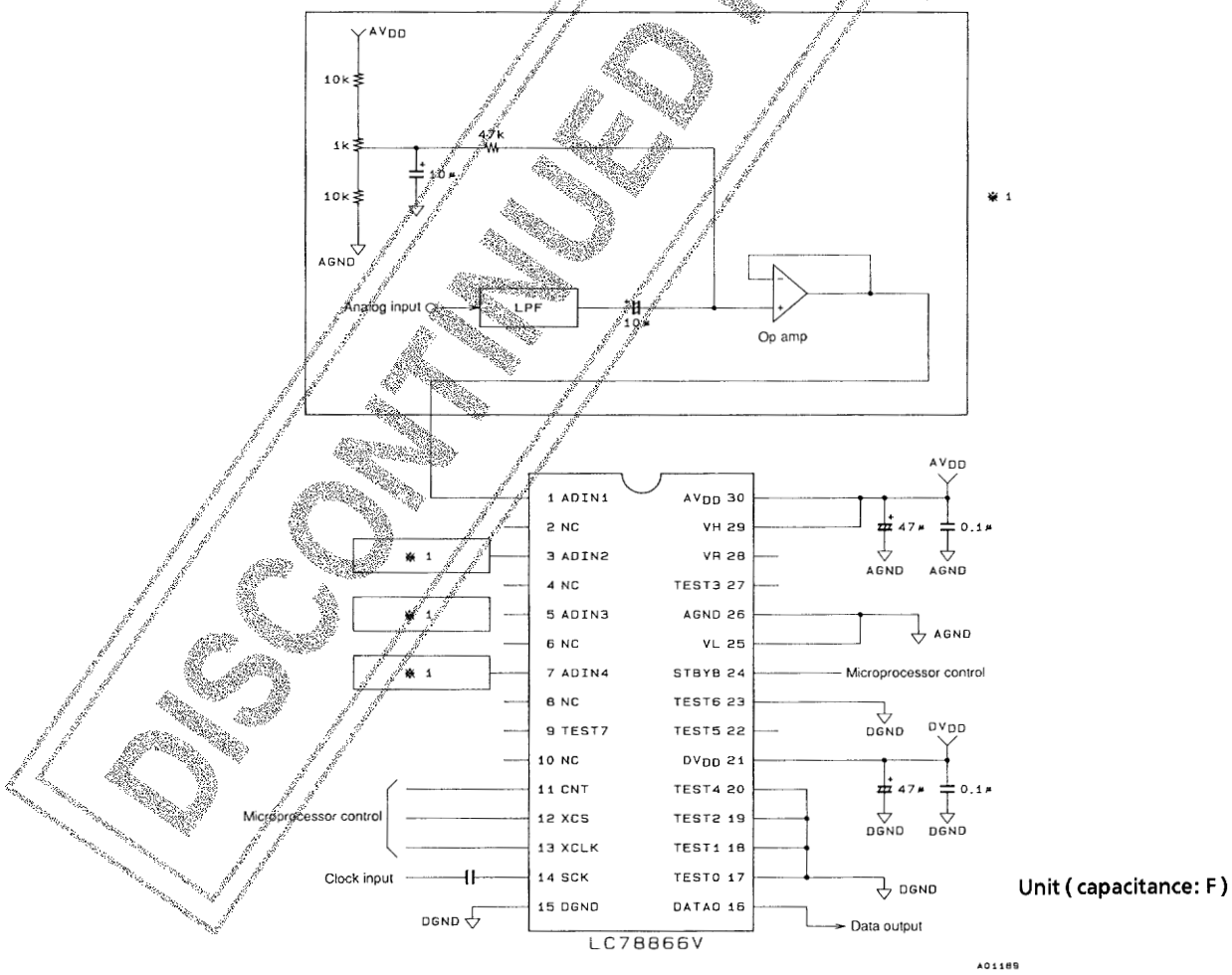


Figure 1 Charge Redistribution Conversion Method



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