Ordering number : EN5946

CMOS IC

LC7982A

LCD Dot Matrix Graphics Display Controller

Overview

The LC7982A is an LCD dot matrix graphics display controller IC. It stores display data sent from an 8-bit microcontroller in external display RAM and generates dot matrix LCD drive signals. Applications can select either of two modes: graphics mode, in which each bit in external RAM controls the on/off state of an individual pixel (dot) on the LCD, and character mode, in which character codes are stored in external RAM and the dot pattern is generated using the built-in character generator ROM. Thus the LC7982A can support a wide range of applications. The LC7982A is fabricated in a CMOS process, and in conjunction with a CMOS microcontroller, can implement low-power LCD display systems. This device differs from the LC7981 only in the data stored in the built-in character generator ROM.

Features

- LCD dot matrix and graphics display controller
- Display control capacity

Graphics mode	512 K dots (2^{16} bytes)
Character mode	4096 characters (2^{12} bytes)

- Character generator ROM 7360 bits
  - · European character support

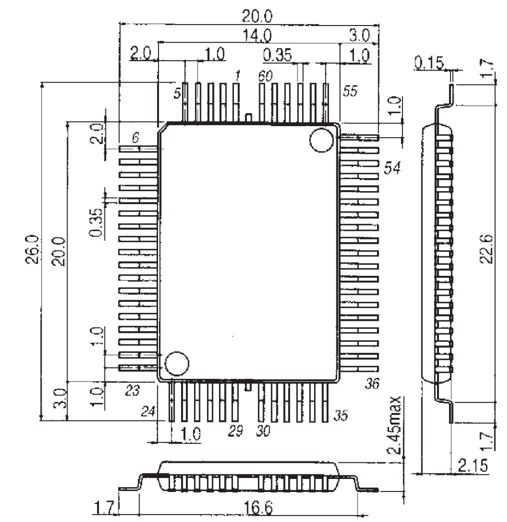
Character font: 5 × 7 dots	160 characters	192 characters total
Character font: 5 × 11 dots	32 characters	

  (Can be expanded by up to 4 KB using external ROM.)
- Supports interfacing with 8-bit microcontrollers.
- Display duty (program selectable)
  — From static to 1/256 duty
- Extensive set of command functions
  — Scroll, cursor on/off/blink, character blinking, bit manipulation
- Display methods : Method A and method B (program selectable)
- Built-in oscillator circuit (Using an external resistor and capacitor)
- Low power
- +5V single-voltage power supply

Package Dimensions

unit: mm

3055A-QFP60C



SANYO: QFP60C (QIP60C)

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Specifications

Absolute Maximum Ratings at Ta = 25°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input voltage	V_I		–0.3 to V_{DD} +0.3	V
Output voltage	V_O		–0.3 to V_{DD} +0.3	V
Allowable power dissipation	Pd max	Ta = 75°C	200	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

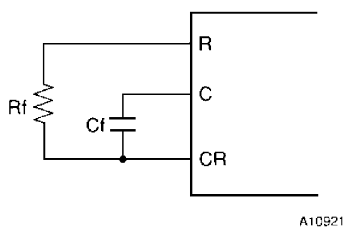
Allowable Operating Ranges at Ta = –20 to +75°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.75		5.25	V
High-level input voltage	$V_{IH}1$	Input and I/O pins other than $\overline{SYNC}$ and CR.	2.2		V_{DD}	V
Low-level input voltage	$V_{IL}1$	Input and I/O pins other than $\overline{SYNC}$ and CR.	0		0.8	V
High-level input voltage	$V_{IH}2$	$\overline{SYNC}$, CR	0.7 V_{DD}		V_{DD}	V
Low-level input voltage	$V_{IL}2$	$\overline{SYNC}$, CR	0		0.3 V_{DD}	V
High-level output voltage	$V_{OH}1$	I_{OH} = –0.6 mA, DB0 to DB7, $\overline{WE}$, MA0 to MA15, MD0 to MD7	2.4		V_{DD}	V
Low-level output voltage	$V_{OL}1$	I_{OL} = 1.6 mA, DB0 to DB7, $\overline{WE}$, MA0 to MA15, MD0 to MD7	0		0.4	V
High-level output voltage	$V_{OH}2$	I_{OH} = –0.6 mA, $\overline{SYNC}$, CPO, FLM, CL1, CL2, D1, D2, MA, MB	V_{DD} – 0.4		V_{DD}	V
Low-level output voltage	$V_{OL}2$	I_{OL} = 0.6 mA, $\overline{SYNC}$, CPO, FLM, CL1, CL2, D1, D2, MA, MB	0		0.4	V
[Internal Clock Operation]						
Clock oscillator frequency	f_{OSC}	Cf = 15 pF ±5%, Rf = 39 kΩ ±2%*1	500	600	700	kHz
[External Clock Operation]						
Clock operating frequency	f_{CP}	*2			2.5	MHz
Clock duty	Duty	*3	47.5	50	52.5	%
Clock rise time	trcp	*3			50	ns
Clock fall time	tfcp	*3			50	ns

Electrical Characteristics at Ta = –20 to +75°C, GND = 0 V, V_{DD} = 5 V ±5%

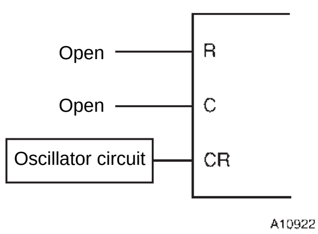
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input leakage current	I_{IN}	V_{IN} = 0 to V_{DD}, $\overline{CS}$, E, RS, R/W, $\overline{RES}$	–5		5	µA
Current drain	$I_{CC}1$	RC oscillator, f_{OSC} = 600 kHz		2	4	mA
	$I_{CC}2$	External clock, f_{CP} = 2.5 MHz		3	5	mA
Pull-up current	I_{PL}	V_{IN} = GND, DB0 to DB7, RD0 to RD7, MD0 to MD7		10	20	µA

(Note 1)

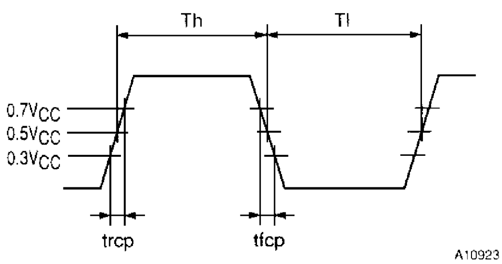


Cf = 15 pF ±5%
Rf = 39 kΩ ±2%
(When f_{OSC} = 600 kHz (typical))

(Note 2)



(Note 3)

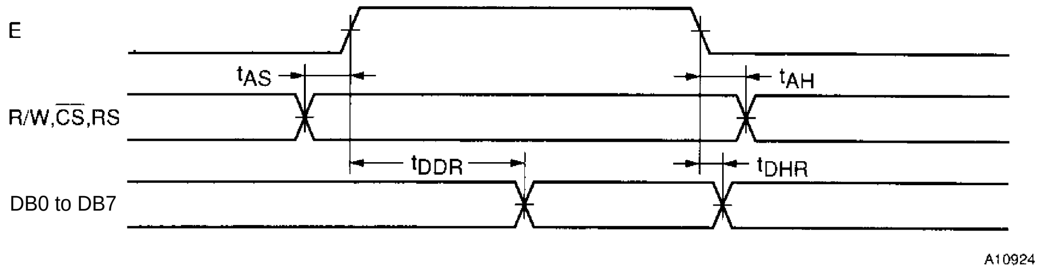


$$\text{Duty} = \frac{\text{Th}}{\text{Th} + \text{T1}} \times 100\%$$

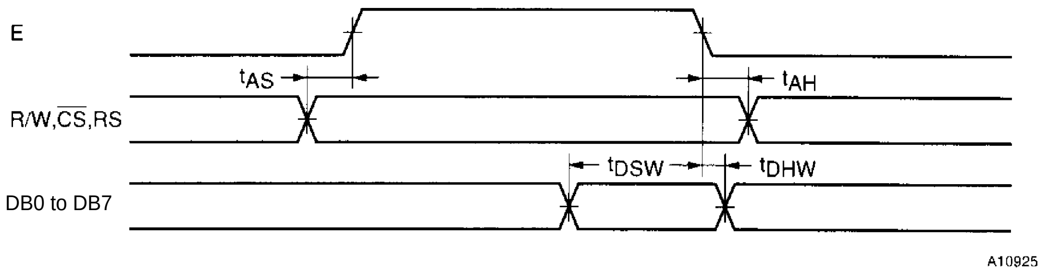
Timing Characteristics

- Bus read/write operation 1

  Read cycle



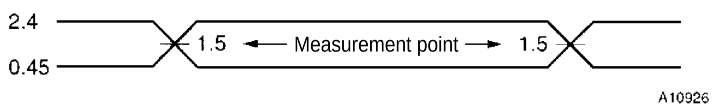
Write cycle



Ta = –20 to +75°C, V_{DD} = 5V ±5%, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Address setup time	t_{AS}		90			ns
Address hold time	t_{AH}		10			ns
Data delay time (read)	t_{DDR}	C_L = 50 pF			140	ns
Data hold time (read)	t_{DHR}		10			ns
Data setup time (write)	t_{DSW}		220			ns
Data hold time (write)	t_{DHW}		20			ns

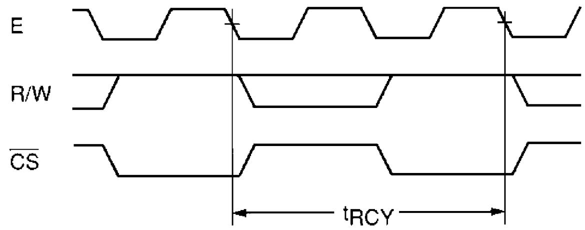
Note: Test waveform definition



Input pins are driven to 2.4 V and 0.45 V, and the timing is measured at 1.5 V

- Bus read/write operation 2

  Data read cycle



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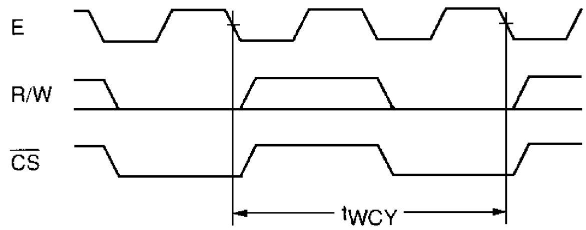
Data write cycle



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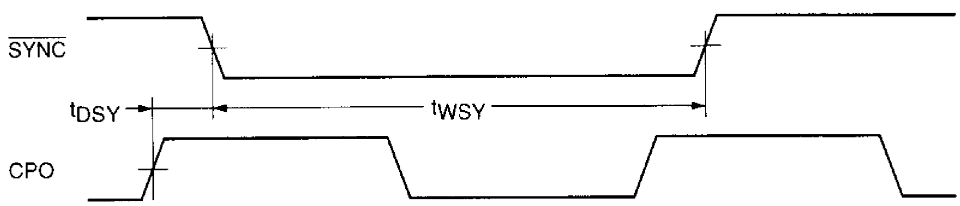
Ta = –20 to +75°C, V_{DD} = 5V ±5%, GND = 0 V

Parameter	Symbol	Instruction register value	Ratings			Unit
			min	typ	max	
Read cycle time	t_{RCY}	0DH			$\frac{(HP+2) \times 10^3}{f_{OSC}} +200$	ns
Write cycle time	$t_{WCY}1$	0EH, 0FH			$\frac{(2HP+2) \times 10^3}{f_{OSC}} +200$	ns
Write cycle time	$t_{WCY}2$	0CH			$\frac{(HP+2) \times 10^3}{f_{OSC}} +200$	ns
Write cycle time	$t_{WCY}3$	00H, 01H, 02H, 03H, 04H, 08H, 09H, 0AH, 0BH			$\frac{2000}{f_{OSC}} +200$	ns

Notes: • For character display, HP is the number of dots in the horizontal direction per character, and for graphics mode, HP is the number of bits shown on the display from each byte of display data.
• f_{OSC} is the oscillator frequency, in units of MHz.
• All measurements are made at 1.5 V.

- Parallel operation (master mode)



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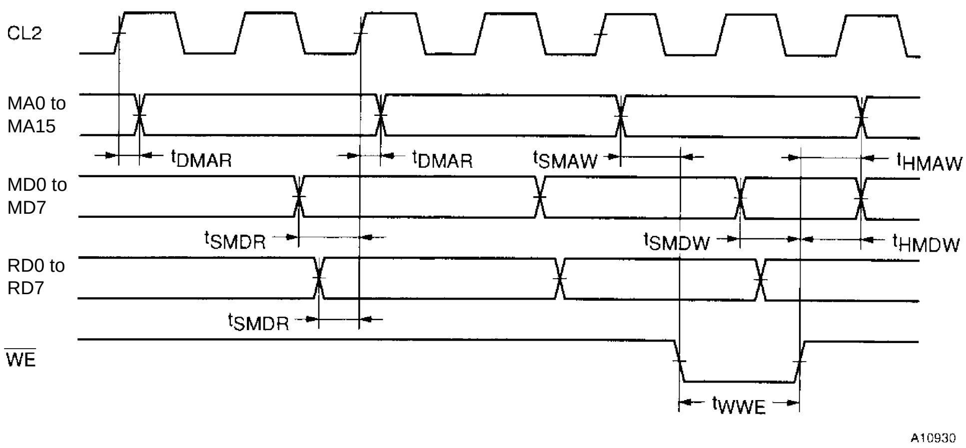
Ta = –20 to +75°C, V_{DD} = 5V ±5%, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
$\overline{\text{SYNC}}$ delay time	t_{DSY}				100	ns
$\overline{\text{SYNC}}$ pulse width	t_{WSY}		350			ns

Notes: • With no loads on any of the output pins.
• Measurements are made at 0.5 V_{DD}.

• External RAM and ROM interface



Read Cycle at Ta = –20 to +75°C, V_{DD} = 5 V ±5%, GND = 0 V

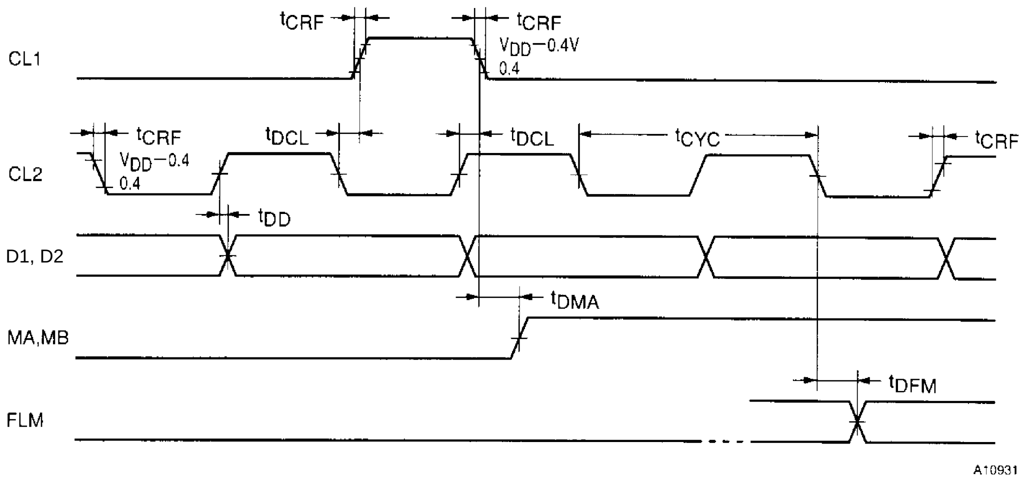
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
MA0 to MA15 read address delay time	t_{DMAR}				95	ns
MD0 to MD7, RD0 to RD7 setup time	t_{SMDR}		105			ns

Write Cycle at Ta = –20 to +75°C, V_{DD} = 5 V ±5%, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Memory address setup time	t_{SMAW}		50			ns
WE pulse width	t_{WWE}		350			ns
Memory data setup time	t_{SMDW}		250			ns
Memory address hold time	t_{HMAW}		50			ns
Memory data hold time	t_{HMDW}		50			ns

Notes: • With no loads on any of the output pins.
• All measurements are made at 1.5 V.

• Driver IC interface

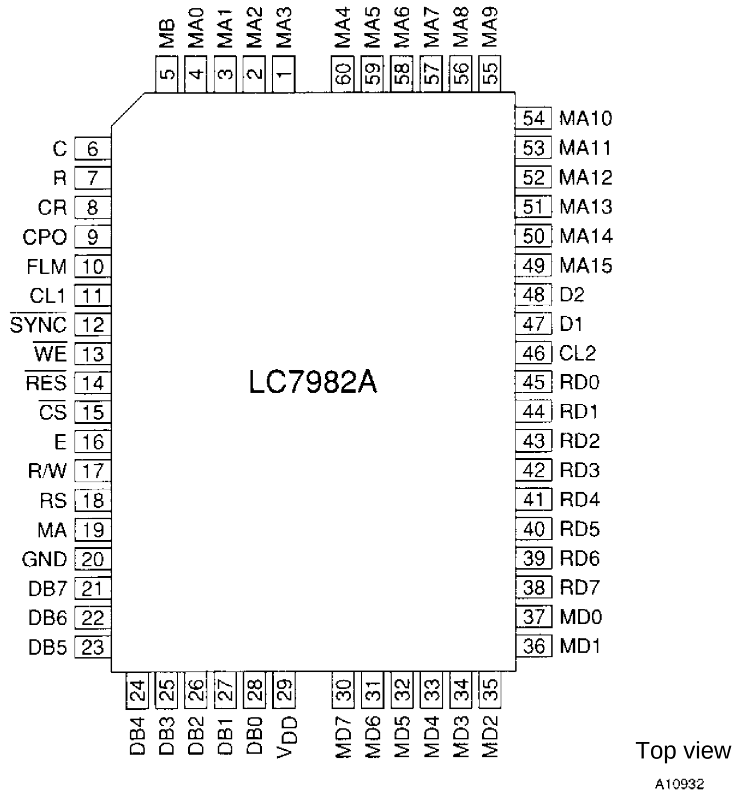


Ta = –20 to +75°C, V_{DD} = 5 V ±5%, GND = 0 V

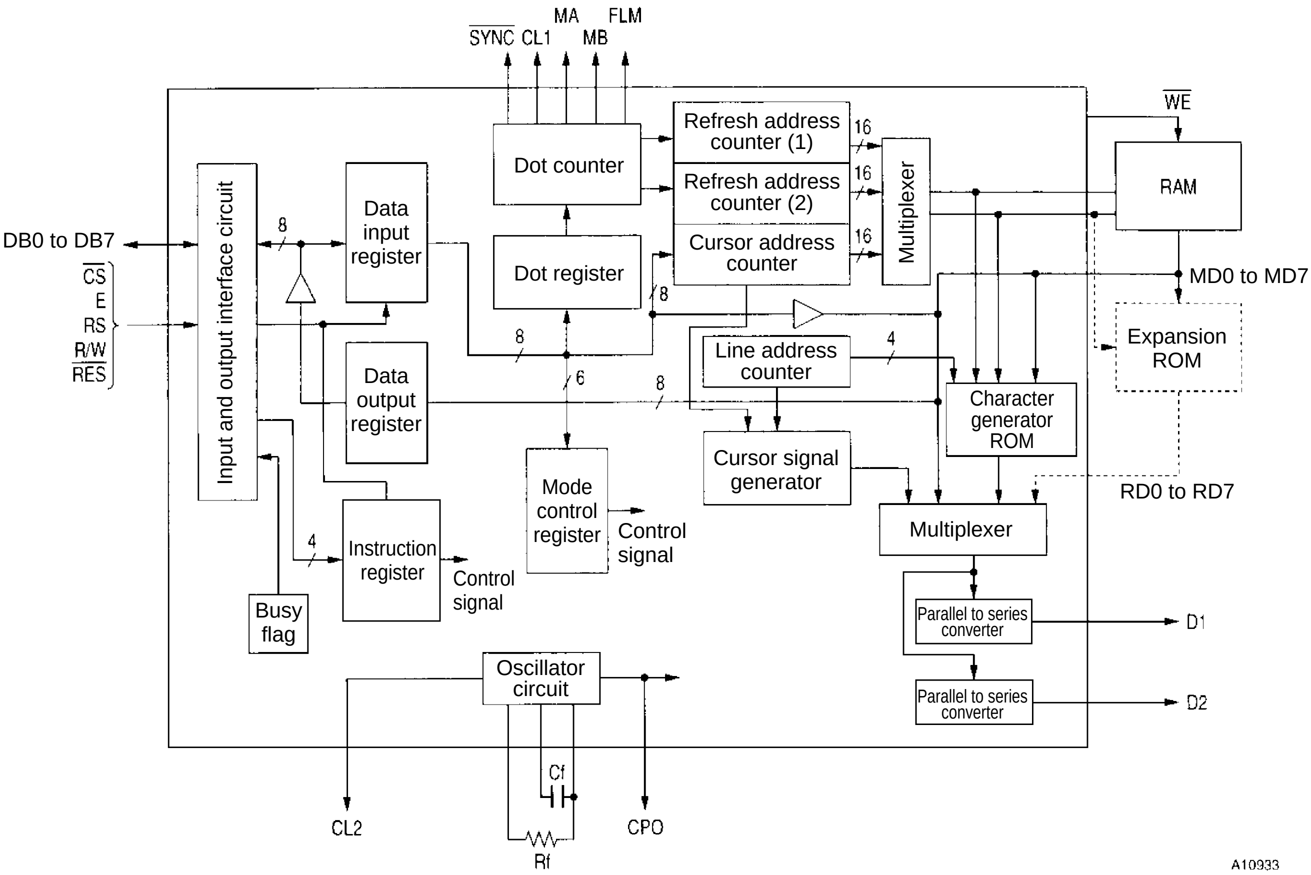
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock cycle time	t_{CYC}		400			ns
Clock phase difference	t_{DCL}				100	ns
Clock rise and fall times	t_{CRF}				30	ns
D1 and D2 phase difference	t_{DD}				100	ns
MA and MB phase difference	t_{DMA}				200	ns
FLM phase difference	t_{DFM}				200	ns

Notes: • With no loads on any of the output pins.
• Measurements other than those with a specified measurement point are made at 0.5 V_{DD}.

Pin Assignment



Block Diagram



• When expansion ROM is used, MA0 to MA11 are used as the RAM address and MA12 to MA15 are used as the expansion ROM address.

Block Functions

Registers

The LC7982A has five internal registers: the instruction register, the data input register, the data output register, the dot register, and the mode control register.

- The instruction register holds the instruction code, which includes the start address and the cursor address. This register is a 4-bit register, and the lower 4 bits (DB0 to DB3) of the data bus are written to this register.
- The data input register is used to temporarily hold data for external RAM, the dot register, the mode control register, and other registers. It is an 8-bit register.
- The data output register is used to temporarily hold data read output from external RAM, and is an 8-bit register. The cursor address passes through the data input register and is written to the cursor address counter, and when a memory readout instruction is loaded into the instruction register, IC internal operations read from external RAM and load it into the data output register. Data transfer to the microcontroller completes when the microcontroller reads the data output register at the next instruction.
- The dot register holds the character pitch, the number of dots in the vertical direction, and other display data. Data from the microcontroller passes through the data input register and is written to this register.
- The mode control register holds display state information for the LCD, such as display on/off state and the cursor on/off/blinking state. It is a 6-bit register. Data from the microcontroller passes through the data input register and is written to this register.

Busy Flag

This flag is set to 1 when the LC7982A is performing internal operations. In this state, the next instruction cannot be accepted. The state of the busy flag is output from DB7 when RS is 1 and R/W is 1. The microcontroller application software must first verify that the busy flag is 0 before writing the next instruction. However, after a data read instruction or a data write instruction, the microcontroller may execute the next instruction without checking the busy flag after the maximum value of the read cycle or write cycle elapses, respectively.

Dot Counter

The dot counter generates LCD display timing according to the contents of the dot register.

Refresh Address Counter

The refresh address counters control the addresses of the external RAM, the character generator ROM, and expansion ROM. There are two refresh address counters, refresh address counter (1) and refresh address counter (2). Refresh address counter (1) is used for the upper screen, and refresh address counters (2) is used for the lower screen. In graphics mode, these registers output 16-bit data that is used as the external RAM address signals. In character mode, the upper 4 bits are ignored and the 4 bits of the line address counter are output in place of those four bits. These 4 bits are used as the expansion ROM address.

Character Generator ROM

The character generator ROM holds the data for 192 characters, a total of 7360 bits. It takes a character code from external RAM and a line code from the line address counter as its address signals, and outputs 5 bits of dot data. Although this ROM holds a font with 192 characters, of which 160 are 5×7 dot characters and 32 are 5×11 dot characters, up to 256 8×16 dot characters can be supported by using expansion ROM.

Cursor Address Counter

Instructions can be used to set up this 16-bit counter in advance. This counter holds the address when reading or writing external RAM (either display dot data or character codes). The cursor address counter is automatically incremented after reading or writing display data or after executing a bit set or bit clear instruction.

Cursor Signal Generator

A cursor can be displayed in character mode under instruction control. A cursor is automatically generated when the cursor address counter and the line address counter reach the stipulated values.

Parallel to Serial Converter

Parallel data from external RAM, the character generator, or expansion RAM is converted to series data by the two parallel to series converter circuits and output at the same time to the LCD drive circuits for the upper and lower screens as series data.

Pin Functions

Pin No.	Pin	Function
21 to 28	DB0 to DB7	Data bus. These are 3-state shared I/O pins and are used for data transfers to and from the microcontroller.
15	$\overline{\text{CS}}$	Chip select: The IC is set to the selected state when $\overline{\text{CS}}$ = 0.
17	R/W	Read/write: R/W = 1 ·········· Microcontroller ← LC7982A R/W = 0 ·········· Microcontroller → LC7982A
18	RS	Register select: RS = 1 ···· Instruction register RS = 0 ···· Data register
16	E	Enable: Data writes are performed when E falls from high to low. Data can be read when E = 1.
6, 7, 8	CR, R, C	RC oscillator connections
14	$\overline{\text{RES}}$	Reset: When this pin is set 0, the display is turned off and slave mode and HP = 6 are selected.
1 to 4 49 to 60	MA0 to MA15	Display RAM address outputs In character display mode, MA12 to MA15 are output as the external CG raster address.
30 to 37	MD0 to MD7	Display data bus: Three-state shared input and output signals
38 to 45	RD0 to RD7	ROM data inputs: Dot data from an external character generator is input using these pins.
13	$\overline{\text{WE}}$	Write enable: The RAM write signal
46	CL2	Display data shift clock
11	CL1	Display data latch signal
10	FLM	Frame signal
19	MA	LCD drive signal: Alternation signal ····· Method A
5	MB	LCD drive signal: Alternation signal ····· Method B
47, 48	D1, D2	Display data serial output: D1 ·············· Upper screen D2 ·············· Lower screen
9	CPO	Slave mode clock
12	$\overline{\text{SYNC}}$	Parallel operation synchronizing signal: Three-state shared input and output signal. Master mode: Outputs a synchronizing signal. Slave mode: Inputs a synchronizing signal.

Display Control Instructions

The display is controlled by writing data to the instruction register and the 13 data registers. The instruction register and the data registers are differentiated using the RS signal. First, with RS set to 1 the application writes 8-bit data to the instruction register and specifies the code for the data register. Then, with RS set to 0, the application writes 8-bit data to the data register, and the specified instruction is executed. Note that another instruction cannot be written while the previous instruction is executing. Since the busy flag is set during this period, applications must verify that the busy flag is 0 before writing an instruction. However, after a data read instruction or a data write instruction, the microcontroller may execute the next instruction without checking the busy flag after the maximum value of the read cycle or write cycle elapses, respectively

- Mode control

  Applications specify the mode control register by writing 00H to the instruction register.
  (The form "00H" is used to express values in hexadecimal.)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	0	0	0	0
Mode control register	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blinking	CG	Graphics/character display
1/0	1/0	0	0	0	0	Cursor off	Internal CG	Character display mode
		0	1			Cursor on		
		1	0			Cursor off/character blinking		
		1	1			Cursor blinking		
		0	0		1	Cursor off	External CG	
		0	1			Cursor on		
		1	0			Cursor off/character blinking		
		1	1			Cursor blinking		
		0	0	1	0			Graphics mode
Display on/of	Master/ slave	Blinking	Cursor	Mode	Internal/ external CG			

DB4 (Master/slave):
1: Master mode
0: Slave mode

DB5 (Display on/of):
1: Display on
0: Display off

- Character pitch setting

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	0	0	0	1
Character pitch register	0	0	(VP - 1) binary				0	(HP - 1) binary		

VP indicates the number of dots in the vertical direction per character. Applications should determine this value based on the desired vertical separation between characters. This setting is only meaningful in character display mode, and is ignored in graphics mode.

In character display mode, HP indicates the number of dots in the horizontal direction per character, and also includes the gap between the current character and the character displayed to the right. In graphics mode, HP indicates the number of bits displayed from each byte of display data from RAM.

HP can be set to one of three values.

Hp	DB2	DB1	DB0	Setting
6	1	0	1	Horizontal character pitch of 6 dots
7	1	1	0	Horizontal character pitch of 7 dots
8	1	1	1	Horizontal character pitch of 8 dots

• Character count setting

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	0	0	1	0
Character count register	0	0	(H_N – 1) binary							

In character display mode, H_N specifies the number of characters displayed in the horizontal direction. In graphics mode, H_N specifies the number of bytes displayed in the horizontal direction. The total number of dots displayed on the screen in the horizontal direction is given by the following formula.

$n = HP \times H_N$

H_N can be set to an even number in the range 2 to 256 (decimal).

• Time division setting (display duty)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	0	0	1	1
Duty register	0	0	(N_X – 1) binary							

N_X specifies the time division setting. That is, the display duty is set to $1/N_X$.

N_X can be set to a value in the range 1 to 256 (decimal).

• Cursor position setting

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	0	1	0	0
Cursor position register	0	0	0	0	0	0	(CP – 1) binary			

In character display mode, CP specifies the line where the cursor is displayed. For example, if CP is set to 8 (decimal), the cursor will be displayed under the character for a 5 × 7 font. The length of the cursor in the horizontal direction will be equal to horizontal direction character pitch HP. While CP can be set to any value in the range 1 to 16 (decimal), if it is set to a value less than or equal to the vertical direction character pitch VP (CP ≤ VP), the cursor display will take priority when cursor display is enabled. Note that if CP > VP, the cursor will not be displayed. The length of the cursor in the horizontal direction will be equal to HP.

• Display start position low-order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	1	0	0	0
Display start address register (Low-order byte)	0	0	(Start address low-order byte) binary							

• Display start position high-order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	1	0	0	1
Display start address register (High-order byte)	0	0	(Start address high-order byte) binary							

These instructions together write the display start address value into the display start address register. The display start address specifies the RAM address where the data to be displayed at the upper left of the screen is stored.

The start address is a 16-bit value formed from high-order and low-order bytes.

• Cursor address (low order) setting (RAM read/write low-order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	1	0	1	0
Cursor address counter (Low-order byte)	0	0	(Cursor address low-order byte) binary							

• Cursor address (high order) setting (RAM read/write high-order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	1	0	1	1
Cursor address counter (High-order byte)	0	0	(Cursor address high-order byte) binary							

These instructions together write the cursor address value into the cursor address register. The cursor address indicates the address used for refering to RAM for the display data or character code. That is, the data at the address specified by the cursor address will be read or written. In character display mode, the cursor is displayed at the position specified by the cursor address.

While the cursor address is a 16-bit value formed from high-order and low-order bytes, applications must only use cursor addresses that obey the following restrictions.

1	When the application rewrites (sets) both the low-order and high-order bytes.	The application must first set the low-order byte and then set the high-order byte.
2	When the application only needs to rewrite the low-order byte	After writing the low-order byte, the application must also write the high-order byte.
3	When the application only needs to rewrite the high-order byte	The application should simply write the high-order byte. There is no need for it to write the low-order byte.

The cursor address counter is a 16-bit increment-only counter with set and reset functions. When the nth bit changes from 1 to 0, bit n+1 is incremented. When the low-order byte is set, if the set caused the MSB in the low-order byte to change from 1 to 0, the LSB in the high-order byte will be incremented. Therefore, applications must set both the low-order and the high-order bytes in that order when setting the cursor address.

• Display data write

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (Pattern data or character code) LSB							

When 8 bits of data are written by writing the instruction code 0CH to the instruction register when RS is 0, that data will be written as either display data or a character code to the RAM address specified by the cursor address counter. The value of the cursor address counter is incremented by 1 after the write.

• Display data read

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (Pattern data or character code) LSB							

Applications can read out data in RAM after the LC7982A has been set to the readout state by writing the instruction code 0DH to the instruction register when RS is 0. The data readout procedure is described below.

When this instruction is executed, the contents of the data output register will be output from the pins DB0 to DB7. After that, the RAM data specified by the cursor address will be transferred to the data output register. Additionally, the cursor address will be incremented by 1. As a result, the correct data will not be read out on the first readout after the cursor address is set, but the specified data will be read out on the second read. Accordingly, applications that read data out after setting the cursor address must perform a single dummy read operation.

• Bit clear

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	1	1	1	0
Bit clear	0	0	0	0	0	0	0	(N_B – 1) binary		

• Bit set

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	1	1	1	1
Bit set	0	0	0	0	0	0	0	(N_B – 1) binary		

The bit clear and bit set instructions set a specified bit in a byte in display data RAM to 0 or 1, respectively. The bit clear instruction clears the bit specified by N_B to 0, and the bit set instruction sets the bit to 1. The RAM address is determined by the cursor address, and the cursor address is automatically incremented by 1 after the instruction is executed. N_B must be a value in the range 1 to 8. A value of 1 specifies the LSB and a value of 8 specifies the MSB.

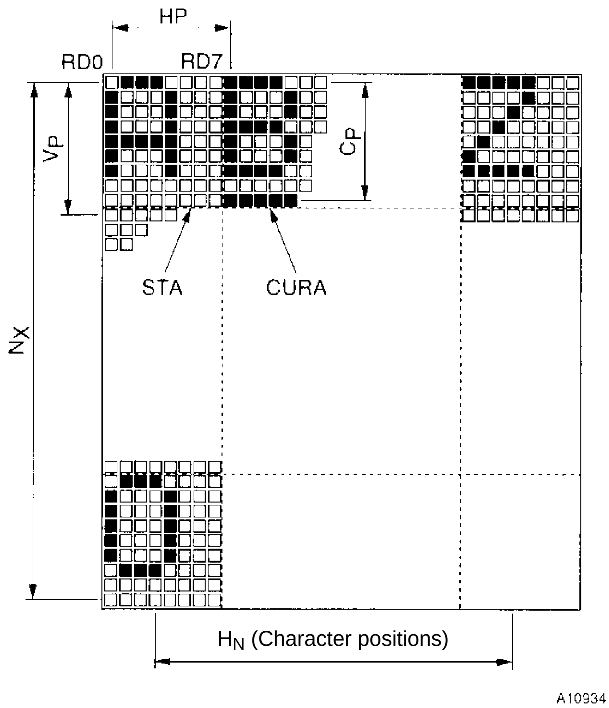
• Busy flag readout

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0	*						

When the LC7982A is set to readout mode when RS is 1, the state of the busy flag will be output from DB7. The busy flag will be 1 during the execution of any of the above thirteen instructions, and will be 0 when instruction execution has completed and the LC7982A can accept the next instruction. When the busy flag is 1, the LC7982A cannot accept instructions. Therefore, applications must check the busy flag and verify that it is 0 before executing an instruction or writing data to the LC7982A. However, after a data read instruction or a data write instruction, the microcontroller may execute the next instruction without checking the busy flag after the maximum value of the read cycle or write cycle, respectively. The busy flag is not changed by writes to the instruction register when RS is 1. Therefore, it is not necessary to check the busy flag immediately after writing the instruction register.

It is not necessary to issue any instruction register commands to read out the busy flag.

Relationship between HP, H_N, VP, CP, and N_X and the LCD Panel



Symbol	Function	Description	Value
HP	Horizontal character pitch	Character pitch in the horizontal direction	6 to 8 dots
H_N	Horizontal characters	Number of characters per line in the horizontal direction or number of words per line (in graphics mode)	An even number in the range 2 to 256
VP	Vertical character pitch	Character pitch in the vertical direction	1 to 16 dots
CP	Cursor position	Number of the line where the cursor will be displayed	1 to 16 lines
N_X	Vertical lines	Display duty	1 to 256 lines

Note: If m is the number of dots in the vertical direction on the screen, and n is the number of dots in the horizontal direction, then the following relationships will be held:

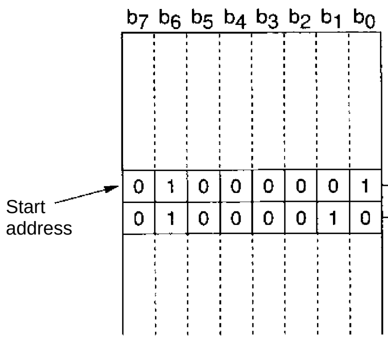
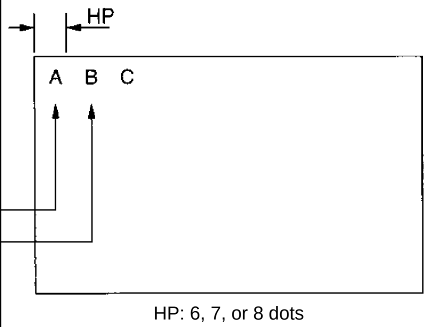
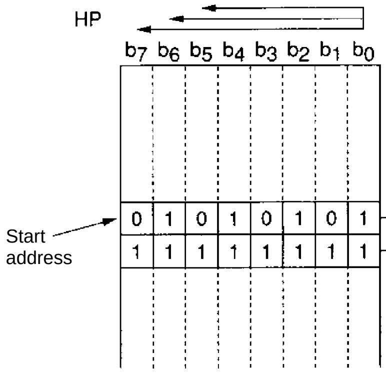
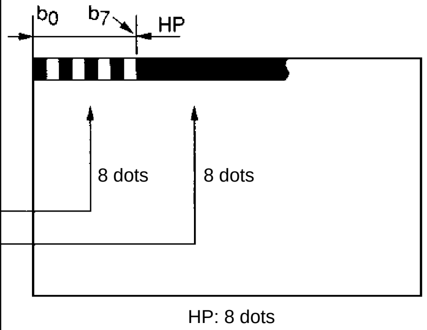
$1/m = 1/N_X$ = Display duty

$n = HP \times H_N$

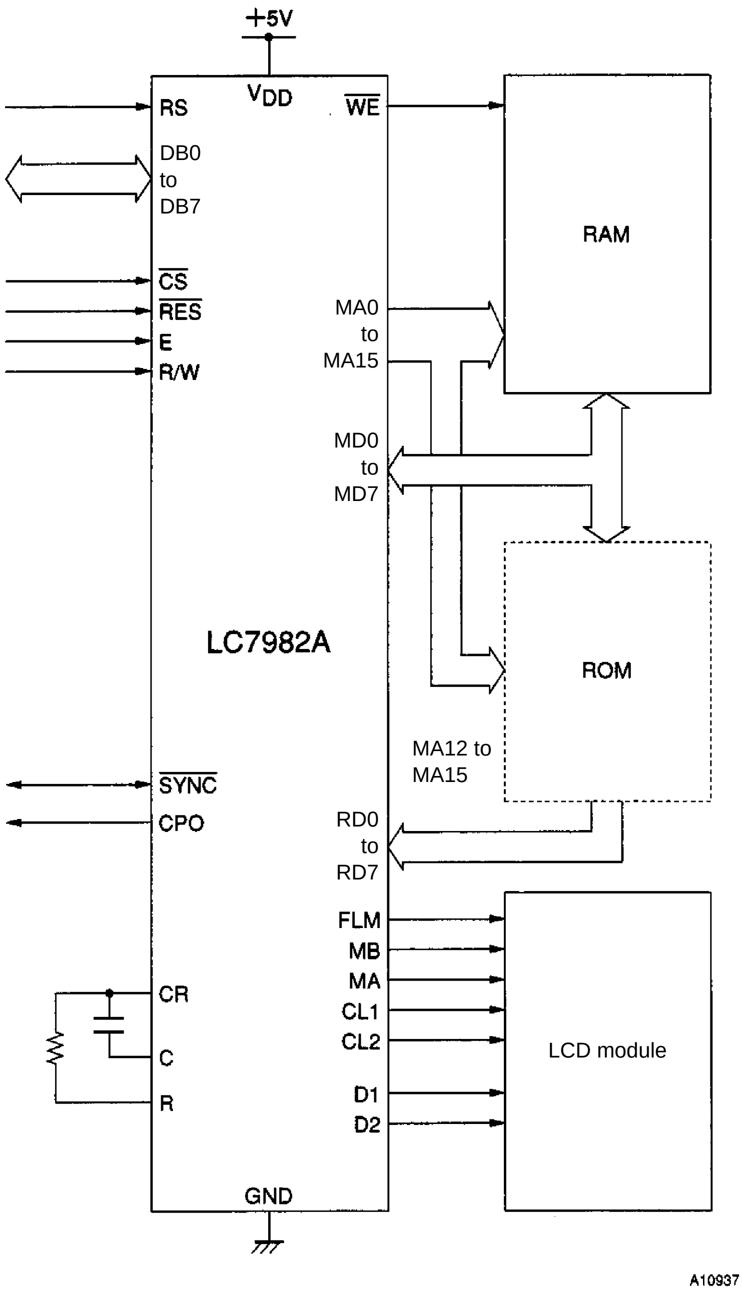
m/VP = Number of lines displayed

$CP \leq VP$

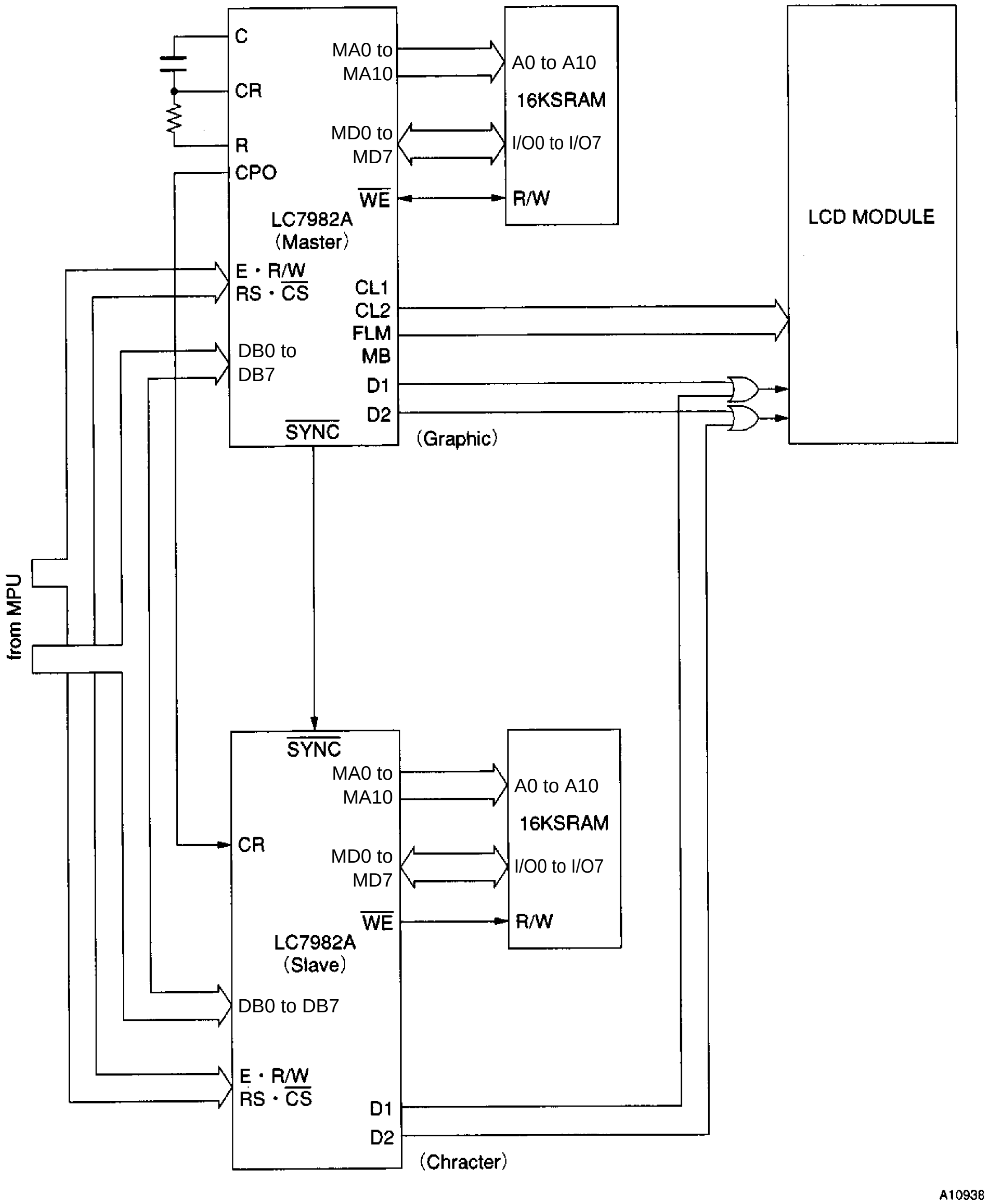
Display Modes

Display mode	Display data from the microcontroller	RAM	LCD panel
Character mode	Display patterns (8 bits)		
Graphics mode	Character codes (8 bits)		

Sample Application Circuit 1

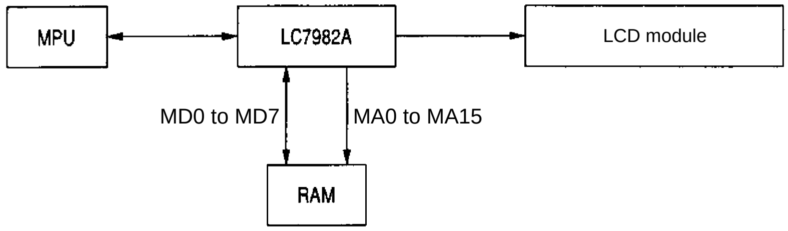


Sample Application Using Combined Graphic and Character Display



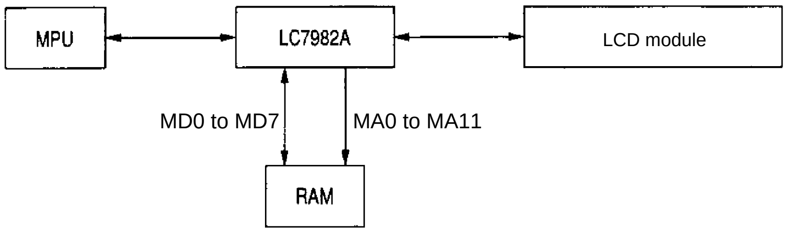
Sample Structures

- Graphics mode



A10939

- Character display mode (1) (On-chip character generator)



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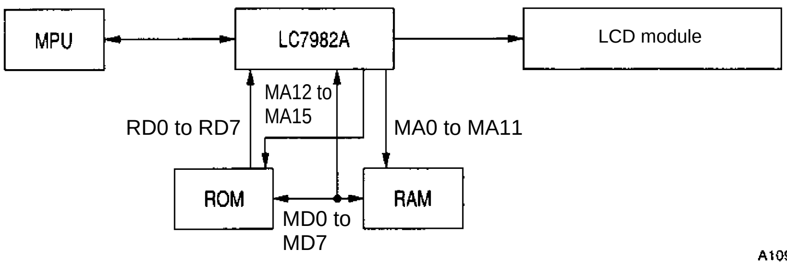
- Character display mode (2) (External character generator)



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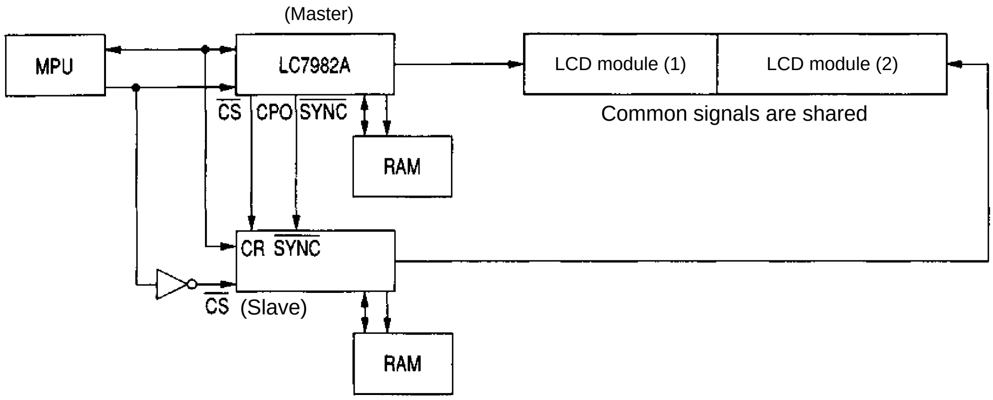
- Parallel operation



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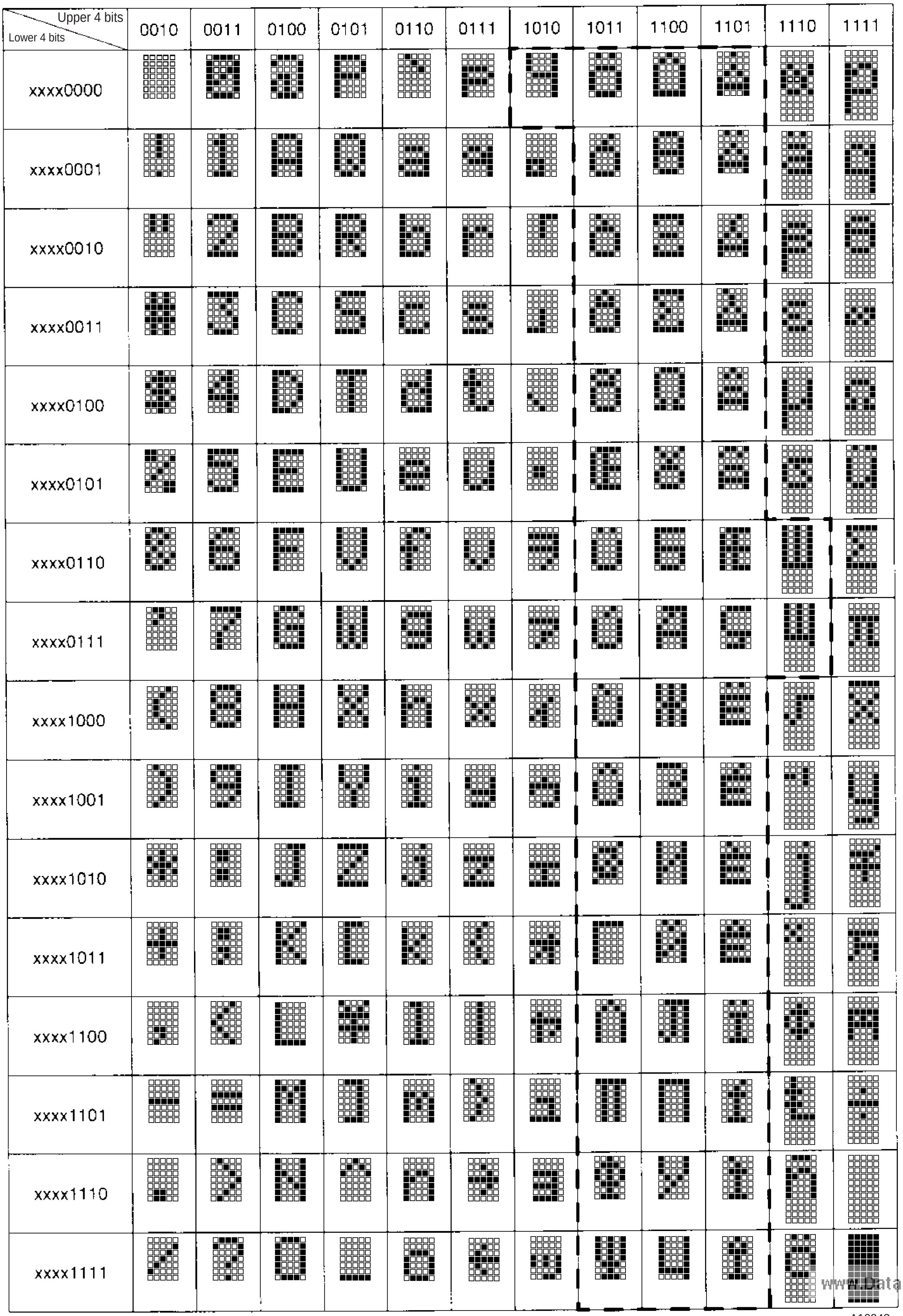
• LC7982A Built-in Character Generator (Only the characters enclosed in the heavy broken line differ from the LC7981.)



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This catalog provides information as of October, 1998. Specifications and information herein are subject to change without notice.