Ordering number : ENA0119A

SANYO Semiconductors
DATA SHEET

LC863864B, LC863856B
LC863848B, LC863840B
LC863832B, LC863828B
LC863824B, LC863820B
LC863816B

CMOS IC
64K/56K/48K/40K/32K/28K/24K/20K/16K-byte ROM, CGROM16K-byte
on-chip 768-byte RAM and 352×9-bit OSD RAM
8-bit 1-chip Microcontroller

Overview

The LC863864B/56B/48B/40B/32B/28B/24B/20B/16B are 8-bit single chip microcontrollers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.424µs
- On-chip ROM capacity
  Program ROM : 64K/56K/48K/40K/32K/28K/24K/20K/16K-bytes
  CGROM : 16K-bytes
- On-chip RAM capacity : 768-bytes
- OSD RAM : 352 × 9-bits
- Closed-Caption TV controller and the on-screen display controller
- Closed-Caption data slicer
- Four channels × 8-bit AD Converter
- Three channels × 7-bit PWM
- Two 16-bit timer/counter, 14-bit base timer
- 8-bit synchronous serial interface circuit
- IIC-bus compliant serial interface circuit (Multi-master type)

Continued on next page.

Note : This product includes the IIC bus interface circuit. If you intend to use the IIC bus interface, please notify us of this in advance of our receiving your program ROM code order.
Purchase of SANYO IIC components conveys a license under the Philips IIC Patents Rights to use these components in an IIC system, provided that the system conforms to the IIC Standard Specification as defined by Philips.

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- ROM correction function
- 16-source 10-vectored interrupt system
- Integrated system clock generator and display clock generator
  Only one X'tal oscillator (32.768kHz) for PLL reference is used for both generators
  TV control and the closed caption function

All of the above functions are fabricated on a single chip.

Features

■Read-only memory (ROM) : 65536 × 8-bits / 57344 × 8-bits / 49152 × 8-bits /
40960 × 8-bits / 32768 × 8-bits / 28672 × 8-bits /
24576 × 8-bits / 20480 × 8-bits / 16384 × 8-bits for program
16128 × 8-bits for CGROM

■Random access memory (RAM) : 768 × 8-bits (including 128 bytes for ROM correction function)
352 × 9-bits (for CRT display)

■OSD functions

- Screen display : 36 characters × 16 lines (by software)
- RAM : 352 words (9-bits per word)
  Display area : 36 words × 8 lines
  Control area : 8 words × 8 lines
- Characters
  Up to 252 kinds of 16 × 32 dot character fonts (4 characters including 1 test character are not programmable)
  Each font can be divided into two parts and used as two fonts : a 16 × 17 dot and 8 × 9 dot character font
  At least 111 characters need to be divide to display the caption fonts.
- Various character attributes
  Character colors : 16 colors
  Character background colors : 16 colors
  Fringe/shadow colors : 16 colors
  Full screen colors : 16 colors
  Rounding
  Underline
  Italic character (slanting)
- Attribute can be changed without spacing
- Vertical display start line number can be set for each row independently (Rows can be overlapped)
- Horizontal display start position can be set for each row independently
- Horizontal pitch (9 to 16 dots) *1 and vertical pitch (1 to 32 dots) can be set for each row independently
- Different display modes can be set for each row independently
  Caption • Text mode/OSD mode 1/OSD mode 2 (Quarter size) /Simplified graphic mode
- Ten character sizes *1
  Horez. × Vert. = (1 × 1), (1 × 2), (2 × 2), (2 × 4), (0.5 × 0.5)
  (1.5 × 1), (1.5 × 2), (3 × 2), (3 × 4), (0.75 × 0.5)
- Shuttering and scrolling on each row
- Simplified graphic display

*1 Note : Range depends on display mode : refer to the manual for details.

■Data Slicer (closed caption format)

- Closed caption data and XDS data extraction
- NTSC/PAL, and extracted line can be specified

■Bus Cycle Time/Instruction-Cycle Time

Bus cycle time	Instruction cycle time	Clock divider	System clock oscillation	Oscillation frequency	Voltage
0.424µs	0.848µs	1/2	Internal VCO (Ref : X'tal 32.768kHz)	14.156MHz	4.5V to 5.5V
7.5µs	15.0µs	1/2	Internal RC	800kHz	4.5V to 5.5V
91.55µs	183.1µs	1/1	Crystal	32.768kHz	4.5V to 5.5V
183.1µs	366.2µs	1/2	Crystal	32.768kHz	4.5V to 5.5V

■Ports

- Input/Output Ports : 5 ports (28 terminals)
  Data direction programmable in nibble units : 1 port (8 terminals)
  (If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.)
  Data direction programmable for each bit individually : 4 ports (20 terminals)

■AD converter

- 4-channels × 8-bit AD converters

■Serial interfaces

- IIC-bus compliant serial interface (Multi-master type)
  Consists of a single built-in circuit with two I/O channels. The two data lines and two clock lines can be connected internally.
- Synchronous 8-bit serial interface

■PWM output

- 3-channels × 7-bit PWM

■Timer

- Timer 0 : 16-bit timer/counter
  With 2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with a programmable prescaler
  Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with a programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of timer is 1 tCYC.
- Timer 1 : 16-bit timer/ PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9 to 16 bits)
  In mode0/1, the resolution of Timer1/PWM is 1 tCYC
  In mode2/3, the resolution is selectable by program; tCYC or 1/2 tCYC
- Base timer
  Generate every 500ms overflow for a clock application
  (using 32.768kHz crystal oscillation for the base timer clock)
  Generate every 976μs, 3.9ms, 15.6ms, 62.5ms overflow
  (using 32.768kHz crystal oscillation for the base timer clock)
  Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0

■Remote control receiver circuit (connected to the P73/INT3/T0IN terminal)

- Noise rejection function
- Polarity switching

■Watchdog timer

External RC circuit is required
Interrupt or system reset is activated when the timer overflows

■ROM correction function

Max 128-bytes/2 addresses

■Interrupts
- 16 sources 10 vectored interrupts
  1. External Interrupt INT0
  2. External Interrupt INT1
  3. External Interrupt INT2, Timer/counter T0L (Lower 8-bits)
  4. External Interrupt INT3, base timer
  5. Timer/counter T0H (Upper 8-bits)
  6. Timer T1H, Timer T1L
  7. SIO0
  8. Data slicer
  9. Vertical synchronous signal interrupt ($\overline{VS}$), horizontal line ($\overline{HS}$), AD
  10. IIC, Port 0
- Interrupt priority control
  Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible.
  Low or high priority can be assigned to the interrupts from 3 to 10 listed above.
  For the external interrupt INT0 and INT1, low or highest priority can be set.

■Sub-routine stack level
- A maximum of 128 levels (stack is built in the internal RAM)

■Multiplication/division instruction
- 16-bits × 8-bits (7 instruction cycle times)
- 16-bits ÷ 8-bits (7 instruction cycle times)

■3 oscillation circuits
- Built-in RC oscillation circuit used for the system clock
- Built-in VCO circuit used for the system clock and OSD
- X'tal oscillation circuit used for base timer, system clock and PLL reference

■Standby function
- HALT mode
  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped.
  This mode can be released by the interrupt request or the system reset.
- HOLD mode
  The HOLD mode is used to stop the oscillations ; RC (internal), VCO, and X'tal oscillations.
  This mode can be released by the following conditions.
  1. Pull the reset terminal ($\overline{RES}$) to low level.
  2. Feed the selected level to either P70/INT0 or P71/INT1.
  3. Input the interrupt condition to Port 0.

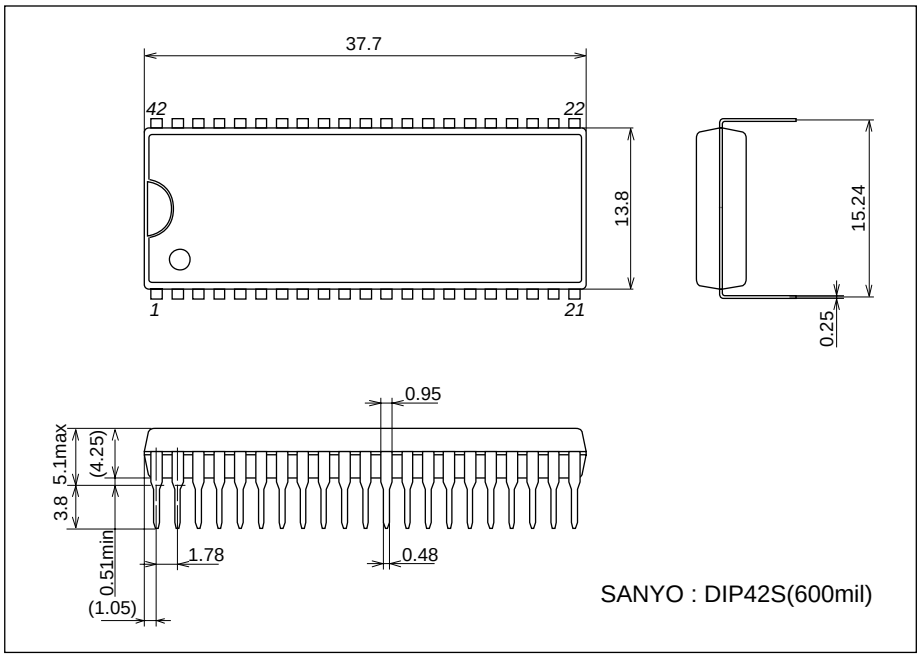
■Package
- DIP42S (Lead-free type)
- QIP48E (Lead-free type)

■Development tools
- Flash EEPROM : LC86F3864A
- Evaluation chip : LC863096
- Emulator : EVA86000 (main) + ECB863200A (evaluation chip board)
  + POD863200 (pod: DIP42S) or POD863201 (QIP48E)
  [Shared with LC8632 Series]

Package Dimensions

unit : mm

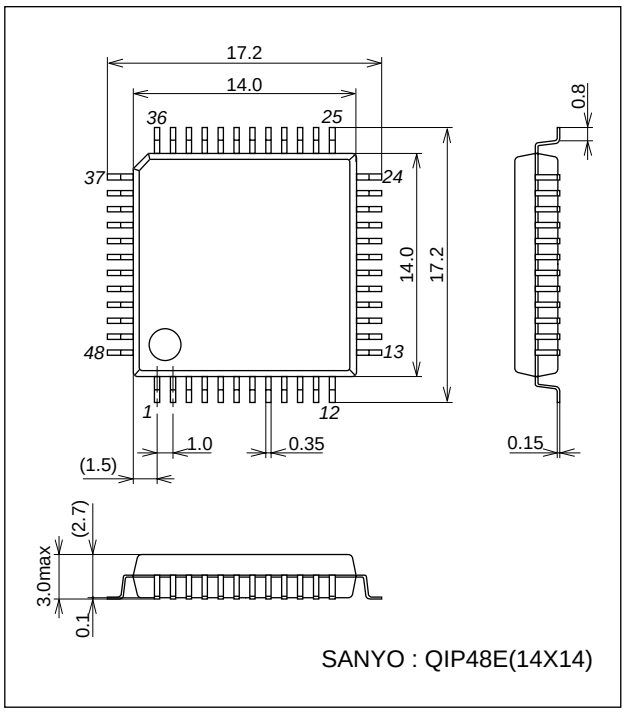
3025C



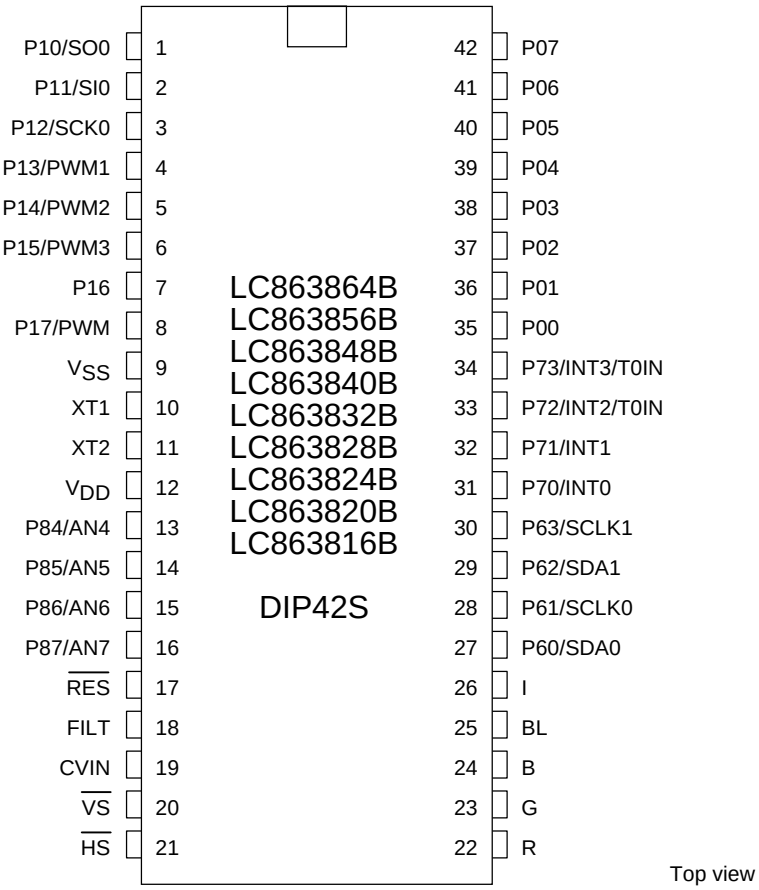
Package Dimensions

unit : mm

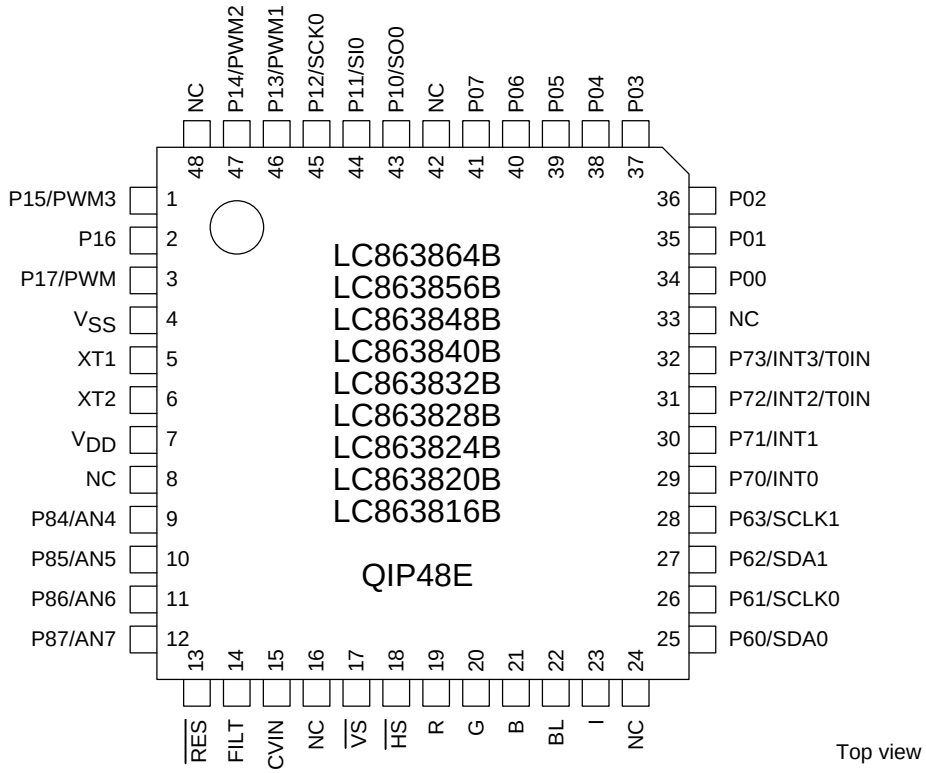
3156A



Pin Assignment

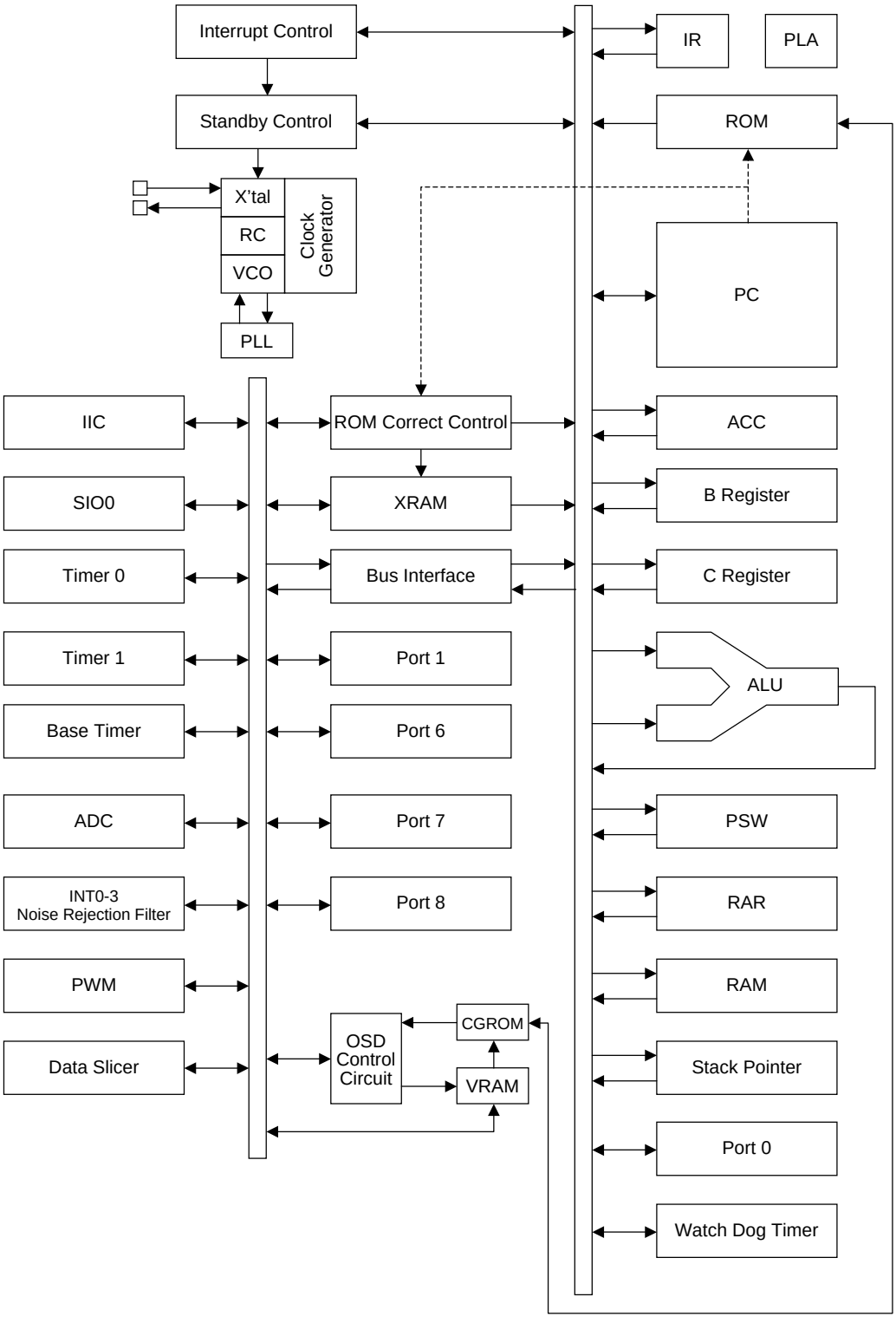


Top view



Top view

System Block Diagram



Pin Description

Terminal	I/O	Function Description	Option
V_{SS}	-	Negative power supply	
XT1	I	Input terminal for crystal oscillator	
XT2	O	Output terminal for crystal oscillator	
V_{DD}	-	Positive power supply	
$\overline{RES}$	I	Reset terminal	
FILT	O	Filter terminal for PLL	
CVIN	I	Video signal input terminal	
$\overline{VS}$	I	Vertical synchronization signal input terminal	
$\overline{HS}$	I	Horizontal synchronization signal input terminal	
R	O	Red (R) output terminal of RGB image output	
G	O	Green (G) output terminal of RGB image output	
B	O	Blue (B) output terminal of RGB image output	
I	O	Intensity (I) output terminal of RGB image output	
BL	O	Fast blanking control signal Switch TV image signal and caption/OSD image signal	
Port 0 P00 to P07	I/O	• 8-bit input/output port, Input/output can be specified in nibble unit • Other functions HOLD release input Interrupt input	Pull-up resistor provided/not provided Output Format CMOS/Nch-OD
Port 1 P10 to P17	I/O	• 8-bit input/output port Input/output can be specified in a bit • Other functions P10: SIO0 data output P11: SIO0 data input/bus input/output P12: SIO0 clock input/output P13: PWM1 output P14: PWM2 output P15: PWM3 output P17: Timer1 (PWM) output	Output Format CMOS/Nch-OD
Port 6 P60 to P63	I/O	• 4-bit input/output port Input/output can be specified for each bit • Other functions P60: IIC0 data I/O P61: IIC0 clock output P62: IIC1 data I/O P63: IIC1 clock output	

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<table>
<tr><th>Terminal</th><th>I/O</th><th>Function Description</th><th>Option</th></tr>
<tr><td>Port 7
P70
P71 to P73</td><td>I/O</td><td>• 4-bit input/output port
Input or output can be specified for each bit
• Other function
<table><tr><td>P70</td><td>INT0 input/HOLD release input/
Nch-Tr. output for watchdog timer</td></tr><tr><td>P71</td><td>INT1 input/HOLD release input</td></tr><tr><td>P72</td><td>INT2 input/Timer 0 event input</td></tr><tr><td>P73</td><td>INT3 input (noise rejection filter connected)/
Timer 0 event input</td></tr></table>Interrupt receiver format, vector addresses
<table><tr><th></th><th>rising</th><th>falling</th><th>rising/
falling</th><th>H level</th><th>L level</th><th>vector</th></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr></table></td><td></td></tr>
<tr><td>Port 8
P84 to P87</td><td>I/O</td><td>• 4-bit input/output port
Input or output can be specified for each bit
• Other function
AD converter input port (4 lines)</td><td></td></tr>
<tr><td>NC</td><td>-</td><td>Unused terminal
Leave open</td><td></td></tr>
</table>

• Output form and existence of pull-up resistor for all ports can be specified for each bit.
• Programmable pull-up resistor is always connected regardless of port option, CMOS or N-ch open drain output in port 1.

• Port status in reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	I	Pull-up resistor OFF, ON after reset release
Port 1	I	Programmable pull-up resistor OFF

Absolute Maximum Ratings / Ta = 25°C, V_{SS} = 0V

Parameter		Symbol	Pins	Conditions		Limits			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	V_{DD}			-0.3		+6.5	V
Input voltage		V_I(1)	$\overline{RES}$, HS, $\overline{VS}$, CVIN			-0.3		V_{DD}+0.3	
Output voltage		V_O(1)	R, G, B, I, BL, FILT			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}	Ports 0, 1, 6, 7, 8			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 7, 8	• CMOS output • For each pin.		-4			mA
		IOPH(2)	R, G, B, I, BL	• CMOS output • For each pin.		-5			
	Total output current	ΣIOAH(1)	Ports 0, 1	The total of all pins.		-20			
		ΣIOAH(2)	Ports 7, 8	The total of all pins.		-10			
		ΣIOAH(3)	R, G, B, I, BL	The total of all pins.		-15			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 6, 8	For each pin.				20	
		IOPL(2)	Port 7	For each pin.				15	
		IOPL(3)	R, G, B, I, BL	For each pin.				5	
	Total output current	ΣIOAL(1)	Ports 0, 1	The total of all pins.				40	
		ΣIOAL(2)	Ports 6, 7, 8	The total of all pins.				40	
		ΣIOAL(3)	R, G, B, I, BL	The total of all pins.				15	
Maximum power dissipation		Pd max	DIP42S	Ta = -10 to +70°C				715	mW
			QIP48E					385	
Operating temperature range		Topr				-10		+70	°C
Storage temperature range		Tstg				-55		+125	

Recommended Operating Range / Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions		Limits			
				V_{DD} [V]	min	typ	max	unit
Operating supply voltage range	V_{DD}(1)	V_{DD}	0.844µs ≤ tCYC ≤ 0.852µs		4.5		5.5	V
	V_{DD}(2)		4µs ≤ tCYC ≤ 400µs		4.5		5.5	
Hold voltage	V_{HD}	V_{DD}	RAMs and the registers data are kept in HOLD mode.		2.0		5.5	
High level input voltage	V_{IH}(1)	Port 0 (Schumitt)	Output disable	4.5 to 5.5	0.6V_{DD}		V_{DD}	
	V_{IH}(2)	• Ports 1, 6 (Schumitt) • Port 7 (Schumitt) port input/interrupt •HS, $\overline{VS}$, $\overline{RES}$ (Schumitt)	Output disable	4.5 to 5.5	0.75V_{DD}		V_{DD}	
	V_{IH}(3)	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	V_{DD}-0.5		V_{DD}	
	V_{IH}(4)	Port 8 Watchdog timer input	Output disable	4.5 to 5.5	0.7V_{DD}		V_{DD}	

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Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
Low level input voltage	V_{IL}(1)	Port 0 (Schumitt)	Output disable	4.5 to 5.5	V_{SS}		$0.2V_{DD}$	V
	V_{IL}(2)	• Ports 1, 6 (Schumitt) • Port 7 (Schumitt) port input/interrupt • $\overline{HS}$, $\overline{VS}$, $\overline{RES}$ (Schumitt)	Output disable	4.5 to 5.5	V_{SS}		$0.25V_{DD}$	
	V_{IL}(3)	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	V_{SS}		$0.6V_{DD}$	
	V_{IL}(4)	Port 8 Watchdog timer input	Output disable	4.5 to 5.5	V_{SS}		$0.3V_{DD}$	
CVIN	VCVIN	CVIN		5.0	1Vp-p -3dB	1Vp-p	1Vp-p +3dB	Vp-p*
Operation cycle time	tCYC(1)		• All functions operating	4.5 to 5.5	0.844	0.848	0.852	µs
	tCYC(2)		• AD converter operating • OSD and Data slicer are not operating	4.5 to 5.5	0.844		30	
	tCYC(3)		• OSD, AD converter and Data slicer are not operating	4.5 to 5.5	0.844		400	
Oscillation frequency range	FmRC		Internal RC oscillation	4.5 to 5.5	0.4	0.8	3.0	MHz

* Vp-p : Peak-to-peak voltage

Electrical Characteristics / Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	Ports 0, 1, 6, 7, 8	• Output disable • Pull-up MOS Tr. OFF • V_{IN} = V_{DD} (Including the off-leak current of the output Tr.)	4.5 to 5.5			1	µA
	I_{IH}(2)	• $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	• V_{IN} = V_{DD}	4.5 to 5.5			1	
Low level input current	I_{IL}(1)	Ports 0, 1, 6, 7, 8	• Output disable • Pull-up MOS Tr. OFF • V_{IN} = V_{SS} (Including the off- leak current of the output Tr.)	4.5 to 5.5	-1			
	I_{IL}(2)	• $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	V_{IN} = V_{SS}	4.5 to 5.5	-1			
High level output voltage	V_{OH}(1)	• CMOS output of ports 0, 1, 71 to 73, 8	I_{OH} = -1.0mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH}(2)	R, G, B, I, BL	I_{OH} = -0.1mA	4.5 to 5.5	V_{DD}-0.5			
Low level output voltage	V_{OL}(1)	Ports 0, 1, 71 to 73, 8	I_{OL} = 10mA	4.5 to 5.5			1.5	
	V_{OL}(2)	Ports 0, 1, 71 to 73, 8	I_{OL} = 1.6mA	4.5 to 5.5			0.4	
	V_{OL}(3)	• R, G, B, I, BL • Port 6	I_{OL} = 3.0mA	4.5 to 5.5			0.4	
	V_{OL}(4)	Port 6	I_{OL} = 6.0mA	4.5 to 5.5			0.6	
	V_{OL}(5)	Port 70	I_{OL} = 1mA	4.5 to 5.5			0.4	
Pull-up MOS Tr. resistance	Rpu	• Ports 0, 1, 7, 8	V_{OH} = $0.9V_{DD}$	4.5 to 5.5	13	38	80	kΩ
Bus terminal short circuit resistance (SCL0 to SCL1, SDA0 to SDA1)	RBS	• P60 to P62 • P61 to P63		4.5 to 5.5		130	300	Ω

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Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD}[V]	min	typ	max	unit
Hysteresis voltage	VHIS	• Ports 0, 1, 6, 7 • $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	Output disable	4.5 to 5.5		$0.1V_{DD}$		V
Input clump voltage	VCLMP	CVIN		5.0	2.3	2.5	2.7	
Pin capacitance	CP	All pins	• f = 1MHz • Every other terminals are connected to V_{SS}. • Ta = 25°C	4.5 to 5.5		10		pF

Serial Input/Output Characteristics at Ta = -10°C to +70°C, V_{SS} = 0V

Parameter			Symbol	Pins	Conditions		Ratings			unit
						V_{DD}[V]	min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	•SCK0 •SCLK0	Refer to figure 4.	4.5 to 5.5	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	•SCK0 •SCLK0	• Use pull-up resistor (1kΩ) when Nch open-drain output. • Refer to figure 4.	4.5 to 5.5	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set up time		tICK	SI0	• Data set-up to SCK0. • Data hold from SCK0. • Refer to figure 4.	4.5 to 5.5	0.1			µs
	Data hold time		tCKI				0.1			
Serial output	Output delay time (Using external clock)		tCKO(1)	SO0	• Data hold from SCK0. • Use pull-up resistor (1kΩ) when Nch open-drain output. • Refer to figure 4.	4.5 to 5.5			7/12tCYC +0.2	
	Output delay time (Using internal clock)		tCKO(2)	SO0		4.5 to 5.5			1/3tCYC +0.2	

IIC Input/Output Conditions / Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Standard		High speed		unit
		min	max	min	max	
SCL frequency	fSCL	0	100	0	400	kHz
BUS free time between stop to start	tBUF	4.7	-	1.3	-	µs
HOLD time of start, restart condition	tHD ; STA	4.0	-	0.6	-	µs
L time of SCL	tLOW	4.7	-	1.3	-	µs
H time of SCL	tHIGH	4.0	-	0.6	-	µs
Set-up time of restart condition	tSU ; STA	4.7	-	0.6	-	µs
HOLD time of SDA	tHD ; DAT	0	-	0	0.9	µs
Set-up time of SDA	tSU ; DAT	250	-	100	-	ns
Rising time of SDA, SCL	tR	-	1000	20 + 0.1Cb	300	ns
Falling time of SDA, SCL	tF	-	300	20 + 0.1Cb	300	ns
Set-up time of stop condition	tSU ; STO	4.0	-	0.6	-	µs

Refer to figure 10

Note: Cb: Total capacitance of all BUS (unit: pF)

Pulse Input Conditions / Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	• Interrupt acceptable • Timer 0-countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (1 tCYC is selected for noise rejection clock.)	• Interrupt acceptable • Timer 0-countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (16 tCYC is selected for noise rejection clock.)	• Interrupt acceptable • Timer 0-countable	4.5 to 5.5	32			
	tPIH(4) tPIL(4)	INT3/T0IN (64 tCYC is selected for noise rejection clock.)	• Interrupt acceptable • Timer 0-countable	4.5 to 5.5	128			
	tPIL(5)	$\overline{RES}$	Reset acceptable	4.5 to 5.5	200			µs
	tPIH(6) tPIL(6)	$\overline{HS}$, $\overline{VS}$	• Display position controllable • The active edge of $\overline{HS}$ and $\overline{VS}$ must be apart at least 1 tCYC. • Refer to figure 6.	4.5 to 5.5	3			
Rising/falling time	tTHL tTLH	$\overline{HS}$	Refer to figure 6.	4.5 to 5.5			500	ns

AD Converter Characteristics / Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
Resolution	N			4.5 to 5.5		8		bit
Absolute precision	ET		(Note 3)				±1.5	LSB
Conversion time	tCAD		ADCR2=0 (Note 4)			16		tCYC
			ADCR2=1 (Note 4)			32		
Analog input voltage range	VAIN	AN4 to AN7			V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN = V_{DD}				1	µA
	IAINL		VAIN = V_{SS}		-1			

Note 3: Absolute precision does not include quantizing error (1/2LSB).

Note 4: Conversion time is the time till the complete digital conversion value for analog input value is set to a register after the instruction to start conversion is sent.

Current Dissipation Characteristics / Ta = -10°C to +70°C, V_{SS} = 0V

The sample current dissipation characteristics is the measurement result of SANYO provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally. The currents through the output transistors and the pull-up MOS transistors are ignored.

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
Current dissipation during basic operation (Note 5)	IDDOP(1)	V_{DD}	• FmX'tal=32.768kHz X'tal oscillation • System clock : VCO • VCO for OSD operating • Internal RC oscillation stops	4.5 to 5.5		10	24	mA
	IDDOP(2)		• FmX'tal=32.768kHz X'tal oscillation • System clock : X'tal (Instruction cycle time: 366.2µs) • VCO for system, VCO for OSD, Internal RC oscillation stop • Data slicer, AD converters stop	4.5 to 5.5		55	300	µA
Current dissipation in HALT mode (Note 5)	IDDHALT(1)		• HALT mode • FmX'tal=32.768kHz X'tal oscillation • System clock : VCO • VCO for OSD stops • Internal RC oscillation stops	4.5 to 5.5		3	9	mA
	IDDHALT(2)		• HALT mode • FmX'tal=32.768kHz X'tal oscillation • VCO for system stops • VCO for OSD stops • System clock : Internal RC	4.5 to 5.5		300	1000	µA
	IDDHALT(3)		• HALT mode • FmX'tal=32.768kHz X'tal oscillation • VCO for system stops • VCO for OSD stops • System clock : X'tal (Instruction cycle time: 366.2µs)	4.5 to 5.5		45	200	
Current dissipation in HOLD mode (Note 5)	IDDHOLD		• HOLD mode • All oscillation stops.	4.5 to 5.5		0.05	20	

(Note 5) The currents through the output transistors and the pull-up MOS transistors are ignored.

Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions :

- Recommended circuit parameters are verified by an oscillator manufacturer using a SANYO provided oscillation evaluation board.
- Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -10 to +70°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rf	Rd		typ	max	
32.768kHz	Seiko Epson	C-002RX	18pF	18pF	OPEN	390kΩ	4.5 to 5.5V	1.0s	1.5s	

Notes : The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)

1. The V_{DD} becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications.
For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +70°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with SANYO sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' V_{SS} should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

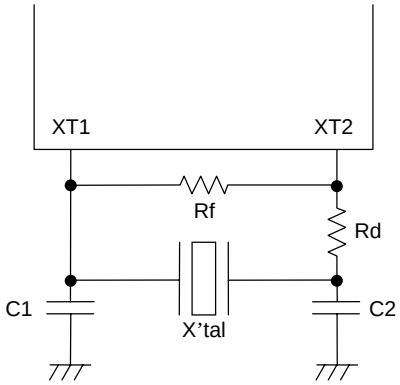
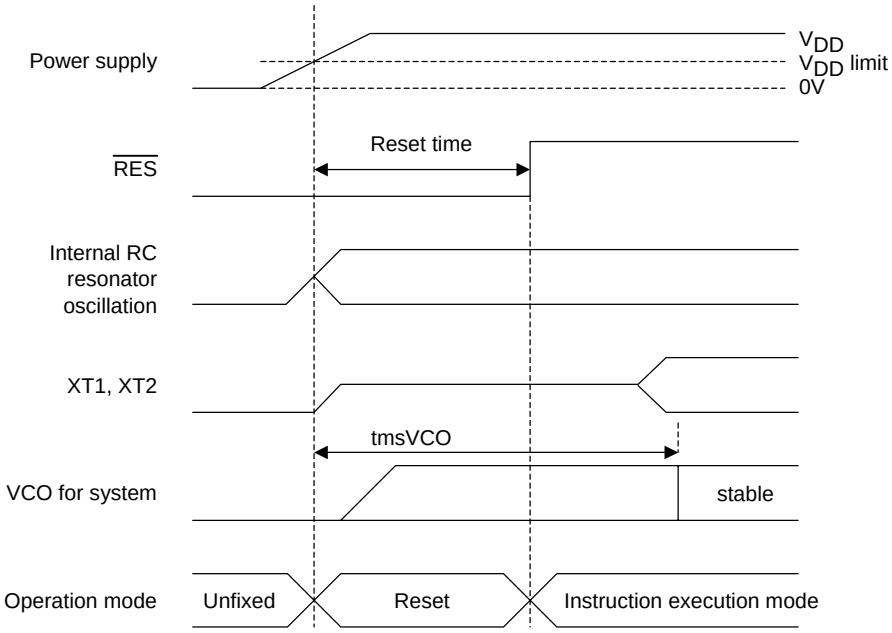
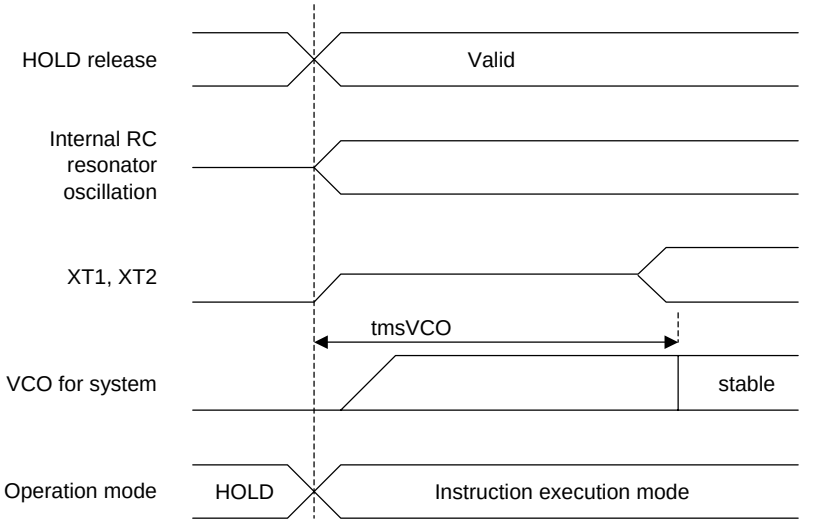


Figure 1 Recommended oscillation circuit

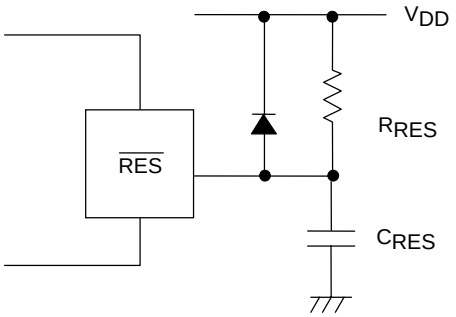


<Reset time and oscillation stabilizing time>



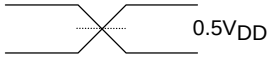
<HOLD release signal and oscillation stabilizing time>

Figure 2 Oscillation stabilizing time

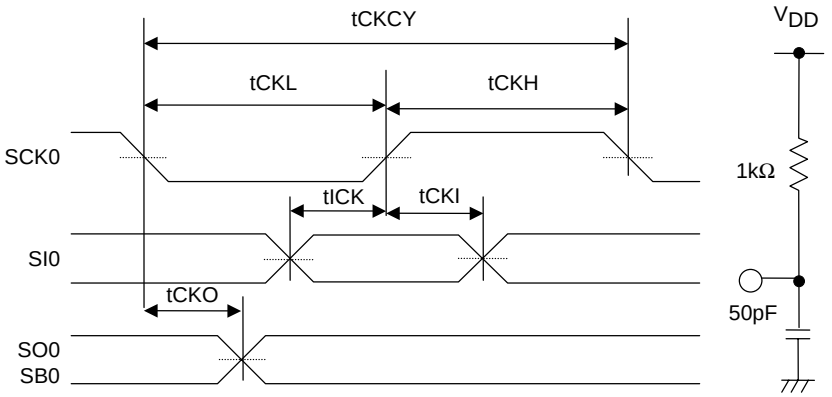


(Note) Determine the CRES, RRES value to generate more than 200μs reset time.

Figure 3 Reset circuit



<AC timing measurement point>



<Timing> <Test load>

Figure 4 Serial input / output test condition

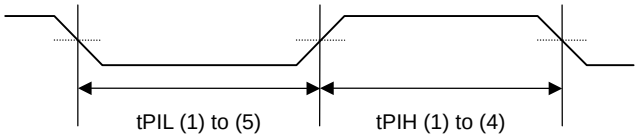


Figure 5 Pulse input timing condition - 1

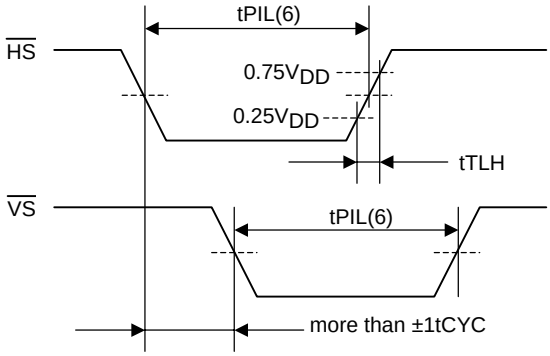


Figure 6 Pulse input timing condition - 2

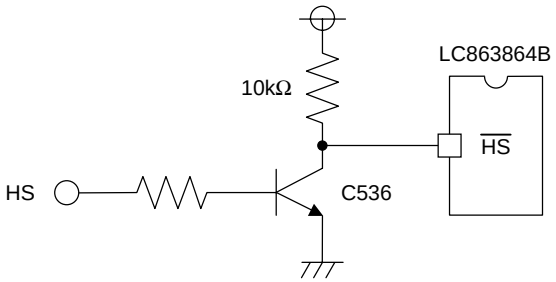
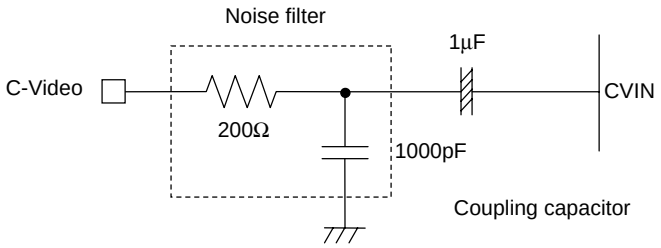


Figure 7 Recommended Interface circuit



Output impedance of C-Video before Noise filter should be less then 100Ω.
Figure 8 CVIN recommended circuit

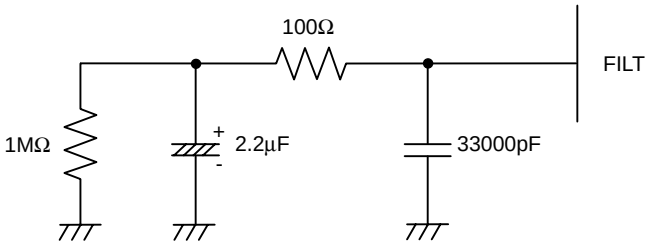
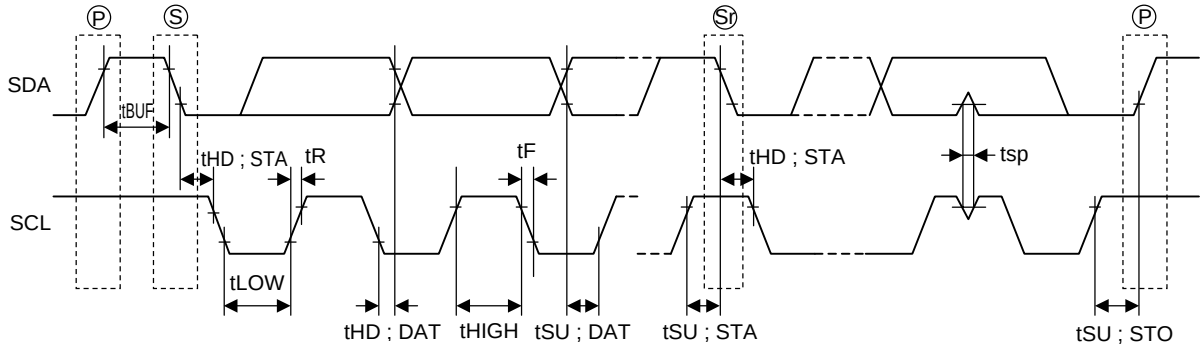


Figure 9 FILT recommended circuit
Note : Place FILT parts on board as close to the microcontroller as possible.



S : start condition
P : stop condition
Sr : restart condition

tsp : Spike suppression

Standard mode : not exist
High speed mode : less than 50ns

Figure 10 IIC timing