# LC864532A/28A/24A/20A/16A/12A/08A

## 8-bit Single Chip Microcontroller

## Overview

The LC864532A/28A/24A/20A/16A/12A/08A microcontrollers are 8-bit single chip microcontrollers for the TV controls with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.5 μs
- On-chip ROM maximum capacity : 32K bytes (LC864532A)
- On-chip RAM capacity : 256 bytes
- CRT display RAM : 160 × 9 bits
- On-Screen Display controller
  Kanji (Chinese character) displaying available
- 16-bit timer/counter
- 16-bit timer/PWM
- 4-channel × 4-bit A/D Converter
- Two 6-bit D/A Converters
- 8-bit synchronous serial-interface circuit

All of the functions above are fabricated on a single chip.

## Package Dimensions

unit : mm

### 3128-DIP52S



[LC864532A, 28A, 24A, 20A, 16A, 12A, 08A]

SANYO : DIP52S
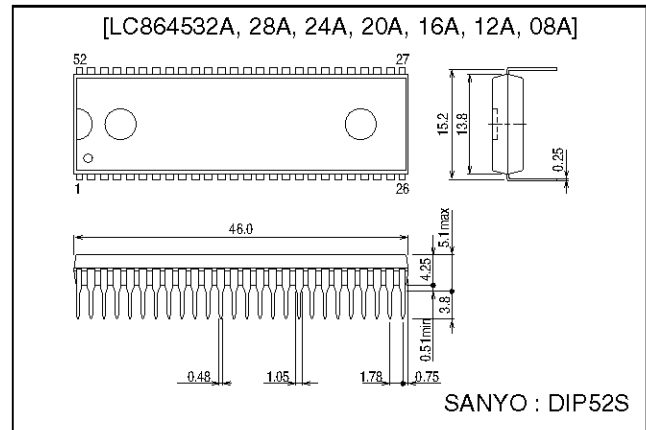
## Feature

(1) Read-Only Memory (ROM) :

| | | | |
|---|---|---|---|
| LC864532A | 32768 × 8 bits | LC864516A | 16384 × 8 bits |
| LC864528A | 28672 × 8 bits | LC864512A | 12288 × 8 bits |
| LC864524A | 24576 × 8 bits | LC864508A | 8192 × 8 bits |
| LC864520A | 20480 × 8 bits | | |

(2) Random Access Memory (RAM) :    256 × 8 bits
    160 × 9 bits  (for CRT display)

(3) Bus cycle time / Instruction-cycle time
The LC864532A/28A/24A/20A/16A/12A/08A microcontrollers are constructed to read the ROM twice within one instruction cycle. It has about 1.7 times performance capability within the same instruction-cycle compared to our 4-bit microcontrollers (LC66000 series).
The bus cycle time indicates the speed to read ROM.

| Bus cycle time | Instruction cycle time | System clock oscillation | Oscillation frequency | Voltage |
|---|---|---|---|---|
| 0.5 μs | 1.0 μs | Ceramic (CF) | 12 MHz | 4.5 V to 5.5 V |
| 7.5 μs | 15.0 μs | Internal RC | 800 kHz | 4.5 V to 5.5 V |

(4) OSD functions
- • Screen for display        : 34 columns × 16 rows (at standard character size)
- • Display RAM              : 160 × 9 bits (6 columns for control + 34 columns for display) × 4 rows × 9 bits
- • 252 kinds of user specified characters
            252 kinds        12 × 18 dots
- • Various character attributes
  Character colors                              : 8 colors
  Character background colors                   : 8 colors
  Fringe / shadow                               : 8 colors
  Full screen colors                            : 8 colors
  Fringe / shadow
  Rounding
- • Adjacent character attribute data changing available
- • Vertical display start line setting in row unit available  (row overlapping available)
- • Horizontal display start position setting available
- • Eight kinds of character size
            Horiz. × Vert.  = (1 × 1),  (1 × 2),  (2 × 2),  (2 × 4)
                                  (1.5 × 1),  (1.5 × 2),  (3 × 2),  (3 × 4)
- • Shuttering and scrolling in row unit available
- • Horizontal character pitch selectable  :  9 to 16 dots
- • Polarity of $\overline{R}$, $\overline{G}$, $\overline{B}$, $\overline{BL}$ output programmable
- • Polarity of $\overline{HS}$, $\overline{VS}$ input programmable

(5) Ports
- - Input/output ports                                          :  2 ports (16 lines)
  Input/output port programmable in nibble units              :  1 port (8 lines)
  (when the N-ch open drain output is selected, the data in a bit can be inputted)
  Input/output port programmable in bit units                 :  1 port (8 lines)
- - Input ports                                                 :  2 ports (8 lines)

(6) A/D converter
- - 4-channel × 4-bit A/D converter (converted with program)

(7) D/A converters
- - Two 7-bit D/A converters

(8) PWM  outputs
- - Ten 7-bit PWMs
- - 10-channel × 7-bit PWM

(9) Timer
- - Timer 0 :  16-bit timer / counter
  2-bit prescaler  +  8-bit built-in programmable prescaler
  Mode 0 :        Two 8-bit timers with a programmable prescaler
  Mode 1 :        8-bit timer with a programmable prescaler + 8-bit counter
  Mode 2 :        16-bit timer with a programmable prescaler
  Mode 3 :        16-bit counter
                  The resolution of Timer is 1 tCYC.
- - Timer 1 :  16-bit timer / PWM
  Mode 0 :        Two 8-bit timers with a programmable prescaler
  Mode 1 :        8-bit timer with a programmable prescaler + 8-bit PWM
  Mode 2 :        16-bit timer with a programmable prescaler
  Mode 3 :        Variable-bit PWM (9 to 16 bits)
                  In Mode 0 and Mode 1, the resolution of Timer and PWM is 1 tCYC.
                  In Mode 2 and Mode 3, the resolution of Timer and PWM selectable : 1 tCYC or 1/2 tCYC by program.

(10) Remote control receiver circuit (shares with the P73/INT3/T0IN pin)
- Noise rejection function
- Polarity switching

(11) Watchdog timer
External RC circuit is required
Interrupt or system reset is selectable.

(12) Interrupts
- 12-source 9-vectored interrupts
1. External interrupt INT0
2. External interrupt INT1
3. External interrupt INT2, Timer/counter T0L (Lower 8 bits)
4. External interrupt INT3
5. Timer/counter T0H (Upper 8 bits)
6. Timer T1H, T1L
7. Serial interface 0 (SIO0)
8. Vertical synchronous signal interrupt $(\overline{VS})$, End of display row
9. Port 0

- Interrupt priority control available
Three interrupt priorities are supported (low, high and the highest) and multilevel nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 10 listed above. For the external interrupt INT0 and INT1, high or the highest priority can be set.

(13) Sub-routine stack level
- A maximum of 128 levels (Sets the stack inside a RAM.)

(14) Multiplication/division instruction
- 16 bits × 8 bits ( 7 instruction cycle times)
- 16 bits / 8 bits ( 7 instruction cycle times)

(15) 3 oscillation circuits
- On-chip RC oscillation circuit for the system clock
- On-chip CF oscillation circuit for the system clock
- On-chip LC oscillation circuit for the CRT synchronization

(16) Standby function
- HALT mode function
The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This mode can be released by the interrupt request signals or the system reset.
- HOLD Mode
The HOLD mode is used to stop oscillations ; the RC (internal) and the ceramic oscillations. This mode can be released by the following conditions.
• Pull the reset pin ($\overline{RES}$) to low level.
• Feed the selected level to either P70/INT0 or P71/INT1.
• Feed the Port0 interrupt condition.

(17) Factory shipments
DIP52S

(18) Development Tools
- Evaluation (EVA) chip        :  LC866098
- EPROM with a window        :  LC86E4564
- One time ROM version        :  LC86P4564
- Emulator        :  EVA86000 (Main) + ECB864500 (Evaluation board) + POD864500 (Pod)

## System Block Diagram
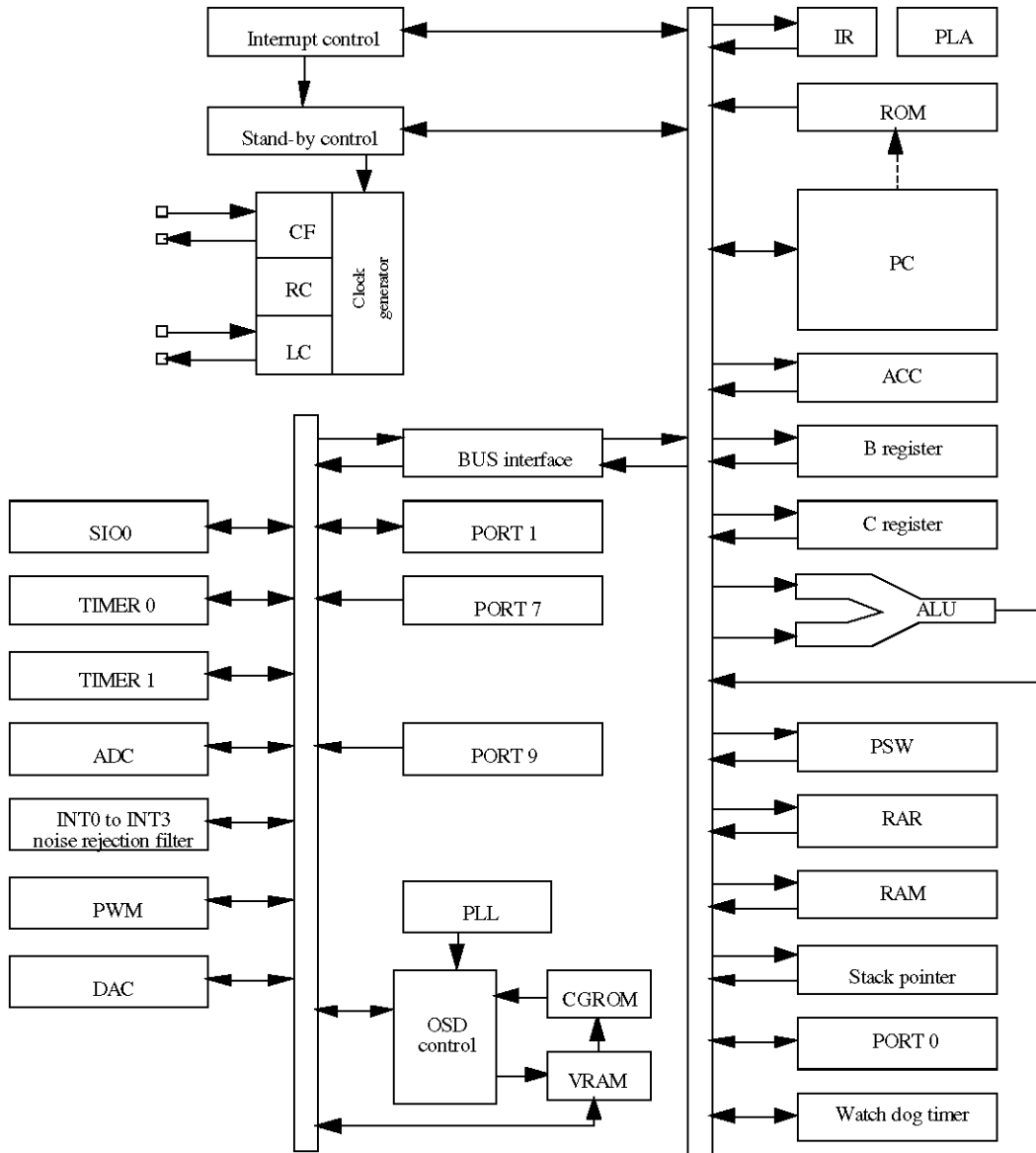
**Pin Assignment**

| | | | |
|---|---|---|---|
| P10/SO0 | 1 | 52 | P07 |
| P11/SI0/SB0 | 2 | 51 | P06 |
| P12/SCK0 | 3 | 50 | P05 |
| P13 | 4 | 49 | P04 |
| P14 | 5 | 48 | P03 |
| P15 | 6 | 47 | P02 |
| P16 | 7 | 46 | P01 |
| P17/PWM | 8 | 45 | P00 |
| DVSS | 9 | 44 | P73/INT3/T0IN |
| CF1 | 10 | 43 | P72/INT2/T0IN |
| CF2 | 11 | 42 | P71/INT1 |
| DVDD | 12 | 41 | P70/INT0 |
| P90/AN0 | 13 | 40 | PWM9 |
| P91/AN1 | 14 | 39 | PWM8 |
| P92/AN2 | 15 | 38 | PWM7 |
| P93/AN3 | 16 | 37 | PWM6 |
| $\overline{\text{RES}}$ | 17 | 36 | PWM5 |
| LC1 | 18 | 35 | PWM4 |
| LC2 | 19 | 34 | PWM3 |
| FILT | 20 | 33 | PWM2 |
| AVDD | 21 | 32 | PWM1 |
| AVSS | 22 | 31 | PWM0 |
| DA0 | 23 | 30 | BL |
| DA1 | 24 | 29 | B |
| $\overline{\text{VS}}$ | 25 | 28 | G |
| $\overline{\text{HS}}$ | 26 | 27 | R |

**Top view**

## Pin Description

• Port option is able to be specified by a bit unit.

Pin Description Table

| Pin name | Pin No. | I/O | Function description | Option |
|---|---|---|---|---|
| DVSS | 9 | — | Negative power terminal for digital circuit | |
| CF1 | 10 | Input | Input terminal for ceramic resonator | |
| CF2 | 11 | Input | Output terminal for ceramic resonator | |
| DVDD | 12 | — | Positive power terminal for digital circuit | |
| $\overline{\text{RES}}$ | 17 | Input | Reset terminal | |
| LC1 | 18 | Input | LC oscillation circuit input terminal | |
| LC2 | 19 | Output | LC oscillation circuit output terminal | |
| FILT | 20 | Output | Filter terminal for PLL | |
| AVDD | 21 | — | Positive power terminal for analog circuit | |
| AVSS | 22 | — | Negative power terminal for analog circuit | |
| DA0 | 23 | Output | DA0 output / general purpose I/O terminal | |
| DA1 | 24 | Output | DA1 output / general purpose I/O terminal | |
| $\overline{\text{VS}}$ | 25 | Input | Vertical synchronization signal input terminal | |
| $\overline{\text{HS}}$ | 26 | Input | Horizontal synchronization signal input terminal | |
| R | 27 | Output | Red (R) output terminal of RGB image output | |
| G | 28 | Output | Green (G) output terminal of RGB image output | |
| B | 29 | Output | Blue (B) output terminal of RGB image output | |
| BL | 30 | Output | Fast blanking control signal<br>Switch TV image signal and OSD image signal | |
| PWM0 to PWM9 | 31 to 40 | Output | PWM0 to 9 output terminal<br>15 V withstand | |
| Port 0<br>P00 to P07 | 45 to 52 | I/O | 8-bit Input/output port<br>Input/output can be specified in nibble units<br>HOLD release input<br>Interrupt input | Pull-up resistor provided/ not provided (in bit units)<br>Output format CMOS/Nch-OD (in bit units) |
| Port 1<br>P10 to P17 | 1 to 8 | I/O | 8-bit Input/output port<br>Input/output can be specified in bit units<br>Other functions<br><br>P10: SIO0 data output<br>P11: SIO0 data input / bus input / output<br>P12: SIO0 clock input / output | Output format CMOS/Nch-OD (in bit units) |
| Port 7<br>P70<br>P71 to P73 | 41<br>42 to 44 | I/O<br>Input | 4-bit input port<br>Other functions<br><br>P70: INT0 input / HOLD release input / Nch-transistor output for watchdog timer<br>P71: INT1 input / HOLD release input<br>P72: INT2 input / timer 0 event input<br>P73: INT3 input (noise rejection filter attached input) / timer 0 event input<br><br>Interrupt receiver format vector address | Pull-up resistor provided/ not provided (in bit units) |
| Port 9<br>P90 to P93 | 13 to 16 | Input | 4-bit input port<br>Other function<br>A/D converter input port (4 lines) | |

Interrupt receiver format vector address

| | Rising | Falling | Rising / Falling | H level | L level | Vector |
|---|---|---|---|---|---|---|
| INT0 | enable | enable | disable | enable | enable | 03H |
| INT1 | enable | enable | disable | enable | enable | 0BH |
| INT2 | enable | enable | enable | disable | disable | 13H |
| INT3 | enable | enable | enable | disable | disable | 1BH |

- Any port option can be selected in bit units.
- Port 0 portion        : Pull-up resistor is provided when CMOS output is selected.
                          The pull-up resister is not provided when N-ch Open Drain is selected.
- Port 1 option         : Programmable pull-up resister is provided when any output form is selected.

- Port status during reset

| Terminal | I/O | Pull-up resistor status at selecting pull-up option |
|----------|-----|----------------------------------------------------|
| Port 0 | Input | Pull-up resistor OFF, ON after reset release |
| Port 1 | Input | Programmable pull-up resistor OFF |
| Port 7 | Input | Fixed pull-up resistor provided |

* AVDD and AVSS are the power terminals for built-in analog circuit. DVDD and DVSS are the power  terminals for built-in digital circuit. Connect them like the following figure to reduce the mutual noise influence.
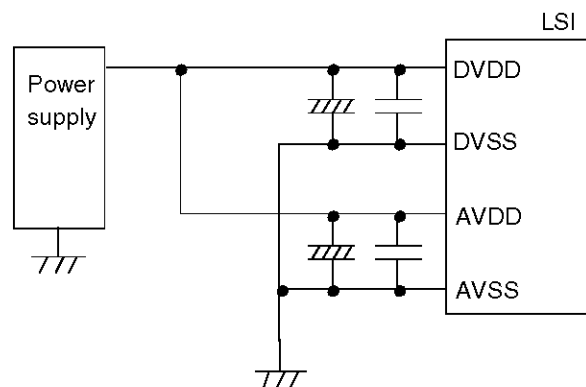
# Specifications

## 1. Absolute Maximum Ratings at Ta = 25°C, V$_{SS}$ = 0 V

| Parameter | | Symbol | Pins | Conditions | V$_{DD}$ [V] | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply voltage | | V$_{DD}$ max | DVDD, AVDD | DVDD = AVDD | | −0.3 | | +7.0 | V |
| Input voltage | | V$_I$(1) | • P71, 72, 73<br>• Port 9<br>• $\overline{RES}$, $\overline{HS}$, $\overline{VS}$ | | | −0.3 | | V$_{DD}$+0.3 | |
| Output voltage | | V$_O$(1) | R, G, B, BL, FILT | | | −0.3 | | V$_{DD}$+0.3 | |
| | | V$_O$(2) | PWM0 to PWM9 | | | −0.3 | | +15 | |
| Input/output voltage | | V$_{IO}$(1) | Ports 0, 1, P70 DA0, 1 | | | −0.3 | | V$_{DD}$+0.3 | |
| High-level output current | Peak output current | I$_{OPH}$(1) | Ports 0, 1 | • Pull-up MOS transistor output<br>• At each pin | | −2 | | | mA |
| | | I$_{OPH}$(2) | Ports 0, 1 DA0, 1 | • CMOS output<br>• At each pin | | −4 | | | |
| | | I$_{OPH}$(3) | R, G, B, BL | • CMOS output<br>• At each pin | | −5 | | | |
| | Total output current | ΣI$_{OAH}$(1) | Port 1 | The total of all pins | | −10 | | | |
| | | ΣI$_{OAH}$(2) | Port 0 | The total of all pins | | −10 | | | |
| | | ΣI$_{OAH}$(3) | R, G, B, BL | The total of all pins | | −15 | | | |
| Low-level output current | Peak output current | I$_{OPL}$(1) | Ports 0, 1 DA0, 1 | At each pin | | | | 20 | |
| | | I$_{OPL}$(2) | P70 | At each pin | | | | 30 | |
| | | I$_{OPL}$(3) | • R, G, B, BL<br>• PWM0 to PWM9 | At each pin | | | | 5 | |
| | Total output current | ΣI$_{OAL}$(1) | Port 0 | The total of all pins | | | | 40 | |
| | | ΣI$_{OAL}$(2) | Port 1, P70 | The total of all pins | | | | 40 | |
| | | ΣI$_{OAL}$(3) | R, G, B, BL | The total of all pins | | | | 15 | |
| | | ΣI$_{OAL}$(4) | PWM0 to PWM9 | The total of all pins | | | | 30 | |
| Maximum power dissipation | | Pd max | DIP52S | Ta = −30 to +70°C | | | | 430 | mW |
| Operating temperature range | | Topr | | | | −30 | | +70 | °C |
| Storage temperature range | | Tstg | | | | −55 | | +150 | |

* DVSS and AVSS must be supplied the same voltage, V$_{SS}$.    V$_{SS}$ = DVSS = AVSS
  DVDD and AVDD must be supplied the same voltage, V$_{DD}$.    V$_{DD}$ = DVDD = AVDD

## 2. Recommended Operating Range at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | $V_{DD}$ [V] | Ratings min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Operating voltage range | $V_{DD}$ | DVDD, AVDD | 0.98 μs ≤ tCYC tCYC ≤ 1.02 μs | | 4.5 | | 5.5 | V |
| Hold voltage | $V_{HD}$ | DVDD, AVDD | RAMs and the registers hold data at HOLD mode. | | 2.0 | | 5.5 | |
| Input high voltage | $V_{IH}(1)$ | Port 0  (Schmitt) | Output disable | 4.5 to 5.5 | $0.6V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}(2)$ | • Port 1  (Schmitt) • P72, 73 • $\overline{HS}$, $\overline{VS}$ | Output disable | 4.5 to 5.5 | $0.75V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}(3)$ | • P70 port input / interrupt • P71 • $\overline{RES}$  (Schmitt) | Output N-channel transistor OFF | 4.5 to 5.5 | $0.75V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}(4)$ | P70 Watchdog timer input | Output N-channel transistor OFF | 4.5 to 5.5 | $V_{DD}-0.5$ | | $V_{DD}$ | |
| | $V_{IH}(5)$ | Port 9  DA0, 1 port input | | 4.5 to 5.5 | $0.7V_{DD}$ | | $V_{DD}$ | |
| Input low voltage | $V_{IL}(1)$ | Port 0       (Schmitt) | Output disable | 4.5 to 5.5 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(2)$ | • Port 1     (Schmitt) • P72, 73 • $\overline{HS}$, $\overline{VS}$ • Port 9 | Output disable | 4.5 to 5.5 | $V_{SS}$ | | $0.25V_{DD}$ | |
| | $V_{IL}(3)$ | • P70 port input / interrupt • P71 • $\overline{RES}$       (Schmitt) | N-channel transistor OFF | 4.5 to 5.5 | $V_{SS}$ | | $0.25V_{DD}$ | |
| | $V_{IL}(4)$ | P70 Watchdog timer input | N-channel transistor OFF | 4.5 to 5.5 | $V_{SS}$ | | $0.6V_{DD}$ | |
| | $V_{IL}(5)$ | Port 9 DA0, 1 port input | | 4.5 to 5.5 | $V_{SS}$ | | $0.3V_{DD}$ | |
| Operation cycle time | tCYC(1) | | OSD function | 4.5 to 5.5 | 0.98 | 1 | 1.02 | μs |
| | tCYC(2) | | Except OSD function | 4.5 to 5.5 | 0.98 | | 30 | |

| Parameter | Symbol | Pins | Conditions | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | V$_{DD}$ [V] | min | typ | max | |
| Oscillation frequency range (Note 1) | FmCF | CF1, CF2 | 12 MHz (ceramic resonator oscillation) Refer to Figure 1. | 4.5 to 5.5 | 11.76 | 12 | 12.24 | MHz |
| | FmLC | LC1, LC2 | 14.11 MHz (LC oscillation) Refer to Figure 2. | 4.5 to 5.5 | | 14.11 | | |
| | FmRC | | RC oscillation | 4.5 to 5.5 | 0.4 | 0.8 | 2.0 | |
| Oscillation stable time period (Note 2) | tmsCF | CF1, CF2 | 12 MHz (ceramic resonator oscillation) Refer to Figure 3. | 4.5 to 5.5 | | 0.02 | 0.2 | ms |

Note 1 : Refer to Table 1 and Table 2 for the oscillation constant.

Note 2 : The oscillation stable time is a period necessary for the oscillation to be stable after the power first applied, the HOLD mode released and the main-clock oscillation stop instruction released.
Refer to the Figure 3 for details.

## 3. Electrical Characteristics at Ta = –30°C to +70°C , $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | $V_{DD}$[V] | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Ratings | | |
| Input high-level current | $I_{IH}(1)$ | • Port 1   DA0, 1<br>• Port 0 without pull-up MOS transistor. | • Output disable<br>• Pull-up MOS transistor OFF<br>• $V_{IN} = V_{DD}$<br>(including the off-leak current of the output transistor) | 4.5 to 5.5 | | | 1 | µA |
| | $I_{IH}(2)$ | • Port 7 without pull-up MOS transistor.<br>• Port 9<br>• $\overline{RES}$<br>• $\overline{HS}$, $\overline{VS}$ | $V_{IN} = V_{DD}$ | 4.5 to 5.5 | | | 1 | |
| Input low-level current | $I_{IL}(1)$ | • Port 1   DA0, 1<br>• Port 0 without pull-up MOS transistor. | • Output disable<br>• Pull-up MOS transistor OFF<br>• $V_{IN} = V_{SS}$<br>(including the off-leak current of the output transistor) | 4.5 to 5.5 | –1 | | | |
| | $I_{IL}(2)$ | • Port 7 without pull-up MOS transistor.<br>• Port 9 | $V_{IN} = V_{SS}$ | 4.5 to 5.5 | –1 | | | |
| | $I_{IL}(3)$ | • $\overline{RES}$<br>• $\overline{HS}$, $\overline{VS}$ | $V_{IN} = V_{SS}$ | 4.5 to 5.5 | –1 | | | |
| Output high-level voltage | $V_{OH}(1)$ | CMOS output of ports 0, 1   DA0, 1 | $I_{OH} = –1.0$ mA | 4.5 to 5.5 | $V_{DD}–1$ | | | V |
| | $V_{OH}(2)$ | R, G, B, BL | $I_{OH} = –0.1$ mA | 4.5 to 5.5 | $V_{DD}–0.5$ | | | |
| Output low-level voltage | $V_{OL}(1)$ | Ports 0,1 | $I_{OL} = 10$ mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(2)$ | Ports 0,1   DA0,1 | • $I_{OL} = 1.6$ mA<br>• The total current of the ports 0, 1 is 40 mA or less. | 4.5 to 5.5 | | | 0.4 | |
| | $V_{OL}(3)$ | • R, G, B, BL<br>• PWM0 to PWM9 | • $I_{OL} = 3.0$ mA<br>• The current of any unmeasured pin is 3 mA or less. | 4.5 to 5.5 | | | 0.4 | |
| | $V_{OL}(4)$ | P70 | $I_{OL} = 1$ mA | 4.5 to 5.5 | | | 0.4 | |
| Pull-up MOS transistor resistance | Rpu | • Ports 0, 1<br>• Port 7 | $V_{OH} = 0.9V_{DD}$ | 4.5 to 5.5 | 13 | 38 | 80 | kΩ |
| Output off-leakage current | $I_{OFF}$ | PWM0 to PWM9 | $V_{OUT} = 13.5$ V | 4.5 to 5.5 | | | 5 | µA |
| Hysteresis voltage | $V_{HIS}$ | • Ports 0, 1<br>• Port 7<br>• $\overline{RES}$<br>• $\overline{HS}$, $\overline{VS}$ | Output disable | 4.5 to 5.5 | | $0.1V_{DD}$ | | V |
| Pin capacitance | CP | All pins | • $f = 1$ MHz<br>• Unmeasured input pins are set to $V_{SS}$ level.<br>• $Ta = 25°C$ | 4.5 to 5.5 | | 10 | | pF |

## 4. Serial Input/Output Characteristics at Ta = –30°C to +70°C , $V_{SS}$ = 0 V

| Parameter | | | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$ [V] | min | typ | max | |
| Serial clock | Input clock | Cycle | tCKCY(1) | • SCK0 • SCLK0 | Refer to Figure 5. | 4.5 to 5.5 | 2 | | | tCYC |
| | | Low-level pulse width | tCKL(1) | | | 4.5 to 5.5 | 1 | | | |
| | | High-level pulse width | tCKH(1) | | | 4.5 to 5.5 | 1 | | | |
| | Output clock | Cycle | tCKCY(2) | • SCK0 • SCLK0 | • Use a pull-up resistor (1 kΩ) during open drain output. • Refer to Figure 5. | 4.5 to 5.5 | 2 | | | |
| | | Low-level pulse width | tCKL(2) | | | 4.5 to 5.5 | | 1/2tCKCY | | |
| | | High-level pulse width | tCKH(2) | | | 4.5 to 5.5 | | 1/2tCKCY | | |
| Serial input | Data set-up time | | tICK | SI0 | • Data set-up to SCK0 rising • Data hold from SCK0 rising • Refer to Figure 5. | 4.5 to 5.5 | 0.1 | | | µs |
| | Data hold time | | tCKI | | | 4.5 to 5.5 | 0.1 | | | |
| Serial output | Output delay time (Serial clock is external clock) | | tCKO(1) | SO0 | • Use a pull-up resistor (1kΩ) during open drain output. • Data set-up to SCK0 falling • Data hold from SCK0 falling • Refer to Figure 5. | 4.5 to 5.5 | | | 7/12tCYC +0.2 | µs |
| | Output delay time (Serial clock is internal clock) | | tCKO(2) | | | 4.5 to 5.5 | | | 1/3tCYC +0.2 | |

## 5. Pulse Input Conditions at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| High/low-level pulse width | tPIH(1) tPIL(1) | • INT0,INT1 • INT2/T0IN | • Interrupt acceptable • Timer0-countable | 4.5 to 5.5 | 1 | | | tCYC |
| | tPIH(2) tPIL(2) | INT3/T0IN (The noise rejection clock is set to 1/1) | • Interrupt acceptable • Timer0-countable | 4.5 to 5.5 | 2 | | | |
| | tPIH(3) tPIL(3) | INT3/T0IN (The noise rejection clock is set to 1/16) | • Interrupt acceptable • Timer0-countable | 4.5 to 5.5 | 32 | | | |
| | tPIL(4) | $\overline{RES}$ | Reset acceptable | 4.5 to 5.5 | 200 | | | μs |
| | tPIH(5) tPIL(5) | $\overline{HS}$, $\overline{VS}$ | Display position controllable Each active edge of $\overline{HS}$, $\overline{VS}$ must be more than 1tCYC. Refer to Figure 7. | 4.5 to 5.5 | 10 | | | tCYC |
| Rising/falling time | tTHL tTLH | $\overline{HS}$ | Refer to Figure 7. | 4.5 to 5.5 | | | 500 | ns |
| Horizontal pull-in range | FH | $\overline{HS}$ | The monitor point in Figure 10 is 1/2 $V_{DD}$. | 4.5 to 5.5 | 15.23 | 15.73 | 16.23 | kHz |

## 6. A/D Converter Characteristics  at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Resolution | N | | | 4.5 to 5.5 | | 4 | | bit |
| Absolute precision | ET | | (Note 3) | 4.5 to 5.5 | | ±1/4 | ±1/2 | LSB |
| Conversion time | tCAD | From Vref selection to when the result is produced | 1 bit conversion time = 2tCYC | 4.5 to 5.5 | | | 1.96 | μs |
| Reference current | $I_{REF}$ | | (Regulate the ladder resistor) | 4.5 to 5.5 | | 1.0 | 2.0 | mA |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN3 | | 4.5 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | $I_{AINH}$ | | $V_{AIN} = V_{DD}$ | 4.5 to 5.5 | | | 1 | μA |
| | $I_{AINL}$ | | $V_{AIN} = V_{SS}$ | 4.5 to 5.5 | –1 | | | |

Note 3 :  Absolute precision excepts quantizing error (±1/2 LSB).

## 7. D/A Converter Characteristics at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Resolution | NDA | | | 4.5 to 5.5 | | 7 | | bit |
| Absolute precision | ETDA | | 7 bits mode (Note 4) | 4.5 to 5.5 | | ±1.5 | ±3 | LSB |
| Settling time | tSDA | | (Note 5) | 4.5 to 5.5 | | 1.0 | | μs |
| Analog input voltage range | VAOUT | DA0 to DA1 | | 4.5 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Output register | RODA | | (Note 6) | 4.5 to 5.5 | 1.7 | 4 | 7 | kΩ |

Note 4 : Absolute precision excepts quantizing error (±1/2 LSB).
Note 5 : Settling time refers to the time from when the D/A conversion instruction is executed to when the analog voltage output corresponding to the digital on the specific port is generated. (No load)
Note 6 : D/A data = 80H

## 8. Current Drain Characteristics at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Current drain during basic operation (Note 7) | $I_{DDOP}(1)$ | DVDD, AVDD | • FmCF = 12 MHz Ceramic resonator oscillation<br>• FmLC = 14.11 MHz LC oscillation<br>• System clock : CF oscillation<br>• Internal RC oscillation stops | 4.5 to 5.5 | | 16 | 28 | mA |
| Current drain in HALT mode (Note 7) | $I_{DDHALT}(1)$ | DVDD, AVDD | • HALT mode<br>• FmCF = 12 MHz Ceramic resonator oscillation<br>• FmLC = 0 Hz (oscillation stops)<br>• System clock : CF oscillation<br>• Internal RC oscillation stops. | 4.5 to 5.5 | | 5 | 10 | mA |
| | $I_{DDHALT}(2)$ | DVDD, AVDD | • HALT mode<br>• FmCF = 0 MHz (oscillation stops)<br>• FmLC = 0 Hz (oscillation stops)<br>• System clock : Internal RC | 4.5 to 5.5 | | 400 | 800 | μA |
| Current drain in HOLD mode (Note 7) | $I_{DDHOLD}(1)$<br>$I_{DDHOLD}(2)$ | DVDD, AVDD | • HOLD mode<br>• All oscillation stops. | 4.5 to 5.5 | | 0.05 | 20 | μA |

Note 7 : The currents of the output transistors and the pull-up MOS transistors are ignored.

| Oscillation type | Manufacturer | Oscillator | C1 | C2 |
|---|---|---|---|---|
| 12 MHz ceramic resonator oscillation | Murata | CSA12.0MTZ | 33 pF | 33 pF |
| | | CST12.0MTW | on chip | |
| | Kyocera | KBR-12.0M | 22 pF | 22 pF |

\* Both C1 and C2 must use a K rank ($\pm$10%) and SL characteristics.

**Table 1.  Ceramic Resonator Oscillation Guaranteed Constant (main-clock)**

| Oscillation type | L | C3 | C4 |
|---|---|---|---|
| 14.11 MHz LC oscillation | 4.7 $\mu$H | 33 pF | 45 pF (Trimmer) |
| | 4.7 $\mu$H$\pm$10% (Variable) | 33 pF | 33 pF |

\* See Figures 10 and 11 for the oscillation frequency.

**Table 2.  LC Oscillation Guaranteed Constant (OSD clock)**

(Notes)  • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
  • If you use other oscillators herein, we provide no guarantee for the characteristics.
  • Adjust the voltage of monitor point in Figure 10 to 1/2$V_{DD}\pm$10% by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.
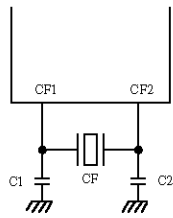


main clock

**Figure 1  Ceramic Resonator Oscillation**
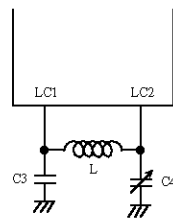
OSD clock

**Figure 2  LC Resonator Oscillation**

Power supply

VDD
VDD lower limit
0V

Reset time

$\overline{\text{RES}}$

Internal RC
resonator
oscillation

tmsCF

CF1, CF2

Operation mode | Unfixed | Reset | Instruction execution mode

< Reset time and oscillation stable time. >

HOLD release signal | Valid

Internal RC
resonator
oscillation

tmsCF

CF1, CF2

Operation mode | HOLD | Instruction execution mode

< HOLD release signal and oscillation stable time. >

**Figure 3  Oscillation Stable Time**

VDD

RRES

$\overline{\text{RES}}$

CRES    (Note) Set the values of CRES, RRES so that
the reset time is 200 μs or longer.

**Figure 4  Reset Circuit**

$$0.5\ V_{DD}$$

< AC timing point >



< Timing >

< Test load >
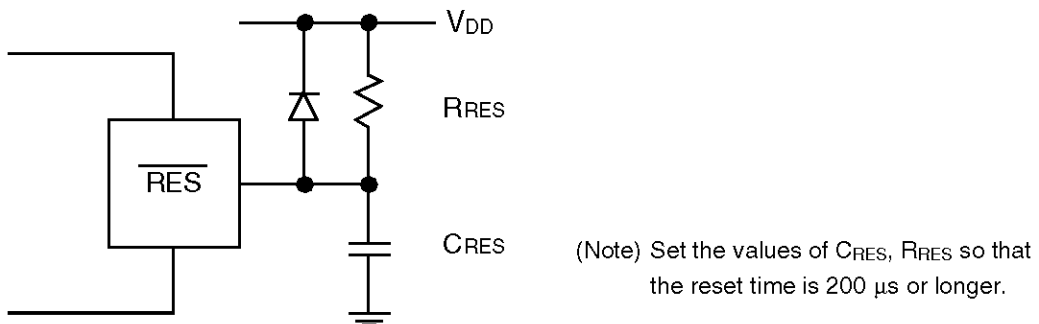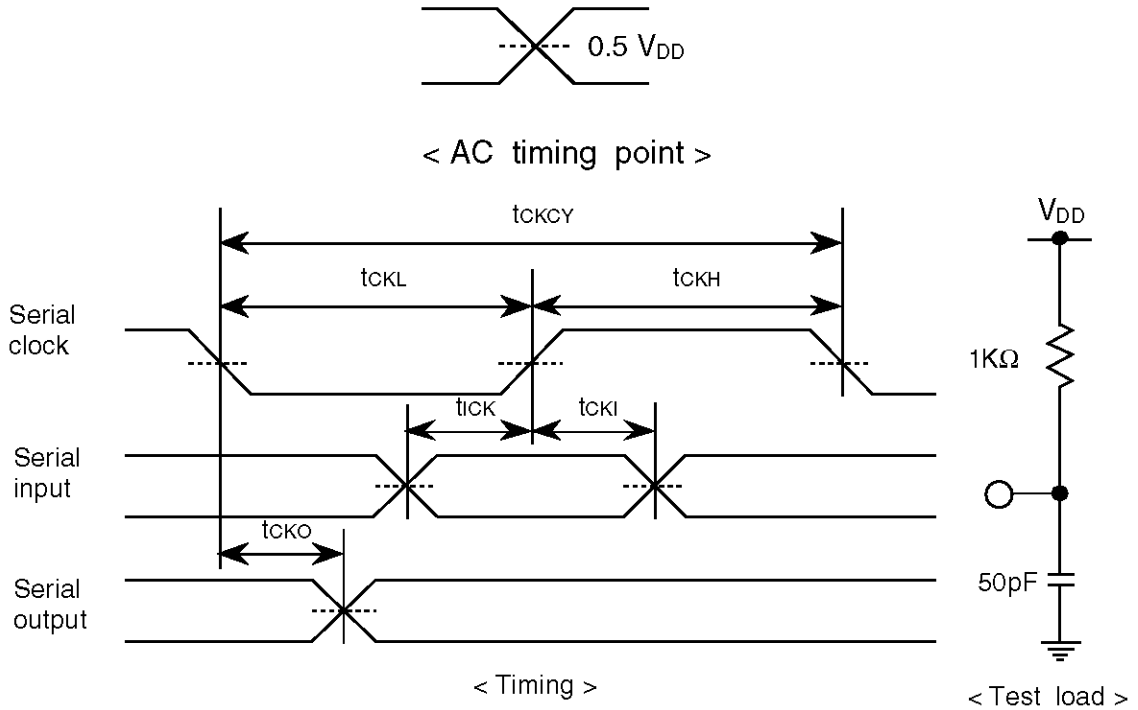
**Figure 5  Serial Input/output Test Condition**
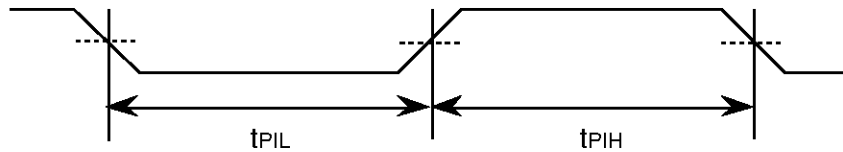


**Figure 6  Pulse Input Timing Condition - 1**



(a)  In case of active low

(b)  In case of active high
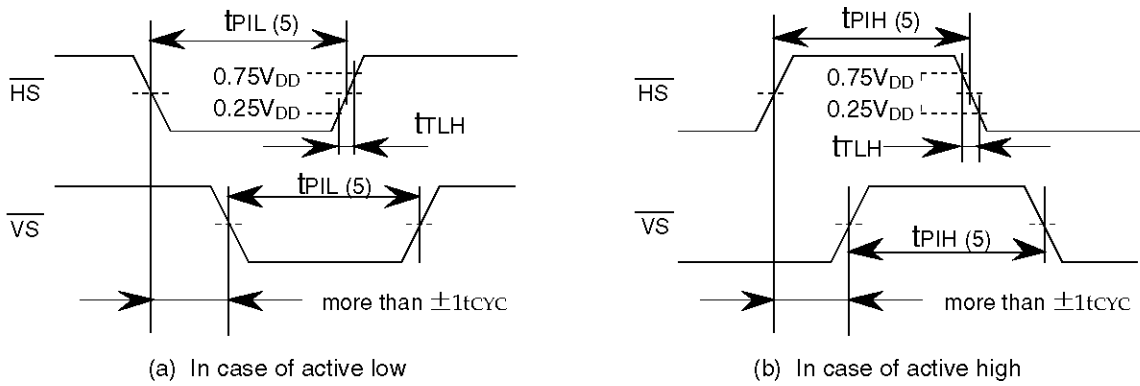
**Figure 7  Pulse Input Timing Condition - 2**
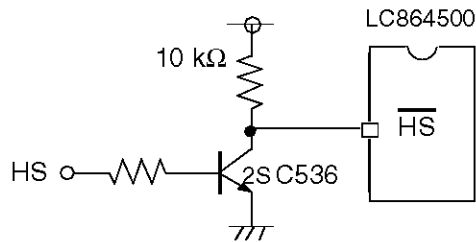


**Figure 8  Recommended Interface Circuit**
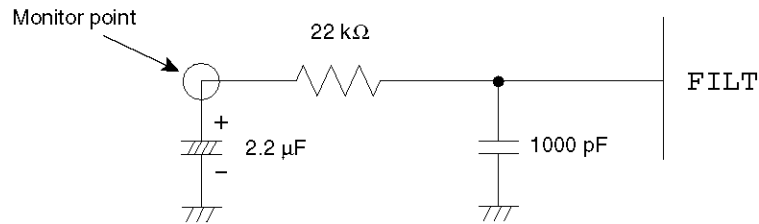
**Figure 9  FILT Recommended Circuit**

(Note)  • Place the parts connected to the FILT terminal as close to the FILT as possible with the shortest pattern length on the board.
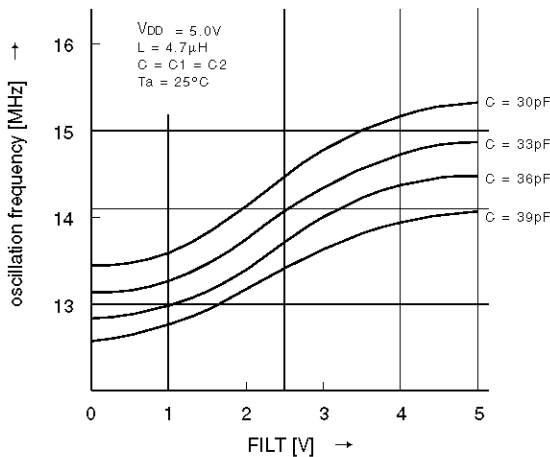


**Figure 10  FILT-LC Oscillation Frequency (1)**
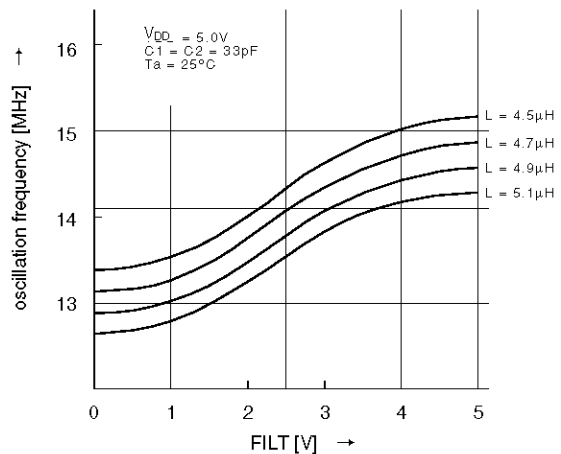


**Figure 11  FILT-LC Oscillation Frequency (2)**

This catalog provides information as of February, 1998. Specifications and information herein are subject to change without notice.