Ordering number: EN4214

CMOS LSI

SANYO No.4214

LC866232A/28A/24A/20A/16A

8-Bit Single Chip Microcomputer

LC866232A	On-chip 32K Bytes ROM and On-chip 640 Bytes 8-Bit Single Chip Microcomputer
LC866228A	On-chip 28K Bytes ROM and On-chip 640 Bytes 8-Bit Single Chip Microcomputer
LC866224A	On-chip 24K Bytes ROM and On-chip 640 Bytes 8-Bit Single Chip Microcomputer
LC866220A	On-chip 20K Bytes ROM and On-chip 640 Bytes 8-Bit Single Chip Microcomputer
LC866216A	On-chip 16K Bytes ROM and On-chip 640 Bytes 8-Bit Single Chip Microcomputer

Overview

The LC866232A/28A/24A/20A/16A microcomputers are 8-bit single chip microcomputers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.5 μs (microsecond)
- On-chip ROM Maximum Capacity : 32K bytes
- On-chip RAM Capacity : 640 bytes
- VFD automatic display controller/driver
- 16-bit timer/counter
- 16-bit timer/PWM
- 8-bit PWM
- 8-channel 8-bit AD converter
- Two 8-bit synchronous serial-interface circuits
- 14-source 10-level vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Read-Only Memory (ROM) :

LC866232A	32512 x 8 bits
LC866228A	28672 x 8 bits
LC866224A	24576 x 8 bits
LC866220A	20480 x 8 bits
LC866216A	16384 x 8 bits

(2) Random Access Memory (RAM) : 640 x 8 bits

(3) Minimum bus cycle time : 0.5 μs (using 12MHz CF resonator oscillation)
Bus cycle time means ROM-read period.

(4) Minimum instruction cycle time : 1 μs (using 12MHz CF resonator oscillation)
ROM data is accessed twice in a instruction cycle time.
The operation of the microcomputers herein is about 1.7 times (0.6 μs) that of LC66000 series, our products in the same specified cycle time.

(5) Ports :

- Input/output ports	: 6 ports	(43 terminals).
Input/output port programmable in nibble units	: 1 port	(8 terminals).
Input/output port programmable in a bit	: 5 ports	(35 terminals).
- Input ports	: 2 ports	(12 port pins).

- VFD output ports : 32 terminals.
- Large current output for digit : 16 terminals.
- Pull-down resistor option available.

(6) VFD automatic display controller
- Segment/digit output pattern programmable.
  Any segment/digit combination available.
  VFD parallel-drive available.
- 16-step dimmer function available.

(7) AD converter
- 8-channel 8-bit AD converter.

(8) Serial-interface
- 2-channel 8-bit serial-interface.
  LSB first / MSB first function available.
- Internal 8-bit baud-rate generator in common with two serial-interface circuits.

(9) 8-bit PWM output
- PWM output terminal.
- Static output available.

(10) Timer
- Timer 0
  16-bit timer/counter.
  2-bit prescaler + 8-bit programmable prescaler .
  Mode 0 : Two 8-bit timers with programmable prescaler.
  Mode 1 : 8-bit timer + 8-bit counter with programmable prescaler.
  Mode 2 : 16-bit timer with programmable prescaler.
  Mode 3 : 16-bit counter.
  Resolution of Timer is Tcyc. (Tcyc : cycle time)
- Timer 1
  16-bit timer/PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9～16 bits)
  In Mode 0 and Mode 1, resolution of Timer and PWM is Tcyc.
  In Mode 2 and Mode 3, resolution of Timer and PWM selectable : Tcyc or 1/2 Tcyc by program.
- Base timer
  Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock).
  Every 976 μ s , 3.9ms , 15.6ms , 62.5ms overflow system (using 32.768kHz crystal oscillation for Base timer clock).
  The Base timer clock selectable; 32.768kHz crystal oscillation, System clock, and Programmable prescaler output of Timer 0.

(11) Buzzer output
- The Buzzer sound frequency selectable; 4KHz, 2KHz (using 32.768kHz crystal oscillation for Base timer clock).

(12) Remote-control receiver (using INT3/P73 terminals)
- Noise rejection available.
- The interrupt polarity selectable.

(13) Watchdog timer
- The watchdog timer is taken on RC outside.
- Watchdog timer operation selectable : interrupt system , system reset.

(14) Interrupt system

- 14-source 10-level vectored interrupts :
  1. External interrupt INT0 (includes watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2 , timer T0L
  4. External interrupt INT3 , base timer
  5. Timer/counter T0H
  6. Timer T1L , timer T1H
  7. Serial-interface SIO0
  8. Serial-interface SIO1
  9. AD converter
  10. VFD display controller , port 0
- Interrupt Priority control available

Interrupt Priority control register included.

These microcomputers are available to 3-level interrupt : low-level, high-level and highest-level.

It is available to assign the priority (low-level or high-level) of the eight interruptions : number 3 to 10 above.

And it is available to assign the priority (low-level or highest-level) of the two interruptions : number 1,2 above.

(15) Real-time service operation

The Real-Time Service (RTS) functions the data-transfer between the Special Function Registers at acknowledging the interrupt request.

The RTS starts within 1 cycle-time and completes within 5 cycle-times after occurring the interrupt request.

(16) Sub-routine stack levels.

- 128 levels (Max.) : Stack area included in the RAM area.

(17) Multiplication and division

16-bit × 8-bit (7 instruction cycle times)

16-bit ／ 8-bit (7 instruction cycle times)

(18) 3 oscillation circuits

- On-chip RC oscillation circuit using for the system clock.
- On-chip CF oscillation circuit using for the system clock.
- On-chip crystal oscillation circuit using for the system clock and for time-base clock.

(19) Standby function

-HALT mode function

The HALT mode is used to reduce power dissipation. In this operation mode , program execution is stopped. This operation mode can be released by interrupt request signals or the system reset.

-HOLD mode function

The HOLD mode is used to freeze all the oscillations ; RC(internal), CF and Crystal oscillations. This mode can be released by the following operations.

·Reset terminal $\overline{\text{RES}}$ set to Low level.

·P70/INT0, P71/INT1 terminals set to assigned level (programmable).

·Port 0 terminal/terminals set to Low level (programmable).

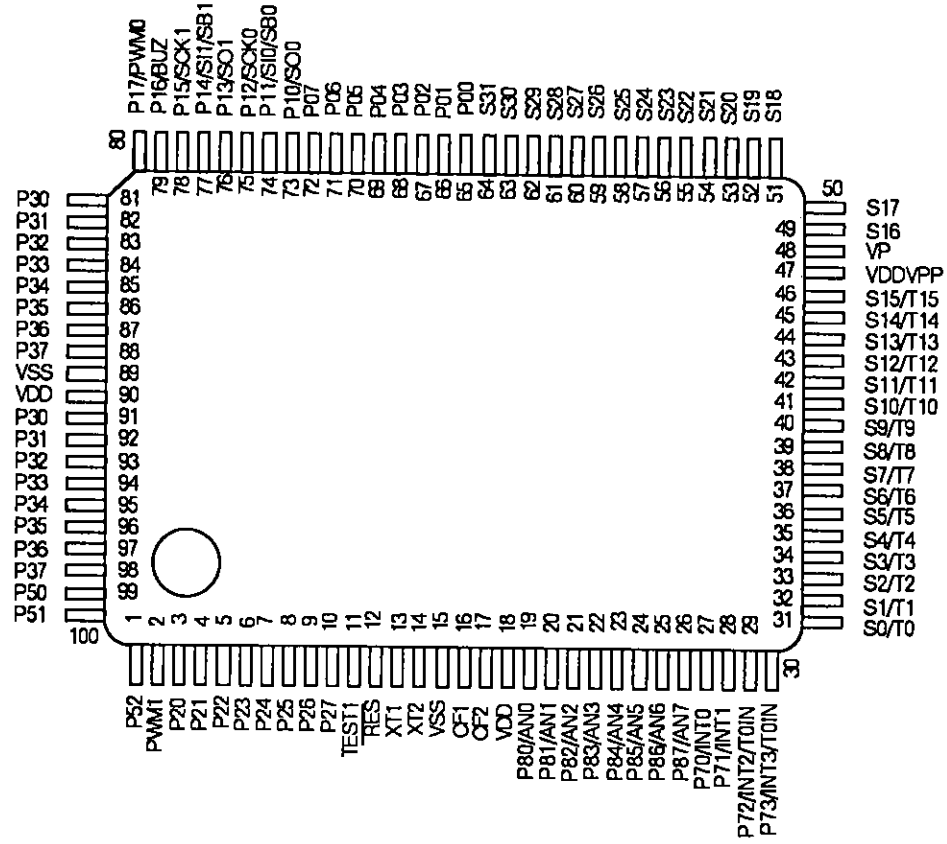
(20) Factory shipment

QFP 100E delivery form

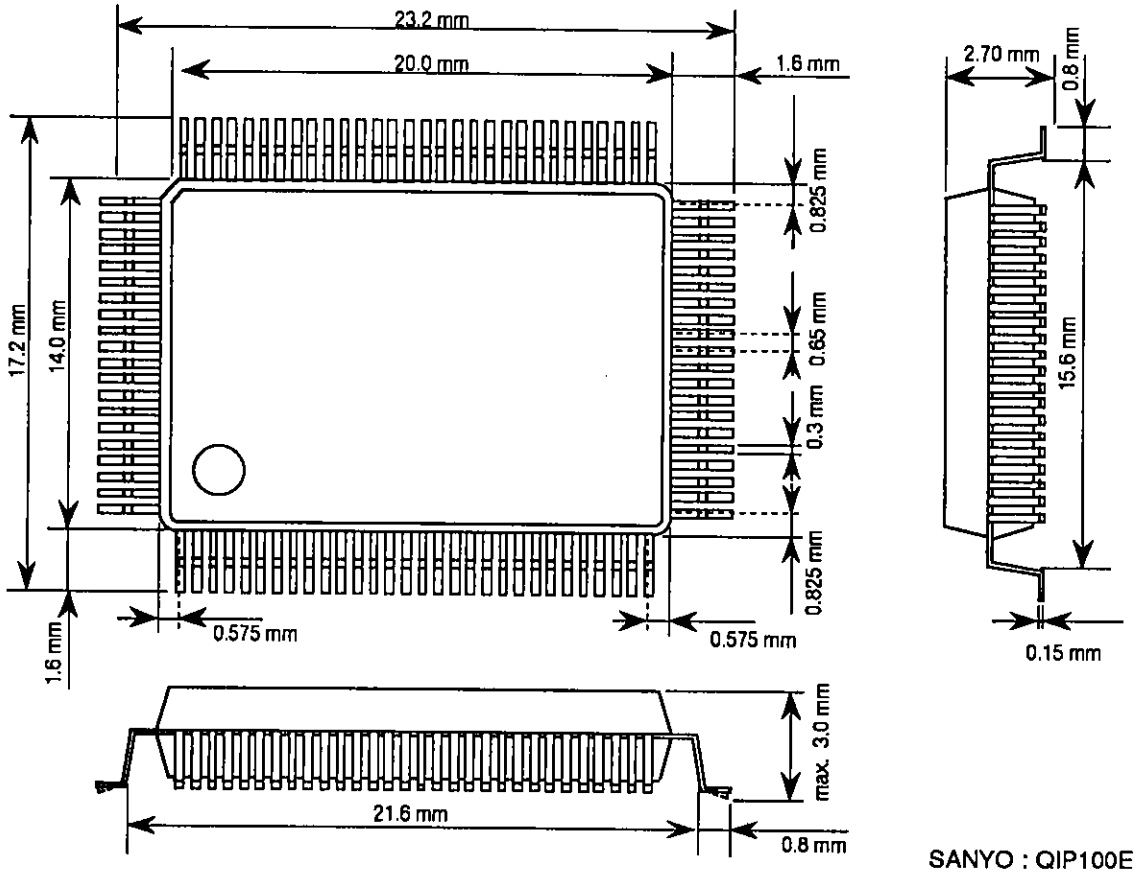
(21) Development support tools

Evaluation (EVA) chip	:	LC866099
EPROM version	:	LC86E6232
One time version	:	LC86P6232
Emulator	:	EVA-86000 + ECB866000(Evaluation chip board) + POD866200(POD)

Pin Assignment

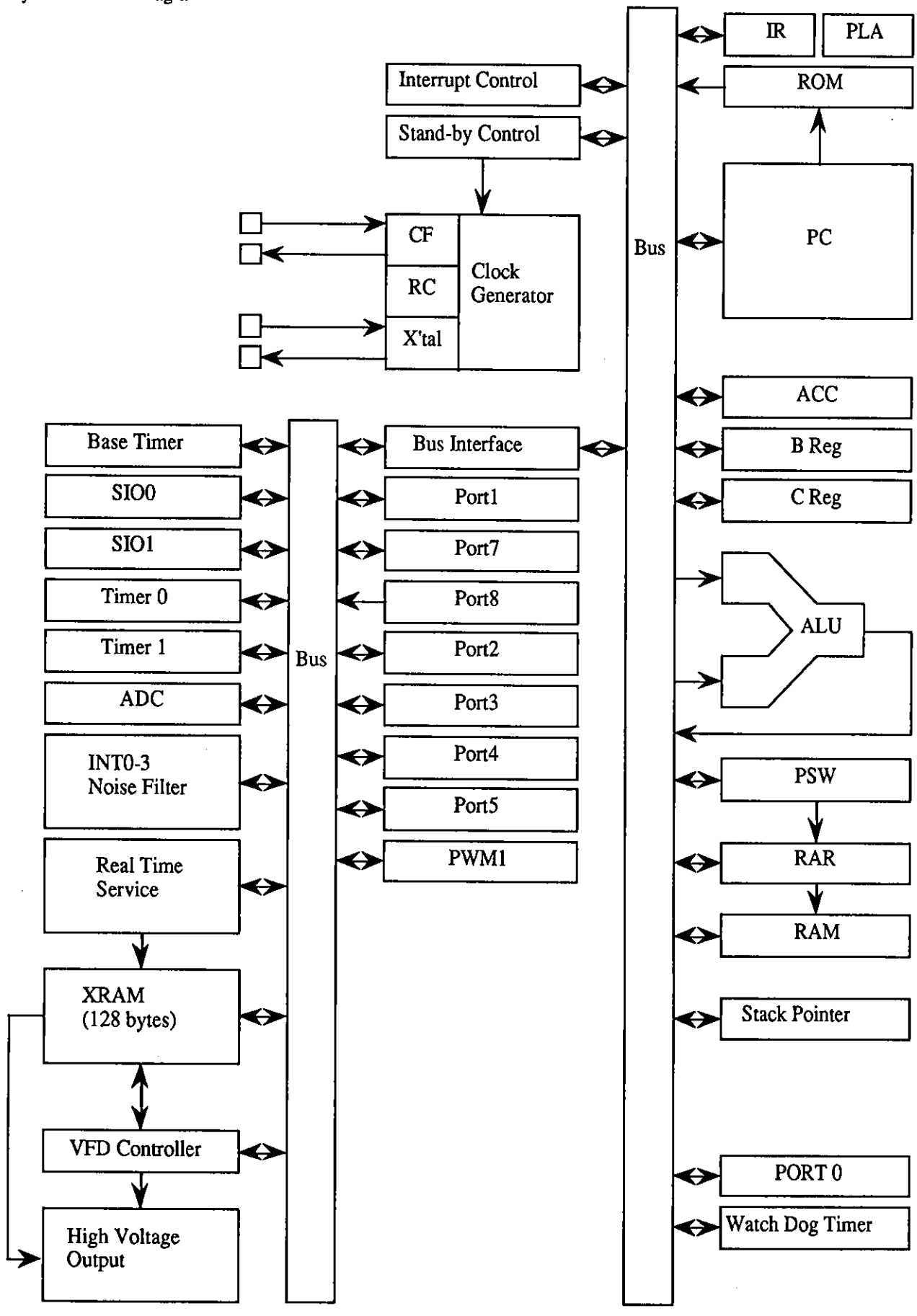


Package Dimensions 3151



SANYO : QIP100E

System Block Diagram



LC866232A/28A/24A/20A/16A Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS</td><td></td><td>Power pin(-).</td><td></td></tr>
<tr><td>VDD</td><td></td><td>Power pin(+).</td><td></td></tr>
<tr><td>VP</td><td></td><td>Power pin(-) for VFD output pulldown resistor</td><td></td></tr>
<tr><td>VDDVPP</td><td></td><td>Power pin(+).</td><td></td></tr>
<tr><td>PORT0
P00～P07</td><td>I/O</td><td>·8-bit input/output port .
·Input for port 0 interrupt.
·Input/output in nibble units.
·Input for HOLD release.</td><td>·Pullup resistor :
Provided / Not provided.
·Output form : CMOS/N-channel
open drain.</td></tr>
<tr><td>PORT1
P10～P17</td><td>I/O</td><td>·8-bit input/output port.
·Input/output can be specified in bit unit.
·Other pin functions
P10 : SIO0 data output
P11 : SIO0 data input / bus input/output
P12 : SIO0 clock input/output
P13 : SIO1 data output
P14 : SIO1 data input / bus input/output
P15 : SIO1 clock input/output
P16 : Buzzer output
P17 : Timer 1 output (PWM output)</td><td>Output form : CMOS/N-channel
open drain.</td></tr>
<tr><td>PORT2
P20～27</td><td>I/O</td><td>·8-bit input/output port.
·Input/output can be specified in bit unit.</td><td>Output form : CMOS/N-channel
open drain.</td></tr>
<tr><td>PORT3
P30～P37</td><td>I/O</td><td>·8-bit input/output port.
·Input/output can be specified in bit unit.
·15V withstand voltage at N-channel open drain output.</td><td>·Pullup resistor :
Provided / Not provided.
·Output form : CMOS/N-channel
open drain.</td></tr>
<tr><td>PORT4
P40～P47</td><td>I/O</td><td>·8-bit input/output port.
·Input/output can be specified in bit unit.
·15V withstand voltage at N-channel open drain output.</td><td>·Pullup resistor :
Provided / Not provided.
·Output form : CMOS/N-channel
open drain.</td></tr>
<tr><td>PORT5
P50～P52</td><td>I/O</td><td>·3-bit input/output port.
·Input/output can be specified in bit unit.
·15V withstand voltage at N-channel open drain output.</td><td>·Pullup resistor :
Provided / Not provided.
·Output form : CMOS/N-channel
open drain.</td></tr>
<tr><td>PORT7

P70

P71～P73</td><td>

I/O

I</td><td>·4-bit input port.
·Other functions.
P70 : INT0 input/HOLD release input/N-channel Tr.
output for watchdogtimer.
P71 : INT1 input/HOLD release input.
P72 : INT2 input/timer 0 event input.
P73 : INT3 input with noise filter/timer 0 event input.
·Interrupt received form , vector address.
<table>
<tr><th></th><th>Leading</th><th>Trailing</th><th>Leading & Trailing</th><th>HIGH Level</th><th>LOW Level</th><th>VECTOR</th></tr>
<tr><td>INT0</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td><td>03H</td></tr>
<tr><td>INT1</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td><td>0BH</td></tr>
<tr><td>INT2</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td><td>13H</td></tr>
<tr><td>INT3</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td><td>1BH</td></tr>
</table></td><td>Pullup resistor :
Provided / Not provided.</td></tr>
</table>

Pin name	I/O	Function description	Option
PORT8 P80～P87	I	·8-bit input port. ·Other functions. AD input port (8 port pins)	
PWM 1	O	8-bit PWM output terminal (CMOS).	
S0/T0～ S6/T6	O	Output for VFD display controller segment/timing in common.	Pulldown resistor : Provided / Not provided. (Usable for static output port at pulldown resistor Not provided.)
S7/T7～ S15/T15	O	Output for VFD display controller segment/timing with internal pulldown resistor in common.	
S16～S31	O	Output for VFD display controller segment.	Pulldown resistor : Provided / Not provided. (Usable for static output port at pulldown resistor Not provided.)
$\overline{RES}$	I	Reset pin with pullup resistor.	
TEST1	O	Test pin. Should be left unconnected.	
XT1	I	Input pin for 32.768kHz crystal oscillation. In case of non use, connect to VDD.	
XT2	O	Output pin for 32.768kHz crystal oscillation. In case of non use, should be left unconnected.	
CF1	I	Input pin for ceramic resonator oscillation.	
CF2	O	Output pin for ceramic resonator oscillation.	

* All of port options can be specified in bit unit.
* A state of pins at reset.

Pin name	Input/output mode	A state of pullup resistor specified at pullup option
Ports 0,7	Input	Fixed pullup resistor exist
Ports 1,2	Input	Programmable pullup resistor OFF
Port 3,4,5	Input	Programmable pullup resistor OFF

Pin name	A state of P-channel transistor
S0/T0～S15/T15	P-channel transistor OFF
S16～S31	P-channel transistor OFF

1. Absolute maximum ratings / VSS = 0 V and Ta = 25℃

Parameter		Symbol	Pins	Conditions		Limits			
					VDD[v]	min.	typ.	max.	unit
Supply voltage		VDD MAX	VDD,VDDVPP	VDD=VDDVPP		-0.3	~	+7.0	V
Input voltage		VI(1)	·Ports 71,72,73 ·Port 8 ·$\overline{RES}$			-0.3	~	VDD+0.3	
		VI(2)	VP			VDD-45	~	VDD+0.3	
Output voltage		VO(1)	·S0/T0~S15/T15 ·S16~S31			VDD-45	~	VDD+0.3	
		VO(2)	PWM 1			-0.3	~	VDD+0.3	
Input/output voltage		VIO(1)	·Ports 0,1,2,70 ·Ports 3,4,5 at CMOS output option.			-0.3	~	VDD+0.3	
		VIO(2)	Ports 3,4,5 at N-ch open drain output option.			-0.3	~	15	
High Level output current	Peak output current	IOPH(1)	·Ports 0,1,2,3,4,5 ·PWM 1	CMOS output at each pins.		-4			mA
		IOPH(2)	S0/T0~S15/T15	At each pins.		-30			
		IOPH(3)	S16~S31	At each pins.		-15			
	Total output current	ΣIOAH(1)	Ports 0,1,3	The total all pins.		-25			
		ΣIOAH(2)	·Ports 2,4,5 ·PWM 1	The total all pins.		-25			
		ΣIOAH(3)	·S0/T0~S15/T15 ·S16~S31	The total all pins.		-140			
Low Level output current	Peak output current	IOPL(1)	·Ports 0,1,2,3,4,5 ·PWM 1	At each pins.				20	
		IOPL(2)	Port 70	At each pins.				15	
	Total output current	ΣIOAL(1)	Ports 0,1	The total all pins.				40	
		ΣIOAL(2)	Port 3	The total all pins.				40	
		ΣIOAL(3)	·Port 2,5,70 ·PWM 1	The total all pins.				40	
		ΣIOAL(4)	Port 4	The total all pins.				40	
Power dissipation (max.)		Pdmax	QFP100E	Ta=-30~+70℃				500	mW
Operating temperature range		Topg				-30	~	70	℃
Storage temperature range		Tstg				-65	~	150	

2. Recommended operating range / Ta =-30℃ to +70℃, VSS = 0 V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[v]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD	0.98 μs ≦ Tcyc ≦ 400 μs		4.5		6.0	V
	VDD(2)		3.9 μs ≦ Tcyc ≦ 400 μs		2.5		6.0	
HOLD voltage	VHD	VDD	RAMs and Registers hold voltage at HOLD mode.		2.0		6.0	
Pulldown voltage	VP	VP		2.5~6.0	-35		VDD	
Input high voltage	VIH(1)	Port 0 (Schmitt)	Output disable	2.5~6.0	0.4VDD +0.9		VDD	
	VIH(2)	·Port 1,2 ·Ports 72,73 ·Port 3,4,5 at CMOS output option. (Schmitt)	Output disable	2.5~6.0	0.75VDD		VDD	
	VIH(3)	Port 3,4,5 at N-ch open drain output option. (Schmitt)	Output disable	2.5~6.0	0.75VDD		13.5	
	VIH(4)	·Port 70 Port input/ interrupt. ·Port 71 ·$\overline{RES}$ (Schmitt)	Output N-channel Tr. OFF	2.5~6.0	0.75VDD		VDD	
	VIH(5)	Port 70 Watchdog timer.	Output N-channel Tr. OFF	2.5~6.0	0.9VDD		VDD	
	VIH(6)	Port 8		2.5~6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0 (Schmitt)	Output disable	2.5~6.0	VSS		0.2VDD	
	VIL(2)	·Port 1,2,3,4,5 ·Ports 72,73 (Schmitt)	Output disable	2.5~6.0	VSS		0.25VDD	
	VIL(3)	·Port 70 Port input/ interrupt. ·Port 71 ·$\overline{RES}$ (Schmitt)	N-channel Tr. OFF	2.5~6.0	VSS		0.25VDD	
	VIL(4)	Port 70 Watchdog timer.	N-channel Tr. OFF	2.5~6.0	VSS		0.8VDD -1.0	
	VIL(5)	Port 8		2.5~6.0	VSS		0.25VDD	
Operation cycle time	Tcyc			4.5~6.0	0.98		400	μs
				2.5~6.0	3.9		400	

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[v]	min.	typ.	max.	unit
Oscillation frequency range (Note 1)	FmCF(1)	CF1,CF2	·12MHz(ceramic resonator oscillation). ·Refer to figure 1	4.5～6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1,CF2	·3MHz(ceramic resonator oscillation). ·Refer to figure 1	2.5～6.0	2.94	3	3.06	
	FmRC		RC oscillation	2.5～6.0	0.4	0.8	2.0	
	FsXtal	XT1,XT2	·32.768kHz(crystal oscillation). ·Refer to figure 2	2.5～6.0		32.768		kHz
Oscillation stable time period (Note 1)	TmsCF(1)	CF1,CF2	·12MHz(ceramic resonator oscillation). ·Refer to figure 3	4.5～6.0		0.02	0.3	ms
	TmsCF(2)	CF1,CF2	·3MHz(ceramic resonator oscillation). ·Refer to figure 3	4.5～6.0		0.1	1	
				2.5～6.0		0.1	3	
	TssXtal	XT1,XT2	·32.768kHz(crystal oscillation). ·Refer to figure 3	4.5～6.0		1	1.5	s
				2.5～6.0		1	3	

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical characteristics / Ta=-30℃ to +70℃, VSS = 0 V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[v]	min.	typ.	max.	unit
Input high current	IIH(1)	Ports 3,4,5 at N-channel open drain output option.	·Output disable ·VIN=13.5V (including off-leak current of output Tr.)	2.5～6.0			5	μA
	IIH(2)	·Ports 1,2,3,4,5 ·Port 0 without pullup MOS Tr.	·Output disable ·Pullup MOS Tr. OFF. VIN=VDD (including off-leak current of output Tr.)	2.5～6.0			1	
	IIH(3)	·Port 7 without pullup MOS Tr. ·Port 8	VIN=VDD	2.5～6.0			1	
	IIH(4)	$\overline{RES}$	VIN=VDD	2.5～6.0			1	
Input low current	IIL(1)	·Port 1,2,3,4,5 ·Port 0 without pullup MOS Tr.	·Output disable. ·Pullup MOS Tr. OFF. VIN=VSS (including off-leak current of output Tr.)	2.5～6.0	-1			
	IIL(2)	·Port 7 without pullup MOS Tr. ·Port 8	VIN=VSS	2.5～6.0	-1			
	IIL(3)	$\overline{RES}$	VIN=VSS	2.5～6.0	-1			
Output high voltage	VOH(1)	·CMOS output of ports 0,1,2,3,4,5	IOH=-1.0mA	4.5～6.0	VDD-1			V
	VOH(2)	·PWM 1	IOH=-0.1mA	2.5～6.0	VDD-0.5			
	VOH(3)	S0/T0～S15/T15	IOH=-20mA	4.5～6.0	VDD-1.8			
	VOH(4)		·IOH=-1.0mA ·The current of any unmeasure-ment pin is not over 1 mA.	2.5～6.0	VDD-1			
	VOH(5)	S16～S31	IOH=-5mA	4.5～6.0	VDD-1.8			
	VOH(6)		·IOH=-1.0mA ·The current of any unmeasure-ment pin is not over 1 mA.	2.5～6.0	VDD-1			

Parameter	Symbol	Pins	Conditions	VDD[v]	Limits min.	typ.	max.	unit
Output low voltage	VOL(1)	·Ports 0,1,2,3,4,5 ·PWM 1	IOL=10mA	4.5～6.0			1.5	V
	VOL(2)		IOL=1.6mA	4.5～6.0			0.4	
	VOL(3)		·IOL=1.0mA ·The current of any unmeasure-ment pin is not over 1 mA.	2.5～6.0			0.4	
	VOL(4)	Port 70	IOL=1mA	4.5～6.0			0.4	
	VOL(5)		IOL=0.5mA	2.5～6.0			0.4	
Pullup MOS Tr. resistor	Rpu	·Ports 0,1,2,3,4,5 ·Port 7	VOH=0.9 VDD	4.5～6.0	15	40	70	kΩ
				2.5～4.5	25	60	120	
Output off-leakage current	IOFF(1)	·S0/T0～S6/T6 ·S16～S31 (Without pull down resistor.)	·Output P-channel Tr . OFF. ·VOUT=VSS	2.5～6.0	-1			μA
	IOFF(2)		·Output P-channel Tr . OFF. ·VOUT=VDD-40v	2.5～6.0	-30			
Pulldown tran-sistor resistor	Rpd	·S0/T0～S15/T15 ·S16～S31 (With pull down resistor.)	·Output P-channel Tr . OFF. ·VOUT=3 v ·Vp=-30 v	5.0	60	100	200	kΩ
Hysteresis voltage	VHIS	·Ports 0,1,2,3,4,5 ·Port 7 ·$\overline{\text{RES}}$	Output disable	2.5～6.0		0.1VDD		V
Pin capacitance	CP	All pins.	·f=1MHz ·Unmeasurement terminals for input are set to VSS level. ·Ta=25℃	2.5～6.0		10		pF

4. Serial input/output characteristics / Ta=-30℃ to +70℃, VSS = 0 V

Parameter			Symbol	Pins	Conditions	VDD[v]	Limits min.	typ.	max.	unit
Serial clock	Input clock	Cycle	TCKCY(1)	SCK0,SCK1	Refer to figure 5	2.5~6.0	2			Tcyc
		Low level pulse width	TCKL(1)			2.5~6.0	1			
		High level pulse width	TCKH(1)			2.5~6.0	1			
	Output clock	Cycle	TCKCY(2)	SCK0,SCK1	·Use pull up resistor (1kΩ) when open drain output. ·Refer to figure 5	2.5~6.0	2			
		Low level pulse width	TCKL(2)			2.5~6.0		1/2Tckcy		
		High level pulse width	TCKH(2)			2.5~6.0		1/2Tckcy		
Serial input	Data set up time		TICK	·SI0,SI1 ·SB0,SB1	·Data set-up to SCK0,1	4.5~6.0	0.1			μs
						2.5~6.0	0.4			
	Data hold time		TCKI		·Data hold from SCK0,1	4.5~6.0	0.1			
					·Refer to figure 5	2.5~6.0	0.4			
Serial output	Output delay time (Serial clock is extrnal clock)		TCKO(1)	·SO0,SO1 ·SB0,SB1	·Use pull up resistor (1kΩ) when open drain output.	4.5~6.0			7/12Tcyc +0.2	
						2.5~6.0			7/12Tcyc +1	
	Output delay time (Serial clock is internal clock)		TCKO(2)		·Data hold from SCK0,1	4.5~6.0			1/3Tcyc +0.2	
					·Refer to figure 5	2.5~6.0			1/3Tcyc +1	

5. Pulse input conditions / Ta=-30℃ to +70℃, VSS = 0 V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[v]	min.	typ.	max.	unit
High/low level pulse width	TPIH(1) TPIL(1)	·INT0,INT1 ·INT2/T0IN	·Interrupt acceptable ·Timer0-countable	2.5~6.0	1			Tcyc
	TPIH(2) TPIL(2)	INT3/T0IN (The noise rejection clock select to 1/1.)	·Interrupt acceptable ·Timer0-countable	2.5~6.0	2			
	TPIH(3) TPIL(3)	INT3/T0IN (The noise rejection clock select to 1/64.)	·Interrupt acceptable ·Timer0-countable	2.5~6.0	128			
	TPIL(4)	$\overline{RES}$	Reset acceptable	2.5~6.0	200			μs

6. A/D converter characteristics /Ta=-30℃ to +70℃, VSS = 0 V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[v]	min.	typ.	max.	unit
Resolution	N			4.5~6.0		8		bit
Absolute precision (Note 2)	ET			4.5~6.0			±1.5	LSB
Conversion time	TCAD		·AD conversion time=16×Tcyc (ADCR2=0) (Note 3)	4.5~6.0	15.68 (Tcyc= 0.98 μs)		65.28 (Tcyc= 4.08 μs)	μs
			·AD conversion time=32×Tcyc (ADCR2=1) (Note 3)		31.36 (Tcyc= 0.98 μs)		130.56 (Tcyc= 4.08 μs)	
Analog input voltage range	VAIN	AN0~AN7		4.5~6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5~6.0			1	μA
	IAINL		VAIN=VSS	4.5~6.0	-1			

(Note 2) Absolute precision excepts quantizing error(±1/2 LSB).

(Note 3) The conversion time means the time to set complete digital conversion value to register from execution of instruction to start conversion.

7.Current dissipation characteristics / Ta=-30℃ to +70℃, VSS = 0 V

Parameter	Symbol	Pins	Conditions	VDD[v]	Limits min.	typ.	max.	unit
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	·FmCF=12MHz Ceramic resonator oscillation. ·FsXtal=32.768 kHz crystal oscillation. ·System clock : CF oscillation , ·Internal RC oscillation stops.	4.5～6.0		10	20	mA
	IDDOP(2)		·FmCF=3MHz Ceramic resonator oscillation. ·FsXtal=32.768 kHz crystal oscillation. ·System clock : CF oscillation. ·Internal RC	4.5～6.0		3	7	
	IDDOP(3)		oscillation stops.	2.5～4.5		1.5	5	
	IDDOP(4)		·FmCF=0Hz (when oscillation stops). ·FsXtal=32.768 kHz crystal oscillation. ·System clock :	4.5～6.0		0.7	1.4	
	IDDOP(5)		RC oscillation.	2.5～4.5		0.4	1.5	
	IDDOP(6)		·FmCF=0Hz (when oscillation stops). ·FsXtal=32.768 kHz crystal oscillation. ·System clock : Xtal oscillation. ·Internal RC	4.5～6.0		35	90	μA
	IDDOP(7)		oscillation stops.	2.5～4.5		15	65	

Parameter	Symbol	Pins	Conditions	VDD[v]	Limits min.	typ.	max.	unit
Current dissipation HALT mode (Note 4)	IDDHALT(1)	VDD	·HALT mode ·FmCF=12MHz Ceramic resonator oscillation. ·FsXtal=32.768 kHz crystal oscillation. ·System clock : CF oscillation. ·Internal RC oscillation stops.	4.5~6.0		5	10	mA
	IDDHALT(2)		·HALT mode FmCF=3MHz Ceramic resonator oscillation. ·FsXtal=32.768 kHz crystal oscillation. ·System clock : CF oscillation. ·Internal RC oscillation stops.	4.5~6.0		1.9	4.8	
	IDDHALT(3)			2.5~4.5		0.8	2.7	
	IDDHALT(4)		·HALT mode FmCF=0Hz (when oscillation stops). ·FsXtal=32.768 kHz crystal oscillation. ·System clock : RC oscillation.	4.5~6.0		400	800	μA
	IDDHALT(5)			2.5~4.5		200	600	
	IDDHALT(6)		·HALT mode FmCF=0Hz (when oscillation stops). ·FsXtal=32.768 kHz crystal oscillation. ·System clock : Xtal oscillation. ·Internal RC oscillation stops.	4.5~6.0		20	70	
	IDDHALT(7)			2.5~4.5		8	50	
Current dissipation HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5~6.0		0.05	30	
	IDDHOLD(2)			2.5~4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up transistors are ignored.

Table 1. Ceramic resonator oscillation guaranteed constant (main-clock)

A kind of oscillation	Producer	Oscillator	C1	C2
12MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33pF	33pF
		CSA12.0MT	33pF	33pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33pF	33pF
3MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub-clock)

A kind of oscillation	Producer	Oscillator	C3	C4
32.768kHz crystal oscillation	Dai Sinku	DT-38(1TA252E00)	18pF	18pF
	Kyocera	KF-38G-13P0200	18pF	18pF

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Note) ·Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
·If you use other oscillators herein, we provide no guarantee for the characteristics.

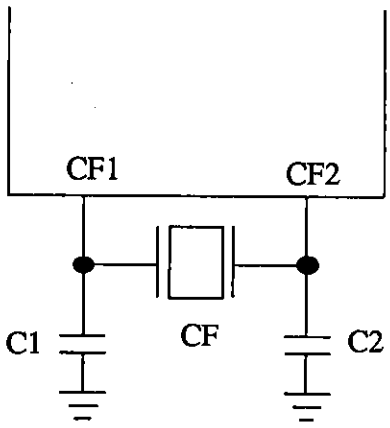
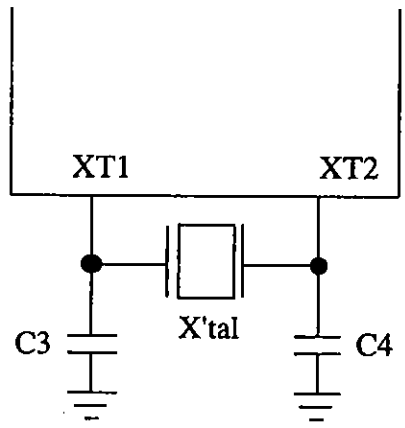


Figure 1 Main-clock circuit
Ceramic resonator oscillation



Fibure 2 Sub-clock circuit
Crystal oscillation

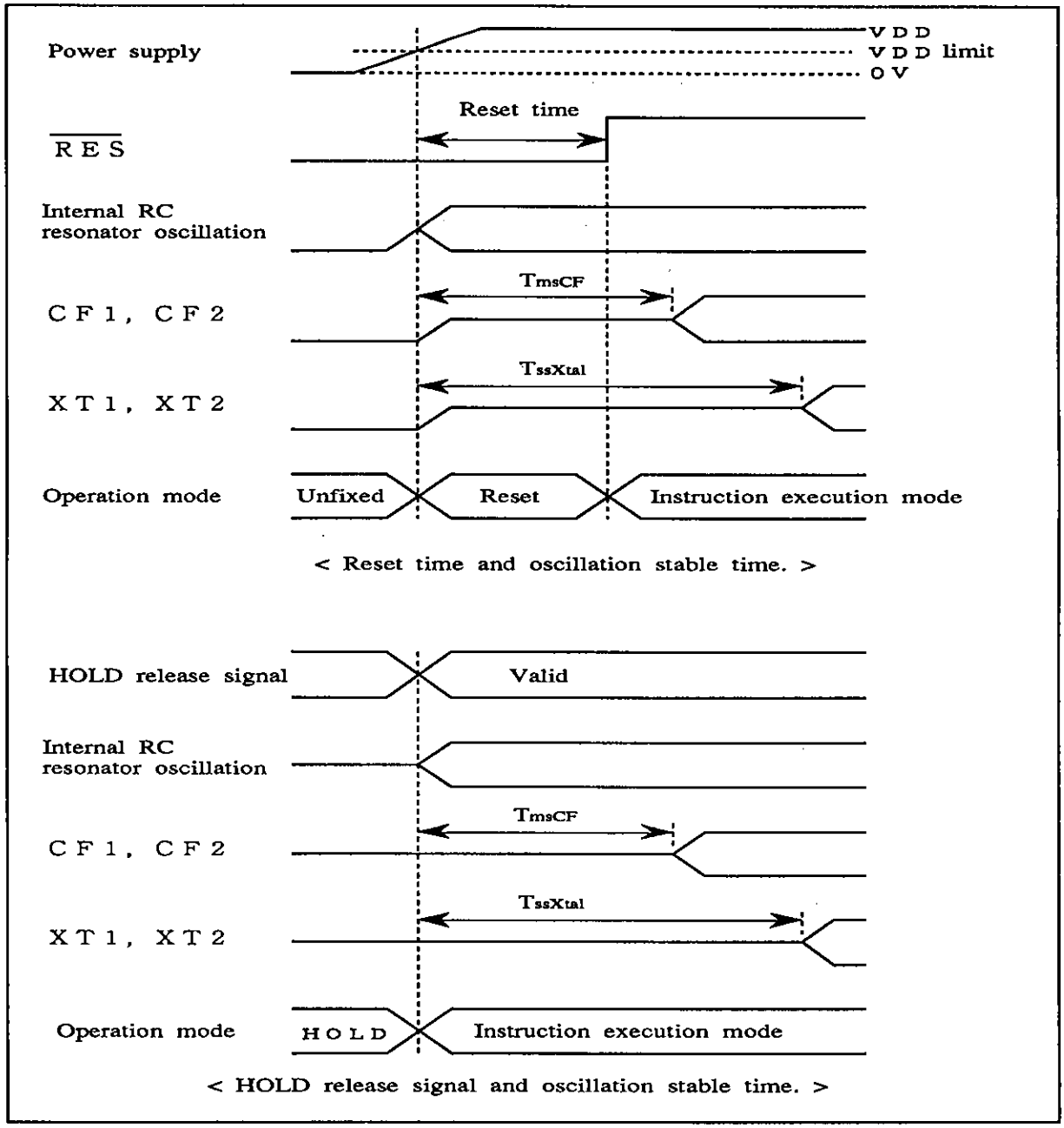
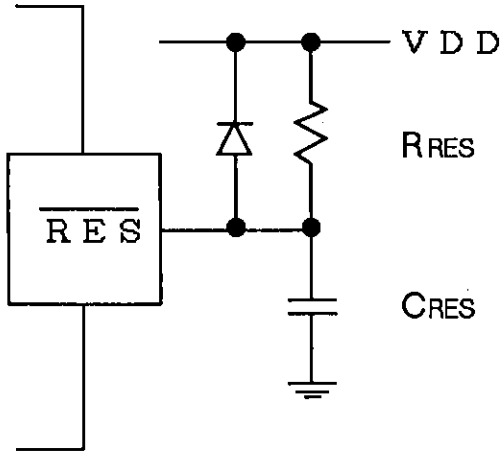
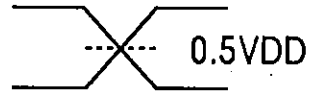


Figure.3 Oscillation stable time

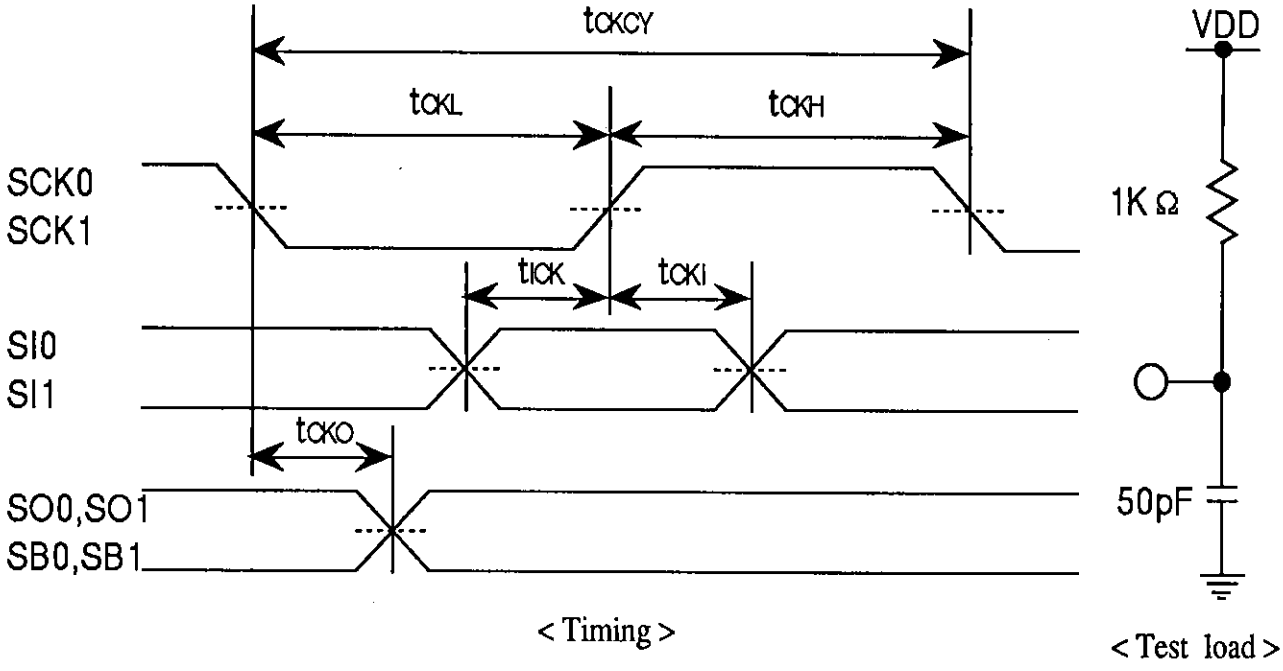


(Note) Fix the value of CRES, RRES that is sure to reset untill 200 μs, after Power supply has been over inferior limit of supply voltage.

Figure. 4 Reset circuit.



< AC timing point >



< Timing >

< Test load >

Figure. 5 Serial input/output test condition.

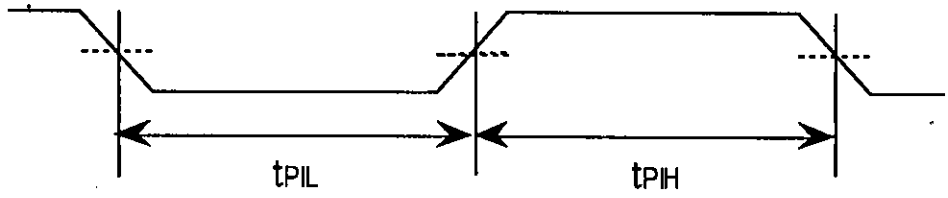


Figure. 6 Pulse input timing condition.