Ordering number : ENN*6722

CMOS IC

LC868364A

8-Bit Single Chip Microcontroller with 64K-Byte ROM and 512-Byte RAM On Chip

Preliminary

Overview

The LC868364A microcontroller is an 8-bit single chip microcontroller with the following on-chip functional blocks:

- CPU: Operable at a minimum bus cycle time of 0.5µs
- On-chip ROM capacity: 64K bytes
- On-chip RAM capacity: 512 bytes
- Dot-matrix liquid crystal display (LCD) automatic display controller/driver
- External memory
- 16-bit timer/counter (or two 8-bit timers)
- 16-bit timer/PWM (or two 8-bit timers)
- 13-source 9-vectored interrupt function

All of the above functions are fabricated on a single chip.

Features

(1) Read Only Memory (ROM): 65,280 × 8 bits

(2) Random Access Memory (RAM): 512 × 8 bits (calculation area)
128 × 8 bits (display area)

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(3) Bus Cycle Time/Instruction Cycle Time

Bus cycle time	Instruction Cycle Time	System Clock Oscillation	Oscillation Frequency	Voltage	Other
0.5µs	1µs	Ceramic (CF)	12MHz	3.3-6.5V	OCR7=0
			6MHz		OCR7=1
0.75µs	1.5µs	Ceramic (CF)	4MHz	2.7-6.5V	OCR7=1
1.0µs	2µs	Ceramic (CF)	6MHz	2.4-6.5V	OCR7=0
			3MHz		OCR7=1
7.5µs	15.0µs	Internal RC (or external RC)	800kHz	2.4-6.5V	OCR7=0
3.8µs	7.5µs				OCR7=1
183µs	366µs	Crystal (Xtal)	32.768kHz	2.2-6.5V	OCR7=0
93µs	183µs				OCR7=1

* Bus cycle time: ROM-read period OCR7: Oscillation control register bit-7

(4) Ports

- Input/output ports: 6 ports (48 terminals)
  - I/O programmable in nibble units: 1 port (8 terminals)
  - I/O programmable for each bit individually: 5 ports (40 terminals)
- Input port: 1 port (4 terminals)
- LCD drive common output ports: 32 terminals/16 terminals (switched by mask option)
- LCD drive segment output ports: 32 terminals/48 terminals (switched by mask option)

(5) External Program Memory Access Function

- Ports
  1. Data input/output: 1 port (8 terminals)
  2. Address output: 2 ports (16 terminals)
  3. Bank address output: Use normal I/O ports as bank address output by program control.
- External program memory access function
  External program memory space: 64K bytes
  Internal/external program can be switched by program. (at initial: internal program operation mode)
  Enabling/disabling of switching from external program to internal program is provided.
- External data memory access function
  By LDC instruction execution:
  External data memory space: 64K bytes (Use normal I/O ports as bank address output by program control.)
  1. When internal program is operating:
     Access to the internal or external ROM data is selectable by program.
  2. When external program is operating:
     Only the external ROM data can be accessed.
     (Only the external program memory space (64K bytes) can be referred.)
- External RAM memory access function (Able to be used when internal program is executed)
  By LDX instruction/STX instruction execution:
  External RAM space: 64K bytes (Use normal I/O ports as bank address output by program control.)
  (When using the external RAM space in the external program operation mode, refer to the “LC868364 User’s Manual” for details.)

(6) LCD Automatic Display Controller/Common Driver/Segment Driver

- Display duty: 1/32 duty, 1/16 duty
- Display bias: 1/5, 1/7 bias
- Graphic display
  A maximum of 1,024 dots capability (without external segment driver)
  32×80 dots display capability per each segment driver (LC868920A) can be expanded, when 1/32 duty is selected.
  Note: If the display capability is expanded by the LC86920A when 1/16 duty is selected, only S1-S32 of the LC868364A can be used, and S33-S48 can not be used. (Refer to the LC868920A specification sheet.)

- LCD contrast
  LCD display contrast is changeable by program.
- LCD power supply (max. 6V): externally boosted output terminal
  (assigned at P40 terminal, The terminal function is selectable by program.)
- LCD driver
  Following two kinds of combination can be switched by mask option.

	Segment Output Terminals	Common Output Terminals
1	32	32
2	48	16

- LCD clock: Select the crystal oscillation circuit output
  (in order to reduce the current consumption when LCD is on)
- LCD drive frequency: 102Hz (32.768kHz crystal oscillation)

(7) Serial Interface
- Synchronous 8-bit serial interface × 2 channels (built-in 8-bit baud rate generator)

(8) Timer
- Timer 0 (T0L, T0H)
  16-bit timer/counter
  2-bit prescaler + 8-bit programmable prescaler
  Mode 0: Two 8-bit timers with programmable prescaler
  Mode 1: 8-bit timer with programmable prescaler + 8-bit counter
  Mode 2: 16-bit timer with programmable prescaler
  Mode 3: 16-bit counter
- Timer 1 (T1L, T1H)
  16-bit timer/PWM
  Mode 0: Two 8-bit timers
  Mode 1: 8-bit timer + 8-bit PWM
  Mode 2: 16-bit timer
  Mode 3: Variable bit PWM (9-16 bits)
- Base Timer
  Generates an overflow every 500ms for a clock application. (using a 32.768kHz crystal oscillation for the base timer clock.)
  Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0.

(9) Buzzer Output
- Built-in 4kHz and 2kHz buzzer generation function

(10) Remote Receiver Circuit (shares with P73/INT3/T0IN terminal)
- Noise rejection function
- Polarity switch function

(11) Watchdog Timer
- External RC circuit is required (connected to P70/INT0 terminal)
- Interrupt or system reset is activated when the timer overflows.

(12) Interrupt

- 13-source and 9-vectored interrupt function:
  1. External interrupt INT0 (including watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, timer/counter T0L (lower 8 bits of Timer 0)
  4. External interrupt INT3, base timer
  5. Timer/counter T0H (upper 8 bits of Timer 0)
  6. Timer T1L (lower 8 bits of Timer 1), Timer T1H (upper 8 bits of Timer 1)
  7. Serial interface SIO0
  8. Serial interface SIO1
  9. Port 0 or Port 3

- Built-in Interrupt Priority Control

  Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible. Low or high priority can be assigned to the 11 interrupt sources, from the external interrupt INT2, Timer/Counter T0L (Timer 0, lower 8 bits) to Port 0 or Port 3. For the external interrupt INT0 and INT1, low or highest priority can be set regardless of the interrupt priority register.

(13) Sub-routine Stack Level

- A maximum of 128 levels: (sets stack inside RAM)

(14) Multiplication/Division Instruction

- 16 bits × 8-bit (7 instruction-cycle-times)
- 16 bits ÷ 8-bit (7 instruction-cycle-times)

(15) Three Types of Oscillation Circuit

- Built-in/external RC oscillation circuit used for the system clock
- CF oscillation circuit used for the system clock
- Xtal oscillation circuit used for the clock, system clock and LCD

  * Crystal oscillation clock is also used as LCD display base clock. The current consumption of this microcontroller becomes smaller than the Sanyo's previous microcontrollers by this configuration.

  Built-in/external RC oscillation circuit: switched by mask option

(16) Standby Function

- HALT mode

  In this operation mode, the program execution is stopped. The mode can be released by a system reset or an interrupt request.

- HOLD mode

  The HOLD mode is used to stop the oscillations;
  CF, RC, and Xtal oscillations. This mode can be released by the following conditions:
  • System reset
  • Feed the selected level to INT0 or INT1 terminals.
  • Feed "L" level to the Port 0 or Port 3.

(17) Operating Supply Voltage Range

- VDD=2.4 to 6.5V
- VLCD=2.5 to 6.5V (LCD power supply)

(18) Shipping Form

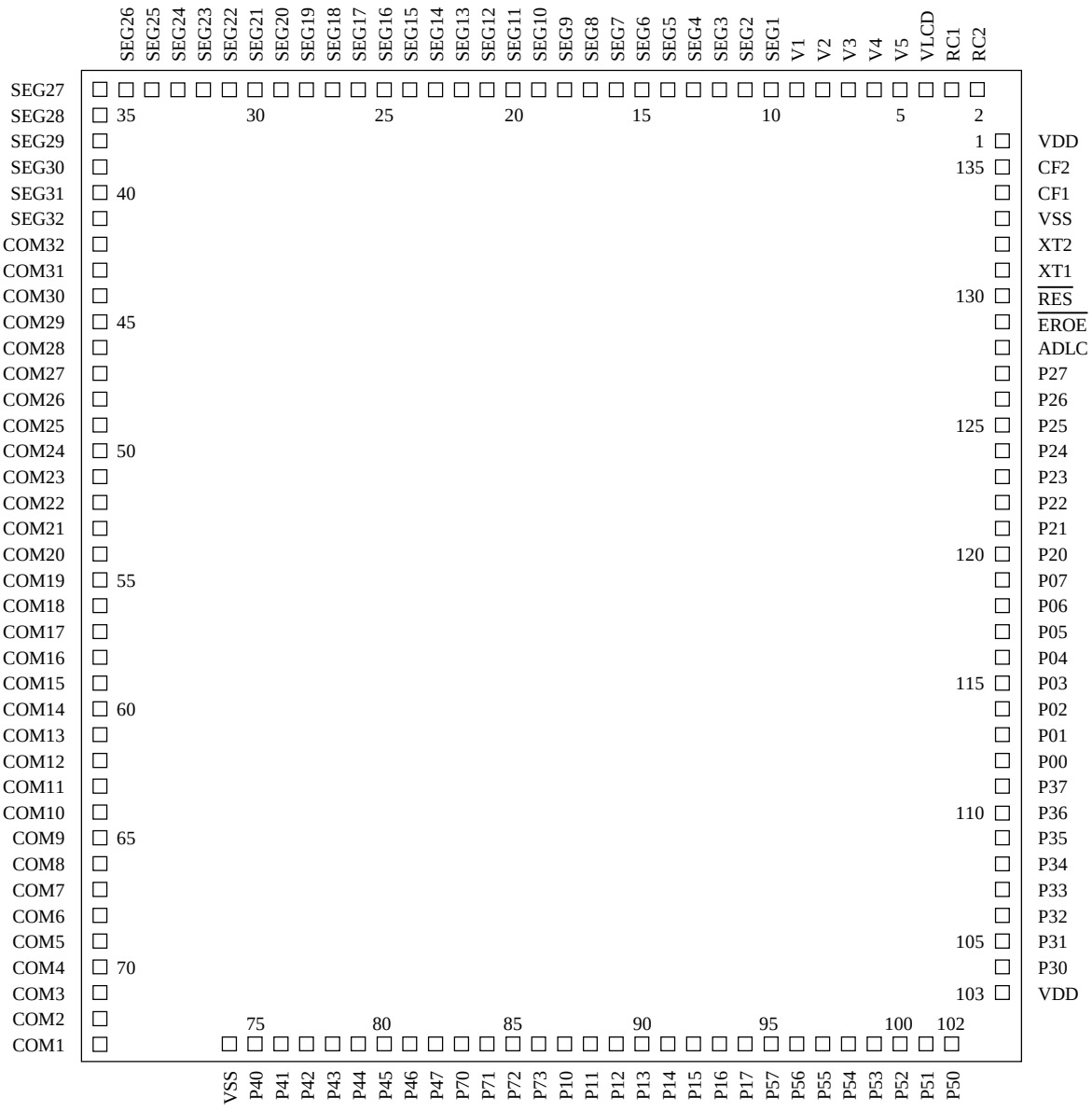
- Chip

(19) Development Tool

- Evaluation (EVA) chip: LC868099
- Emulator: EVA86000(main) + ECB868300 (evaluation board)

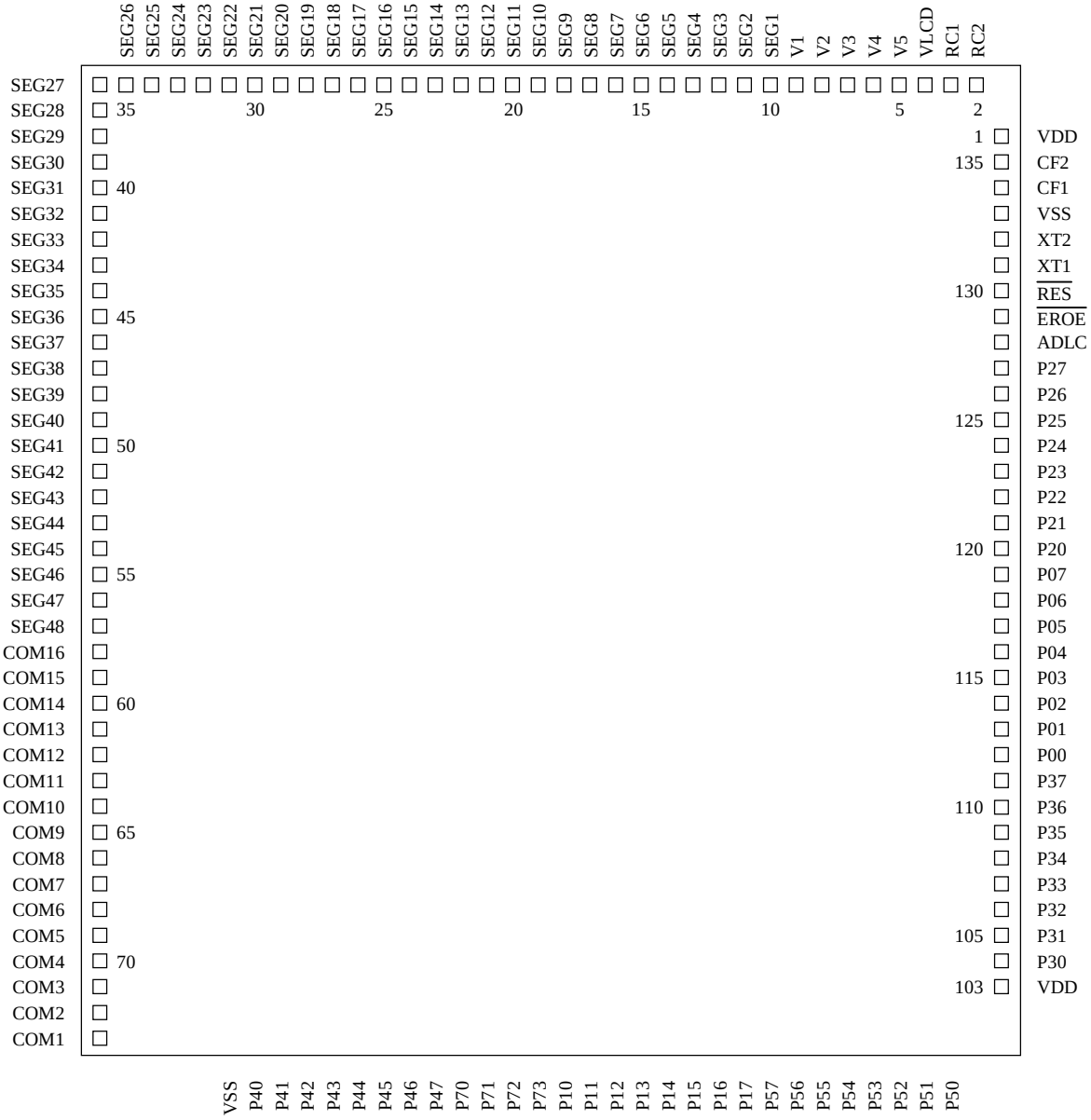
Pad Assignment (Display duty: 1/32 duty)

- Chip size (X × Y): 5.38mm × 4.84mm
- Thickness of chip : 480µm
- Pad size : 100µm × 100µm
- Pad pitch : 120µm

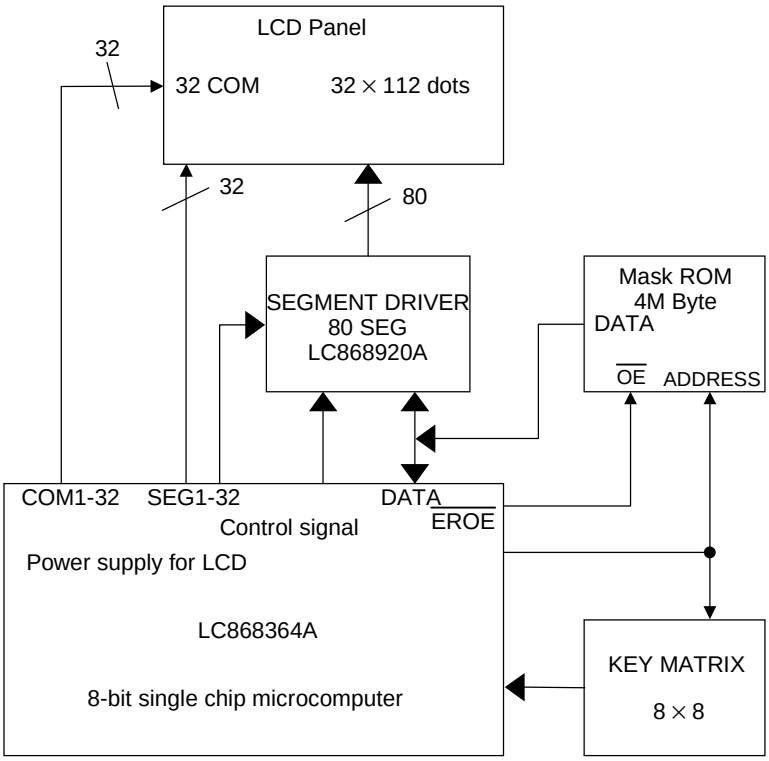


Pad Assignment (Display duty: 1/16 duty)

- Chip size (X × Y): 5.38mm × 4.84mm
- Thickness of chip : 480μm
- Pad size : 100μm × 100μm
- Pad pitch : 120μm



Application Circuit (Display duty: 1/32 duty)



Pad Name and Coordinates Table (Display duty: 1/32 duty)

Pad No.	Name	Coordinates	
		Xμm	Yμm
1	VDD	2178	2330
2	RC2	1967	2449
3	RC1	1836	2449
4	VLCD	1663	2449
5	V5	1543	2449
6	V4	1423	2449
7	V3	1303	2449
8	V2	1183	2449
9	V1	1063	2449
10	SEG1	942	2450
11	SEG2	822	2450
12	SEG3	702	2450
13	SEG4	582	2450
14	SEG5	462	2450
15	SEG6	342	2450
16	SEG7	223	2450
17	SEG8	103	2450
18	SEG9	-17	2450
19	SEG10	-137	2450
20	SEG11	-257	2450
21	SEG12	-377	2450
22	SEG13	-497	2450
23	SEG14	-617	2450
24	SEG15	-737	2450
25	SEG16	-857	2450
26	SEG17	-977	2450
27	SEG18	-1097	2450
28	SEG19	-1217	2450
29	SEG20	-1337	2450
30	SEG21	-1457	2450
31	SEG22	-1577	2450
32	SEG23	-1697	2450
33	SEG24	-1817	2450
34	SEG25	-1937	2450
35	SEG26	-2057	2450
36	SEG27	-2177	2450
37	SEG28	-2179	2172
38	SEG29	-2179	2052
39	SEG30	-2179	1932
40	SEG31	-2179	1812
41	SEG32	-2179	1692
42	COM32	-2179	1572
43	COM31	-2179	1452
44	COM30	-2179	1332
45	COM29	-2179	1212
46	COM28	-2179	1092
47	COM27	-2179	972
48	COM26	-2179	852
49	COM25	-2179	732
50	COM24	-2179	612
51	COM23	-2179	492
52	COM22	-2179	372
53	COM21	-2179	252
54	COM20	-2179	132
55	COM19	-2179	12
56	COM18	-2179	-108
57	COM17	-2179	-228
58	COM16	-2179	-348
59	COM15	-2179	-468
60	COM14	-2179	-588
61	COM13	-2179	-708
62	COM12	-2179	-828
63	COM11	-2179	-948
64	COM10	-2179	-1068
65	COM9	-2179	-1188
66	COM8	-2179	-1308
67	COM7	-2179	-1428
68	COM6	-2179	-1548
69	COM5	-2179	-1668
70	COM4	-2179	-1788
71	COM3	-2179	-1908
72	COM2	-2179	-2028
73	COM1	-2179	-2148
74	VSS	-1673	-2442
75	P40	-1543	-2442
76	P41	-1413	-2442
77	P42	-1283	-2442
78	P43	-1153	-2442
79	P44	-1023	-2442
80	P45	-893	-2442
81	P46	-763	-2442
82	P47	-633	-2442
83	P70	-503	-2442
84	P71	-373	-2442
85	P72	-243	-2442
86	P73	-113	-2442
87	P10	17	-2442
88	P11	147	-2442
89	P12	277	-2442
90	P13	407	-2442
91	P14	537	-2442
92	P15	667	-2442
93	P16	797	-2442
94	P17	927	-2442
95	P57	1057	-2442
96	P56	1187	-2442
97	P55	1317	-2442
98	P54	1447	-2442
99	P53	1577	-2442
100	P52	1707	-2442
101	P51	1837	-2442
102	P50	1967	-2442
103	VDD	2178	-2294
104	P30	2178	-2104
105	P31	2178	-1974
106	P32	2178	-1844
107	P33	2178	-1714
108	P34	2178	-1584
109	P35	2178	-1454
110	P36	2178	-1324
111	P37	2178	-1194
112	P00	2178	-1064
113	P01	2178	-934
114	P02	2178	-804
115	P03	2178	-674
116	P04	2178	-544
117	P05	2178	-414
118	P06	2178	-284
119	P07	2178	-154
120	P20	2178	-24
121	P21	2178	106
122	P22	2178	236
123	P23	2178	366
124	P24	2178	496
125	P25	2178	626
126	P26	2178	756
127	P27	2178	886
128	ADLC	2178	1216
129	$\overline{\text{EROE}}$	2178	1346
130	$\overline{\text{RES}}$	2178	1476
131	XT1	2178	1606
132	XT2	2178	1736
133	VSS	2178	1866
134	CF1	2178	1996
135	CF2	2178	2126

The values (X, Y) indicate the coordinates of each pad center with the center of the chip as the origin.

Pad Name and Coordinates Table (Display duty: 1/16 duty)

Pad No.	Name	Coordinates	
		Xμm	Yμm
1	VDD	2178	2330
2	RC2	1967	2449
3	RC1	1836	2449
4	VLCD	1663	2449
5	V5	1543	2449
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36	SEG27	-2177	2450
37	SEG28	-2179	2172
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52	SEG43	-2179	372
53	SEG44	-2179	252
54	SEG45	-2179	132
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56	SEG47	-2179	-108
57	SEG48	-2179	-228
58	COM16	-2179	-348
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60	COM14	-2179	-588
61	COM13	-2179	-708
62	COM12	-2179	-828
63	COM11	-2179	-948
64	COM10	-2179	-1068
65	COM9	-2179	-1188
66	COM8	-2179	-1308
67	COM7	-2179	-1428
68	COM6	-2179	-1548
69	COM5	-2179	-1668
70	COM4	-2179	-1788
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74	VSS	-1673	-2442
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107	P33	2178	-1714
108	P34	2178	-1584
109	P35	2178	-1454
110	P36	2178	-1324
111	P37	2178	-1194
112	P00	2178	-1064
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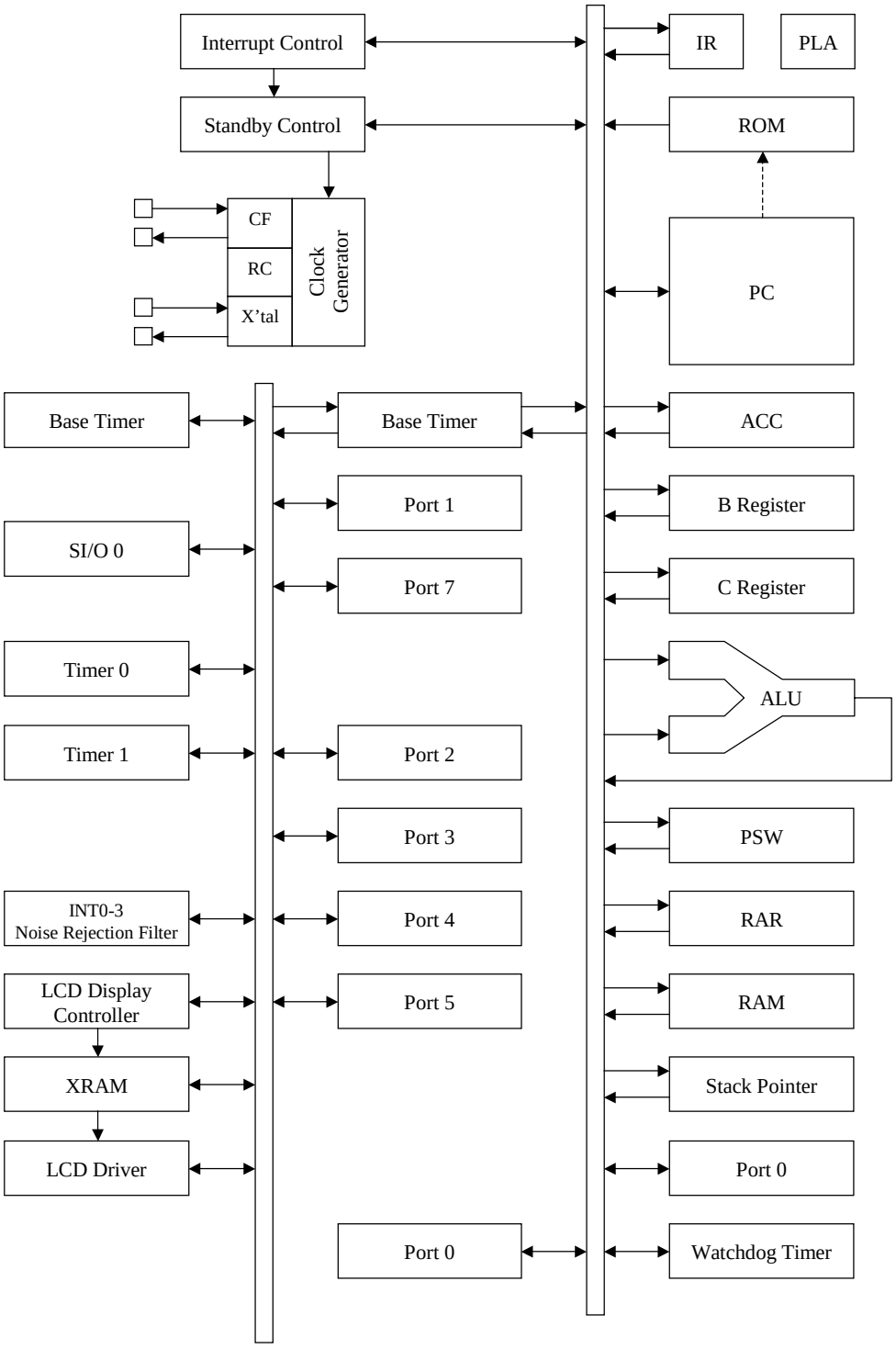
The values (X, Y) indicate the coordinates of each pad center with the center of the chip as the origin.

System Block Diagram



Pad Description

Name	No.	I/O	Function Description	Option
VSS	74,133	-	Power terminal (-)	-
VDD	1,103	-	Power terminal (+)	-
VLCD	4	-	Power terminal (+) for LCD driver (for bleeder resistor)	-
V1 to V5	9-5	-	Voltage supply terminals to LCD drivers	-
Port0 P00 to P07	112-119	I/O	・8-bit input/output port ・Data direction programmable in nibble units ・External memory mode 1. EXT register bit 2=0 Address output of lower 8 bits, input/output of data 2. EXT register bit 2=1 ・Input/output of data ・Input for key interrupt (P30INT=0) *(Note 2)*	・Pull-up resistor: provided/not provided ・Output form: CMOS/N-ch open drain *(Note 1)*
Port1 P10 to P17	87-94	I/O	・8-bit input/output port ・Data direction programmable for each bit individually ・Other functions P10: SIO0 data output P11: SIO0 data input, bus input/output P12: SIO0 clock input/output P13: SIO1 data output P14: SIO1 data input, bus input/output P15: SIO1 clock input/output P16: Buzzer output P17: Timer 1 output (PWM output)	・Output form: CMOS/N-ch open drain *(Note 1)*
Port2 P20 to P27	120-127	I/O	・8-bit input/output port ・Input/output can be specified in a bit ・External memory mode Address output of upper 8 bits	・Output form: CMOS/N-ch open drain *(Note 1)*
Port3 P30 to P37	104-111	I/O	・8-bit input/output port ・Data direction programmable for each bit individually ・External memory mode 1. EXT register bit 2=0: input/output port 2. EXT register bit 2=1: address output of lower 8 bits for external memory ・Input for key interrupt (P30INT=L) *(Note 2)*	・Pull-up resistor: provided/not provided ・Output form: CMOS/N-ch open drain *(Note 1)*
Port4 P40 to P47	75-82	I/O	・8-bit input/output port ・Input/output can be specified each upper 2 bits and lower 6 bits ・Other functions P40: Externally boosted clock — 2KOUT P41: Shift clock — CL2 P42: System clock for expansion driver — LCDP2 P43: Alternate signal — M P44: General output port — P44 P45: General output port — P45 P46: Read signal — $\overline{RD}$ P47: Write signal — $\overline{WR}$ (P40-P43: LCD expansion signal, P46, P47: External RAM access signal)	・Pull-up resistor: provided/not provided ・Output form: CMOS/N-ch open drain *(Note 1)*

<table>
<tr><th>Name</th><th>No.</th><th>I/O</th><th>Function Description</th><th>Option</th></tr>
<tr><td>Port5

P50 to P57</td><td>

102-95</td><td>I/O</td><td>· 8-bit input/output port
· Data direction programmable for each bit individually</td><td>· Pull-up resistor:
provided/not provided
· Output form:
CMOS/N-ch open drain
(Note 1)</td></tr>
<tr><td>Port7

P70 to P73</td><td>

83-86</td><td>I</td><td>· 4-bit input port
· Other functions
P70: INT0 input/HOLD release/N-ch Tr. output for watchdog timer
P71: INT1 input/HOLD release input
P72: INT2 input/Timer 0 event input
P73: INT3 input with noise filter/Timer 0 event input
· Interrupt detection style, vector address
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ Falling</th><th>H level</th><th>L level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td><td>03H</td></tr>
<tr><td>INT1</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td><td>0BH</td></tr>
<tr><td>INT2</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td><td>13H</td></tr>
<tr><td>INT3</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td><td>1BH</td></tr>
</table></td><td>· Pull-up resistor:
provided/not provided</td></tr>
<tr><td>C1 to C32
(Note 3)</td><td>73-42</td><td>O</td><td>LCD output terminals for common</td><td>· Segment output/
common output</td></tr>
<tr><td>S1 to S32</td><td>10-41</td><td>O</td><td>LCD output terminals for segment</td><td>-</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>130</td><td>I</td><td>Reset</td><td>-</td></tr>
<tr><td>ADLC</td><td>128</td><td>O</td><td>Address control signal for external memory</td><td>-</td></tr>
<tr><td>$\overline{\text{EROE}}$</td><td>129</td><td>O</td><td>Enable signal of external ROM output</td><td>-</td></tr>
<tr><td>XT1</td><td>131</td><td>I</td><td>Input terminal for 32.768kHz Xtal
When not in use, connect to VDD.</td><td>-</td></tr>
<tr><td>XT2</td><td>132</td><td>O</td><td>Output terminal for 32.768kHz Xtal
When not in use, leave open circuit.</td><td>-</td></tr>
<tr><td>CF1</td><td>134</td><td>I</td><td>Input terminal for ceramic resonator
When not in use, connect to VDD.</td><td>-</td></tr>
<tr><td>CF2</td><td>135</td><td>O</td><td>Output terminal for ceramic resonator
When not in use, leave open circuit.</td><td>-</td></tr>
<tr><td>RC1</td><td>3</td><td>I</td><td>Input terminal for RC oscillation (when external RC oscillation is used)
Put a resistor between RC1 and RC2, and a capacitor between RC1 and VSS externally.
Leave open when internal RC oscillation is used.</td><td>Internal/external</td></tr>
<tr><td>RC2</td><td>2</td><td>O</td><td>Output terminal for RC oscillation (when external RC oscillation is used)
Put a resistor between RC1 and RC2 externally.
Leave open when internal RC oscillation is used.</td><td>Internal/external</td></tr>
</table>

(Note 1) Nch-OD: N-channel open-drain output
(Note 2) P30INT: Bit 0 of Port 3 interrupt control register (P3INT).
** Port options can be specified for each bit individually.*
(Note 3) C1-C32 are the terminal names when 1/32 duty is selected.
C1-C16 and S48-S33 are the terminal names when 1/16 duty is selected.
Refer to "Pad Assignment" in pages 5-6.

* A state of port at initial

Pin Name	Input/output Mode	Style of pull-up resistors when pull-up option is enabled
Port 0, 7	Input	Fixed pull-up resistor provided
Ports 1, 2 Ports 3, 5	Input	Programmable pull-up resistor OFF
Port 4	Input	Programmable pull-up resistor ON

Name	Output Level
C1 to C32	VSS (display OFF)
S1 to S32	VSS (display OFF)

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Supply Voltage		VDDMAX	VDD			-0.3	-	+7.0	V
Input Voltage		VI(1)	·Ports 71,72,73 ·$\overline{\text{RES}}$			-0.3	-	VDD+0.3	
		VI(2)	VLCD			-0.3	-	+7.0	
Output Voltage		VO(1)	·C1 to C32 ·S1 to S32			-0.3	-	VLCD+0.3	
		VO(2)	ADLC, $\overline{\text{ER0E}}$			-0.3	-	VDD+0.3	
Input/output Voltage		VIO(1)	·Ports 0,1,2,3,4,5 ·Port 70 ·ADLC			-0.3	-	VDD+0.3	
High Level Output Current	Peak Output Current	IOPH(1)	·Ports 0,1,2,3,4,5 ·ADLC, $\overline{\text{ER0E}}$	·CMOS output ·For each pin		-4			mA
	Total Output Current	ΣIOAH(1)	·Ports 0,2,3 ·C1-C32,S1-S32 ·ADLC, $\overline{\text{ER0E}}$	Total of all pins		-25			
		ΣIOAH(2)	Ports 1, 4, 5	Total of all pins		-25			
Low Level Output Current	Peak Output Current	IOPL(1)	·Ports 0,1,2,3,4,5 ·ADLC, $\overline{\text{ER0E}}$	For each pin				20	
		IOPL(2)	Port 70	For each pin				15	
	Total Output Current	ΣIOAL(1)	Port 0	Total of all pins				40	
		ΣIOAL(2)	·Port 2 ·ADLC, $\overline{\text{ER0E}}$	Total of all pins				40	
		ΣIOAL(3)	Port 3	Total of all pins				40	
		ΣIOAL(4)	Ports 1, 5	Total of all pins				40	
		ΣIOAL(5)	Port 4	Total of all pins				40	
		ΣIOAL(6)	Port 70	Total of all pins				15	
		ΣIOAL(7)	C1-C32,S1-S32	Total of all pins				30	
Operating Temperature Range		Topr				-30	-	+70	°C
Storage Temperature Range		Tstg				-55	-	+125	

Notes:
The specification above indicates the state when a die is mounted in a package, SQFC144.
However, we ship this product in a chip, not in a package.
Make sure that the operational characteristics may vary by the user's package techniques.

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Operating Supply Voltage Range	VDD(1)	VDD	0.98µs ≤ tCYC ≤ 400µs		3.3		6.5	V
	VDD(2)		1.49µs ≤ tCYC ≤ 400µs		2.7		6.5	
	VDD(3)		1.98µs ≤ tCYC ≤ 400µs		2.4		6.5	
Hold Voltage	VHD	VDD	RAM and register data are kept in HOLD mode.		2.0		6.5	
LCD Display Voltage	VLCD	VLCD		2.4-2.5	2.5		6.5	
				2.5-3.0	VDD		6.5	
				3.0-6.5	VDD		6.5	
Input High Voltage	VIH(1)	Port 0 (Schmitt)	Output disable	2.4-6.5	0.4VDD +0.9		VDD	
	VIH(2)	·Ports 1,2,3,4,5 ·Ports 72,73 (Schmitt)	Output disable	2.4-6.5	0.7VDD		VDD	
	VIH(3)	·Port 70 for Port input/interrupt ·Port 71 ·$\overline{RES}$ (Schmitt)	Output N-channel Tr. OFF	2.4-6.5	0.7VDD		VDD	
	VIH(4)	Port 70 for watchdog timer	Output N-channel Tr. OFF	2.4-6.5	0.9VDD		VDD	
Input Low Voltage	VIL(1)	Port 0 (Schmitt)	Output disable	2.4-6.5	VSS		0.2VDD	
	VIL(2)	·Ports 1,2,3,4,5 ·Ports 72,73 (Schmitt)	Output disable	2.4-6.5	VSS		0.3VDD	
	VIL(3)	·Port 70 Port input/interrupt ·Port 71 ·$\overline{RES}$	Output N-channel Tr. OFF	2.4-6.5	VSS		0.3VDD	
	VIL(4)	Port 70 for watchdog timer	Output N-channel Tr. OFF	2.4-6.5	VSS		0.8VDD -1.0	
Operation Cycle Time	tCYC			3.3-6.5	0.98		400	µs
				2.7-6.5	1.49		400	
				2.4-6.5	1.98		400	
Oscillation Frequency Range *(Note 1)*	FmRC	RC1, RC2	·External RC oscillation ·Refer to figure 3	2.4-6.5	0.3		3	MHz

(Note 1): Oscillation parameters are shown in "Recommended Oscillation Circuit and Characteristics" in page 20.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Input High Current	IIH(1)	·Ports 1,2,3,4,5 ·Port 0 without pull-up MOS Tr.	·Output disable ·Pull-up MOS Tr. OFF ·VIN=VDD (including the off-leak current of the output Tr.)	2.5-6.5			1	μA
	IIH(2)	Port 7 without pull-up MOS Tr.	·Output Nch Tr. OFF ·VIN=VDD (including the off-leak current of the output Tr.)	2.5-6.5			1	
	IIH(3)	$\overline{\text{RES}}$	VIN=VDD	2.5-6.5			1	
Input Low Current	IIL(1)	·Ports 1,2,3,4,5 ·Port 0 without pull-up MOS Tr.	·Output disable ·Pull-up MOS Tr. OFF ·VIN=VSS (including the off-leak current of the output Tr.)	2.5-6.5	-1			
	IIL(2)	Port 7 without pull-up MOS Tr.	·Output Nch Tr. OFF ·VIN=VSS (including the off-leak current of the output Tr.)	2.5-6.5	-1			
	IIL(3)	$\overline{\text{RES}}$	VIN=VSS	2.5-6.5	-1			
Output High Voltage	VOH(1)	Port 0 of CMOS output, P46,P47	IOH=-10mA	4.5-6.5	VDD-1.5			V
	VOH(2)		IOH=-1mA	2.5-6.5	VDD-0.4			
	VOH(3)	·Ports 1,2,3,4(P40-P45),5 of CMOS output ·ADLC, $\overline{\text{ER0E}}$	IOH=-1.0mA	4.5-6.5	VDD-1			
	VOH(4)		IOH=-0.1mA	2.5-6.5	VDD-0.5			
Output Low Voltage	VOL(1)	·Ports 0,1,2,3,4,5 ·ADLC, $\overline{\text{ER0E}}$	IOL=10mA	4.5-6.5			1.5	
	VOL(2)		IOL=1.6mA	4.5-6.5			0.4	
	VOL(3)		·IOL=1.0mA ·Every pin's IOL≤1mA	2.5-6.5			0.4	
	VOL(4)	Port 70	IOL=1mA	4.5-6.5			0.4	
	VOL(5)		IOL=0.5mA	2.5-6.5			0.4	
Pull-up MOS Tr. resistor	Rpu	·Ports 0,1,2,3,4,5 ·Port 7	VOH=0.9VDD	4.5-6.5	50	70	100	kΩ
				2.5-4.5	60	100	200	
Hysteresis Voltage	VHIS	·Ports 0,1,2,3,4,5 ·Port 7 ·$\overline{\text{RES}}$	Output disable	2.5-6.5		0.1VDD		V
Pin Capacitance	CP	All pins	·f=1MHz ·All pins except the measured terminal: VIN=VSS ·Ta=25°C	2.5-6.5		10		pF
Built-in RC Oscillation Frequency				2.5-6.5	0.3	0.8	2	MHz

4. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
High/low Level Pulse Width	tPIH(1) tPIL(1)	·INT0, INT1 ·INT2/T0IN ·Refer to figure 7	·Interrupt acceptable ·Timer 0-countable	2.5-6.5	1			tCYC
	tPIH(2) tPIL(2)	·INT3/T0IN (The noise rejection clock is selected to 1/1.) ·Refer to figure 7	·Interrupt acceptable ·Timer 0-countable	2.5-6.5	2			
	tPIH(3) tPIL(3)	·INT3/T0IN (The noise rejection clock is selected to 1/64.) ·Refer to figure 7	·Interrupt acceptable ·Timer 0-countable	2.5-6.5	128			
	tPIL(4)	·$\overline{\text{RES}}$ ·Refer to figure 7	Reset acceptable	2.5-6.5	200			μs

5. Sample Current Consumption Characteristics at Ta=-30°C to +70°C, VSS=0V

The sample current consumption characteristics are the measurement result of Sanyo provided evaluation board. The currents through the output transistors, the pull-up MOS transistors and the bleeder resistors for the LCD are not included.

Parameter	Symbol	Pins	Conditions			Ratings			unit
				OCR7	VDD[V]	min.	typ.	max.	
Current Drain During Basic Operation *(Note 2)*	IDDOP(1)	VDD	·FmCF=12MHz by ceramic resonator ·FsXtal=32.768kHz by Xtal ·System clock: 12MHz ·Internal RC oscillation stops.	0	4.5-6.5		10	25	mA
	IDDOP(2)		·FmCF=6MHz by ceramic resonator ·FsXtal=32.768kHz by Xtal ·System clock: 6MHz ·Internal RC oscillation stops.	1	4.5-6.5		10	25	
	IDDOP(3)		·FmCF=3MHz by ceramic resonator ·FsXtal=32.768kHz by Xtal ·System clock: 3MHz ·Internal RC oscillation stops.	0	4.5-6.5		3	9	
	IDDOP(4)			1			6	15	
	IDDOP(5)			0	2.5-4.5		1.5	5	
	IDDOP(6)		·FmCF=0Hz (when oscillation stops) ·FsXtal=32.768kHz by Xtal ·System clock: RC oscillation	0	4.5-6.5		0.7	3.4	
	IDDOP(7)			1			1.2	4.5	
	IDDOP(8)			0	2.5-4.5		0.4	2.8	
	IDDOP(9)			1			0.8	3.6	
	IDDOP(10)		·FmCF=0Hz (when oscillation stops) ·FsXtal=32.768kHz by Xtal ·System clock: 32.768kHz ·Internal RC oscillation stops.	0	5.0		30	45	μA
	IDDOP(11)			1			50	80	
	IDDOP(12)			0	3.0		10	20	
	IDDOP(13)			1			20	30	

OCR7: Bit 7 of the oscillation control register.

Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	OCR7	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current Drain in HALT Mode *(Note 2)*	IDDHALT(1)	VDD	·HALT mode ·FmCF=12MHz Ceramic resonator oscillation ·FsXtal=32.768kHz Crystal oscillation ·System clock: 12MHz ·Internal RC oscillation stops. ·Refer to figure 8.	0	5.0		4.0	7.0	mA
	IDDHALT(2)		·HALT mode ·FmCF=6MHz Ceramic resonator oscillation ·FsXtal=32.768kHz Crystal oscillation ·System clock: 6MHz ·Internal RC oscillation stops. ·Refer to figure 8.	1	5.0		4.0	7.0	
	IDDHALT(3)		·HALT mode ·FmCF=3MHz Ceramic resonator oscillation ·FsXtal=32.768kHz Crystal oscillation ·System clock: 3MHz ·Internal RC oscillation stops ·Refer to figure 8.	0	5.0		1.5	2.6	
	IDDHALT(4)			1			2.3	4.0	
	IDDHALT(5)			0	3.0		0.5	0.9	
	IDDHALT(6)		·HALT mode ·FmCF=0Hz (when oscillation stops) ·FsXtal=32.768kHz crystal oscillation ·System clock: RC oscillation ·Refer to figure 8.	0	5.0		400	1600	μA
	IDDHALT(7)			1			600	2400	
	IDDHALT(8)			0	3.0		200	1300	
	IDDHALT(9)			1			300	1500	
	IDDHALT(10)		·HALT mode ·FmCF=0Hz (when oscillation stops) ·FsXtal=32.768kHz crystal oscillation ·System clock: 32.768kHz ·Internal RC oscillation stops ·Refer to figure 8.	0	5.0		20	35	
	IDDHALT(11)			1			30	50	
	IDDHALT(12)			0	3.0		7	13	
	IDDHALT(13)			1			10	18	
Current Drain in HOLD Mode *(Note 2)*	IDDHOLD(1)	VDD	·HOLD mode ·Refer to figure 8. ·Ta≤50°C		4.5-6.5		0.05	30	
	IDDHOLD(2)				2.5-4.5		0.02	20	

(Note 2) The currents of the output transistors, pull-up MOS transistors, the LCD bleeder resistors and the LCD driver are not included.

6. LCD Voltage and LCD Driver Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins, Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
VX-Ci Drop Voltage (X: 1 to 5) (i: 1 to 32)	|VD1|	·Only a Ci terminal for –15μA ·LCD display ON ·1/5 bias ·V5=VLCD=VDD	2.9			120	mV
			5.0			200	
VX-Ci Drop Voltage (X: 1 to 5) (i: 1 to 32)	|VD2|	·Only a Ci terminal for +15μA ·LCD display ON ·1/5 bias ·V5=VLCD=VDD	2.9	-120			
			5.0	-200			
VX-Si Drop Voltage (X: 1 to 5) (i: 1 to 32)	|VD3|	·Only a Si terminal for -15μA ·LCD display ON ·1/5 bias ·V5=VLCD=VDD	2.9			120	
			5.0			200	
VX-Si Drop Voltage (X: 1 to 5) (i: 1 to 32)	|VD4|	·Only a Si terminal for +15μA ·LCD display ON ·1/5 bias ·V5=VLCD=VDD	2.9	-120			
			5.0	-200			
V4 Output Voltage	VV4	·LCD clock frequency=0Hz ·LCD display ON ·1/5 bias ·V5=VLCD=VDD ·Refer to figure 10	2.9	0.75VDD	0.80VDD	0.85VDD	V
			5.0				
V3 Output Voltage	VV3		2.9	0.55VDD	0.60VDD	0.65VDD	
			5.0				
V2 Output Voltage	VV2		2.9	0.35VDD	0.40VDD	0.45VDD	
			5.0				
V1 Output Voltage	VV1		2.9	0.15VDD	0.20VDD	0.25VDD	
			5.0				

7. Sample LCD Driver Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins, Conditions		VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
LCD Display Current	ILCD1	·LCD display ON ·1/5 bias ·VLCD=5V ·V1-V5 are open. ·Refer to figure 9	100kΩ mode	2.9	5	10	20	μA
				5	5	10	20	
	ILCD2		50kΩ mode	2.9	10	20	40	
				5	10	20	40	
Contrast Current	ILC1	·LCD display ON ·VLCD=5V ·V5=VLCD-0.5V ·Refer to figure 11	VCCR=1	2.9	125	250	500	
	ILC2		VCCR=2	2.9	62	125	250	
	ILC3		VCCR=4	2.9	31	62	125	
	ILC4		VCCR=8	2.9	15	31	62	
	ILC5		VCCR=10H	2.9	8	15	31	

VCCR: LCD contrast control register

Recommended Oscillation Circuit and Characteristics

The oscillation circuit characteristics in the table below are based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- The characteristics are the results of the evaluation with the recommended circuit parameters connected externally.

Recommended Ceramic Oscillation Circuit and Characteristics (Ta = -30°C to +70°C)

Frequency	Manufacturer	Oscillator	Recommended Circuit Parameter			Operating supply Voltage Range	Oscillation Stabilizing Time Period (typ.) *	Notes
			C1	C2	Rd1			
12MHz	MURATA	CSA12.0MTZ	30pF	30pF	0kΩ	3.3 to 6.5V	0.06ms	
		CST12.0MTW	(30pF)	(30pF)	0kΩ	3.3 to 6.5V	0.06ms	built-in capacitor type
	KYOCERA	KBR-12.0M	22pF	22pF	0kΩ	3.3 to 6.5V	0.04ms	
6MHz	MURATA	CSA6.00MG	30pF	30pF	0kΩ	2.8 to 6.5V	0.08ms	
		CSTS0600MG03	(15pF)	(15pF)	0kΩ	2.4 to 6.5V	0.04ms	built-in capacitor type
	KYOCERA	KBR-6.0MSA	33pF	33pF	0kΩ	2.4 to 6.5V	0.05ms	
4MHz	MURATA	CSA4.00MG	30pF	30pF	0kΩ	2.7 to 6.5V	0.05ms	
		CSTS0400MG03	(15pF)	(15pF)	0kΩ	2.4 to 6.5V	0.03ms	built-in capacitor type
	KYOCERA	KBR-4.0MSA	33pF	33pF	0kΩ	2.4 to 6.5V	0.04ms	
3MHz	MURATA	CSA3.00MG	30pF	30pF	0kΩ	2.4 to 6.5V	0.06ms	
		CST3.00MGW	(30pF)	(30pF)	0kΩ	2.4 to 6.5V	0.06ms	built-in capacitor type
	KYOCERA	KBR-3.0MS	33pF	33pF	0kΩ	2.4 to 6.5V	0.05ms	

Recommended Crystal Oscillation Circuit and Characteristics (Ta = -30°C to +70°C)

Frequency	Manufacturer	Oscillator	Recommended Circuit Parameter			Operating supply Voltage Range	Oscillation Stabilizing Time Period (typ.) *	Notes
			C3	C4	Rd2			
32.768kHz	Seiko Instruments	VT-200	12pF	12pF	330kΩ	2.2 to 6.5V	0.6s	
	Seiko Epson	C-002RX/MC-306	12pF	12pF	330kΩ	2.2 to 6.5V	0.8s	

* The oscillation stabilizing time period is the time until the oscillation becomes stable after the VDD becomes higher than the minimum operating voltage.

Notes: • *Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.*
• *If you use other oscillators herein, we provide no guarantee for the characteristics.*

The oscillation circuit characteristics may differ by applications. For further assistance, please contact with the oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -30°C to +70°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.

Since the oscillation circuit characteristics are affected by the noise, wiring capacity, etc., refer to the following notices.

- The distance between the clock I/O terminal and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or the signal line with large amplitude such as middle withstand voltage port or LCD driver output should be allocated away from the clock oscillation circuit.
- The signal lines with large current should be allocated away from the oscillation circuit.

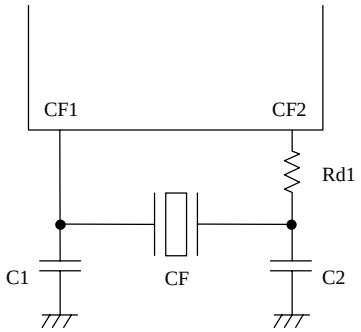


Figure 1 Ceramic Oscillation Circuit.

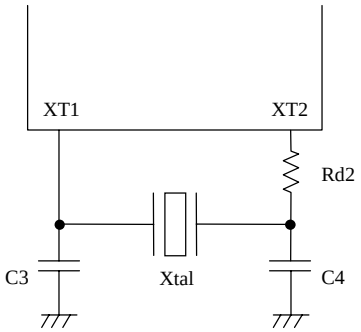


Figure 2 Crystal Oscillation Circuit.

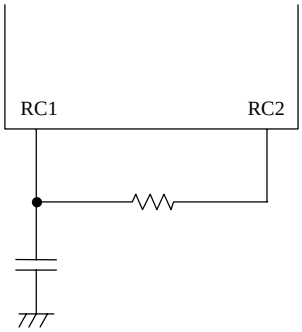
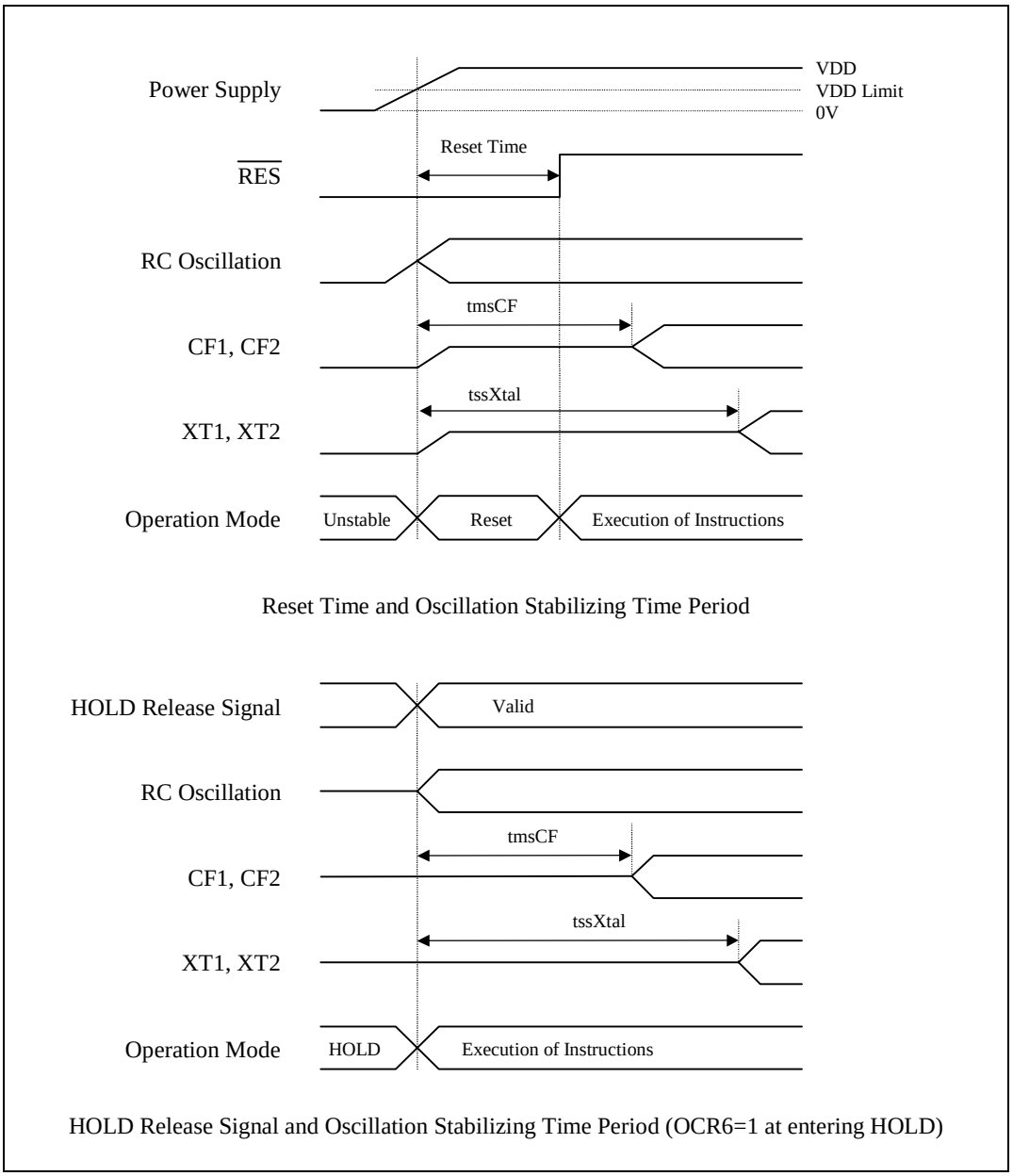
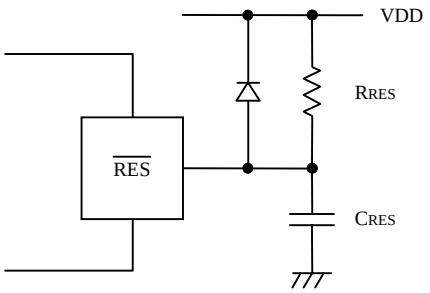


Figure 3 RC Oscillation Circuit.
(when external RC oscillation is selected)



tmsCF: Oscillation stabilizing time period when using the ceramic resonator oscillator.
tssXtal: Oscillation stabilizing time period when using the Xtal oscillator.

Figure 4 Oscillation Stabilizing Time Period.



(Note) Determine the CRES, RRES value to generate more than 200μs reset time.

Figure 5 Reset Circuit.

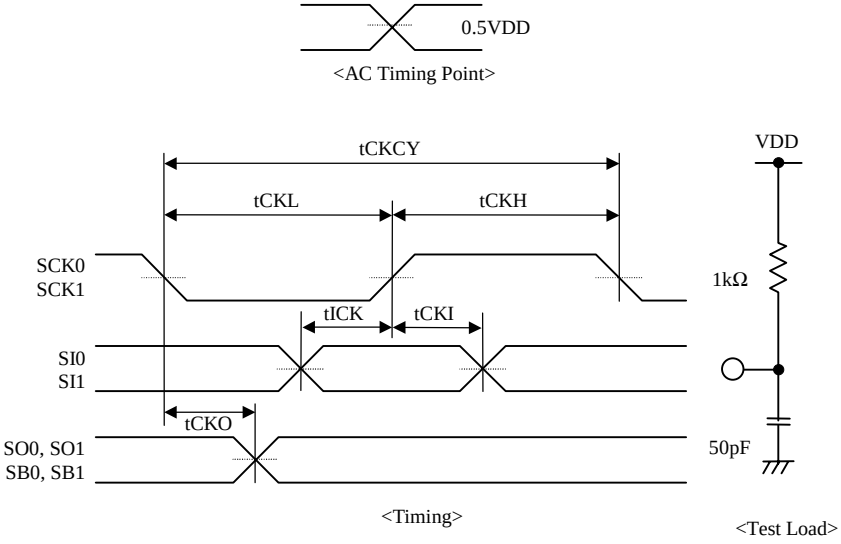


Figure 6 Serial Input/Output Test Condition.

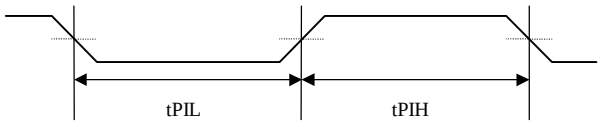


Figure 7 Pulse Input Timing Condition.

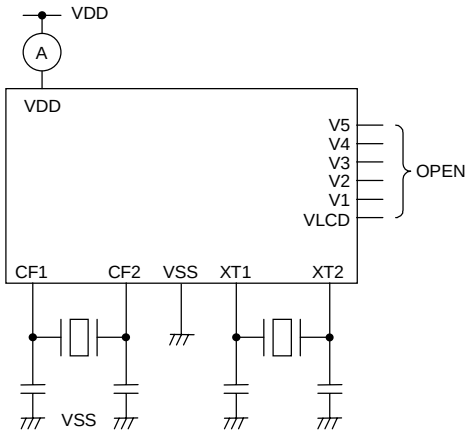


Figure 8 Current Consumption Measurement.

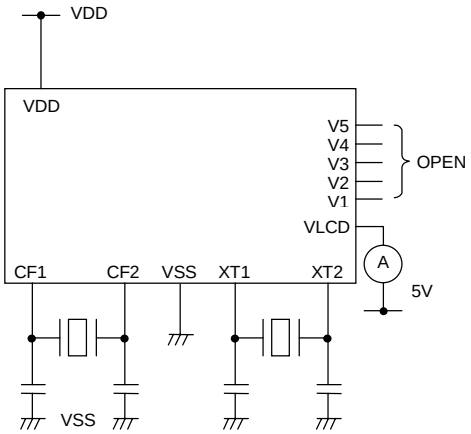


Figure 9 LCD Display Current Measurement.

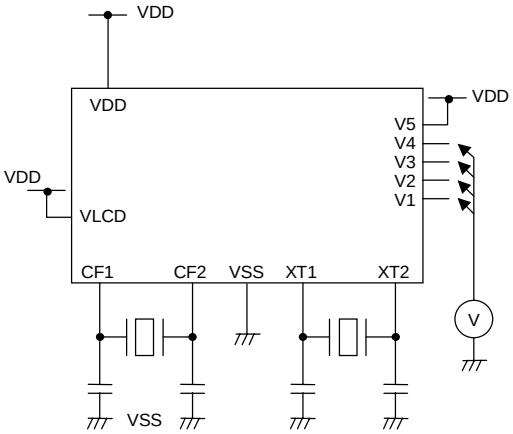


Figure 10 Output Voltage of V1-V4 Measurement.

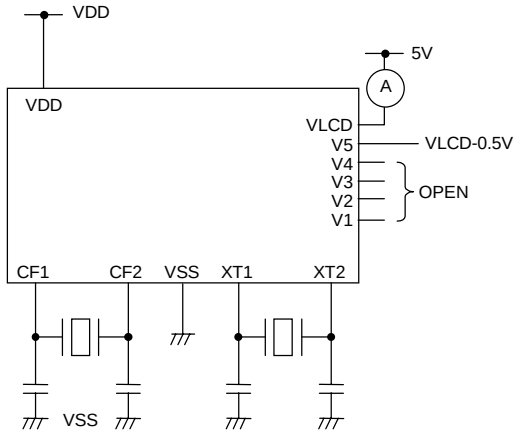


Figure 11 Contrast Current Measurement.

Notes: • *Figure 8-11 indicate the measurement circuits when using the internal RC oscillator.*

• *When external RC oscillation is selected, an external circuit needs to be connected to RC1 and RC2 terminals.*

AC Characteristics at Ta=-30°C to +70°C, VSS=0V

Load capacity: 100pF (Port 0, ADLC, $\overline{\text{EROE}}$)
Load capacity: 80pF (Output terminals except above)
*tCLCL=1tCYC/12

External Program Memory Timing

Parameter	Symbol	Pads and Conditions		Ratings		unit
			VDD[V]	min.	max.	
ADLC Pulse Width	tLHLL		4.5 to 6.5	2tCLCL-40		ns
			2.5 to 6.5	2tCLCL-160		
Address Settling Time	tAVLL	For ADLC	4.5 to 6.5	tCLCL-40		
			2.5 to 6.5	tCLCL-160		
Address Hold Time	tLLAX	For ADLC	4.5 to 6.5	tCLCL-35		
			2.5 to 6.5	tCLCL-140		
ADLC → Control Signal	tLLEL	For $\overline{\text{EROE}}$	4.5 to 6.5	tCLCL-25		
			2.5 to 6.5	tCLCL-100		
$\overline{\text{EROE}}$ Pulse Width	tELEH		4.5 to 6.5	3tCLCL-35		
			2.5 to 6.5	3tCLCL-140		
Data Delay Time	tELIV	From $\overline{\text{EROE}}$	4.5 to 6.5		3tCLCL-125	
			2.5 to 6.5		3tCLCL-400	
Data Hold Time	tEHIX	For $\overline{\text{EROE}}$	4.5 to 6.5	0		
			2.5 to 6.5	0		
$\overline{\text{EROE}}$ → Address in	tEHAV		4.5 to 6.5	tCLCL-8		
			2.5 to 6.5	tCLCL-32		

Refer to figure 12.

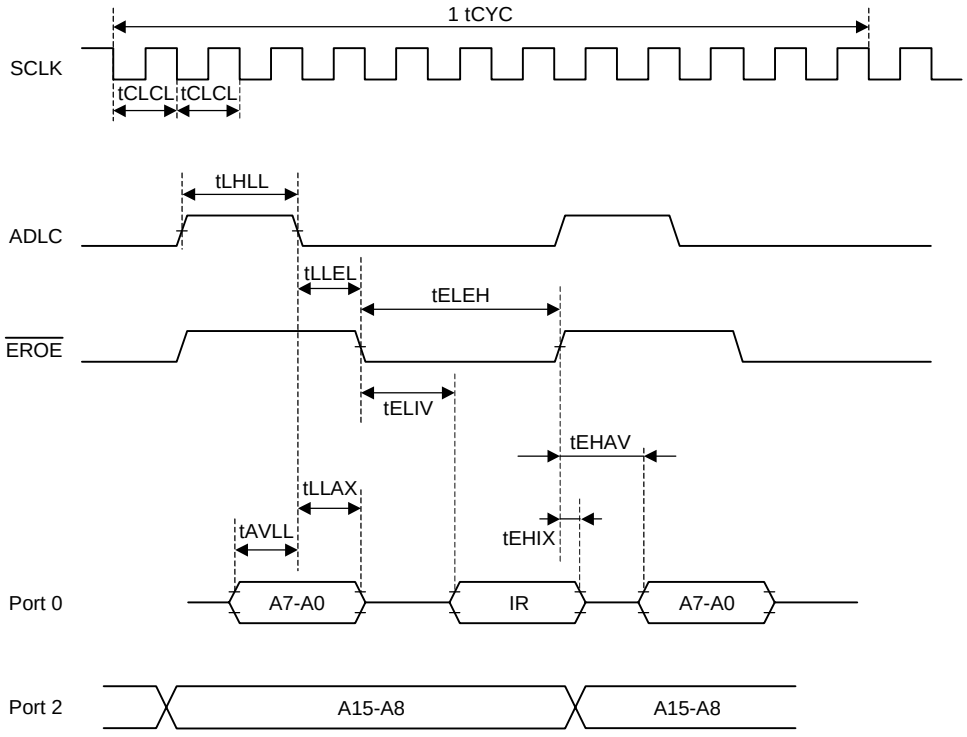


Figure 12 Timing of the External Program Memory/Data Memory.

External Data Memory Timing

Parameter	Symbol	Pads and Conditions		Ratings		unit
			VDD[V]	min.	max.	
$\overline{RD}$ Pulse Width	tRLRH		4.5 to 6.5	6tCLCL-80		ns
			2.5 to 6.5	6tCLCL-320		
$\overline{WR}$ Pulse Width	tWLWH		4.5 to 6.5	6tCLCL-80		
			2.5 to 6.5	6tCLCL-320		
Data Address Hold Time	tLLAX	For ADLC (read)	4.5 to 6.5	3tCLCL-35		
			2.5 to 6.5	3tCLCL-140		
		For ADLC (write)	4.5 to 6.5	2tCLCL-35		
			2.5 to 6.5	2tCLCL-140		
Data Delay Time	tRLDV	From $\overline{RD}$	4.5 to 6.5		5tCLCL-125	
			2.5 to 6.5		5tCLCL-400	
Data Hold Time	tRHDX	From $\overline{RD}$	4.5 to 6.5	0		
			2.5 to 6.5	0		
Data Floating Time	tRHDZ	From $\overline{RD}$	4.5 to 6.5	2tCLCL-70	2tCLCL+70	
			2.5 to 6.5	2tCLCL-280	2tCLCL+280	
Data Address Setting Time	tAVLL	For ADLC	4.5 to 6.5	2tCLCL-40		
			2.5 to 6.5	2tCLCL-160		
ADLC → Control Signal	tLLRL	For $\overline{RD}$	4.5 to 6.5	3tCLCL-50	3tCLCL+50	
			2.5 to 6.5	3tCLCL-200	3tCLCL+200	
	tLLWL	For $\overline{WR}$	4.5 to 6.5	3tCLCL-50	3tCLCL+50	
			2.5 to 6.5	3tCLCL-200	3tCLCL+200	
Data Settling Time	tQVWL	For $\overline{WR}$	4.5 to 6.5	tCLCL-60		
			2.5 to 6.5	tCLCL-240		
Data in $\overline{WR}$ =1	tQVWH		4.5 to 6.5	7tCLCL-140		
			2.5 to 6.5	7tCLCL-560		
Data Hold Time	tWHQX	From $\overline{WR}$	4.5 to 6.5	tCLCL-50		
			2.5 to 6.5	tCLCL-200		
Control Signal → ADLC	tRHLH	For $\overline{RD}$	4.5 to 6.5	tCLCL-50	tCLCL+50	
			2.5 to 6.5	tCLCL-200	tCLCL+200	
	tWHLH	For $\overline{WR}$	4.5 to 6.5	tCLCL-50	tCLCL+50	
			2.5 to 6.5	tCLCL-200	tCLCL+200	

Refer to figure 13.

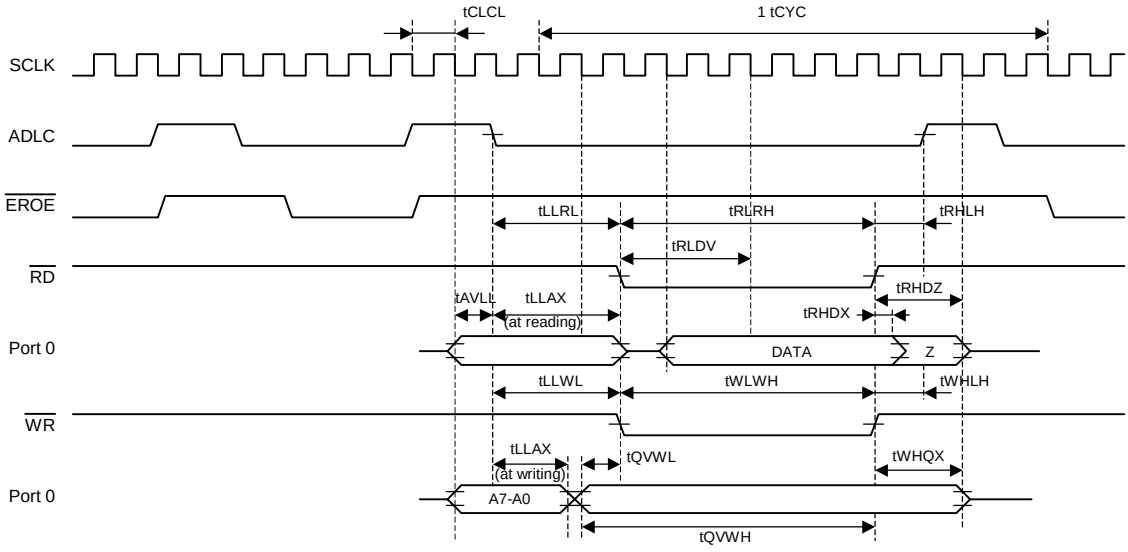
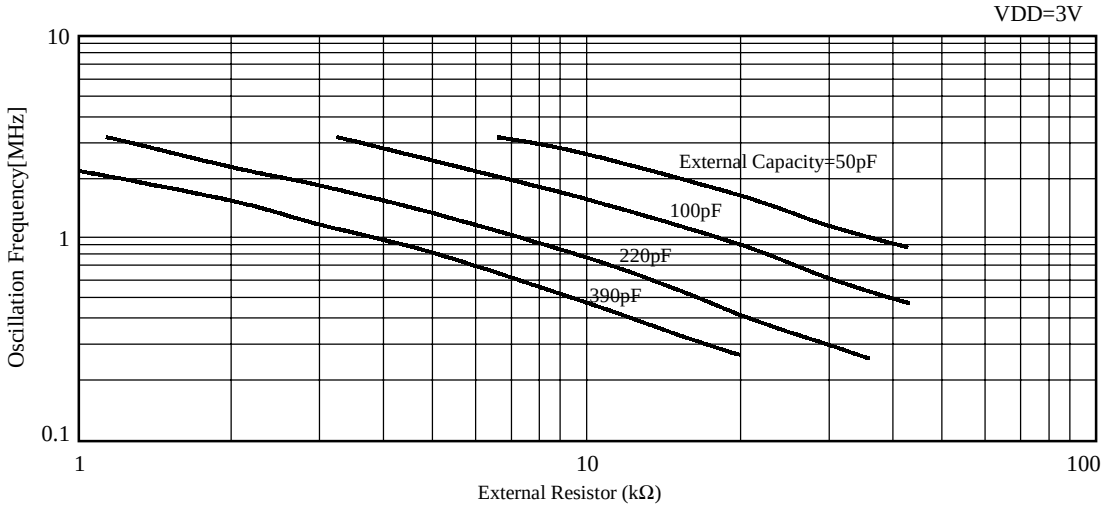
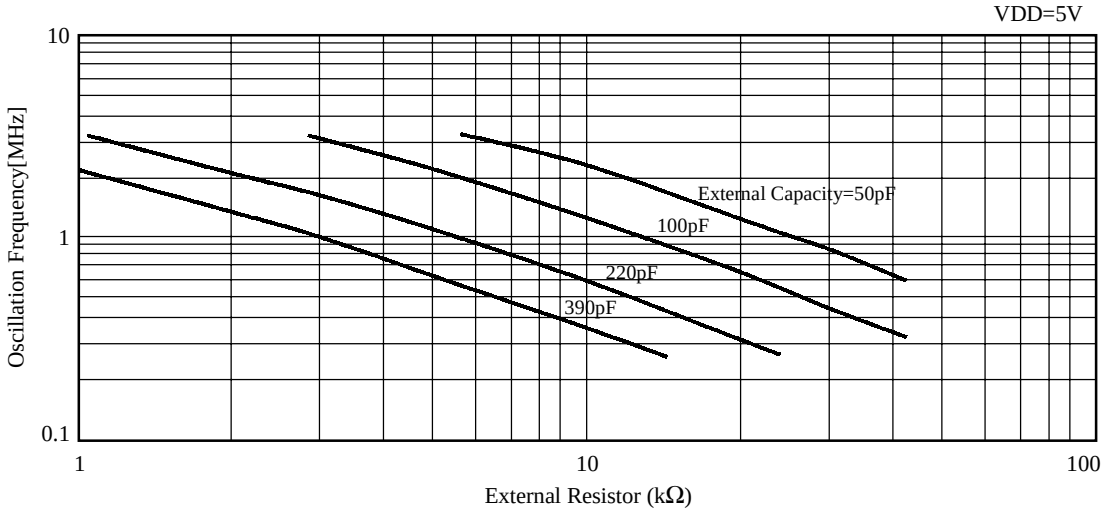


Figure 13 Timing of the External RAM.





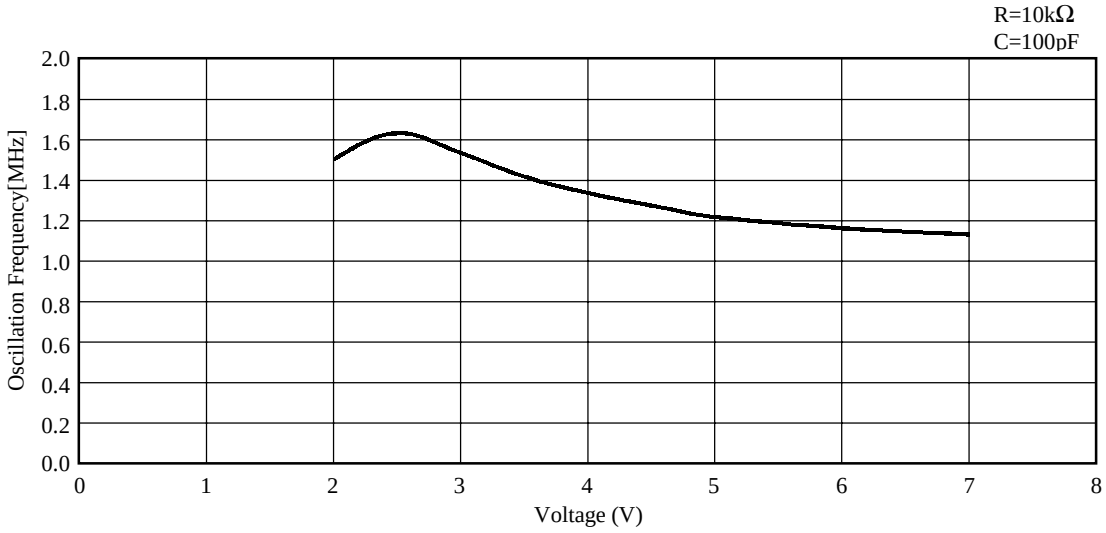


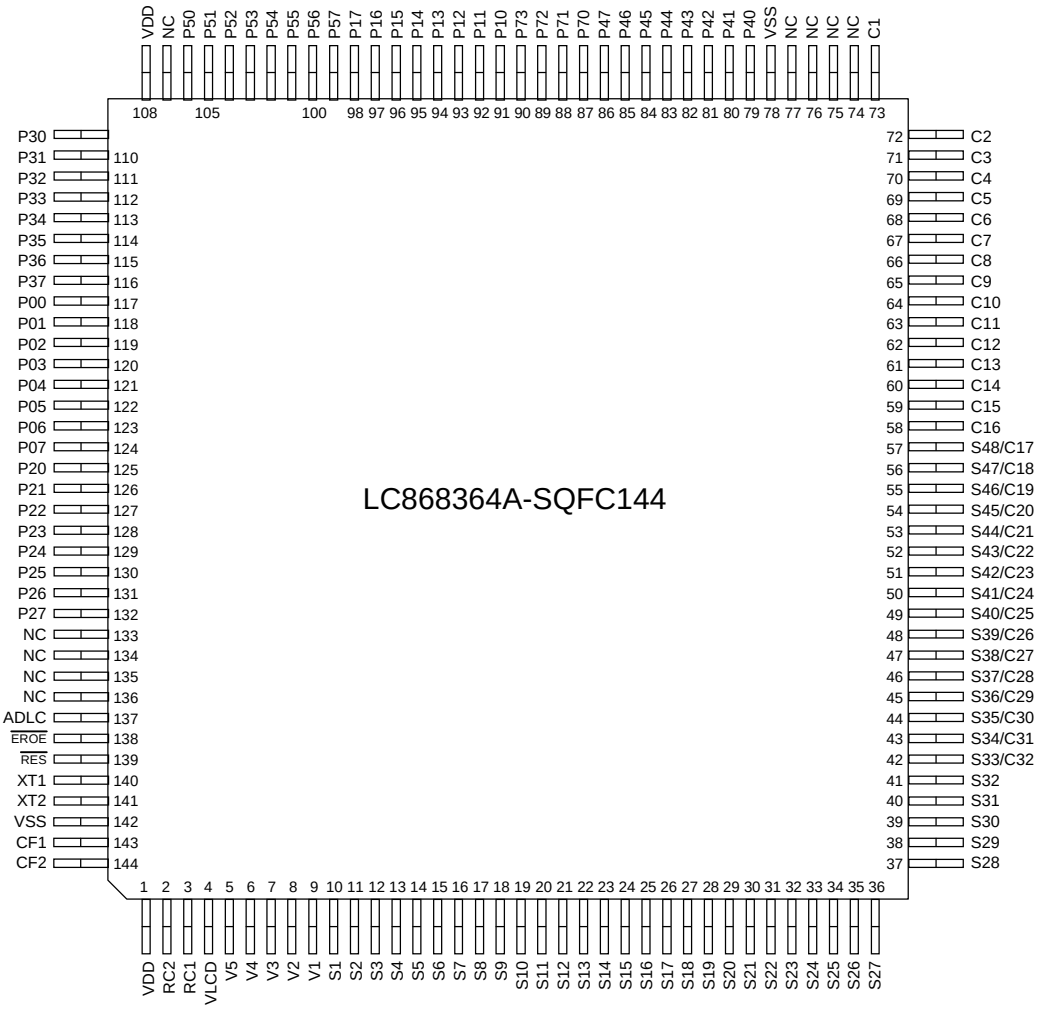
Figure 14 External RC Oscillation Frequency Characteristics. (Ta=25°C)

■ Evaluation Sample (ES)

Shipping Form: LC868364: chip, Evaluation sample: SQFC144 (shown below) or chip

If you use the ES in the package to design and fabricate an evaluation board, refer to the following pin assignment.

• Pin Assignment of evaluation sample (Package type)



memo: