Ordering number : ENN*6686A

CMOS IC

LC86F1216A

8-Bit Single Chip Microcontroller with 16K-Byte ROM and 1220-Byte RAM On Chip

Preliminary

Overview

The LC86F1216A is an 8-bit single chip microcontroller with the following on-chip functional blocks:

- CPU: Operable at a minimum bus cycle time of 0.5µs
  - On-chip Flash EEPROM capacity: 144 Kbytes
  - On-chip RAM capacity: 1222 bytes
  - Dot matrix liquid crystal display controller / driver
  - 16-bit timer/counter (or two channels × 8-bit timer)
  - 16-bit timer/PWM (or two channels × 8-bit timer)
  - Serial interface circuit

  All of the above functions are fabricated on a single chip.

Features

(1)Flash EEPROM: 64K × 8 bits: (program/data area) + 64K × 8 bits (data area)
16K × 8 bits: (program area)

(2) Mask ROM: 4K × 8 bits: (4K: BIOS program area)

(3) Random Access Memory (RAM): 512 × 8 bits (calculation area) + 512 × 8 bits
198 × 8 bits (display area)

(4) Bus Cycle Time

Bus Cycle Time	Cycle Time	System Clock Oscillation	Oscillation Frequency	Voltage	Notes
0.5µs	1.0µs	Ceramic	6MHz	3.15–3.85V	OCR7 = 1
3.8µs	7.5µs	External RC	600kHz		OCR7 = 1
93µs	183µs	X'tal	32.768kHz		OCR7 = 1

Note: Bus cycle time means cycle time of reading ROM. OCR7: Bit 7 of the oscillation control register

(5) Ports
- Input / Output Ports: 2 ports (16 terminals)
- Input port: 1 port (4 terminals)

*Flash memory products are manufactured and sold by SANYO Electric Co., Ltd. under license from Silicon Storage Technology, Inc. (USA).

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(6) Dot matrix liquid crystal display controller / driver
- Display duty: 1/33 duty
- Display bias: 1/5 bias
- LCD power supply (max. 6V)
- LCD driver (max. 1584 dots capability)
  Common output ports: 33 ports
  Segment output ports: 48 ports
- Externally boosted clock

(7) Serial interfaces
- Synchronous 8-bit serial interface × 2 (with 8-bit baud rate generator)

(8) Timers
- Timer 0 (T0H/T0L)
  16-bit timer/counter
- Timer 1 (T1H/T1L)
  16-bit timer/PWM

(9) Interrupts
- 13 sources 10 vectored interrupts

(10) Sub-routine stack level
- A maximum of 128 levels (stack is built in the internal RAM)

(11) 3 oscillation circuits
- External RC oscillation circuit / CF oscillation circuit / X'tal oscillation circuit

(12) Power voltage
- VDD = 3.15V – 3.85V

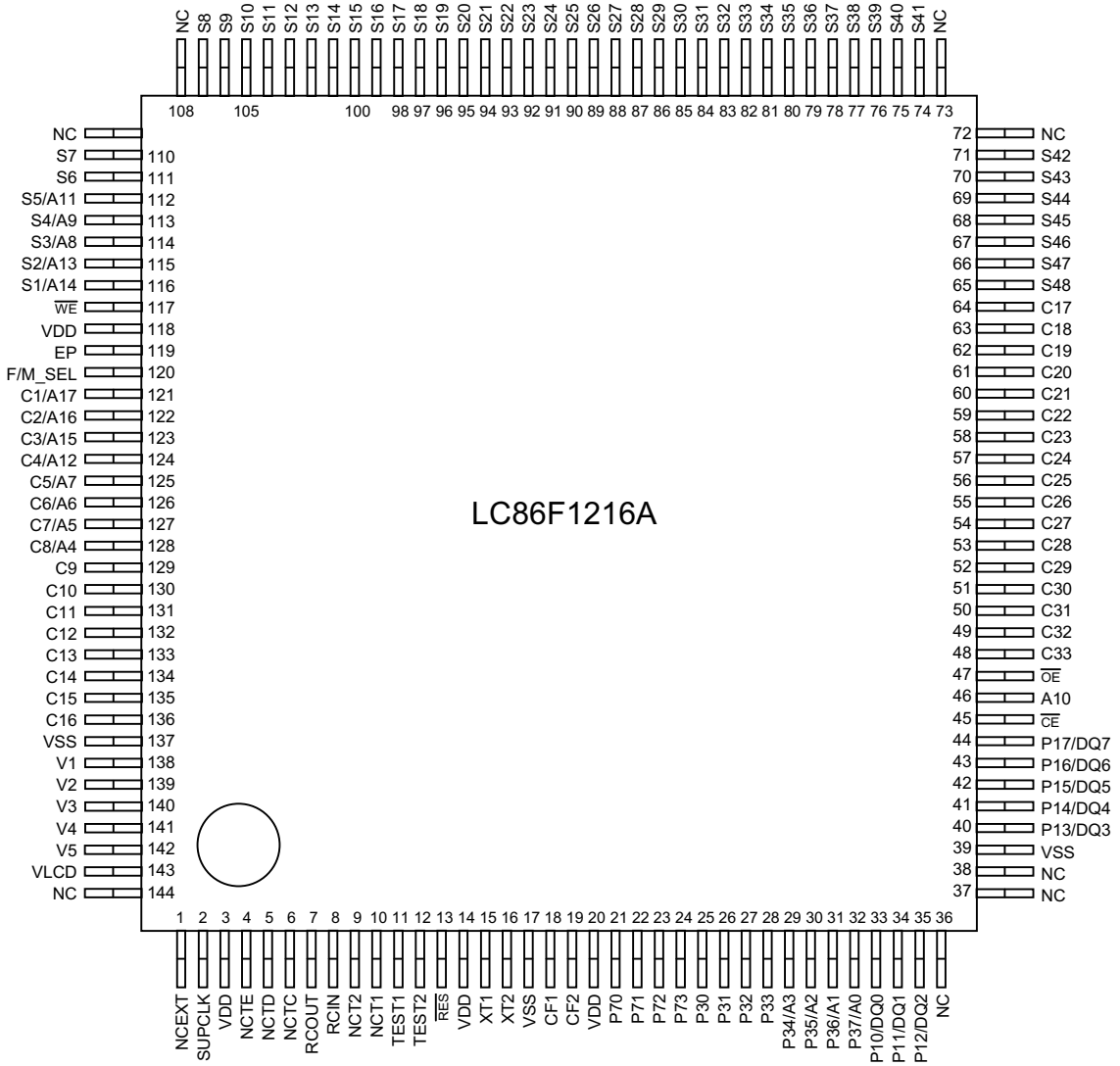
(13) Shipping form
- Chip or SQFP144

(14) Flash memory
- Erasing block unit size: 128 bytes
- Erasing / writing voltage range: 3.15V – 5.5V
- Maximum number of erase-write cycle: 50,000 times (Ta = +25°C) (with memory management program)

Note
The microcontroller will malfunction if the power supply voltage is less than the specified operable supply voltage. To prevent a malfunction, the low voltage detect circuit should be connected externally, and the voltage should always be set to the proper level. If the power supply voltage becomes lower than the voltage which is detected by the low voltage detect reset IC, then the microcontroller should be reset to restore stable operation. Use the low voltage detect reset IC which detects the lowest specification voltage of the power supply.
We cannot ensure the integrity of the block data, if the microcontroller is reset while writing to the flash memory. Therefore, in such a case, we recommend disabling any flash writing operation by user's program when the voltage decreases to a level just above the voltage which is detected by the low voltage detect reset IC.

Pin Assignment

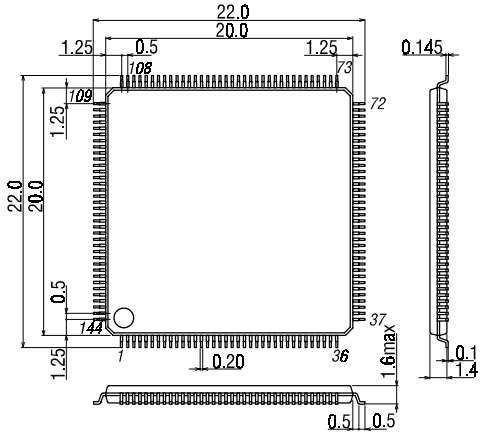
SQFP144



Package Dimension

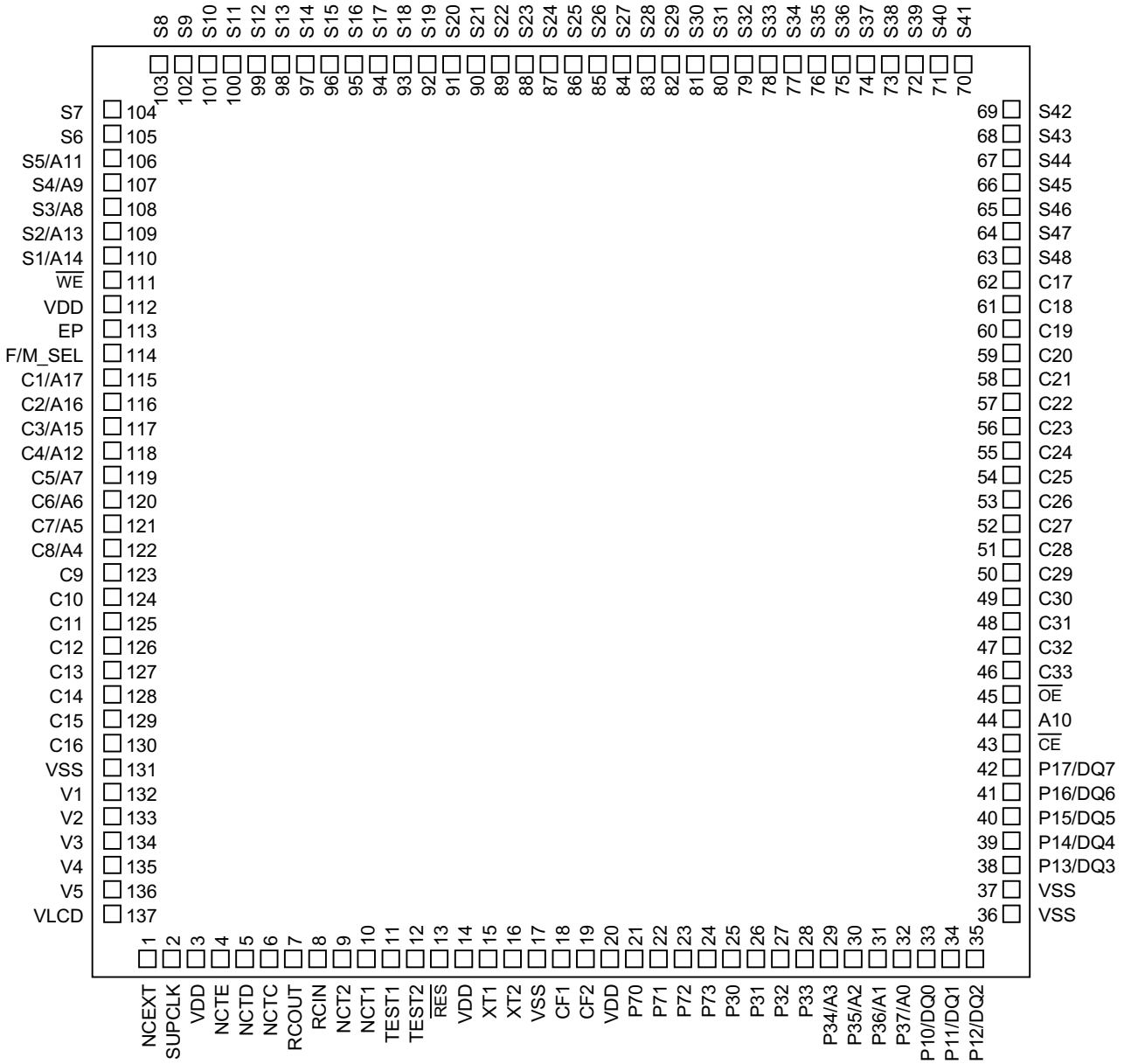
(unit : mm)

3214



SANYO : SQFP-144

Pad Assignment



Pad Name and Coordinates Table

PAD No.	Pin Name	X-cord	Y-cord	SQFP-144
1	NCEXT	-2965	-3540	1
2	SUPCLK	-2791	-3540	2
3	VDD	-2617	-3540	3
4	NCTE	-2443	-3540	4
5	NCTD	-2269	-3540	5
6	NCTC	-2096	-3540	6
7	RCOUT	-1922	-3540	7
8	RCIN	-1748	-3540	8
9	NCT2	-1574	-3540	9
10	NCT1	-1400	-3540	10
11	TEST1	-1226	-3540	11
12	TEST2	-1052	-3540	12
13	RES#	-879	-3540	13
14	VDD	-705	-3540	14
15	XT1	-531	-3540	15
16	XT2	-357	-3540	16
17	VSS	-183	-3540	17
18	CF1	-9	-3540	18
19	CF2	165	-3540	19
20	VDD	338	-3540	20
21	P70	512	-3540	21
22	P71	686	-3540	22
23	P72	860	-3540	23
24	P73	1034	-3540	24
25	P30	1208	-3540	25
26	P31	1382	-3540	26
27	P32	1556	-3540	27
28	P33	1729	-3540	28
29	P34/A3	1903	-3540	29
30	P35/A2	2077	-3540	30
31	P36/A1	2251	-3540	31
32	P37/A0	2425	-3540	32
33	P10/DQ0	2599	-3540	33
34	P11/DQ1	2773	-3540	34
35	P12/DQ2	2946	-3540	35
36	VSS	3333	-2756	39
37	VSS	3333	-2582	39
38	P13/DQ3	3333	-2408	40
39	P14/DQ4	3333	-2234	41
40	P15/DQ5	3333	-2061	42
41	P16/DQ6	3333	-1887	43
42	P17/DQ7	3333	-1713	44
43	CE#	3333	-1539	45
44	A10	3333	-1365	46
45	OE#	3333	-1191	47
46	C33	3333	-872	48

PAD No.	Pin Name	X-cord	Y-cord	SQFP-144
47	C32	3333	-698	49
48	C31	3333	-524	50
49	C30	3333	-350	51
50	C29	3333	-176	52
51	C28	3333	-2	53
52	C27	3333	171	54
53	C26	3333	345	55
54	C25	3333	519	56
55	C24	3333	693	57
56	C23	3333	867	58
57	C22	3333	1041	59
58	C21	3333	1215	60
59	C20	3333	1388	61
60	C19	3333	1562	62
61	C18	3333	1736	63
62	C17	3333	1910	64
63	S48	3333	2084	65
64	S47	3333	2258	66
65	S46	3333	2432	67
66	S45	3333	2605	68
67	S44	3333	2779	69
68	S43	3333	2953	70
69	S42	3333	3127	71
70	S41	2860	3539	74
71	S40	2686	3539	75
72	S39	2512	3539	76
73	S38	2339	3539	77
74	S37	2165	3539	78
75	S36	1991	3539	79
76	S35	1817	3539	80
77	S34	1643	3539	81
78	S33	1469	3539	82
79	S32	1295	3539	83
80	S31	1122	3539	84
81	S30	948	3539	85
82	S29	774	3539	86
83	S28	600	3539	87
84	S27	426	3539	88
85	S26	252	3539	89
86	S25	78	3539	90
87	S24	-95	3539	91
88	S23	-269	3539	92
89	S22	-443	3539	93
90	S21	-617	3539	94
91	S20	-791	3539	95
92	S19	-965	3539	96

PAD No.	Pin Name	X-cord	Y-cord	SQFP-144
93	S18	-1139	3539	97
94	S17	-1313	3539	98
95	S16	-1486	3539	99
96	S15	-1660	3539	100
97	S14	-1834	3539	101
98	S13	-2008	3539	102
99	S12	-2182	3539	103
100	S11	-2356	3539	104
101	S10	-2530	3539	105
102	S9	-2703	3539	106
103	S8	-2877	3539	107
104	S7	-3333	2992	110
105	S6	-3333	2818	111
106	S5/A11	-3333	2644	112
107	S4/A9	-3333	2470	113
108	S3/A8	-3333	2296	114
109	S2/A13	-3333	2122	115
110	S1/A14	-3333	1949	116
111	WE#	-3333	1749	117
112	VDD	-3333	1549	118
113	EP	-3333	1375	119
114	F/MSEL	-3333	1202	120
115	C1/A17	-3333	1010	121
116	C2/A16	-3333	836	122
117	C3/A15	-3333	662	123
118	C4/A12	-3333	488	124
119	C5/A7	-3333	314	125
120	C6/A6	-3333	140	126
121	C7/A5	-3333	-34	127
122	C8/A4	-3333	-207	128
123	C9	-3333	-381	129
124	C10	-3333	-555	130
125	C11	-3333	-729	131
126	C12	-3333	-903	132
127	C13	-3333	-1077	133
128	C14	-3333	-1251	134
129	C15	-3333	-1425	135
130	C16	-3333	-1598	136
131	VSS	-3333	-1772	137
132	V1	-3333	-1946	138
133	V2	-3333	-2120	139
134	V3	-3333	-2294	140
135	V4	-3333	-2468	141
136	V5	-3333	-2642	142
137	VLCD	-3333	-2815	143

Terminal Function

Terminal	Pin No.	Pad No.	Input/ Output	Function Description
VSS	17,39,137	17,36-37,131	-	·Negative power supply
VDD	3,14,20,118	3,14,20,112	-	·Positive power supply
VLCD	143	137	-	·Positive power supply (power supply for LCD driver)
V1-5	138-142	132-136	-	·Power supply for LCD driver
PORT3	25-32	25-32	I/O	·8 bit I/O port (Output format: CMOS with pull-up resistor: P30-P37) ·I/O programmable for each bit individually ·Used for switch input ·Key interrupt input
PORT1	33-35 40-44	33-35 38-42	I/O	·8 bit I/O port (Output format: CMOS: P16, P17 Nch-OD: P10, P11, P12, P13, P14, P15) (pull-up resistor: P10 - P17) ·I/O programmable for each bit individually ·Other functions
				Terminal: Serial
				P10: Serial OUT0
				P11: Serial IN0
				P12: Serial Clock0
				P13: Serial OUT1
				P14: Serial IN1
				P15: Serial Clock1
				P16: Buzzer output
				P17: Timer1 output (PWM output)
PORT7	21-24	21-24	I	·4bit input port (pull-up resistor: P70 - P73) ·External interrupt function ·Input only
C01-C33	121-136 64-48	115-130 62-46	O	·LCD controller Common output terminals
S01-S48	116-110 107-74 71-65	110-63	O	·LCD controller Segment output terminals
SUPCK	2	2	O	·Externally boosted clock output terminal
CF1	18	18	I	·Input terminal for ceramic resonator
CF2	19	19	O	·Output terminal for ceramic resonator
XT1	15	15	I	·Input terminal for 32.768kHz X'tal
XT2	16	16	O	·Output terminal for 32.768kHz X'tal
RCIN	8	8	I	·Input terminal for RC oscillation Connect R between RCIN and RCOUT, and C between RCIN and VSS.
RCOUT	7	7	O	·Output terminal for RC oscillation Connect R between RCOUT and RCIN.
$\overline{\text{RES}}$	13	13	I	·Reset terminal
TEST1	11	11	-	·Test terminal Leave open circuit.
TEST2	12	12	-	·Test terminal Leave open circuit.

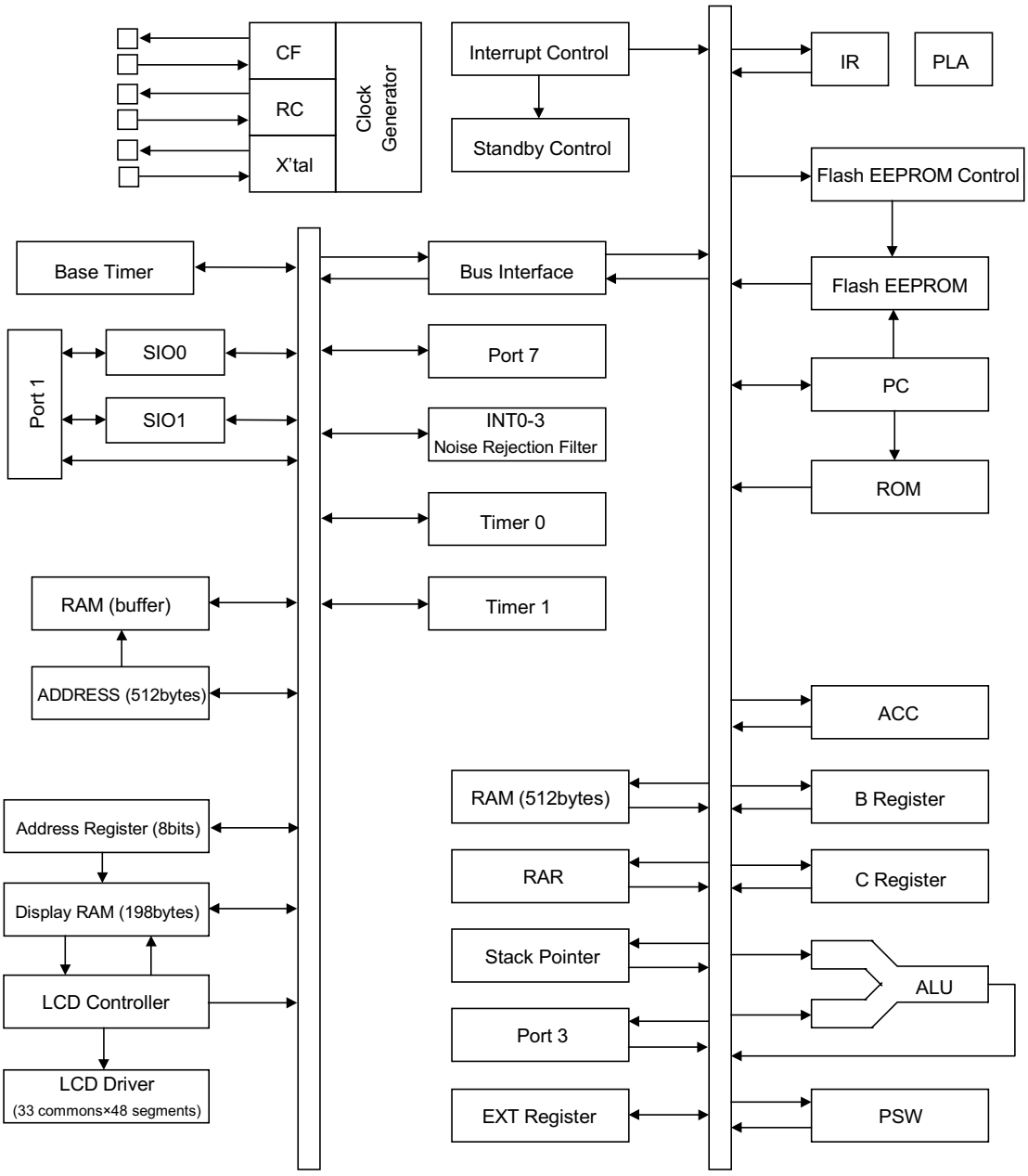
Continued.

Terminal	Pin No.	Pad No.	Input/ Output	Function Description
NCT1, NCT2, NCTC, NCTD, NCTE	10,9, 6,5 4	10,9 6,5 4	-	·Test terminal Leave open circuit.
$\overline{CE}$, $\overline{OE}$, $\overline{WE}$	45,47,117	43,45	I	·Memory test terminal Pull up to VDD.
EP, A10	119,46	113,44	I	·Memory test terminal Leave open circuit.
F/M_SEL	120	114	I	·Connect to VDD.
NC	36,37,38, 72,73,108, 109,144		-	·Unused terminal Leave open circuit.
NCEXT	1	1	I	·Test terminal Connect this terminal to VSS.

*Initial Port Status

Terminal	Input/Output	Pull-up Resistor Status
Port1	I	Programmable pull-up resistor: OFF
Port3	I	Programmable pull-up resistor: OFF

System Block Diagram



1. Absolute Maximum Ratings at Ta=+25°C, VSS=0V

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings Min.	Typ.	Max.	Unit
Supply voltage		VDDMAX	VDD			-0.3	to	+6.0	V
Input voltage		VI(1)	Port 71, 72, 73 $\overline{RES}$			-0.3	to	VDD+0.3	
		VI(2)	VLCD			-0.3	to	+6.5	
Output voltage		VO(1)	C1 to C33 S1 to S48			-0.3	to	VLCD+0.3	
		VO(2)	TEST1, TEST2, SUPCK			-0.3	to	VDD+0.3	
Input/output voltage		VIO(1)	Port 1, 3 Port 70 TEST1			-0.3	to	VDD+0.3	
High level output current	Peak output current	IOPH(1)	Port 1, 3 TEST1, TEST2, SUPCK	·CMOS output ·For each pin		-4			mA
	Total output current	ΣIOAH(1)	Port 3 C1 to C33, S1 to S48 TEST1, TEST2, SUPCK	Total of all pins		-25			
		ΣIOAH(2)	Port 1	Total of all pins		-25			
Low level output current	Peak output current	IOPL(1)	Port 1, 3 TEST1, TEST2, SUPCK	For each pin				20	
		IOPL(2)	Port 70	For each pin				15	
	Total output current	ΣIOAL(1)	Port 1	Total of all pins				40	
		ΣIOAL(2)	TEST1, TEST2, SUPCK	Total of all pins				40	
		ΣIOAL(3)	Port 70	Total of all pins				15	
		ΣIOAL(4)	C1 to C33, S1 to S48	Total of all pins				30	
		ΣIOAL(5)	Port 70	Total of all pins				15	
Maximum power consumption		Pdmax	SQFP144	Ta = 0°C to +50°C				400	mW
Operating temperature range		Topr				0		+50	°C
Storage temperature range		Tstg				-55		+125	

2. Recommended Operating Range at Ta=0°C to +50°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				VDD[V]	Min.	Typ.	Max.	
Operating supply voltage range	VDD(1)	VDD	98μs≦tCYC≦400μs		3.15		3.85	V
Hold voltage	VHD	VDD	RAM and register data are kept in HOLD mode.		2.0		3.85	
LCD voltage	VLCD	VLCD		3.15-3.85	VDD		6.0	
High level input voltage	VIH(1)	·Port 1, 3 ·Port 72, 73 (schmitt)	Output disable	3.15-3.85	0.7VDD		VDD	
	VIH(2)	·P70 port input/interrupt ·P71 $\overline{\text{RES}}$ (schmitt)	Output N-ch Tr.: OFF	3.15-3.85	0.7VDD		VDD	
Low level input voltage	VIL(1)	·Port 1, 3 ·Port 72, 73 (schmitt)	Output disable	3.15-3.85	VSS		0.3VDD	
	VIL(2)	·P70 port input/interrupt ·P71 $\overline{\text{RES}}$ (schmitt)	Output N-ch Tr.: OFF	3.15-3.85	VSS		0.3VDD	
Operation cycle time	tCYC			3.15-3.85	0.98		400	μs

3. Electrical Characteristics at Ta=0°C to +50°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings Min.	Ratings Typ.	Ratings Max.	Unit
High level input current	IIH(1)	Port 1, 3	·Output disable ·Pull-up MOS Tr.: OFF ·VIN=VDD (including OFF state leak current of output Tr.)	3.15–3.85			1	μA
	IIH(2)	Port 7 without pull-up MOS Tr.	·Output N-ch Tr.: OFF ·VIN=VDD (including OFF state leak current of output Tr.)	3.15–3.85			1	
	IIH(3)	$\overline{RES}$	VIN=VDD	3.15–3.85			1	
	IIH(4)	$\overline{CE}$, $\overline{OE}$, $\overline{WE}$	VIN=VDD	3.15–3.85			1	
Low level input current	IIL(1)	Port 1,3	·Output disable ·Pull-up MOS Tr.: OFF ·VIN=VSS (including OFF state leak current of output Tr.)	3.15–3.85	-1			
	IIL(2)	Port 7 without pull-up MOS Tr.	·Output N-ch Tr.: OFF ·VIN=VSS (including OFF state leak current of output Tr.)	3.15–3.85	-1			
	IIL(3)	$\overline{RES}$	VIN=VSS	3.15–3.85	-1			
	IIL(4)	A10, EP, F/M_SEL $\overline{CE}$, $\overline{OE}$, $\overline{WE}$	VIN=VSS	3.15–3.85	-1			
High level output voltage	VOH(1)	Port 0, 1, 3: CMOS output TEST1, TEST2, SUPCK	IOH=-0.1mA	3.15–3.85	VDD-0.5			V
Low level output voltage	VOL(1)	Port 1,3 TEST1, TEST2, SUPCK	·IOL=1mA ·IOL at any single pin is not over 1mA.	3.15–3.85			0.4	
	VOL(2)	Port 70	IOL=0.5mA	3.15–3.85			0.4	
Pull-up MOS Tr. resistance	Rpu	Port 1, 3, Port 7	VOH=0.9VDD	3.15–3.85	20	60	120	kΩ
Pull-down MOS Tr. resistance	Rpd	A10, EP, F/M_SEL	VOL=0.1VDD	3.15–3.85	25	50	100	
Hysteresis voltage	VHIS	Port 1, 3 Port 7 $\overline{RES}$	Output disable	3.15–3.85		0.1VDD		V
Pin capacitance	CP	All pins	·f=1MHz ·Every other terminal is connected to VSS. ·Ta=+25°C	3.15–3.85		10		pF

4. Serial Input/Output Characteristics at Ta=0°C to +50°C, VSS=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings Min.	Ratings Typ.	Ratings Max.	Unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5.	3.15-3.85	2			tCYC
		Low level pulse width	tCKL(1)			3.15-3.85	1			
		High level pulse width	tCKH(1)			3.15-3.85	1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	Refer to figure 5.	3.15-3.85	2			
		Low level pulse width	tCKL(2)			3.15-3.85		1/2tCYC		
		High level pulse width	tCKH(2)			3.15-3.85		1/2tCYC		
Serial input	Data set-up time		tICK	·SI0, SI1 ·SB0, SB1	·Data set-up to SCK0 and SCK1 ·Refer to figure 5.	3.15-3.85	0.4			µs
	Data hold time		tCKI			3.15-3.85	0.4			
Serial output	Output delay time (Using external clock)		tCKO(1)	·SO0, SO1 ·SB0, SB1	·Data hold from SCK0 and SCK1 ·Refer to figure 5.	3.15-3.85			7/12tCYC +1	µs
	Output delay time (Using internal clock)		tCKO(2)	·SO0, SO1 ·SB0, SB1	·Data hold from SCK0 and SCK1 ·Refer to figure 5.	3.15-3.85			1/3tCYC +1	

5. Pulse Input Conditions at Ta=0°C to +50°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings Min.	Ratings Typ.	Ratings Max.	Unit
High/low level pulse width	tPIH(1) tPIL(1)	·INT0, INT1 ·INT2/T0IN ·Refer to figure 6.	·Interrupt acceptable ·Timer 0-countable	3.15-3.85	1			tCYC
	tPIH(2) tPIL(2)	·INT3/T0IN (1/1 is selected for noise rejection clock.) ·Refer to figure 6.	·Interrupt acceptable ·Timer 0-countable	3.15-3.85	2			
	tPIH(3) tPIL(3)	·INT3 (1/64 is selected for noise rejection clock.) ·Refer to figure 6.	·Interrupt acceptable	3.15-3.85	128			
	tPIL(4)	·$\overline{\text{RES}}$ ·Refer to figure 6.	·Reset acceptable	3.15-3.85	200			µs

6. Sample Current Consumption Characteristics at Ta=0°C to +50°C, VSS=0V

The sample current consumption characteristics are the measurement result of Sanyo provided evaluation board.
The currents through the output transistors and the pull-up MOS transistors are ignored.

• Flash Memory Operation

Parameter	Symbol	Pins	Conditions	OCR7	VDD[V]	Ratings Min.	Typ.	Max.	Unit
Current consumption during normal operation *(Note 1)*	IDDOP(6)	VDD	·FmCF=6MHz by ceramic resonator ·FsX'tal=32.768kHz by X'tal ·System clock: CF oscillation ·RC oscillation stops.	1	3.15-3.85		8	20	mA
	IDDOP(7)		·FmCF=0Hz (No oscillation)	0			2.0	4	
	IDDOP(8)		·FsX'tal=32.768kHz by X'tal ·System clock: RC oscillation	1			2.5	5	
	IDDOP(9)		·FmCF=0Hz (No oscillation)	0	3.15-3.85		200	500	μA
	IDDOP(10)		·FsX'tal=32.768kHz by X'tal ·System clock: X'tal ·RC oscillation stops.	1			450	750	

• BIOS Program Operation

Parameter	Symbol	Pins	Conditions	OCR7	VDD[V]	Ratings Min.	Typ.	Max.	Unit
Current consumption during writing to flash memory *(Note 1)*	IDDOP(11)	VDD	·FmCF=6MHz by ceramic resonator ·FsX'tal=32.768kHz by X'tal ·System clock: CF oscillation ·RC oscillation stops.	1	3.15-3.85		8	15	mA
	IDDOP(12)		·FmCF=0Hz (No oscillation)	0	3.15-3.85		4.5	10	
			·FsX'tal=32.768kHz by X'tal ·System clock: RC oscillation	1			5	12	

*OCR7: Bit 7 of the oscillation control register

• BIOS Program Operation

Parameter	Symbol	Pins	Conditions	OCR7	VDD[V]	Ratings Min.	Ratings Typ.	Ratings Max.	Unit
Current consumption in HALT mode *(Note 1)*	IDDHALT(1)	VDD	·HALT mode ·FmCF=6MHz by ceramic resonator ·FsX'tal=32.768kHz by X'tal ·System clock: CF oscillation ·RC oscillation stops. ·Refer to figure 7.	1	3.15-3.85		2.5	5	mA
	IDDHALT(2)		·HALT mode ·FmCF=0Hz (No oscillation) ·FsX'tal=32.768kHz by X'tal ·System clock: RC oscillation ·Refer to figure 7.	0	3.15-3.85		250	600	µA
	IDDHALT(3)			1			350	700	
	IDDHALT(4)		·HALT mode ·FmCF=0Hz (No oscillation) ·FsX'tal=32.768kHz by X'tal ·System clock: X'tal ·RC oscillation stops. ·Refer to figure 7.	0	3.15-3.85		15	50	µA
	IDDHALT(5)			1			20	70	
Current consumption in HOLD mode *(Note 1)*	IDDHOLD(1)	VDD	·HOLD mode ·Refer to figure 7.		3.15-3.85		0.05	30	

• Flash Memory Operation

Parameter	Symbol	Pins	Conditions	OCR7	VDD[V]	Ratings Min.	Ratings Typ.	Ratings Max.	Unit
Current consumption in HALT mode *(Note 1)*	IDDHALT(6)	VDD	·HALT mode ·FmCF=6MHz by ceramic resonator ·FsX'tal=32.768kHz by X'tal ·System clock: CF oscillation ·RC oscillation stops. ·Refer to figure 7.	1	3.15-3.85		2.5	5	mA
	IDDHALT(7)		·HALT mode ·FmCF=0Hz (No oscillation) ·FsX'tal=32.768kHz by X'tal ·System clock: RC oscillation ·Refer to figure 7.	0	3.15-3.85		200	500	µA
	IDDHALT(8)			1			400	800	
	IDDHALT(9)		·HALT mode ·FmCF=0Hz (No oscillation) ·FsX'tal=32.768kHz by X'tal ·System clock: X'tal ·RC oscillation stops. ·Refer to figure 7.	0	3.15-3.85		15	50	µA
	IDDHALT(10)			1			20	70	

Note 1: The current through the output transistors, the pull-up MOS transistors, and the bleeder resistors for the display power supply are ignored.

7. LCD Driver Characteristics at Ta=0°C to +50°C, VSS=0V

Parameter	Symbol	Pins, Conditions	VDD[V]	Ratings Min.	Typ.	Max.	Unit
Voltage drop between Vx and Ci (x: 1-5) (i: 1-33)	|VD1|	·-15μA (only on Ci terminal) ·LCD: ON ·1/5 bias ·V5=VDD	3.3			120	mV
Voltage drop between Vx and Ci (x: 1-5) (i: 1-33)	|VD2|	·+15μA (only on Ci terminal) ·LCD: ON ·1/5 bias ·V5=VDD	3.3	-120			
Voltage drop between Vx and Si (x: 1-5) (i: 1-48)	|VD3|	·-15μA (only on Si terminal) ·LCD: ON ·1/5 bias ·V5=VDD	3.3			120	
Voltage drop between Vx and Si (x: 1-5) (i: 1-48)	|VD4|	·+15μA (only on Si terminal) ·LCD: ON ·1/5 bias ·V5=VDD	3.3	-120			
V4 output voltage	VV4	·LCD clock frequency=0Hz ·LCD: ON ·1/5 bias ·V5=VDD ·Refer to figure 9.	3.3	0.75VDD	0.8VDD	0.85VDD	V
V3 output voltage	VV3		3.3	0.55VDD	0.6VDD	0.65VDD	
V2 output voltage	VV2		3.3	0.35VDD	0.4VDD	0.45VDD	
V1 output voltage	VV1		3.3	0.15VDD	0.2VDD	0.25VDD	

Sample LCD Power Supply Characteristics at Ta=0°C to +50°C, VSS=0V

The sample current consumption characteristics are the measurement result of Sanyo provided evaluation board.

Parameter	Symbol	Pins, Conditions		VDD[V]	Ratings Min.	Typ.	Max.	Unit
LCD Power supply	ILCD1	·LCD: ON ·1/5 bias ·VLCD=VDD ·V1-V5: open ·Refer to figure 8.	20kΩmode	3.3	15	29	60	μA

VCCR: LCD contrast control register

Notes: • *Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.*

• *When using the ceramic resonator or the X'tal, please contact with the oscillator manufacturer for the circuit parameters.*

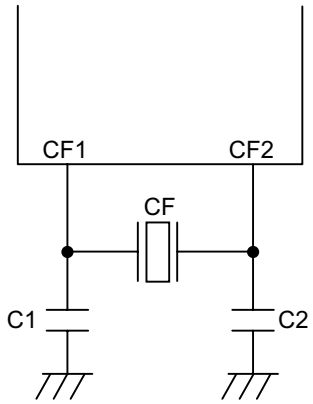


Figure 1 Ceramic Oscillation Circuit.

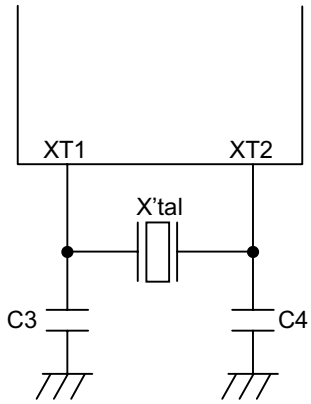


Figure 2 X'tal Oscillation Circuit.

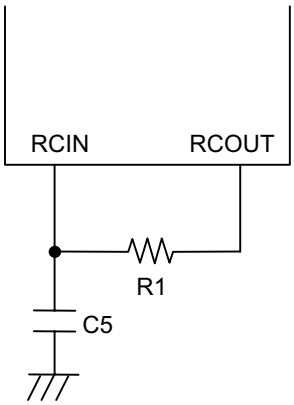


Figure 3 RC Oscillation Circuit.

Recommended Oscillation Circuit and Characteristics

The oscillation circuit characteristics in the table below are based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- The characteristics are the results of the evaluation with the recommended circuit parameters connected externally.

Recommended Oscillation Circuit Parameters and Characteristics (Ta = 0°C to +50°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameter	Operating supply voltage range	Oscillation stabilizing time (*)	
					Typ.	Max.
6MHz	MURATA MANUFACTURING CO., LTD.	CSA6.00MG	C1=33pF C2=33pF	3.15-3.85V	TmsCF	
					0.02ms	0.2ms
32.768kHz	CITIZEN WATCH CO., LTD.	CFS-308	C3=20pF C4=20pF	3.15-3.85V	TssX'tal	
					1.00s	3.00s

(*) Note: The oscillation stabilizing time period is the time until the oscillation becomes stable after the VDD becomes higher than the minimum operating voltage.

The oscillation circuit characteristics may differ by applications. For further assistance, please contact with the oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.

Since the oscillation circuit characteristics are affected by the noise, wiring capacity, etc., refer to the following notices.

- The distance between the clock I/O terminal and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or the signal line with large amplitude such as middle withstand voltage port or LCD driver output should be allocated away from the clock oscillation circuit.
- The signal lines with large current should be allocated away from the oscillation circuit.

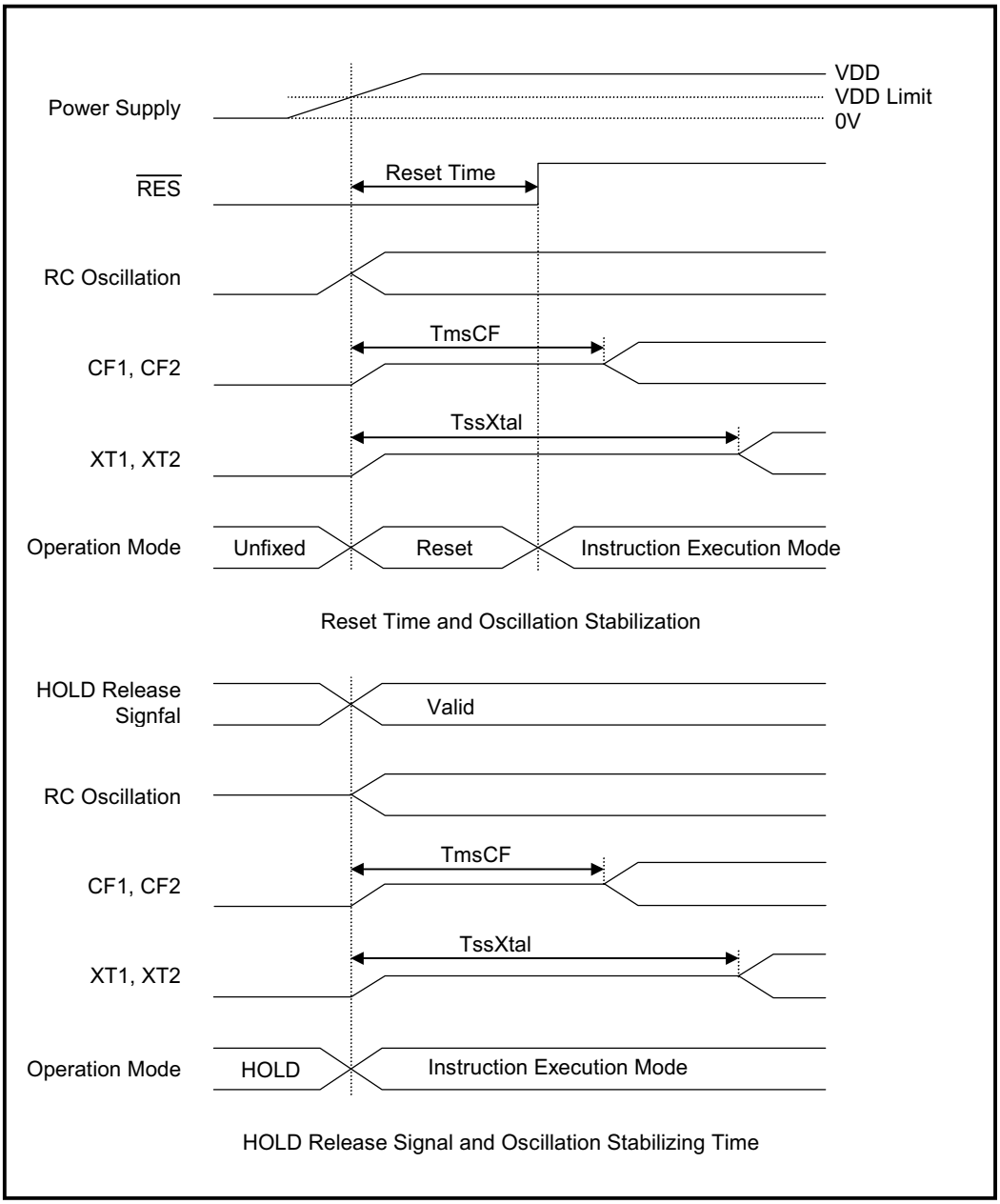
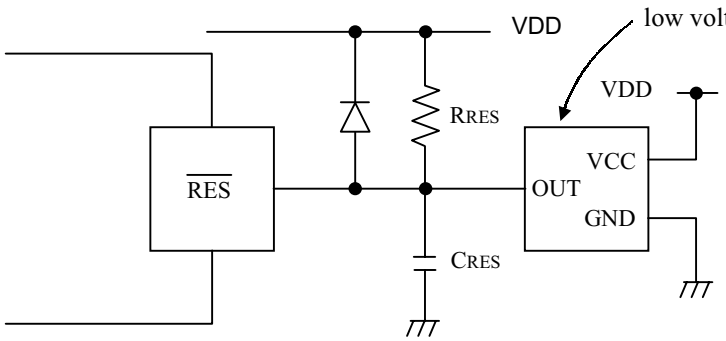
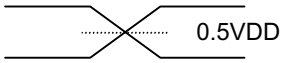


Figure 3 Oscillation Stabilizing Time.



Note: Use the low voltage detect reset IC which resets the microcontroller when the power supply voltage drops below the limit of the operable supply voltage.

Figure 4 Reset Circuit.



AC Timing Measurement Point

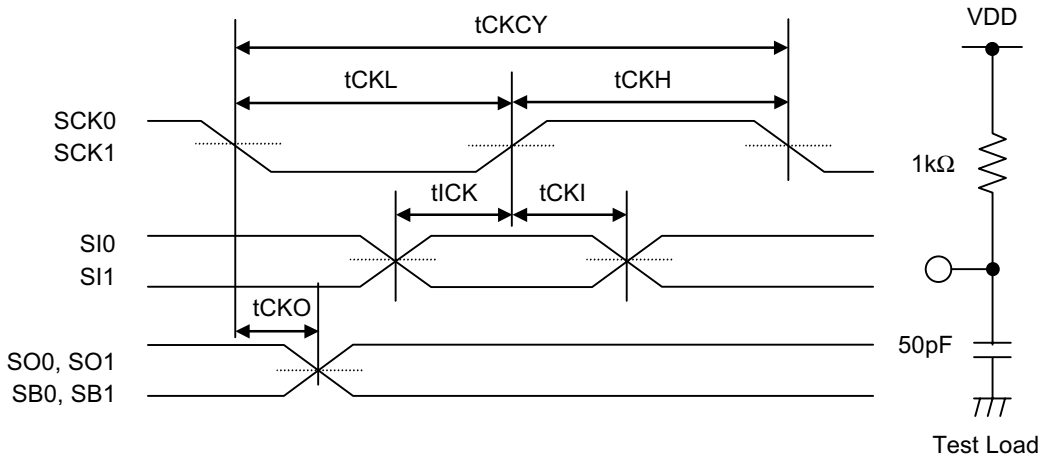


Figure 5 Serial Input Test Condition.

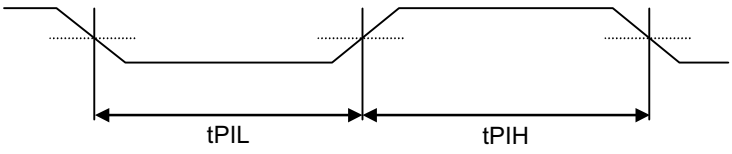


Figure 6 Pulse Input Timing Condition.

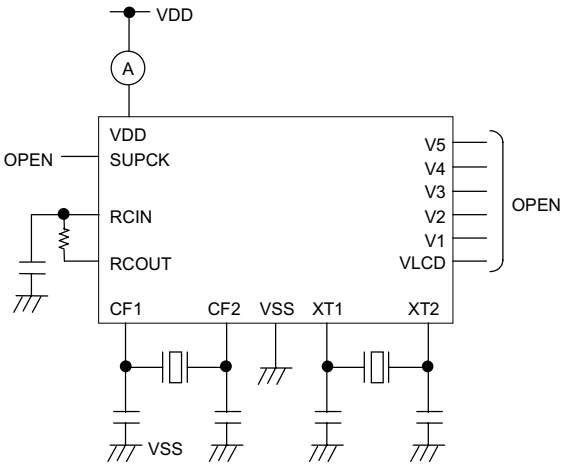


Figure 7 Current Consumption Measurement Circuit.

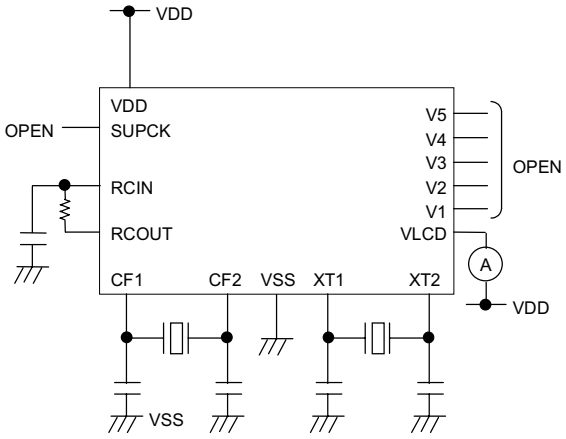


Figure 8 LCD Current Measurement Circuit.

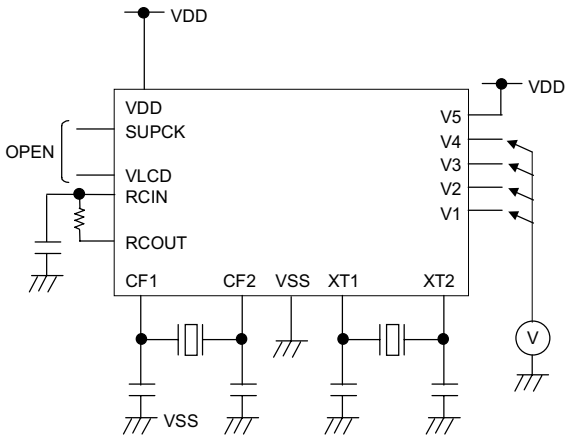


Figure 9 V1 - V4 Terminal Output Voltage Measurement Circuit.

- Evaluation Sample

The evaluation sample of LC86F1216 is provided in QIC144 (package). Take note that the package size will be a little different from the one made in mass-production.