Ordering number : ENA0120A

SANYO Semiconductors
DATA SHEET

LC86F3448B

CMOS IC
64K-byte Flash Memory (ROM 48K-byte+CGROM 16K-byte)
on-chip 640-byte RAM and 352x9 bit Display RAM

8-bit 1-chip Microcontroller

Overview

The LC86F3448B is a CMOS 8-bit single chip microcontroller with Flash Memory for the LC863400series.
This microcontroller contains the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.424µs
- On-chip ROM capacity: 64K bytes Flash Memory
  Program ROM: 48K bytes
  CGROM: 16K bytes
- On-chip RAM capacity: 640 bytes
- OSD RAM: 352×9 bits
- Closed-Caption TV controller and the on-screen display controller
- Closed-Caption data slicer
- Four channels×6-bit AD Converter
- Three channels×7-bit PWM
- Two 16-bit timer/counter, 14-bit base timer
- IIC-bus compliant serial interface circuit (Multi-master type)
- ROM correction function
- 11-source 8-vectored interrupt system

Continued on next page.

Note : This product includes the IIC bus interface circuit. If you intend to use the IIC bus interface, please notify us of this in advance of our receiving your program ROM code order.
Purchase of SANYO IIC components conveys a license under the Philips IIC Patents Rights to use these components in an IIC system, provided that the system conforms to the IIC Standard Specification as defined by Philips.

Trademarks
IIC is a trademark of Philips Corporation.

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Continued from preceding page.

- Integrated system clock generator and display clock generator
  Only one X'tal oscillator (32.768kHz) for PLL reference is used for both generators

All of the above functions are fabricated on a single chip.
The program is rewritable by using the on-board writing system after the LSI has been installed on the application board.
The LC86F3448B change to LC863500 series by writing program data of LC863500 series into the Flash Memory

Features

■Built-in Flash Memory
64K bytes
- Program ROM 48K bytes
- Character ROM 16K bytes
- Rewritable in page units 128 bytes / page
- Page erase / program cycle 100 cycle per page (Ta=25±2°C)

■Random Access Memory (RAM)
640 × 8 bits (including 128 bytes for ROM correction function)
352 × 9 bits (for CRT display)

The LC86F3448B consists of 48K bytes of Program ROM space and 640 bytes of RAM space. For this microcontroller, the usable program ROM capacity and RAM capacity are the same size for the mask ROM version.

Mask ROM versions compatible with the LC86F3448B	Program ROM limit set for the LC86F3448B	RAM limit set for the LC86F3448B (including 128 bytes for the ROM correction function)
LC863448 / LC863548	49152 bytes	640 bytes
LC863440 / LC863540	40960 bytes	640 bytes
LC863432 / LC863532	32768 bytes	512 bytes
LC863428 / LC863528	28672 bytes	512 bytes
LC863424 / LC863524	24576 bytes	512 bytes
LC863420 / LC863520	20480 bytes	512 bytes
LC863416/ LC863516	16384 bytes	512 bytes

When using on-board rewriting system is selected by the option, the rewriting program (loader program) is allocated in the last 2K-byte of the memory ,following to 46K-byte (B800h)

■OSD Functions
- Screen display : 36 characters×16 lines (by software)
- RAM : LC863400 series : 352 words (9 bits per word)
  Display area : 36 words×8 lines
  Control area : 8 words×8 lines
  LC863500 series : 176 words (9 bits per word)
  Display area : 36 words×4 lines
  Control area : 8 words×4 lines
- Characters
  Up to 252 kinds of 16×32 dot character fonts (4 characters including 1 test character are not programmable)
  Each font can be divided into two parts and used as two fonts (Ex. 16×16 dot character font×2)
  At least 111 characters need to be divide between a 16×18 dot and 8×9 dot character font to display the caption fonts.
- Various character attributes
  Character colors : 16colors (analog mode: lVp-p output) / 8colors (digital mode)
  Character background colors : 16colors (analog mode: lVp-p output) / 8colors (digital mode)
  Fringe / shadow colors : 16colors (analog mode: lVp-p output) / 8colors (digital mode)
  Full screen colors : 16colors (analog mode: lVp-p output) / 8colors (digital mode)
  Rounding
  Underline
  Italic character (slanting)
- Attribute can be changed without spacing

- Vertical display start line number can be set for each row independently (Rows can be overlapped)
- Horizontal display start position can be set for each row independently
- Horizontal pitch (9 to 16 dots)*1 and vertical pitch (1 to 32 dots) can be set for each row independently
- Different display modes can be set for each row independently
  Caption • Text mode / OSD mode 1 / OSD mode 2 (Quarter size) / Simplified graphic mode
- Ten character sizes *1
  Horez. × Vert. = (1×1), (1×2), (2×2), (2×4), (0.5×0.5)
  (1.5×1), (1.5×2), (3×2), (3×4), (0.75×0.5)

- Shuttering and scrolling on each row
- Simplified Graphic Display

Note *1: range depends on display mode : refer to the manual for details.

■Data Slicer (closed caption format)
- Closed caption data and XDS data extraction
- NTSC/PAL, and extracted line can be specified

■Bus Cycle Time / Instruction-Cycle Time

Bus Cycle Time	Instruction Cycle Time	Clock Divider	System Clock Oscillation	Oscillation Frequency	Voltage
0.424µs	0.848µs	1/2	Internal VCO	14.156MHz	4.5V to 5.5V
7.5µs	15.0µs	1/2	Internal RC	800kHz	4.5V to 5.5V
91.55µs	183.1µs	1/1	Crystal	32.768kHz	4.5V to 5.5V
183.1µs	366.2µs	1/2	Crystal	32.768kHz	4.5V to 5.5V

■Ports
- Input / Output Ports : LC863400 series : 4 ports (23 terminals)
  : LC863500 series : 4 ports (24 terminals)

  Data direction programmable in nibble units : 1 port (8 terminals)
  (If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.)
  Data direction programmable for each bit individually: LC863400 series : 4 ports (15 terminals)
  : LC863500 series : 4 ports (16 terminals)

■AD Converter
- 4 channels×6-bit AD converters

■Serial Interfaces
- IIC-bus compliant serial interface (Multi-master type)
  Consists of a single built-in circuit with two I/O channels. The two data lines and two clock lines can be connected internally.

■PWM Output
- 3 channels×7-bit PWM

■Timer
- Timer 0 : 16-bit timer/counter
  With 2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with a programmable prescaler
  Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with a programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of timer is 1 tCYC.
- Timer 1 : 16-bit timer/PWM (LC863500 series only)
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable bit PWM (9 to 16 bits)
  In mode 0/1, the resolution of Timer1/PWM is 1 tCYC
  In mode 2/3, the resolution is selectable by program; tCYC or 1/2 tCYC

• Base Timer
Generate every 500ms overflow for a clock application
(using 32.768kHz crystal oscillation for the base timer clock)
Generate every 976μs, 3.9ms, 15.6ms, 62.5ms overflow
(using 32.768kHz crystal oscillation for the base timer clock)
Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0

■Remote Control Receiver Circuit (connected to the P73/INT3/T0IN terminal)
- Noise rejection function
- Polarity switching

■Watchdog Timer
External RC circuit is required
Interrupt or system reset is activated when the timer overflows

■ROM Correction Function
Max 128 bytes / 2 addresses

■Interrupts
- LC863400 series : 12 source 8 vectored interrupts
  LC863500 series : 13 source 8 vectored interrupts
  1. External Interrupt INT0
  2. External Interrupt INT1
  3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
  4. External Interrupt INT3, base timer
  5. Timer/counter T0H (Upper 8 bits)
  6. Data slicer(LC863400 series only)
     Timer TIH,TIL (LC863500 series only)
  7. Vertical synchronous signal interrupt ($\overline{VS}$), Scan line
  8. IIC, Software
- Interrupt Priority Control
  Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 8 listed above. For the external interrupt INT0 and INT1, low or highest priority can be set.

■Sub-routine Stack Level
- A maximum of 128 levels (stack is built in the internal RAM)

■Multiplication/Division Instruction
- 16 bits×8 bits (7 instruction cycle times)
- 16 bits÷8 bits (7 instruction cycle times)

■3 Oscillation Circuits
- Built-in RC oscillation circuit used for the system clock
- Built-in VCO circuit used for the system clock and OSD
- X'tal oscillation circuit used for base timer, system clock and PLL reference

■Standby Function
- HALT mode
  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This mode can be released by the interrupt request or the system reset.
- HOLD mode
  The HOLD mode is used to stop the oscillations; RC (internal), VCO, and X'tal oscillations. This mode can be released by the following conditions.
  - Pull the reset terminal ($\overline{RES}$) to low level.
  - Feed the selected level to either P70/INT0 or P71/INT1.

■Applicable Mask ROM Version
- LC863448 / LC863440 / LC863432 / LC863428 / LC863424/ LC863420 / LC863416
- LC863548 / LC863540 / LC863532 / LC863528 / LC863524/ LC863520 / LC863516

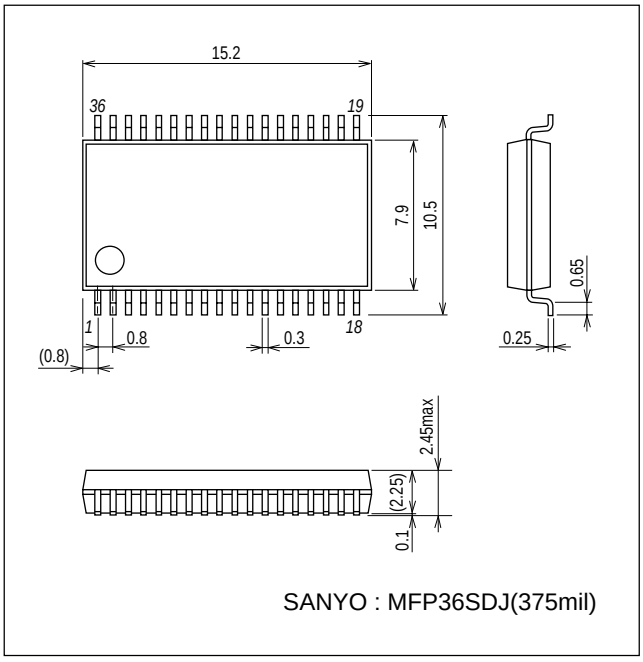
■Package
- MFP36SDJ (Lead-free type)
- DIP36S (Lead-free type)

■Development Tools
- Evaluation chip: LC863096
- Emulator: EVA86000 (main) + ECB863400 (evaluation chip board)
  + POD36-CABLE (cable)
  + POD36-DIP (for DIP36S)
  or POD36-MFP (for MFP36SDJ)

Write Flash Memory SANYO provides special services including writing data to Flash Memory and stamping. There is a charge for these services. Please feel free to ask our sales persons for details.

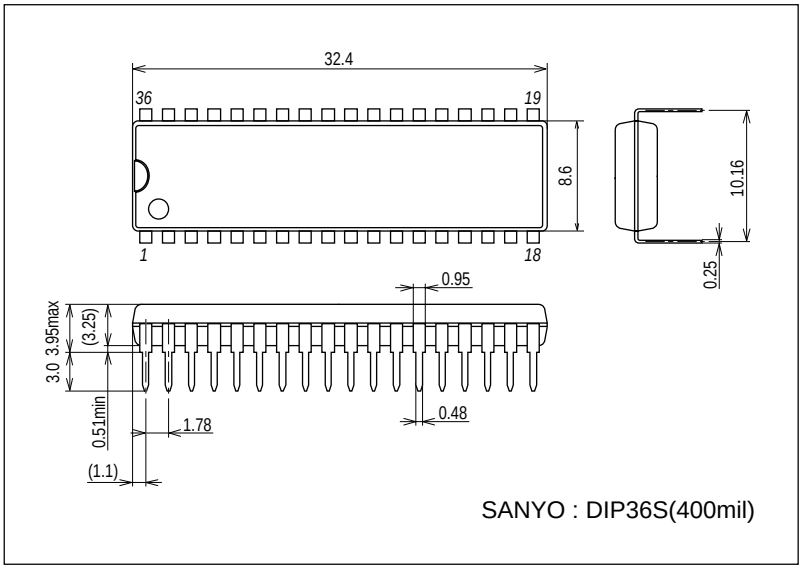
Package Dimensions

unit : mm (typ)
3263

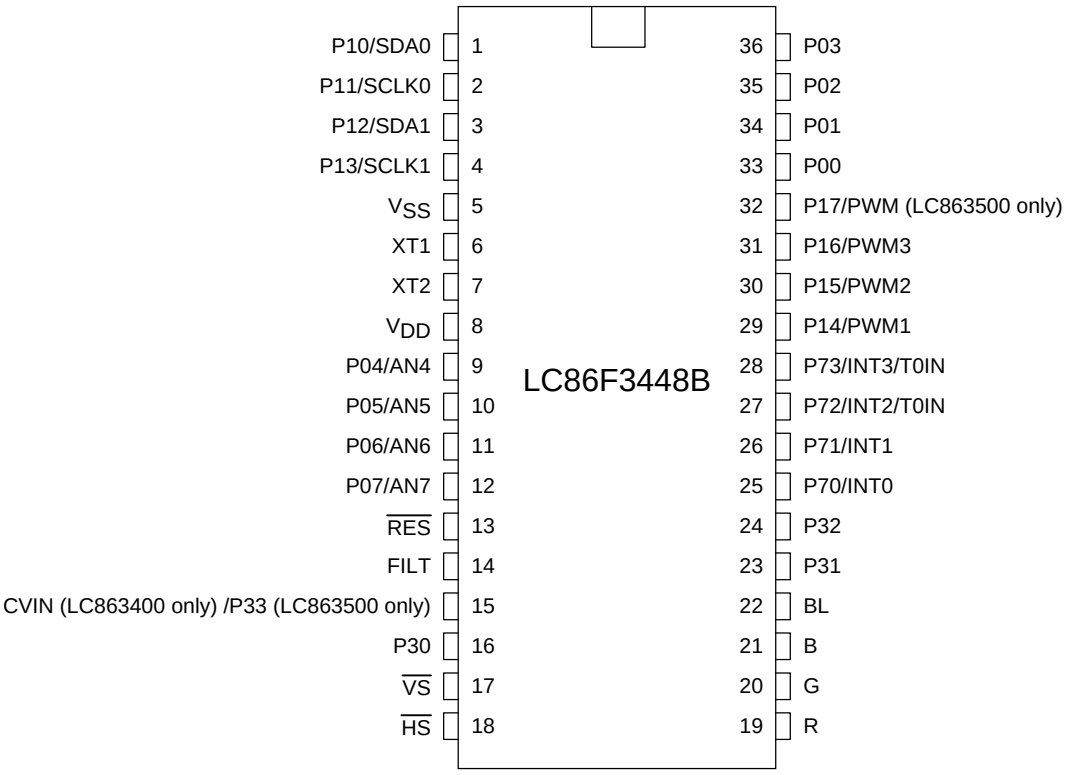


Package Dimensions

unit : mm (typ)
3170A



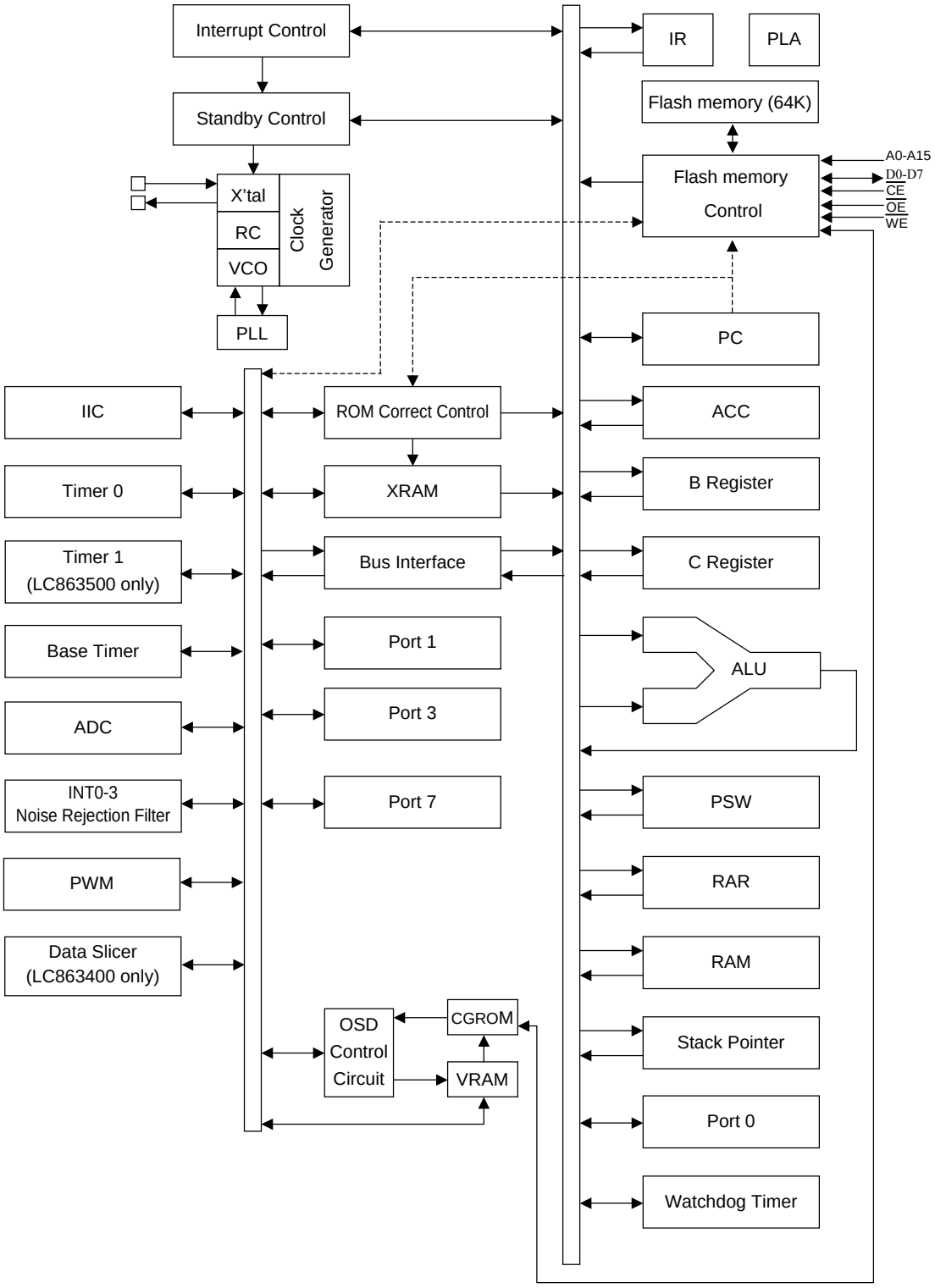
Pin Assignment



Top view

SANYO: MFP36SDJ “Lead-free Type”
SANYO: DIP36S “Lead-free Type”

System Block Diagram



Pin Description

Pin Description Table

<table>
<tr><th>Terminal</th><th>I/O</th><th>Function Description</th><th>Option</th><th>Flash Memory Mode
(Parallel input/
output mode)</th></tr>
<tr><td>V_{SS}</td><td>-</td><td>Negative power supply</td><td></td><td></td></tr>
<tr><td>XT1</td><td>I</td><td>Input terminal for crystal oscillator</td><td></td><td></td></tr>
<tr><td>XT2</td><td>O</td><td>Output terminal for crystal oscillator</td><td></td><td></td></tr>
<tr><td>V_{DD}</td><td>-</td><td>Positive power supply</td><td></td><td></td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset terminal</td><td></td><td>Input to set up mode</td></tr>
<tr><td>FILT</td><td>O</td><td>Filter terminal for PLL</td><td></td><td></td></tr>
<tr><td>CVIN</td><td>I</td><td>Video signal input terminal(LC863400 only)</td><td></td><td></td></tr>
<tr><td>$\overline{VS}$</td><td>I</td><td>Vertical synchronization signal input terminal</td><td></td><td>Input to set up mode</td></tr>
<tr><td>$\overline{HS}$</td><td>I</td><td>Horizontal synchronization signal input terminal</td><td></td><td></td></tr>
<tr><td>R</td><td>O</td><td>Red (R) output terminal of RGB image output</td><td></td><td>Address input A8</td></tr>
<tr><td>G</td><td>O</td><td>Green (G) output terminal of RGB image output</td><td></td><td>Address input A9</td></tr>
<tr><td>B</td><td>O</td><td>Blue (B) output terminal of RGB image output</td><td></td><td>Address input A10</td></tr>
<tr><td>BL</td><td>O</td><td>Fast blanking control signal
Switch TV image signal and caption/OSD image signal</td><td></td><td>Address input A11</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>•8-bit input/output port,
Input/output can be specified in nibble unit
•Other functions
AD converter input port (P04 to P07)</td><td>Pull-up resistor
provided/not provided
Output Format
CMOS/Nch-OD</td><td>Address input
A0 to A7</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>•8-bit input/output port
Input/output can be specified for each bit
(programmable pull-up resister provided)
•Other functions
P10: IIC0 data I/O
P11: IIC0 clock output
P12: IIC1 data I/O
P13: IIC1 clock output
P14: PWM1 output
P15: PWM2 output
P16: PWM3 output
P17: Timer1 (PWM) output (LC863500 only)</td><td>Output Format
CMOS/Nch-OD</td><td>Data input/output
D0 to D7</td></tr>
<tr><td>Port 3
P30 to P33</td><td>I/O</td><td>•LC863400:3-bit input/output port(P30toP32)
LC863500: 4-bit input/output port(P30toP33)
Input/output can be specified for each bit
(CMOS output/input with programmable pull-up resister)</td><td></td><td>Control signal $\overline{WE}$
Control signal $\overline{OE}$
Control signal $\overline{CE}$</td></tr>
<tr><td>Port 7
P70
P71 to P73</td><td>I/O</td><td>•4-bit input/output port
Input or output can be specified for each bit
P70: I/O with programmable pull-up resister
P71 to P73: CMOS output/input with programmable pull-up resister
•Other functions
P70: INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer
P71: INT1 input/HOLD release input
P72: INT2 input/Timer 0 event input
P73: INT3 input (noise rejection filter connected)/ Timer 0 event input
Interrupt receiver format, vector addresses
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ Falling</th><th>H level</th><th>L level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>Address input
A12 to A15</td><td></td></tr>
</table>

Note: A capacitor of at least 10μF must be inserted between V_{DD} and V_{SS} when using this IC.

- Output form and existence of pull-up resistor for all ports can be specified for each bit.
- Programmable pull-up resistor is always connected regardless of port option, CMOS or N-ch open drain output in port 1.

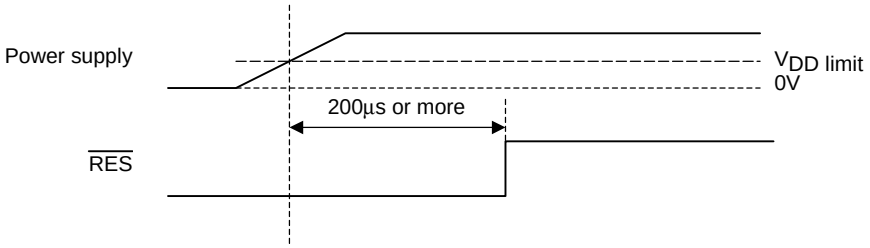
User Options

User options can be changed using Flash Memory data.

A kind of option	Pin, Circuits	
Input/output form of input/output ports	Port 0 (Specified in a bit)	1. Input: Without pull-up MOS Tr. Output: N-channel open drain 2. Input: With pull-up MOS Tr. Output: CMOS
	Port 1 (Specified in a bit)	1. Input: With programmable pull-up MOS Tr. Output: N-channel open drain 2. Input: With programmable pull-up MOS Tr. Output: CMOS

Notice for Use

- Input level of terminal $\overline{\text{RES}}$ at power on
  Terminal $\overline{\text{RES}}$ must be held low for at least 200μs after the supply voltage exceeds the power supply lower limit.



- Difference between the Mask version and Flash version
  1. The operation after release of reset: The mask version operates the program from the address 0 in the program counter as soon as detecting the H level on the reset port.
     The flash version operates the program from the address 0 in the program counter after setting the option.
  2. Current dissipation : Please refer to the latest semiconductor news.

- Conditions during reset and after release of reset
  Port options are set using Flash Memory data.
  Port options are set internally within approximately 3ms after logic HIGH is applied to the RESET terminal. The configuration of the port outputs change over the duration of this period. Then the Program Counter is set to 0 and program execution begins.
  During reset, and in the few hundred milliseconds after reset is released, the port options on certain of the ports will not yet have been set. The conditions of the various ports during reset or on release of reset have been collected in the following table. Please refer to it when analyzing circuits where these conditions apply.

Pins	Options	Condition during and on release of reset
P0	Input: Without pull-up MOS transistor Output: N-channel open drain	Output -off Input mode: High impedance
	Input: With pull-up MOS transistor Output: CMOS	Output-off Flash version: During reset and in the first few hundred µs after reset is released, the pull-up MOS transistor is OFF. Thereafter, set to input mode with pull-up MOS Tr. ON Mask version: During reset the pull-up MOS transistor is OFF. After soon, set to input mode with pull-up MOS Tr. ON
P1	Input: With programmable pull-up MOS transistor Output: N-channel open drain	Output-off Input mode: High impedance
	Input: With programmable pull-up MOS transistor Output: CMOS	
P3	No options Input: With programmable pull-up MOS transistor Output: CMOS	Output -off Input mode: High impedance
P7	No options Input: With programmable pull-up MOS transistor Output: With pull-up MOS (P70) CMOS (P71 to P73)	Output-off Input mode: High impedance

On-board writing system

The LC86F3448B has the On-board writing system. The program is renewable by using SANYO Flash On-board System after the LSI has been installed on the application board.
This system is composed of 4 types divided by the combination of mode setting pin and communication pin.
Each type system has to connect the 6 pins (V_{DD}, V_{SS}, $\overline{RES}$, communication pins) with the interface board of SANYO Flash On-board System.
It is necessary that the pins to be used for the rewriting system should be able to be separated from the application board properly.
The system type is selected by the option setting program (Su86K.exe).

types	mode setting pin	communication pins
type1	$\overline{RES}$ pin (high voltage (12V) applied)	P30(DATA1), P31(DATA0), P32(CLK)
type2	$\overline{RES}$ pin (high voltage (12V) applied)	P30(DATA1), P11(DATA0), P10(CLK)
type3	P30 pin (High level voltage (5V) applied)	P30(ENA/DATA1), P31(DATA0), P32(CLK)
type4	P30 pin (High level voltage (5V) applied)	P30(ENA/DATA1), P11(DATA0), P10(CLK)

• Type 3 or 4 is selected : P30 is exclusive for the on-board system. This pin must always be pulled-down, so this pin can't be used for other applications.

• The loader program must be written into the ROM to use On-board writing system.
The loader program should be written into the ROM before the LSI has been installed on the board by the general purpose PROM programs.
When the option setting selects the this system to use, the loader program automatically links on the user program linking.

Please ask to our sales persons before using On-board writing system.

Method of how to rewrite it in FLASH programmer / SANYO FLASH writing tool (SFWS)

When reading or writing data to the LC86F3448B , FLASH programmer of our recommendation or SANYO FLASH writing tool (SFWS) is used. In both cases, exclusive conversion board (W86F3448D, W86F3448M) is needed.

(1) FLASH programmer of our recommendation

Single Word Write

Manufacture	Name of device	version	applicable device (code)	Data protection setting after write operation
Flash Support Group co. (the former Ando Electric)	AF9708	Rev2.43	SANYO LC86F3448B (3B223)	Protected

Write Multiple Words

Manufacture	Name of device	version	applicable device (code)	Data protection setting after write operation
Flash Support Group co. (the former Ando Electric)	AF9723 + AF9833	RevX.XX *1	SANYO LC86F3448B (XXXX)	Protected

*1: Registration is being requested.

The LC86F3448B does not support a silicon signature feature.
Do not use the feature (automatic device type selection) when programming this device.
To avoid erasing the program, confirm the setting of the protection for activating the written program before using.
It can't be written with device code 29EE512

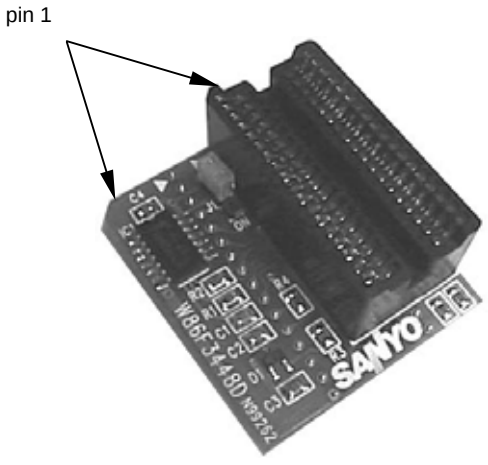
(2) SANYO FLASH writing tool (SFWS)

PC is connected with writer unit (SKK) by USB cable and it uses it.

(3) Exclusive writing conversion board

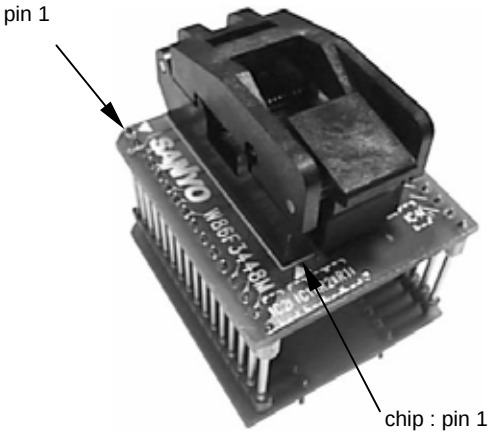
- W86F3448D • • • DIP36S purpose (It is common with production discontinuance model (LC86F3448A / LC86F3548A))
- W86F3448M • • • MFP36SDJ purpose (It is common with production discontinuance model (LC86F3448A/ LC86F3548A))

When using the conversion board, all of the jumper SW must be set to the OFF position.
If set to the ON position, read/write operations will not perform correctly.
Pin 1 of the conversion board should be located as indicated below.



Set jumper SW to OFF

W86F3448D



Set jumper SW to OFF

W86F3448M

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter		Symbol	Pins	Conditions	V_{DD}[V]	Ratings min	Ratings typ	Ratings max	unit
Maximum supply voltage		V_{DD} max	V_{DD}			-0.3		+6.5	V
Input voltage		V_I(1)	$\overline{RES}$, $\overline{HS}$, $\overline{VS}$, CVIN (LC863400 only)			-0.3		V_{DD}+0.3	V
Output voltage		V_O(1)	R, G, B, BL, FILT			-0.3		V_{DD}+0.3	V
Input/output voltage		V_{IO}	Ports 0, 1, 3, 7			-0.3		V_{DD}+0.3	V
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 3, 7	•CMOS output •For each pin.		-4			mA
		IOPH(2)	R, G, B, BL	•CMOS output •For each pin.		-5			mA
	Total output current	ΣIOAH(1)	Ports 0, 1	The Total of all pins.		-20			mA
		ΣIOAH(2)	Ports 3, 7	The Total of all pins.		-10			mA
		ΣIOAH(3)	R, G, B, BL	The Total of all pins		-12			mA
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3	For each pin.				20	mA
		IOPL(2)	Port 7	For each pin.				15	mA
		IOPL(3)	R, G, B, BL	For each pin.				5	mA
	Total output current	ΣIOAL(1)	Ports 0, 1	The Total of all pins				40	mA
		ΣIOAL(2)	Ports 3, 7	The Total of all pins.				30	mA
		ΣIOAL(3)	R, G, B, BL	The Total of all pins.				15	mA
Maximum power dissipation		Pd max	MFP36SDJ	Ta=-10 to +70ºC				350	mW
			DIP36S					610	mW
Operating temperature range		Topr				-10		+70	ºC
Storage temperature range		Tstg				-55		+125	ºC

Recommended Operating Range at Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				V_{DD}[V]	min	typ	max	
Operating supply voltage range	V_{DD}(1)	V_{DD}	0.844µs ≤ tCYC ≤ 0.852µs		4.5		5.5	V
	V_{DD}(2)		4µs ≤ tCYC ≤ 400µs		4.5		5.5	
Hold voltage	VHD	V_{DD}	RAMs and the registers data are kept in HOLD mode.		2.0		5.5	
High level input voltage	V_{IH}(1)	Port 0	Output disable	4.5 to 5.5	0.6V_{DD}		V_{DD}	
	V_{IH}(2)	•Ports 1, 3 (Schumitt) •Port 7 (Schumitt) port input/interrupt • $\overline{HS}$, $\overline{VS}$, $\overline{RES}$ (Schumitt)	Output disable	4.5 to 5.5	0.75V_{DD}		V_{DD}	
	V_{IH}(3)	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	V_{DD}-0.5		V_{DD}	
Low level input voltage	V_{IL}(1)	Port 0	Output disable	4.5 to 5.5	V_{SS}		0.2V_{DD}	
	V_{IL}(2)	•Ports 1, 3 (Schumitt) •Port 7 (Schumitt) port input/interrupt • $\overline{HS}$, $\overline{VS}$, $\overline{RES}$ (Schumitt)	Output disable	4.5 to 5.5	V_{SS}		0.25V_{DD}	
	V_{IL}(3)	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	V_{SS}		0.6V_{DD}	
CVIN	VCVIN	CVIN(LC863400 only)		5.0	0.7Vp-p	1Vp-p	1.4Vp-p	Vp-p*
Operation cycle time	tCYC(1)		•All functions operating	4.5 to 5.5	0.844	0.848	0.852	µs
	tCYC(2)		•AD converter operating •OSD and Data slicer are not operating	4.5 to 5.5	0.844		30	
	tCYC(3)		•OSD, AD converter and Data slicer are not operating	4.5 to 5.5	0.844		400	
Oscillation frequency range	FmRC		Internal RC oscillation	4.5 to 5.5	0.4	0.8	3.0	MHz

* Vp-p: Peak-to-peak voltage

Electrical Characteristics at Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Ratings min	Ratings typ	Ratings max	unit
High level input current	I_{IH}(1)	Ports 0, 1, 3, 7	•Output disable •Pull-up MOS Tr. OFF •V_{IN}=V_{DD} (including the off-leak current of the output Tr.)	4.5 to 5.5			1	μA
	I_{IH}(2)	• $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	•V_{IN}=V_{DD}	4.5 to 5.5			1	
Low level input current	I_{IL}(1)	Ports 0, 1, 3, 7	•Output disable •Pull-up MOS Tr. OFF •V_{IN}=V_{SS} (including the off-leak current of the output Tr.)	4.5 to 5.5	-1			
	I_{IL}(2)	• $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	V_{IN}=V_{SS}	4.5 to 5.5	-1			
High level output voltage	V_{OH}(1)	•CMOS output of ports 0, 1, 3, 71 to 73	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH}(2)	R, G, B, BL	I_{OH}=-0.1mA R. G. B: digital mode	4.5 to 5.5	V_{DD}-0.5			
Low level output voltage	V_{OL}(1)	Ports 0, 1, 3, 71 to 73	I_{OL}=10mA	4.5 to 5.5			1.5	
	V_{OL}(2)	Ports 0, 3, 71 to 73	I_{OL}=1.6mA	4.5 to 5.5			0.4	
	V_{OL}(3)	•R, G, B, BL •Port 1	I_{OL}=3.0mA R. G. B: digital mode	4.5 to 5.5			0.4	
	V_{OL}(4)	Port 70	I_{OL}=1mA	4.5 to 5.5			0.4	
Pull-up MOS Tr. resistance	Rpu	Ports 0, 1, 3, 7	V_{OH}=0.9V_{DD}	4.5 to 5.5	13	38	80	kΩ
Bus terminal short circuit resistance (SCL0-SCL1, SDA0-SDA1)	RBS	•P10 to P12 •P11 to P13		4.5 to 5.5		130	300	Ω
Hysteresis voltage	VHYS	•Ports 1, 3, 7 • $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	Output disable	4.5 to 5.5		0.1V_{DD}		V
Input clump voltage	VCLMP	CVIN (LC863400 only)		5.0	2.3	2.5	2.7	
Pin capacitance	CP	All pins	•f=1MHz •Every other terminals are connected to V_{SS}. •Ta=25ºC	4.5 to 5.5		10		pF

IIC Input/Output Conditions at Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Standard		High speed		unit
		min	max	min	max	
SCL Frequency	fSCL	0	100	0	400	kHz
BUS free time between stop - start	tBUF	4.7		1.3		µs
HOLD time of start, restart condition	tHD;STA	4.0		0.6		µs
L time of SCL	tLOW	4.7		1.3		µs
H time of SCL	tHIGH	4.0		0.6		µs
Set-up time of restart condition	tSU;STA	4.7		0.6		µs
HOLD time of SDA	tHD;DAT	0		0	0.9	µs
Set-up time of SDA	tSU;DAT	250		100		ns
Rising time of SDA, SCL	tR		1000	20+0.1Cb	300	ns
Falling time of SDA, SCL	tF		300	20+0.1Cb	300	ns
Set-up time of stop condition	tSU;STO	4.0		0.6		µs

Refer to figure 8

Note Cb: Total capacitance of all BUS (unit : pF)

Pulse Input Conditions at Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD}[V]	min	typ	max	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (1tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (16tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	32			
	tPIH(4) tPIL(4)	INT3/T0IN (64tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	128			
	tPIL(5)	$\overline{RES}$	Reset acceptable	4.5 to 5.5	200			µs
	tPIH(6) tPIL(6)	$\overline{HS}$, $\overline{VS}$	•Display position controllable •The active edge of $\overline{HS}$ and $\overline{VS}$ must be apart at least 1tCYC. •Refer to figure 4.	4.5 to 5.5	3			
Rising/falling time	tTHL tTLH	$\overline{HS}$	Refer to figure 4.	4.5 to 5.5			500	ns

AD Converter Characteristics at Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD}[V]	min	typ	max	
Resolution	N			4.5 to 5.5		6		bit
Absolute precision	ET		(Note)				±1	LSB
Conversion time	tCAD	Vref selection to conversion finish	1 bit conversion time=2×tCYC			1.69		µs
Analog input voltage range	VAIN	AN4 to AN7			V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}				1	µA
	IAINL		VAIN=V_{SS}		-1			

Note Absolute precision does not include quantizing error (1/2LSB).

Analog Mode RGB Characteristics at Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions	Ratings				
				V_{DD}[V]	min.	typ.	max.	unit
Analog output voltage		R.G.B Analog output mode	Low level output	5.0	0.45	0.5	0.55	V
			Intensity output		0.90	1.0	1.10	
			High level output		1.35	1.5	1.65	
Time setting		R.G.B	70% 10pf load				50	ns

Sample Current Dissipation Characteristics at Ta = -10°C to +70°C, V_{SS} = 0V

The sample current dissipation characteristics is the measurement result of Sanyo provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally.
The currents through the output transistors and the pull-up MOS transistors are ignored.

Parameter	Symbol	Pins	Conditions	Ratings				unit
				V_{DD}[V]	min	typ	max	
Current dissipation during basic operation	IDDOP(1)	V_{DD}	•FmX'tal=32.768kHz X'tal oscillation •System clock : VCO •VCO for OSD operating •OSD is Digital mode •Internal RC oscillation stops	4.5 to 5.5		12	24	mA
	IDDOP(2)	V_{DD}	•FmX'tal=32.768kHz X'tal scillation •System clock : VCO •VCO for OSD operating •OSD is Analog mode •Internal RC oscillation stops	4.5 to 5.5		20	32	
	IDDOP(3)	V_{DD}	•FmX'tal=32.768kHz X'tal scillation •System clock : X'tal (Instruction cycle time: 366.2µs) •VCO for system stops •VCO for OSD stops •Internal RC oscillation stop •Data slicer, AD converters stop	4.5 to 5.5		70	300	µA
Current dissipation in HALT mode	IDDHALT(1)	V_{DD}	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •System clock : VCO •VCO for OSD stops •Internal RC oscillation stops	4.5 to 5.5		3	7	mA
	IDDHALT(2)	V_{DD}	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock : Internal RC	4.5 to 5.5		400	1000	µA
	IDDHALT(3)	V_{DD}	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock : X'tal	4.5 to 5.5		55	200	
Current dissipation in HOLD mode	IDDHOLD	V_{DD}	•HOLD mode •All oscillation stops.	4.5 to 5.5		0.05	20	µA

Note 3: The currents of the output transistors and the pull-up MOS transistors are ignored.

Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions:
Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -10°C to +70°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rf	Rd		typ	max	
32.768kHz	SEIKO EPSON	C-002RX	18pF	18pF	OPEN	510kΩ	4.5 to 5.5V	1.0s	1.5s	

Notes: The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)
1. The V_{DD} becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +70°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' V_{SS} should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

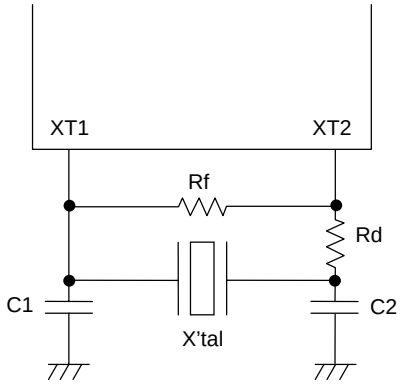
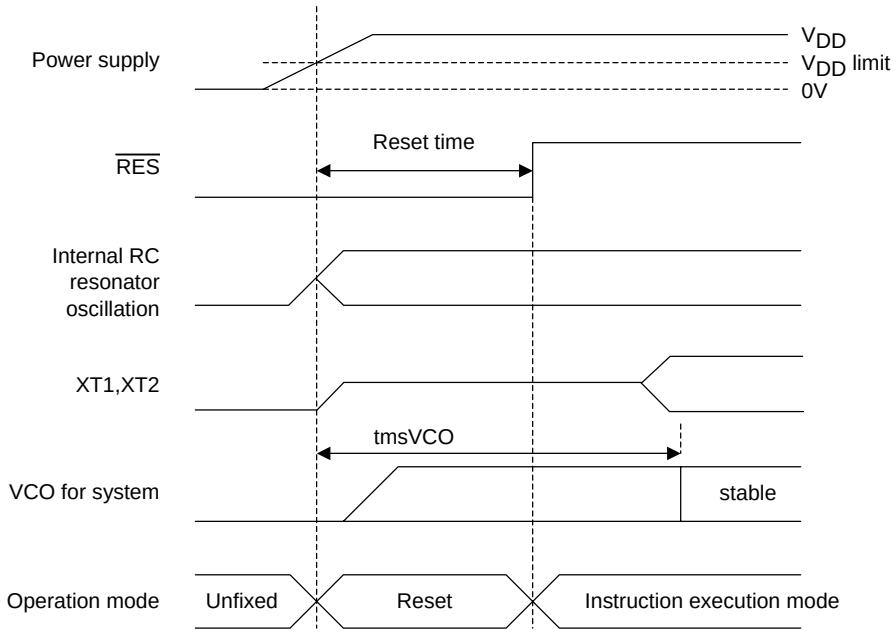
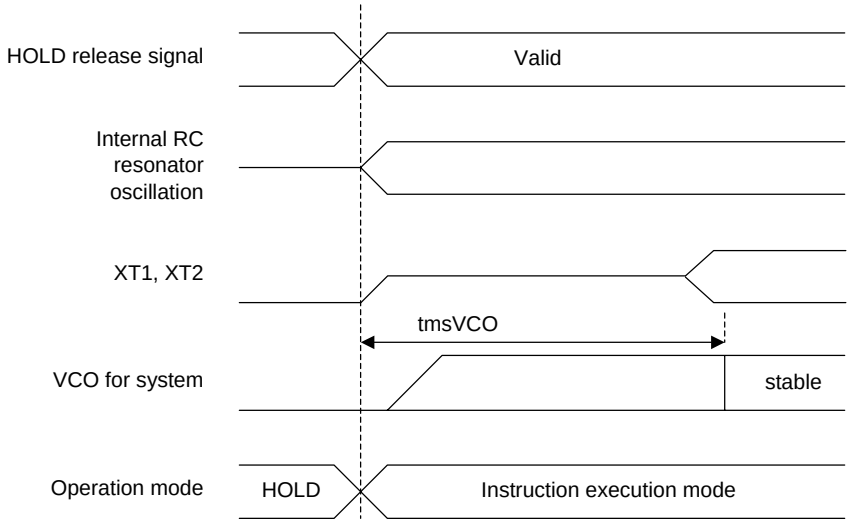


Figure 1 Recommended Oscillation Circuit



Reset Time and Oscillation Stabilizing Time



HOLD release signal and oscillation stabilizing time
Figure 2 Oscillation Stabilizing Time

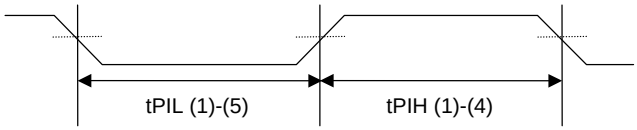


Figure 3 Pulse Input Timing Condition - 1

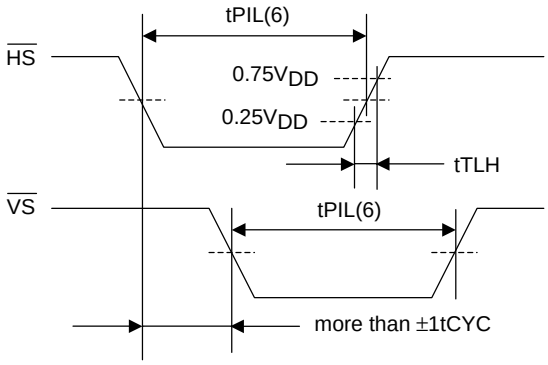


Figure 4 Pulse Input Timing Condition - 2

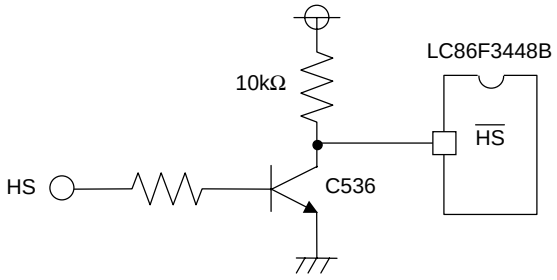
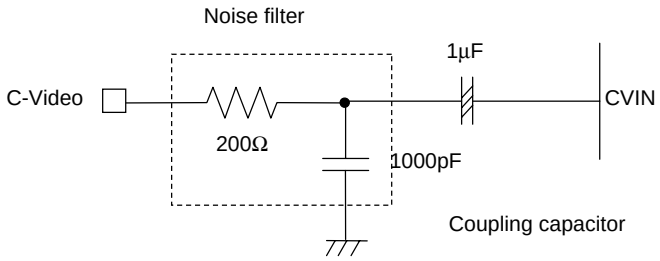


Figure 5 Recommended Interface Circuit



Output impedance of C-Video before Noise filter should be less then 100Ω.

Figure 6 CVIN Recommended Circuit

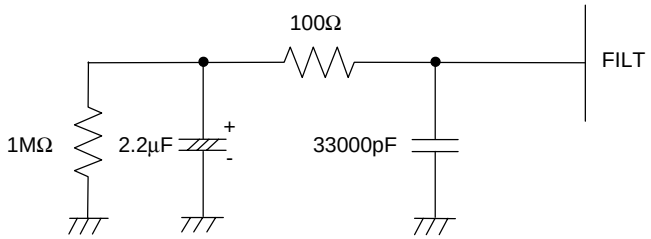
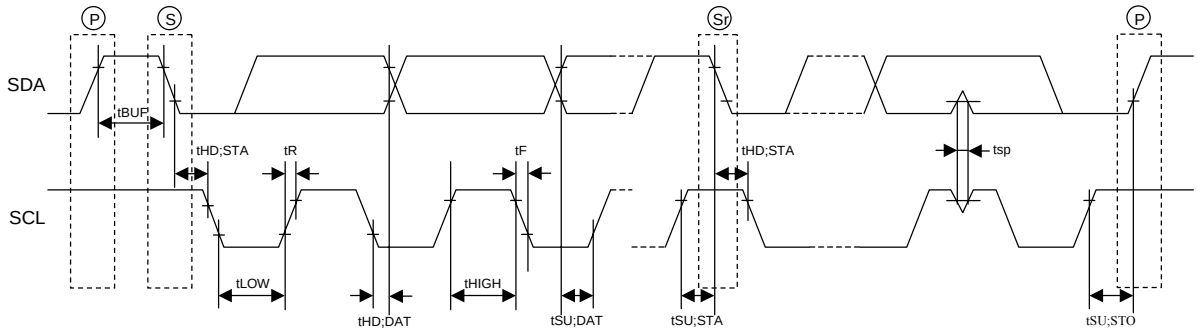


Figure 7 FILT Recommended Circuit
Note: Place FILT parts on board as close to the microcontroller as possible.



S : start condition
P : stop condition
Sr : restart condition

tsp : spike suppression

Standard mode : not exist
High speed mode : less than 50ns

Figure 8 IIC Timing

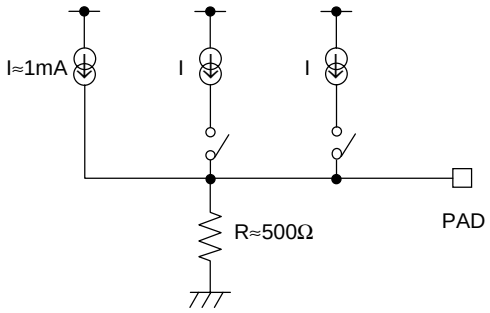


Figure 9 R.G.B. Analog Output Equivalent Circuit