



SANYO Semiconductors

DATA SHEET

LC86F3G64A

CMOS IC

96K-byte Flash Memory (ROM 64K-byte+CGROM 16K-byte
+Extended ROM 16K-byte)

on-chip 768-byte RAM and 352×9-bit Display RAM

8-bit 1-chip Microcontroller

Overview

The LC86F3G64A is a CMOS 8-bit single chip microcontroller with Flash Memory for the LC863G00 series. This microcontroller contains the following on-chip functional blocks:

- CPU: Operable at a minimum bus cycle time of 0.424μs
- On-chip ROM capacity: 96K bytes Flash Memory
(Program ROM: 64K bytes, CGROM: 16K bytes, Extended ROM: 16K bytes)
- On-chip RAM capacity: 768 bytes
- Display RAM: 352 × 9 bits
- Closed-Caption TV controller and the on-screen display controller
- Closed-Caption data slicer
- Five channels × 8-bit AD Converter
- Three channels × 7-bit PWM
- Two 16-bit timer/counters, 14-bit base timer
- 8-bit synchronous serial interface circuit
- IIC-bus compliant serial interface circuit (Multi-master type)
- UART interface circuit (full duplex)
- ROM correct function
- 16-source 10-vectored interrupt system

Continued on next page.

Note : This product includes the IIC bus interface circuit. If you intend to use the IIC bus interface, please notify us of this in advance of our receiving your program ROM code order.

Purchase of SANYO IIC components conveys a license under the Philips IIC Patents Rights to use these components in an IIC system, provided that the system conforms to the IIC Standard Specification as defined by Philips.

Trademarks

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Continued from preceding page.

- Integrated system clock generator and display clock generator

Only one X'tal oscillator (32.768kHz) for PLL reference is used for both generators

All of the above functions are fabricated on a single chip.

The program is rewritable by using the on-board writing system after the LSI has been installed on the application board.

The LC86F3G64A change to LC863200/ LC863300/ LC863800 series by writing program data of LC863200/ LC863300/ LC863800 series into the Flash Memory.

Features

■ Built-in Flash Memory

96K bytes

- Program ROM 64K bytes
- Character ROM 16K bytes
- Extended ROM 16K bytes
- Rewritable in page units 128 bytes / page
- Page erase / program cycle 100 cycle per page

■ Random Access Memory (RAM)

768 × 8 bits (including 128 bytes for ROM correction function)

352 × 9 bits (for CRT display)

The LC86F3G64A consists of 64K of ROM space and 768 bytes of RAM space. For this microcontroller, the usable program ROM capacity and RAM capacity are the same size for the mask ROM version.

Mask ROM versions compatible with the LC86F3G64A	Program ROM limit set for the LC86F3G64A	RAM limit set for the LC86F3G64A (including 128 bytes for the ROM correction function)
LC863G64/LC863864	65536 bytes	768 bytes
LC863264/LC863364	65536 bytes	640 bytes
LC863G56/LC863856	57344 bytes	768 bytes
LC863256/LC863356	57344 bytes	640 bytes
LC863G48/LC863848	49152 bytes	768 bytes
LC863248/LC863348	49152 bytes	640 bytes
LC863G40/LC863840	40960 bytes	768 bytes
LC863240/LC863340	40960 bytes	640 bytes
LC863G32/LC863832	32768 bytes	768 bytes
LC863232/LC863332	32768 bytes	512 bytes
LC863G28/LC863828	28672 bytes	768 bytes
LC863228/LC863328	28672 bytes	512 bytes
LC863G24/LC863824	24576 bytes	768 bytes
LC863224/LC863324	24576 bytes	512 bytes
LC863820	20480 bytes	768 bytes
LC863220/LC863320	20480 bytes	512 bytes
LC863816	16384 bytes	768 bytes
LC863216/LC863316	16384 bytes	512 bytes

■ OSD Functions

- Screen display : 36 characters × 16 lines (by software)
- RAM : 352 words (9 bits per word)
 - Display area : 36 words × 8 lines
 - Control area : 8 words × 8 lines

• Characters

Up to 252 kinds of 16 × 32 dot characters

(4 characters including 1 test character are not programmable)

Each font can be divided into two parts and used as two fonts (Ex. 16 × 16 dot character font × 2)

At least 111 characters need to be divide between a 16×17 dot and 8 × 9 dot character font to display the caption fonts.

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- Various character attributes

- Character colors : 16 colors
- Character background colors : 16 colors
- Fringe / shadow colors : 16 colors
- Full screen colors : 16 colors
- Rounding
- Underline
- Italic character (slanting)

- Attribute can be changed without spacing
- Vertical display start line number can be set for each row independently (Rows can be overlapped)
- Horizontal display start position can be set for each row independently
- Horizontal pitch (9 to 16 dot)^{*1} and vertical pitch (1 to 32 dot) can be set for each row independently
- Different display modes can be set for each row independently
Caption • Text mode / OSD mode 1 / OSD mode 2 (Quarter size) / Simplified graphic mode

- Ten character sizes^{*1}

- Horiz. × Vert. = (1 × 1), (1 × 2), (2 × 2), (2 × 4)
- (1.5 × 1), (1.5 × 2), (3 × 2), (3 × 4),
- (0.5 × 0.5), (0.75 × 0.5)

- Shuttering and scrolling on each row
- Simplified Graphic Display
- External OSD clock input enable (LC863G00 series only)

Note *1: range depends on display mode : refer to manual for details.

■ Data Slicer : closed caption format (LC863200/LC863800/LC863G00 series only)

- Closed caption data and XDS data extraction
- NTSC/PAL, and extracted line can be specified (LC863800/LC863G00 series)
- NTSC, and fixed line 21 (LC863200 series)

■ Bus Cycle Time / Instruction-Cycle Time

Bus Cycle Time	Instruction Cycle Time	Clock Divider	System Clock Oscillation	Oscillation Frequency	Voltage
0.424μs	0.848μs	1/2	Internal VCO (Ref: X'tal 32.768kHz)	14.156MHz	4.5V to 5.5V
7.5μs	15.0μs	1/2	Internal RC	800kHz	4.5V to 5.5V
91.55μs	183.1μs	1/1	Crystal	32.768kHz	4.5V to 5.5V
183.1μs	366.2μs	1/2	Crystal	32.768kHz	4.5V to 5.5V

■ Ports

- Input / Output Ports : 5 ports (28 terminals)
Data direction programmable in nibble units : 1 port (8 terminals)
(If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.)
Data direction programmable for each bit individually: 4 ports (20 terminals)
- Input port (LC863300 series only) : 1 port (1 terminal)

■ AD converter

- 4-channels × 8-bit AD converters (LC863200/LC863800/LC863G00 series)
- 5-channels × 8-bit AD converters (LC863300 series)

■ Serial interfaces

- IIC-bus compatible serial interface (Multi-master type)
Consists of a single built-in circuit with two I/O channels the two data lines and two clock lines can be short circuited internally.
- Synchronous 8-bit serial interface

■UART (LC863G00 series only)

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit
- Built-in baudrate generator

■PWM Output

- 3 channels×7-bit PWM

■Timer

- Timer 0: 16-bit timer/counter

With 2-bit prescaler + 8-bit built-in programmable prescaler

Mode 0: Two 8-bit timers with a programmable prescaler

Mode 1: 8-bit timer with a programmable prescaler + 8-bit counter

Mode 2: 16-bit timer with a programmable prescaler

Mode 3: 16-bit counter

The resolution of timer is 1 tCYC.

- Timer 1: 16-bit timer/PWM

Mode 0: Two 8-bit timers

Mode 1: 8-bit timer + 8-bit PWM

Mode 2: 16-bit timer

Mode 3: Variable bit PWM (9 to 16 bits)

In mode 0/1, the resolution of Timer1/PWM is 1 tCYC

In mode 2/3, the resolution is selectable by program; tCYC or 1/2 tCYC

- Base timer

Generate every 500ms overflow for a clock application

(using 32.768kHz crystal oscillation for the base timer clock)

Generate every 976μs, 3.9ms, 15.6ms, 62.5ms overflow

(using 32.768kHz crystal oscillation for the base timer clock)

Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0

■Remote Control Receiver Circuit (connected to the P73/INT3/T0IN terminal)

- Noise rejection function
- Polarity switching

■Watchdog Timer

External RC circuit is required

Interrupt or system reset is activated when the timer overflows

■ROM Correction Function

Max 128 bytes / 2 addresses

■Interrupts

- 18 source 10 vectored interrupts: (LC863G00 series)
- 16 source 10 vectored interrupts: (LC863200/LC863800 series)
- 15 source 9 vectored interrupts: (LC863300 series)
 1. External Interrupt INT0
 2. External Interrupt INT1
 3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
 4. External Interrupt INT3, base timer
 5. Timer/counter T0H (Upper 8 bits)
 6. Timer T1H, T1L
 7. SIO0, UART receive(LC863G00 series only)
 8. Data slicer (LC863200/LC863800/LC863G00 series only), UART transmit (LC863G00 series only)
 9. Vertical synchronous signal interrupt (\overline{VS}), scanning line, AD
 10. IIC, Port 0

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- Interrupt priority control
Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible.
Low or high priority can be assigned to the interrupts from 3 to 10 listed above.
For the external interrupt INT0 and INT1, low or highest priority can be set.

■ Sub-routine Stack Level

- A maximum of 128 levels (stack area is assigned on the internal RAM)

■ Multiplication/Division Instruction

- 16 bits×8 bits (7 instruction cycle times)
- 16 bits÷8 bits (7 instruction cycle times)

■ 3 Oscillation Circuits

- Built-in RC oscillation circuit used for the system clock
- Built-in VCO circuit used for the system clock and OSD clock
- On-chip X'tal oscillation circuit used for PLL reference and the system clock and base timer clock

■ Standby Function

- HALT mode
The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped.
This mode can be released by the interrupt request or the system reset.
- HOLD mode
The HOLD mode is used to stop the oscillations; RC (internal), VCO, and X'tal oscillations. This mode can be released by the following conditions.
 - Pull the reset terminal (RES) to low level.
 - Feed the selected level to either P70/INT0 or P71/INT1.
 - Feed the Port 0 interrupt condition

■ Applicable Mask ROM Version

- LC863G64/LC863G56/LC863G48/LC863G40/LC863G32/LC863G28/LC863G24
- LC863864/LC863856/LC863848/LC863840/LC863832/LC863828/LC863824/LC863820/LC863816
- LC863364/LC863356/LC863348/LC863340/LC863332/LC863328/LC863324/LC863320/LC863316
- LC863264/LC863256/LC863248/LC863240/LC863232/LC863228/LC863224/LC863220/LC863216

■ Package

- DIP42S (Lead-free type)
- QIP48E (Lead-free type)

■ Development Tools

- Evaluation chip: LC863096
- Emulator:
 - LC863G00 series: Special ROM monitor tool
(When debugging it, one terminal in the I/O port is used as a pin only for the tool)
 - LC863800 series: EVA86000(main) + ECB863200A (evaluation chip board)
+ POD863200 (pod:DIP42S) [Shared with LC8632 Series]
or POD863201 (QIP48E) [Shared with LC8632 Series]
 - LC863300 series: EVA86000(main) + ECB863200*1 or ECB863200A (evaluation chip board)
+ POD863300 (pod:DIP42S) or POD863301 (QIP48E)
 - LC863200 series: EVA86000(main) + ECB863200*1 or ECB863200A (evaluation chip board)
+ POD863200 (pod:DIP42S) or POD863201 (QIP48E)

*1 This product is no longer available

Write Flash Memory

SANYO provides special services including writing data to Flash Memory and stamping.

There is a charge for these services.

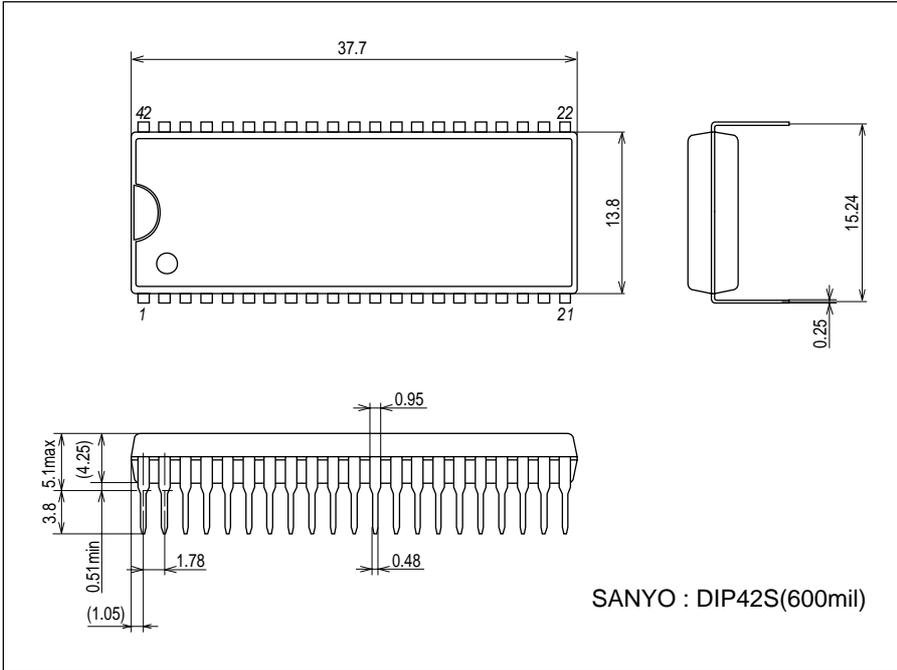
Please feel free to ask our sales persons for details.

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Package Dimensions

unit : mm (typ)

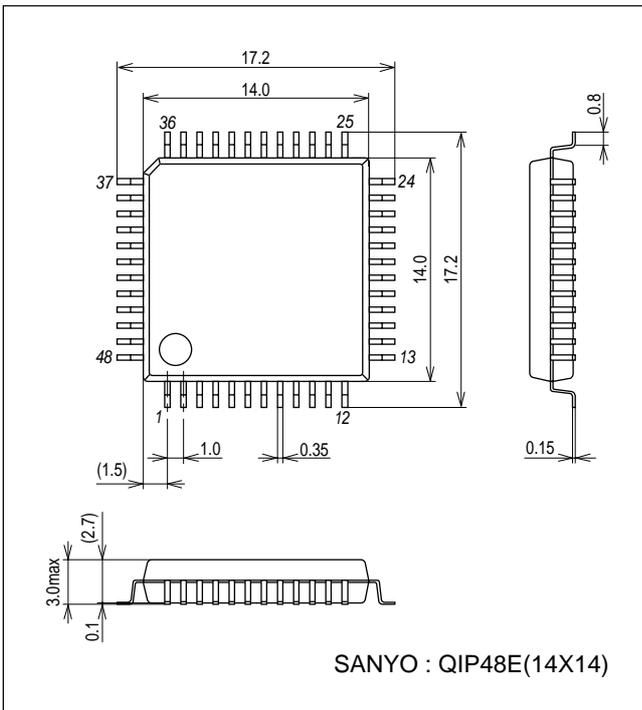
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Package Dimensions

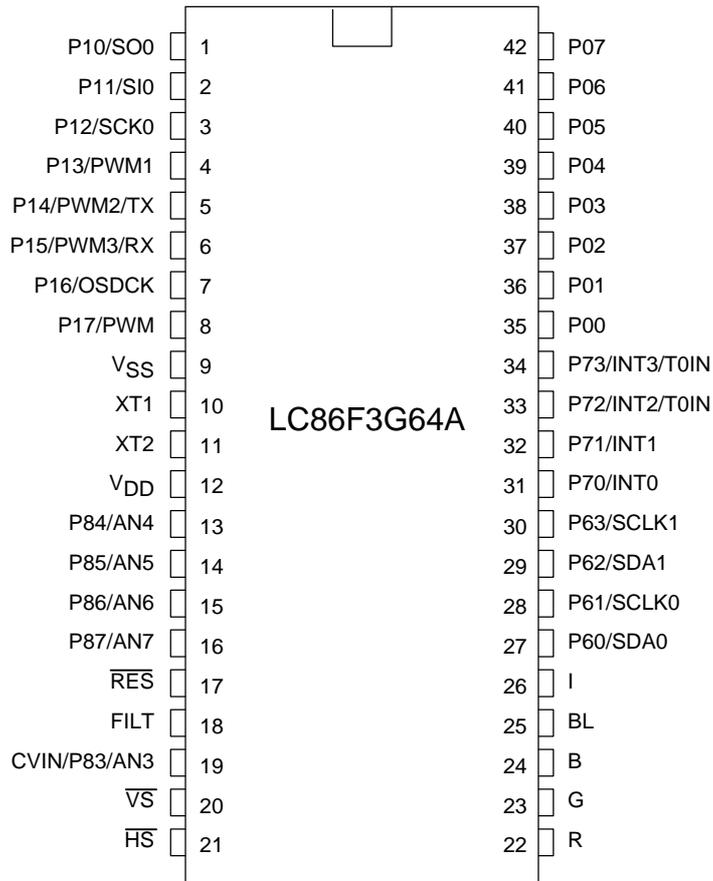
unit : mm (typ)

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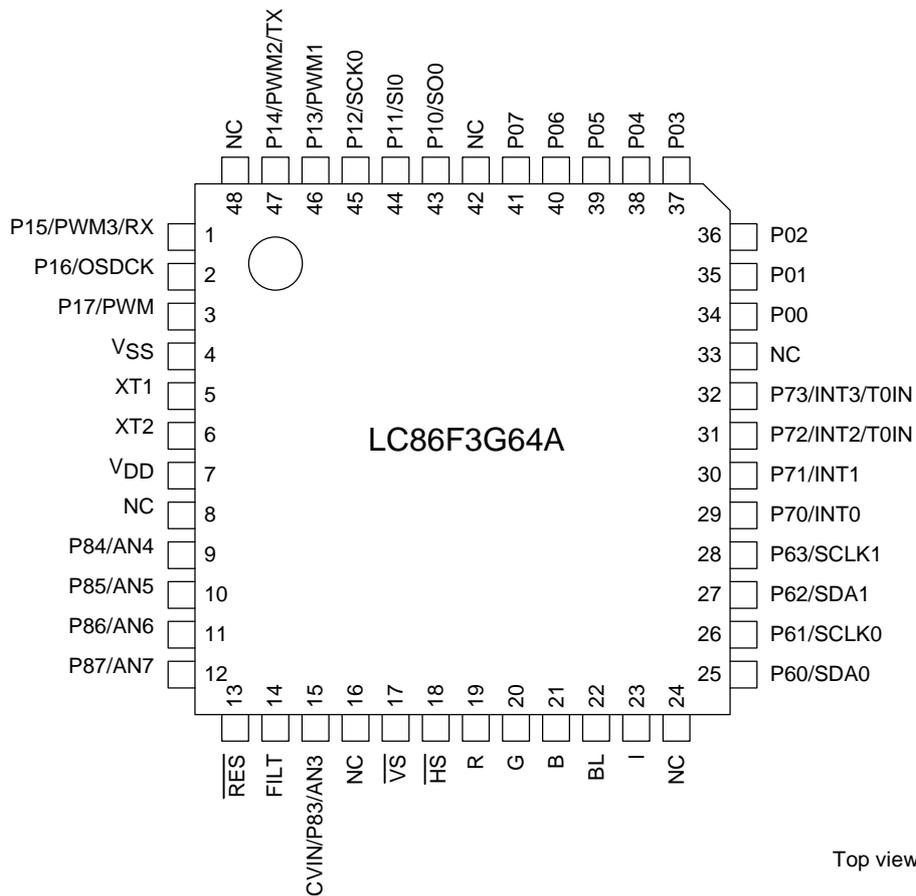


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Pin Assignments



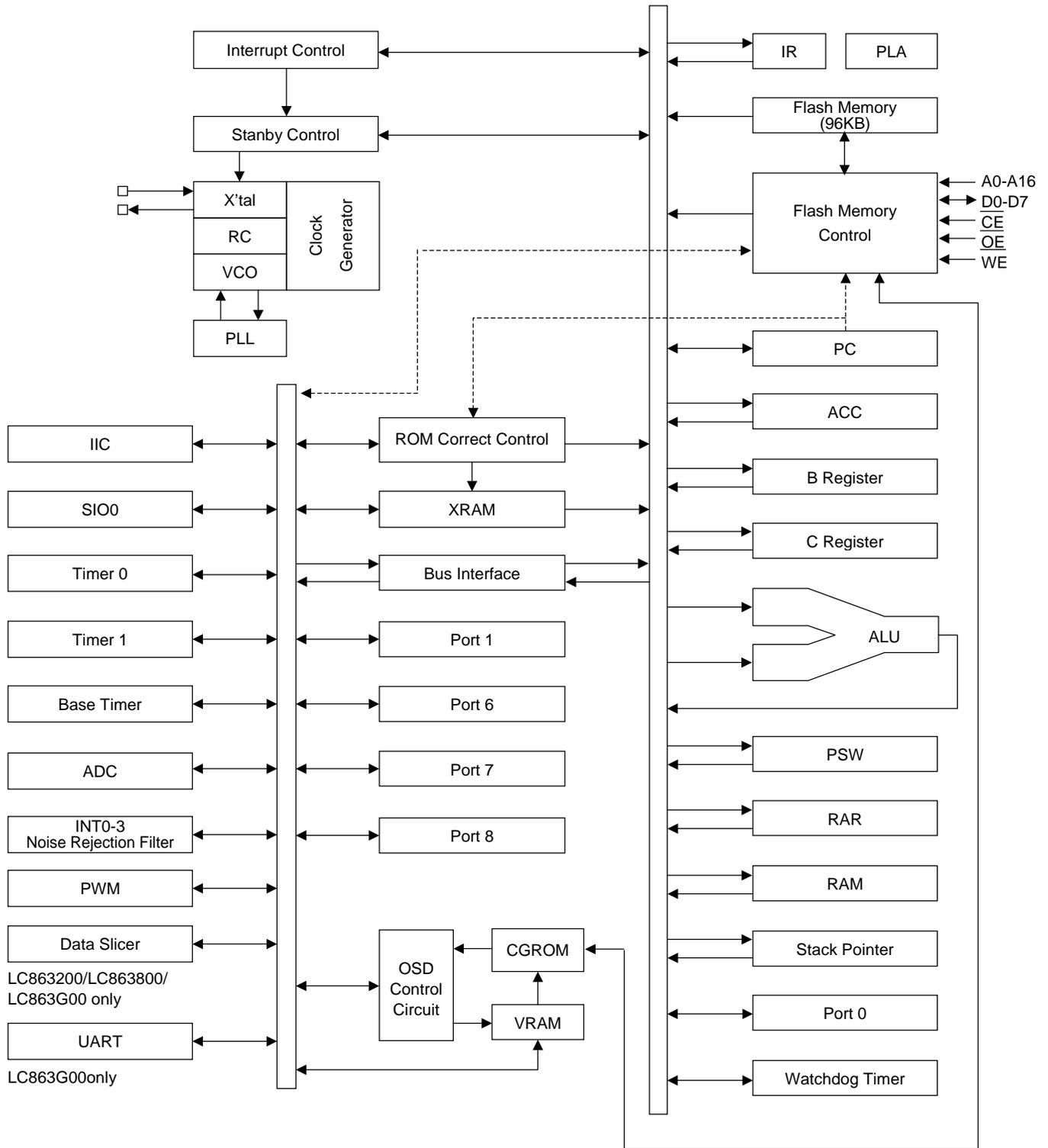
Top view



Top view

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System Block Diagram



LC86F3G64A

Pin Description

Pin Description Table

Terminal	I/O	Function Description	Option	Flash memory mode (Parallel input/ output mode)																
V _{SS}	-	Negative power supply																		
XT1	I	Input terminal for crystal oscillator																		
XT2	O	Output terminal for crystal oscillator																		
V _{DD}	-	Positive power supply																		
$\overline{\text{RES}}$	I	Reset terminal		Input to set up mode																
FILT	O	Filter terminal for PLL		Address input A16																
CVIN	I	Video signal input terminal (LC863200/LC863800/LC863G00 only)																		
$\overline{\text{VS}}$	I	Vertical synchronization signal input terminal		Input to set up mode																
$\overline{\text{HS}}$	I	Horizontal synchronization signal input terminal																		
R	O	Red (R) output terminal of RGB image output																		
G	O	Green (G) output terminal of RGB image output																		
B	O	Blue (B) output terminal of RGB image output		Address input A15																
I	O	Intensity (I) output terminal of RGB image output		Address input A13																
BL	O	Fast blanking control signal Switch TV image signal and caption/OSD image signal		Address input A14																
Port 0 P00 - P07	I/O	<ul style="list-style-type: none"> •8-bit input/output port, Input/output can be specified in nibble unit •Other functions HOLD release input Interrupt input 	<ul style="list-style-type: none"> Pull-up register Present/ not present Output Format CMOS/Nch-OD 	Address input A0 to A7																
Port 1 P10 - P17	I/O	<ul style="list-style-type: none"> •8-bit input/output port Input/output can be specified in a bit •Other functions <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>P10</td><td>SIO0 data output</td></tr> <tr><td>P11</td><td>SIO0 data input/bus input/output</td></tr> <tr><td>P12</td><td>SIO0 clock input/output</td></tr> <tr><td>P13</td><td>PWM1 output</td></tr> <tr><td>P14</td><td>PWM2 output / UART transmit (LC863G00 only)</td></tr> <tr><td>P15</td><td>PWM3 output / UART receive (LC863G00 only)</td></tr> <tr><td>P16</td><td>External OSD clock input (LC863G00 only)</td></tr> <tr><td>P17</td><td>Timer1 (PWM) output</td></tr> </table>	P10	SIO0 data output	P11	SIO0 data input/bus input/output	P12	SIO0 clock input/output	P13	PWM1 output	P14	PWM2 output / UART transmit (LC863G00 only)	P15	PWM3 output / UART receive (LC863G00 only)	P16	External OSD clock input (LC863G00 only)	P17	Timer1 (PWM) output	Output Format CMOS/Nch-OD	Data input/output D0 to D7
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P14	PWM2 output / UART transmit (LC863G00 only)																			
P15	PWM3 output / UART receive (LC863G00 only)																			
P16	External OSD clock input (LC863G00 only)																			
P17	Timer1 (PWM) output																			
Port 6 P60 - P63	I/O	<ul style="list-style-type: none"> •4-bit input/output port Input/output can be specified for each bit •Other functions <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>P60</td><td>IIC0 data I/O</td></tr> <tr><td>P61</td><td>IIC0 clock output</td></tr> <tr><td>P62</td><td>IIC1 data I/O</td></tr> <tr><td>P63</td><td>IIC1 clock output</td></tr> </table>	P60	IIC0 data I/O	P61	IIC0 clock output	P62	IIC1 data I/O	P63	IIC1 clock output		<ul style="list-style-type: none"> control signal $\overline{\text{CE}}$ control signal $\overline{\text{OE}}$ control signal $\overline{\text{WE}}$ Address input A12 								
P60	IIC0 data I/O																			
P61	IIC0 clock output																			
P62	IIC1 data I/O																			
P63	IIC1 clock output																			

Continued on next page.

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Continued from preceding page.

Terminal	I/O	Function Description	Option	Flash memory mode (Parallel input/ output mode)																																											
Port 7 P70 P71 - P73	I/O	<p>•4-bit input/output port Input or output can be specified for each bit</p> <p>•Other function</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;">P70</td> <td>INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer</td> </tr> <tr> <td>P71</td> <td>INT1 input/HOLD release input</td> </tr> <tr> <td>P72</td> <td>INT2 input/Timer 0 event input</td> </tr> <tr> <td>P73</td> <td>INT3 input (noise rejection filter attached)/ Timer 0 event input</td> </tr> </table> <p>Interrupt receiver format, vector addresses</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th>rising</th> <th>falling</th> <th>rising/ falling</th> <th>H level</th> <th>L level</th> <th>vector</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>03H</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>0BH</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>13H</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>1BH</td> </tr> </tbody> </table>	P70	INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer	P71	INT1 input/HOLD release input	P72	INT2 input/Timer 0 event input	P73	INT3 input (noise rejection filter attached)/ Timer 0 event input		rising	falling	rising/ falling	H level	L level	vector	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH		Address input A8 to A11
P70	INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer																																														
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INT2	enable	enable	enable	disable	disable	13H																																									
INT3	enable	enable	enable	disable	disable	1BH																																									
Port 8																																															
P83	I	<p>•1-bit input port (LC863300 only)</p> <p>•Other function AD converter input port (1 lines)</p>																																													
P84 - P87	I/O	<p>•4-bit input/output port Input or output can be specified for each bit</p> <p>•Other function AD converter input port (4 lines)</p>																																													
NC	-	<p>unused terminal Leave open</p>																																													

- Output form and existence of pull-up resistor for every port can be specified for each bit.
- Programmable pull-up resistor is always connected regardless of port option, CMOS or N-ch open drain output in port 1.

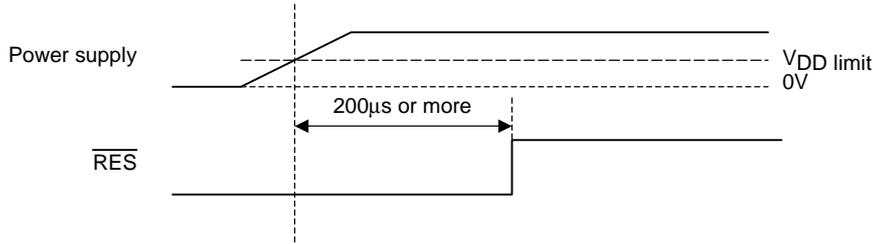
User Options

User options can be changed using Flash Memory data.

A kind of option	Pin, Circuits	
Input/output form of input/output ports	Port 0 (Specified in a bit)	<p>1. Input: Without pull-up MOS Tr. Output: N-channel open drain</p> <p>2. Input: With pull-up MOS Tr. Output: CMOS</p>
	Port 1 (Specified in a bit)	<p>1. Input: With programmable pull-up MOS Tr. Output: N-channel open drain</p> <p>2. Input: With programmable pull-up MOS Tr. Output: CMOS</p>

Notice for Use

- Input level of terminal $\overline{\text{RES}}$ at power on
Terminal $\overline{\text{RES}}$ must be held low for at least 200 μs after the supply voltage exceeds the power supply lower limit.



- Difference between the Mask version and Flash version
 1. The operation after release of reset: The mask version operates the program from the address 0 in the program counter as soon as detecting the H level on the reset port. The flash version operates the program from the address 0 in the program counter after setting the option.
 2. Current dissipation : Please refer to the latest semiconductor news.

- Conditions during reset and after release of reset
Port options are set using Flash Memory data.
Port options are set internally within approximately 3ms after logic HIGH is applied to the RESET terminal. The configuration of the port outputs change over the duration of this period. Then the Program Counter is set to 0 and program execution begins.
During reset, and in the few hundred milliseconds after reset is released, the port options on certain of the ports will not yet have been set. The conditions of the various ports during reset or on release of reset have been collected in the following table. Please refer to it when analyzing circuits where these conditions apply.

Pins	Options	Condition during and on release of reset
P0	Input: Without pull up MOS transistor Output: N-channel open drain	Output -off Input mode: High impedance
	Input: With pull up MOS transistor Output: CMOS	Output-off During reset and in the first few hundred μs after reset is released, the pull-up MOS transistor is OFF. Thereafter, set to input mode with pull-up MOS Tr. ON
P1	Input: With programmable pull up MOS transistor Output: N-channel open drain	Output-off Input mode: High impedance
	Input: With programmable pull up MOS transistor Output: CMOS	
P6	No options Output: N-channel open drain	Output -off Input mode: High impedance
P7	No options Input: With programmable pull up MOS transistor Output: N-channel open drain (P70) CMOS (P71 - P73)	Output-off Input mode: Pull up MOS transistor off
P8	No options Input: With programmable pull up MOS Transistor (P83: without it) Output: CMOS (P83: input only)	Output-off Input mode: Pull up MOS transistor off

On-board writing system

The LC86F3G64A has the On-board writing system. The program is renewable by using SANYO Flash On-board System after the LSI has been installed on the application board.

This system is composed of 4 types divided by the combination of the mode setting pin and communication pin.

Each type system has to connect the 6 pins (V_{DD} , V_{SS} , \overline{RES} , communication pins) with the interface board of SANYO Flash On-board System.

It is necessary that the pins to be used for the rewriting system should be able to be separated from the application board properly.

The system type is selected by the option setting program (Su86K.exe).

types	mode setting pin	communication pins
type1	\overline{RES} pin (high voltage(12V) applied)	P00(DATA1), P01(DATA0), P02(CLK)
type2	\overline{RES} pin (high voltage(12V) applied)	P00(DATA1), P60(DATA0), P61(CLK)
type3	P00 pin (High level voltage applied)	P00(ENA/DATA1), P01(DATA0), P02(CLK)
type4	P00 pin (High level voltage applied)	P00(ENA/DATA1), P60(DATA0), P61(CLK)

- Type 3 or 4 is selected: P00 is exclusive for the on-board system.

This pin must always be pulled-down, so this pin can't be used for other applications.

Please set P00 pin N-channel open drain output.(option setting)

In the user program, "0" is always set to the P00 latch (bit 0 in the Port 0 latch (140h)) because the P0 interrupt must not be requested on the P00 pin .

- The loader program must be written into the ROM to use On-board writing system.

The loader program should be written into the ROM before the LSI has been installed on the board by the general purpose PROM programs.

When the option setting selects the this system to use, the loader program automatically links to the extended ROM field (14000h-147FFh) on the user program linking.

Please ask to our sales persons before using On-board writing system.

LC86F3G64A

Method of how to rewrite it in FLASH programmer / SANYO FLASH writing tool (SFWS)

When reading or writing data to the LC86F3G64A, FLASH programmer of our recommendation or SANYO FLASH writing tool (SFWS) is used. In both cases, exclusive conversion board (W86F3264D, W86F3264Q) is needed.

(1) FLASH programmer of our recommendation

Single Word Write

Manufacture	Name of device	version	applicable device (code)	Data protection setting after write operation
Flash Support Group co. (the former Ando Electric)	AF9708	Rev2.43	SANYO LC86F3G64A (3B225)	Protected

Write Multiple Words

Manufacture	Name of device	version	applicable device (code)	Data protection setting after write operation
Flash Support Group co. (the former Ando Electric)	AF9723 + AF9833	Rev2.04 +Rev01.85 *1	SANYO LC86F3G64A (3B225)	Protected

*1: Registration is being requested.

The LC86F3G64A does not support a silicon signature feature.

Do not use the feature (automatic device type selection) when programming this device.

To avoid erasing the program, confirm the setting of the protection for activating the written program before using.

It can't be written with device code 29EE010

(2) SANYO FLASH writing tool (SFWS)

PC is connected with writer unit (SKK) by USB cable and it uses it.

(3) Exclusive writing conversion board

- W86F3264D ••• DIP42S purpose (It is common with production discontinuance model (LC86F3264A/LC86F3364A/LC86F3864A))
- W86F3264Q ••• QIP48E purpose (It is common with production discontinuance model (LC86F3264A/LC86F3364A/ LC86F3864A))

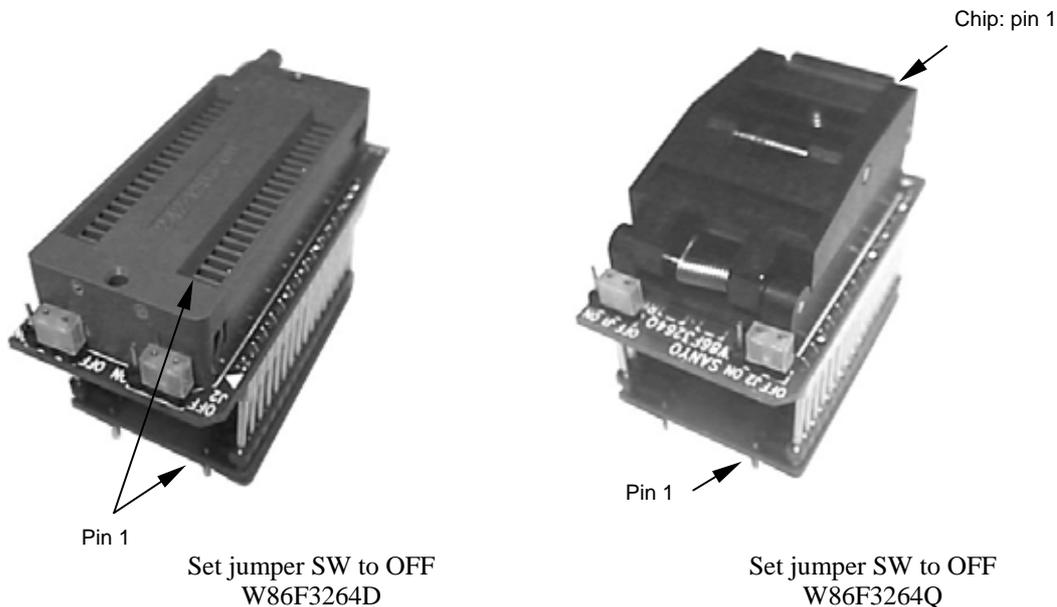
When using the conversion board, all of the jumper SW must be set to the OFF position.

If set to the ON position, read/write operations will not perform correctly.

Pin 1 of the conversion board should be located as indicated below.

W86F3264D: when viewing from the edge closest to jumper SW, pin 1 is located on the lower right of both the chip and conversion board.

W86F3264Q: when viewing from the edge closest to jumper SW, pin 1 of the chip is located on the upper right while pin 1 of the conversion board is located on the lower right.



LC86F3G64A

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Pins	Conditions	Specification				unit
				$V_{DD}[\text{V}]$	min	typ	max	
Maximum supply voltage	$V_{DD \text{ max}}$	V_{DD}			-0.3		+6.5	V
Input voltage	$V_{I(1)}$	•RES, HS, VS, CVIN/P83			-0.3		$V_{DD}+0.3$	
Output voltage	$V_{O(1)}$	R, G, B, I, BL, FILT			-0.3		$V_{DD}+0.3$	
Input/output voltage	$V_{IO(1)}$	•Ports 0, 1, 6, 7, 84-87			-0.3		$V_{DD}+0.3$	
High level output current	Peak output current	IOPH(1)	•Ports 0, 1, 7, 84-87	•CMOS output •For each pin.		-4		mA
		IOPH(2)	R, G, B, I, BL	•CMOS output •For each pin.		-5		
	Total output current	$\Sigma\text{IOAH}(1)$	•Ports 0, 1	The total of all pins.		-20		
		$\Sigma\text{IOAH}(2)$	Ports 7, 84-87	The total of all pins.		-10		
		$\Sigma\text{IOAH}(3)$	R, G, B, I, BL	The total of all pins.		-15		
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 6, 84-87	For each pin.			15	
		IOPL(2)	Port 7	For each pin.			15	
		IOPL(3)	R, G, B, I, BL	For each pin.			5	
	Total output current	$\Sigma\text{IOAL}(1)$	Ports 0, 1	The total of all pins.			40	
		$\Sigma\text{IOAL}(2)$	Ports 6, 7, 84-87	The total of all pins.			35	
		$\Sigma\text{IOAL}(3)$	R, G, B, I, BL	The total of all pins.			15	
Maximum power dissipation	$P_d \text{ max}$	DIP42S		$T_a = -30$ to $+85^\circ\text{C}$			500	mW
		QIP48E					280	
Operating temperature range	T_{opr}				-30		+85	$^\circ\text{C}$
Storage temperature range	T_{stg}				-55		+125	

LC86F3G64A

Recommended Operating Range at $T_a = -30^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Pins	Conditions	Specification				
				$V_{DD}[\text{V}]$	min	typ	max	unit
Operating supply voltage range	$V_{DD}(1)$	V_{DD}	$0.844\mu\text{s} \leq t_{CYC} \leq 0.852\mu\text{s}$		4.5		5.5	V
	$V_{DD}(2)$		$4\mu\text{s} \leq t_{CYC} \leq 400\mu\text{s}$		4.5		5.5	
Hold voltage	VHD	V_{DD}	RAMs and the registers data are kept in HOLD mode.		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Port 0 (Schmitt)	Output disable	4.5 to 5.5	$0.6V_{DD}$		V_{DD}	
	$V_{IH}(2)$	•Ports 1,6 (Schmitt CMOS) •Port 7 (Schmitt) port input/interrupt • \overline{HS} , \overline{VS} , \overline{RES} , (Schmitt CMOS)	Output disable	4.5 to 5.5	$0.75V_{DD}$		V_{DD}	
	$V_{IH}(3)$	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	$V_{DD}-0.5$		V_{DD}	
	$V_{IH}(4)$	•Port 8 port input	Output disable	4.5 to 5.5	$0.7V_{DD}$		V_{DD}	
	$V_{IH}(5)$	•Port 16 (TTL) •Port 6, \overline{HS} , \overline{VS} (Schmitt TTL) LC863G00 only	Output disable	4.5 to 5.5	$0.45V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Port 0 (Schmitt)	Output disable	4.5 to 5.5	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	•Ports 1,6 (Schmitt CMOS) •Port 7 (Schmitt) port input/interrupt • \overline{HS} , \overline{VS} , \overline{RES} , (Schmitt CMOS)	Output disable	4.5 to 5.5	V_{SS}		$0.25V_{DD}$	
	$V_{IL}(3)$	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	V_{SS}		$0.6V_{DD}$	
	$V_{IL}(4)$	Port 8 port input	Output disable	4.5 to 5.5	V_{SS}		$0.3V_{DD}$	
	$V_{IL}(5)$	•Port 16 (TTL) •Port 6, \overline{HS} , \overline{VS} (Schmitt TTL) LC863G00 only	Output disable	4.5 to 5.5	V_{SS}		$0.18V_{DD}$	
CVIN	VCVIN	CVIN		5.0	1Vp-p -3dB	1Vp-p	1Vp-p +3dB	Vp-p^*
Operation cycle time	$t_{CYC}(1)$		•All functions operating	4.5 to 5.5	0.844	0.848	0.852	μs
	$t_{CYC}(2)$		•AD converter operating •OSD and Data slicer are not operating	4.5 to 5.5	0.844		30	
	$t_{CYC}(3)$		•OSD, AD converter and Data slicer are not operating	4.5 to 5.5	0.844		400	
Oscillation frequency range	FmRC		Internal RC oscillation	4.5 to 5.5	0.4	0.8	3.0	MHz
External OSD clock input frequency range	FmICK	P16/OSDCK (LC863G00 only)	DUTY50±5% of external OSD clock	4.5 to 5.5	13	14	15	MHz

* Vp-p : Peak-to-peak voltage

LC86F3G64A

Electrical Characteristics at Ta = -30°C to +85°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	Specification				unit
				VDD[V]	min	typ	max	
High level input current	I _{IH} (1)	Ports 0, 1, 6, 7, 8	<ul style="list-style-type: none"> •Output disable •Pull-up MOS Tr. OFF •VIN=V_{DD} (including the off- leak current of the output Tr.)	4.5 to 5.5			1	μA
	I _{IH} (2)	<ul style="list-style-type: none"> •$\overline{\text{RES}}$ •$\overline{\text{HS}}$, $\overline{\text{VS}}$ 	•VIN=V _{DD}	4.5 to 5.5			1	
Low level input current	I _{IL} (1)	Ports 0, 1, 6, 7, 8	<ul style="list-style-type: none"> •Output disable •Pull-up MOS Tr. OFF •VIN=V_{SS} (including the off- leak current of the output Tr.)	4.5 to 5.5	-1			
	I _{IL} (2)	<ul style="list-style-type: none"> •$\overline{\text{RES}}$ •$\overline{\text{HS}}$, $\overline{\text{VS}}$ 	VIN=V _{SS}	4.5 to 5.5	-1			
High level output voltage	V _{OH} (1)	•CMOS output of ports 0,1,71-73, 84-87	I _{OH} =-1.0mA	4.5 to 5.5	V _{DD} -1			
	V _{OH} (2)	R, G, B, I, BL	I _{OH} =-0.1mA	4.5 to 5.5	V _{DD} -0.5			
Low level output voltage	V _{OL} (1)	Ports 0,1,71-73, 84-87	I _{OL} =10mA	4.5 to 5.5			1.5	V
	V _{OL} (2)	Ports 0,1,71-73, 84-87	I _{OL} =1.6mA	4.5 to 5.5			0.4	
	V _{OL} (3)	<ul style="list-style-type: none"> •R, G, B, I, BL •Port 6 	I _{OL} =3.0mA	4.5 to 5.5			0.4	
	V _{OL} (4)	Port 6	I _{OL} =6.0mA	4.5 to 5.5			0.6	
	V _{OL} (5)	Port 70	I _{OL} =1mA	4.5 to 5.5			0.4	
Pull-up MOS Tr. resistance	R _{pu}	•Ports 0, 1, 7, 84-87	V _{OH} =0.9V _{DD}	4.5 to 5.5	13	38	80	kΩ
Bus terminal short circuit resistance (SCL0-SCL1, SDA0-SDA1)	R _{BS}	<ul style="list-style-type: none"> •P60-P62 •P61-P63 		4.5 to 5.5		130	300	Ω
Hysteresis voltage	V _{HYS}	<ul style="list-style-type: none"> •Ports 0, 1, 6, 7 •$\overline{\text{RES}}$ •$\overline{\text{HS}}$, $\overline{\text{VS}}$ 	Output disable	4.5 to 5.5		0.1V _{DD}		V
Input clump voltage	V _{CLMP}	CVIN		5.0	2.3	2.5	2.7	
Pin capacitance	CP	All pins	<ul style="list-style-type: none"> •f=1MHz •Every other terminals are connected to V_{SS}. •Ta=25°C 	4.5 to 5.5		10		pF

LC86F3G64A

Serial input/output characteristics at Ta = -30°C to +85°C, VSS = 0V

Parameter		Symbol	Pins	Conditions	VDD[V]	Specification			unit
						min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	•SCK0 •SCLK0	Refer to figure 4.	4.5 to 5.5	2		tCYC
		Low Level pulse width	tCKL(1)				1		
		High Level pulse width	tCKH(1)				1		
	Output clock	Cycle	tCKCY(2)	•SCK0 •SCLK0	•Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 4.	4.5 to 5.5	2		
		Low Level pulse width	tCKL(2)					1/2tCKCY	
		High Level pulse width	tCKH(2)					1/2tCKCY	
Serial input	Data set up time	tICK	SIO	•Data set-up to SCK0. •Data hold from SCK0. •Refer to figure 4.	4.5 to 5.5	0.1		μs	
	Data hold time	tCKI				0.1			
Serial output	Output delay time (Using external clock)	tCKO(1)	SO0	•Data hold from SCK0. •Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 4.	4.5 to 5.5			7/12tCYC +0.2	
	Output delay time (Using internal clock)	tCKO(2)	SO0		4.5 to 5.5			1/3tCYC +0.2	

IIC Input/Output Conditions at Ta = -30°C to +85°C, VSS = 0V

Parameter	Symbol	Standard		High speed		unit
		min	max	min	max	
SCL Frequency	fSCL	0	100	0	400	kHz
BUS free time between stop - start	tBUF	4.7		1.3		μs
HOLD time of start, restart condition	tHD;STA	4.0		0.6		μs
L time of SCL	tLOW	4.7		1.3		μs
H time of SCL	tHIGH	4.0		0.6		μs
Set-up time of restart condition	tSU;STA	4.7		0.6		μs
HOLD time of SDA	tHD;DAT	0		0	0.9	μs
Set-up time of SDA	tSU;DAT	250		100		ns
Rising time of SDA, SCL	tR		1000	20+0.1Cb	300	ns
Falling time of SDA, SCL	tF		300	20+0.1Cb	300	ns
Set-up time of stop condition	tSU;STO	4.0		0.6		μs

Refer to figure 10

Note Cb: Total capacitance of all BUS (unit: pF)

LC86F3G64A

UART (Full Duplex) Operating Conditions at Ta = -30°C to +85°C, VSS = 0V (LC863G00 only)

Parameter	Symbol	Pin/Remarks	Condition	Specification				
				VDD[V]	min	typ	max	unit
Transfer rate*	UBR(1)	P14, 15	0.844μs ≤ tCYC ≤ 400μs	4.5 to 5.5	16/6		8192/6	tCYC
	UBR(2)							

* High speed mode: $UBR = (n+1) \times (8/6)tCYC$

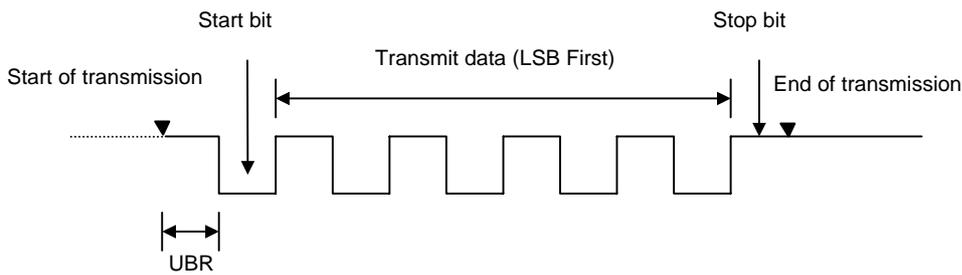
Low speed mode: $UBR = (n+1) \times (32/6)tCYC$ n=1 to 255

Data length: 7/8/9 bits(LSB First)

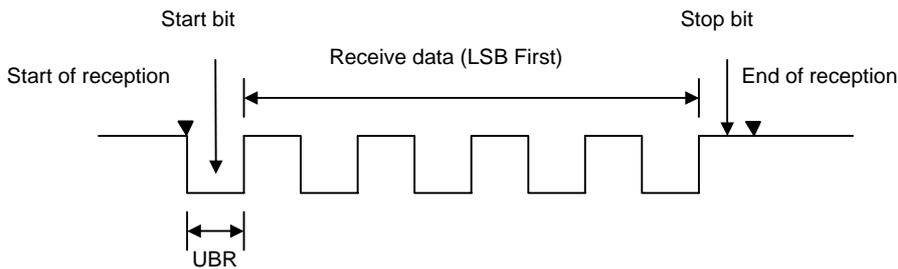
Stop bits: 1 bit

Parity bits: None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)



LC86F3G64A

Pulse Input Conditions at Ta = -30°C to +85°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	Specification				
				VDD[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1tCYC.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 16tCYC.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock is selected to 64tCYC.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	128			
	tPIL(5)	RES	Reset acceptable	4.5 to 5.5	200			μs
	tPIH(6) tPIL(6)	HS, VS	•Display position controllable •The active edge of HS and VS must be apart at least 1 tCYC. •Refer to figure 6.	4.5 to 5.5	3			
Rising/falling time	tTHL tTLH	HS	Refer to figure 6.	4.5 to 5.5			500	ns
External OSD clock input	tOSCK	OSDCK (P16)	Refer to figure 7.	4.5 to 5.5	10			ns

AD Converter Characteristics at Ta = -30°C to +85°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	Limits					
				VDD[V]	min	typ	max	unit	
Resolution	N			4.5 to 5.5		8		bit	
Absolute precision	ET		(Note 3)				±1.5	LSB	
Conversion time	tCAD		ADCR2=0 (Note 4)			16		tCYC	
			ADCR2=1 (Note 4)			32			
Analog input voltage range	VAIN	AN4 - AN7 (LC863300: AN3-AN7)				VSS		VDD	V
Analog port input current	I _{AINH}		VAIN=VDD				1		μA
	I _{AINL}		VAIN=VSS		-1				

Note 3: Absolute precision does not include quantizing error (1/2LSB).

Note 4: Conversion time is the time till the complete digital conversion value for analog input value is set to a register after the instruction to start conversion is sent.

LC86F3G64A

Sample Current Dissipation Characteristics at Ta = -30°C to +85°C, VSS = 0V

The sample current dissipation characteristics is the measurement result of Sanyo provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally.

The currents through the output transistors and the pull-up MOS transistors are ignored.

Parameter	Symbol	Pins	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Current dissipation during basic operation (Note 3)	IDDOP(1)	V _{DD}	<ul style="list-style-type: none"> •FmX'tal=32.768kHz X'tal oscillation •System clock: VCO for system •VCO for OSD operating •Internal RC oscillation stops 	4.5 to 5.5		12	24	mA
	IDDOP(2)		<ul style="list-style-type: none"> •FmX'tal=32.768kHz X'tal oscillation •System clock: X'tal (Instruction cycle time: 366.2μs) •VCO for system, VCO for OSD, Internal RC oscillation stop •Data slicer, AD converters stop 	4.5 to 5.5		60	300	μA
Current dissipation in HALT mode (Note 3)	IDDHALT(1)	V _{DD}	<ul style="list-style-type: none"> •HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •System clock: VCO for system • Internal RC stops 	4.5 to 5.5		3	9	mA
	IDDHALT(2)		<ul style="list-style-type: none"> •HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock: Internal RC 	4.5 to 5.5		350	1000	μA
	IDDHALT(3)		<ul style="list-style-type: none"> •HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock: X'tal (Instruction cycle time: 366.2μs) 	4.5 to 5.5		40	200	
Current dissipation in HOLD mode (Note 3)	IDDHOLD	V _{DD}	<ul style="list-style-type: none"> •HOLD mode •All oscillation stops. 	4.5 to 5.5		0.05	20	μA

Note 3: The currents of the output transistors and the pull-up MOS transistors are ignored.

Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions:
 Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.

Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -30°C to +85°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rf	Rd		typ	max	
32.768kHz	SEIKO EPSON	C-002RX	18pF	18pF	OPEN	680kΩ	4.5 to 5.5V	1.0s	1.5s	

Notes: The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)

1. The VDD becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -30°C to +85°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

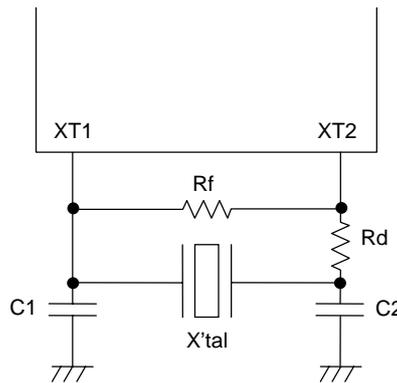
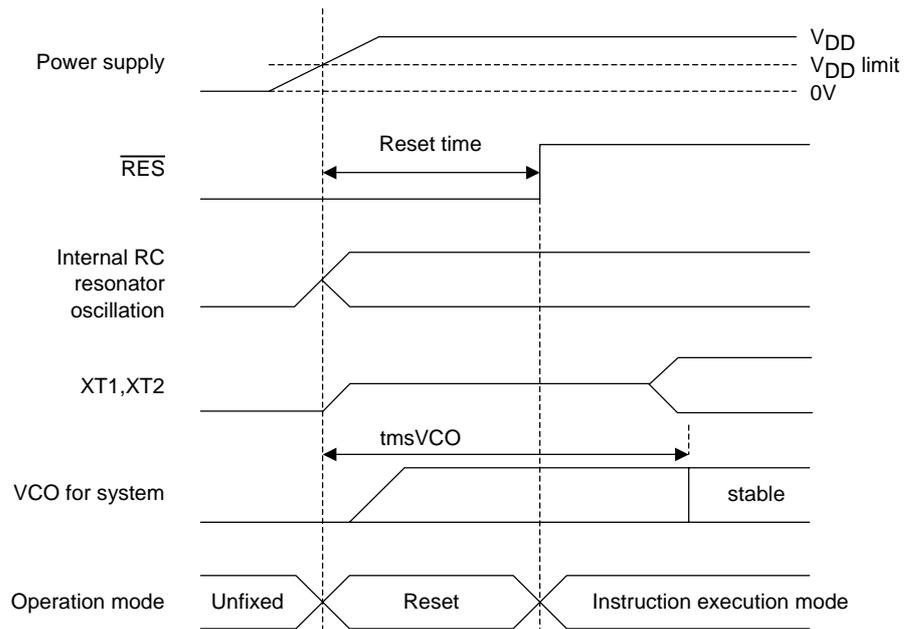
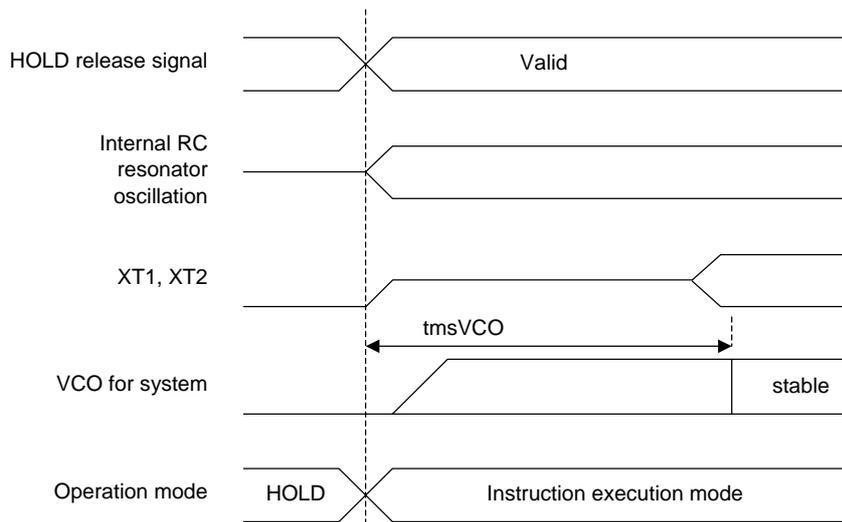


Figure 1 Recommended Oscillation Circuit

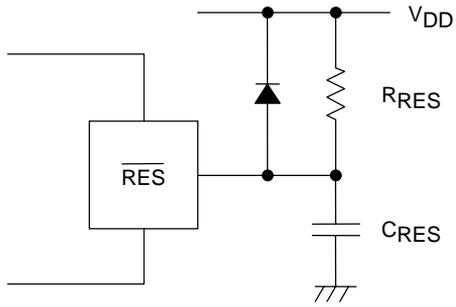


Reset Time and Oscillation Stabilizing Time



Hold release signal and oscillation stabilizing time.

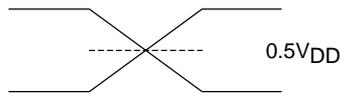
Figure 2 Oscillation Stabilizing Time



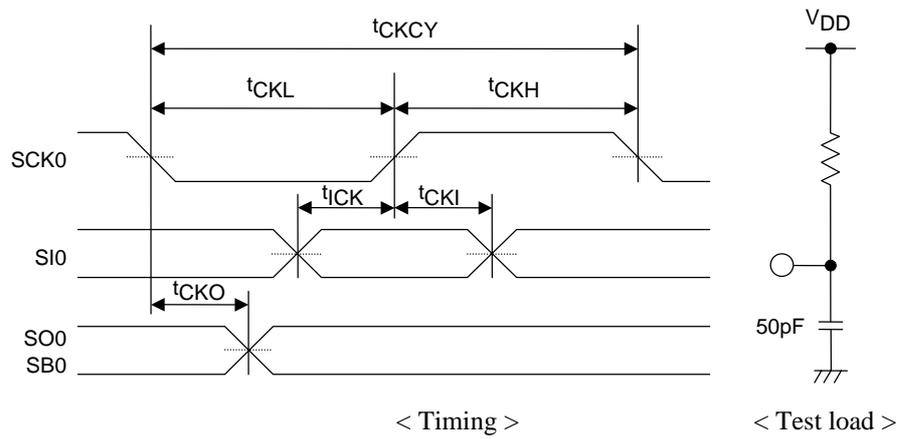
(Note)

Determine the C_{RES} , R_{RES} value to get more than 200 μ s reset time.

Figure 3 Reset Circuit



< AC timing measurement point >



< Timing >

< Test load >

Figure 4 Serial Input/Output Test Condition

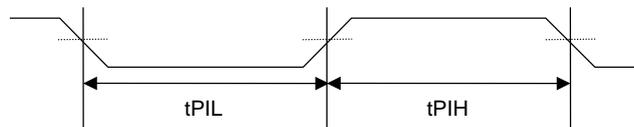


Figure 5 Pulse Input Timing Condition-1

LC86F3G64A

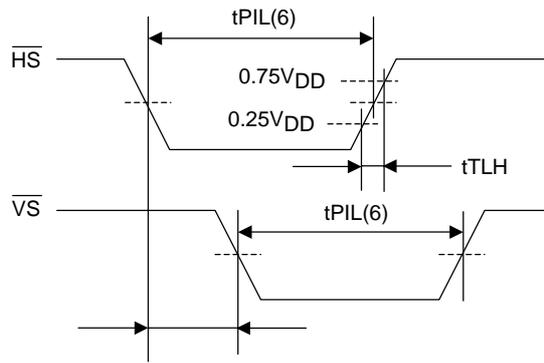
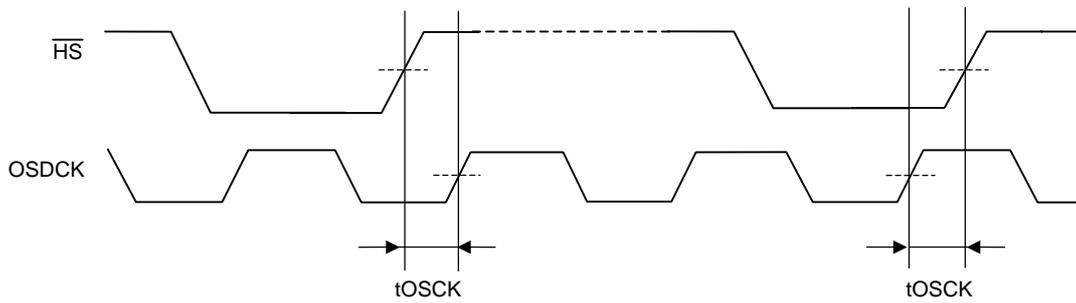


Figure 6 Pulse Input Timing Condition - 2



Note: t_{OSCK} must be saving constant

Figure 7 Pulse Input Timing Condition - 3

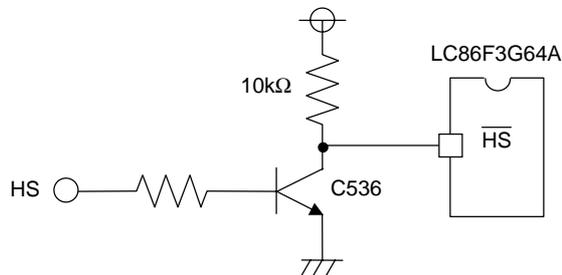
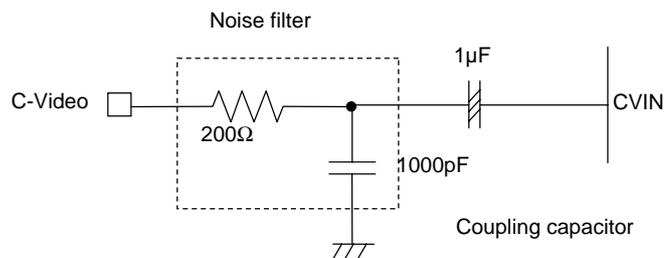


Figure 8 Recommended Interface Circuit



Output impedance of C-Video before Noise filter should be less than 100Ω.

Figure 9 CVIN Recommended Circuit

LC86F3G64A

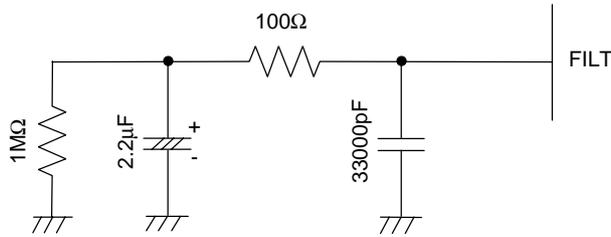
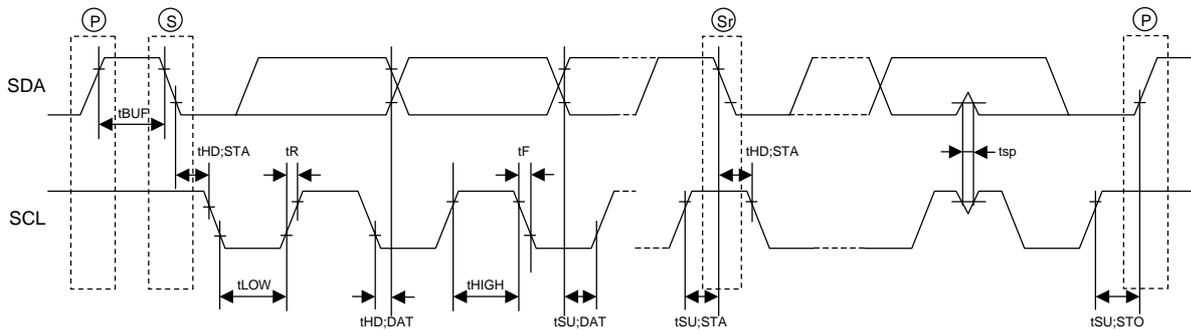


Figure 10 FILT Recommended Circuit

Note: Place FILT parts on board as close to the microcontroller as possible.



S : start condition

P : stop condition

Sr : restart condition

tsp : spike suppression

Standard mode : not exist

High speed mode : less than 50ns

Figure 11 IIC Timing

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