

**LC86P4332**

## One-time PROM built-in 8-bit Single Chip Microcontroller

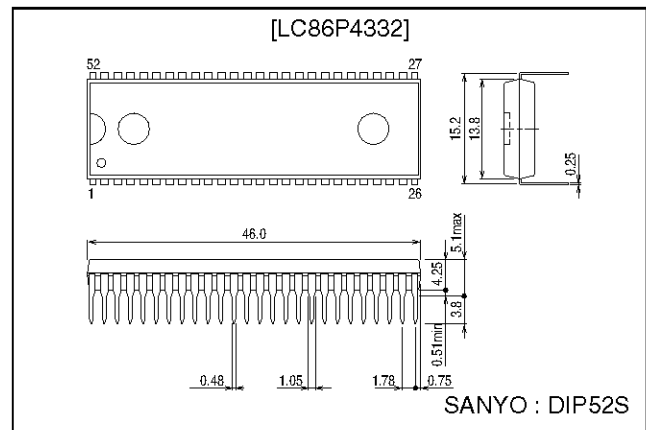
**Preliminary****Overview**

The LC86P4332 is a CMOS 8-bit single chip microcontroller with One-time PROM for the LC864300 series.

This microcontroller has the same function and the pin description as the LC864300 series mask ROM version, and the 32K-byte PROM. It is suitable for developing programs.

**Package Dimensions**

unit : mm

**3128-DIP52S****Features**

- (1) Option switching by PROM data  
The option function of the LC864300 series can be specified by the PROM data.  
The functions of the trial pieces can be evaluated using mass production board.
- (2) Internal PROM capacity : 32768 bytes (for program)  
: 16384 x 12 bits (for character)
- (3) Internal RAM capacity : 384 bytes

Mask ROM version	PROM capacity	RAM capacity
LC864332	32512 bytes	384 bytes
LC864328	28672 bytes	384 bytes
LC864324	24576 bytes	384 bytes
LC864320	20480 bytes	384 bytes
LC864316	16384 bytes	384 bytes
LC864312	12288 bytes	384 bytes

- (4) Operating supply voltage : 4.5 V to 6.0 V
- (5) Instruction cycle time : 0.99  $\mu$ s to 40  $\mu$ s
- (6) Operating temperature : -30°C to +70°C
- (7) The pin and the package compatible with the LC864300 series mask ROM devices
- (8) Applicable mask ROM version : LC864332/LC864328/LC864324/LC864320/LC864316/LC864312
- (9) Factory shipment : DIP52S

**SANYO Electric Co.,Ltd. Semiconductor Business Headquarters**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

# LC86P4332

## Usage Notes

The LC86P4332 is provided for the first release and small shipping of the LC864300 series.  
At using, take notice of the followings.

(1) Differences between LC86P4332 and the LC864300 series

Item	LC86P4332	LC864332/28/24/20/16/12
Operation after reset releasing	The option is specified by degrees until 3 ms after going to a 'H' level to the reset terminal. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to the reset terminal.
Operating supply voltage range ( $V_{DD}$ )	4.5 V to 5.5 V	4.5 V to 5.5 V
Power dissipation	Refer to 'electrical characteristics' on the semiconductor news.	

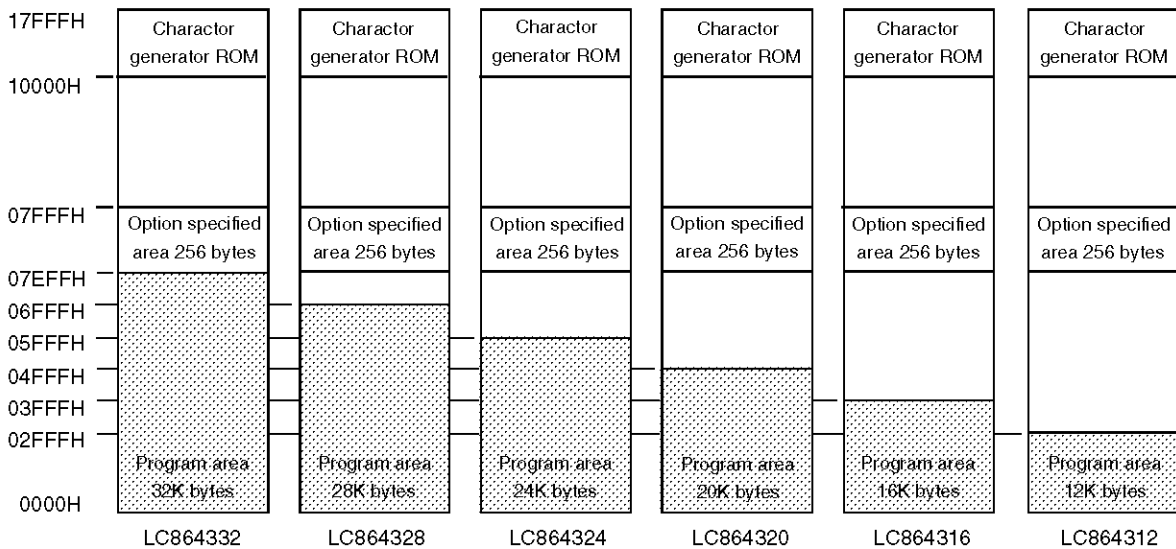
The LC86P4332 uses the program memory area of 256 bytes from 7F00H to 7FFFH to select the options.

(2) Option

The option data is written with the option specifying program "SU86K.EXE". The option data is linked to the program area by the linkage loader "L86K.EXE".

(3) ROM space

The LC86P4332 and LC864300 series use the program memory area of 256 bytes from 7F00H to 7FFFH to select the options. The program memory capacity of the series is 32512 bytes addressed on 0000H to 7EFFFH.



## How to Use

(1) Create a programming data for LC86P4332

Programming data for EPROM of the LC86P4332 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program EVA2HEX.EXE. The HEX file is used as the programming data for the LC86P4332.

(2) How to program for the PROM

The LC86P4332 can be programmed by the PROM programmer with attachment W86EP4164D.

- Recommended EPROM programmer

Manufacturer	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL1890A

- "27010 (V<sub>pp</sub> = 12.5 V) Intel high speed programming" mode should be adopted.
- A jumper (DASEC) must be set to 'OFF' at programming.
- There are two ways to program the data of the hexa-decimal file described above to the PROM of the LC86P4332.
  1. How to program the program and the character data individually.
    - First, the hexa-decimal data of 00h to 07FFFh is programmed into the address 00h to 07FFFh of the EPROM.
    - Next, write the hexa-decimal data for character addressed 10000h to 17FFFh into the address of 10000h to 17FFFh.
  2. How to program the program and the character data simultaneously.
    - First, copy the program data addressed from 00h to 07FFFh into the addresses 8000h to 0FFFFh with an EPROM programmer.
    - Next, write the data of 00h to 17FFFh into the EPROM of the LC86E4332.

An error will occur when the hexa-decimal data generated by the EVA2HEX program is programmed to the PROM of the LC86P4332 directly.

(3) How to use the data security function

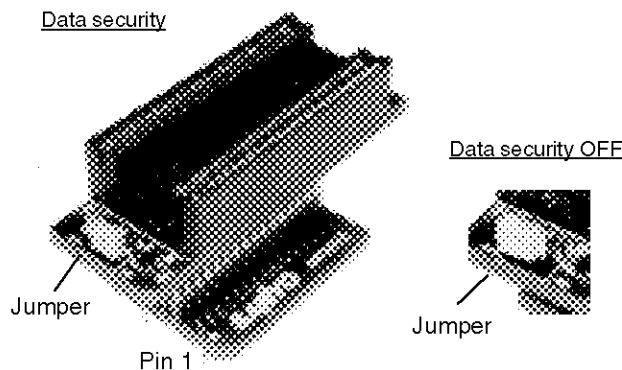
"Data security" is the function to disable the PROM data from being read out.

The following is the process in order to execute the data security function.

1. Set the jumper of attachment 'ON'.
2. Program again. The EPROM programmer will display an error. The error means that the data security functions normally. It is not trouble the EPROM programmer or the LSI.

Notes

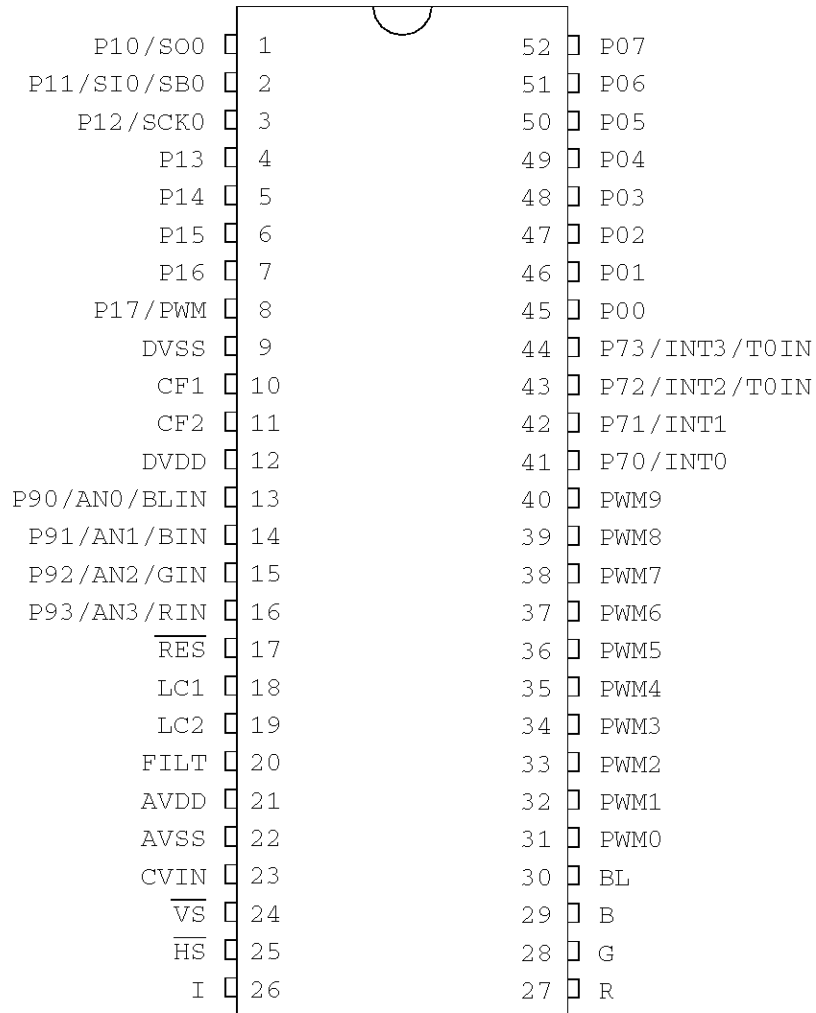
- Data security is not executed when the data of all address have 'FF' at procedure 2 above.
- Data security cannot be executed by programming the sequential operation "BLANK=>PROGRAM=>VERIFY" at procedure 2 above.
- Set the jumper to 'OFF' after executing the data security.



W86EP4164D

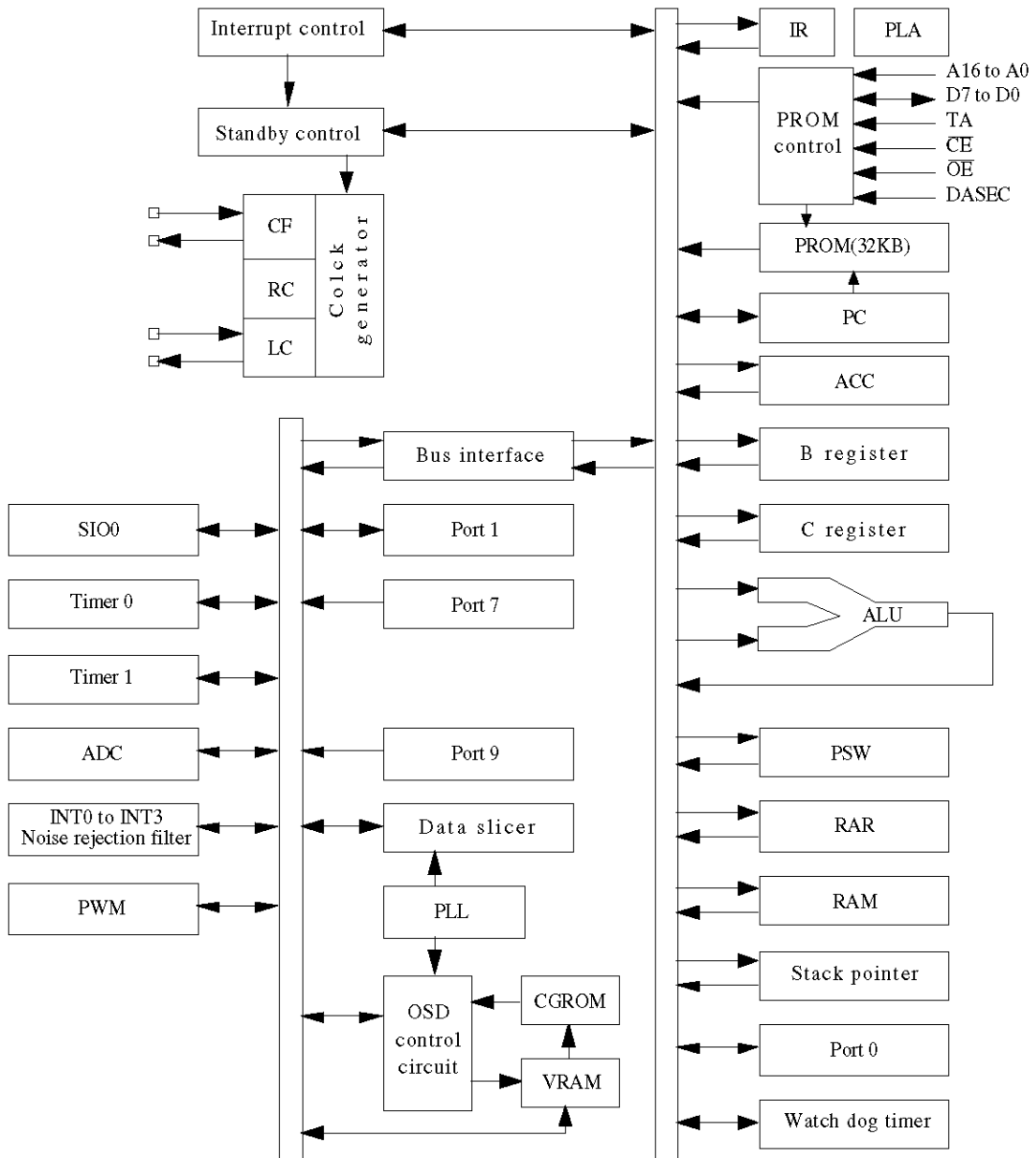
# LC86P4332

## Pin Assignment



Top view

System Block Diagram



# LC86P4332

## Pin Description

- Port option can be specified by bit units.
- At port 0, 'Pull-up resistor provided' when specifying CMOS output.  
'Pull-up resistor not provided' when specifying N-ch open drain output.
- At port 1, 'Programmable pull-up resistor provided' when specifying either CMOS or N-ch open drain output.

Pin Description Table

Pin name	Pin No.	I/O	Function description	Option	PROM mode								
DVSS	9	–	Negative power supply for digital circuit										
CF1	10	I	Input terminal for ceramic resonator										
CF2	11	O	Output terminal for ceramic resonator										
DVDD	12	–	Positive power supply for digital circuit										
RES	17	I	Reset terminal										
LC1	18	I	LC oscillation circuit input terminal										
LC2	19	O	LC oscillation circuit output terminal										
FILT	20	O	Filter terminal for PLL										
AVDD	21	–	Positive power supply for analog circuit										
AVSS	22	–	Negative power supply for analog circuit										
CVIN	23	I	Video signal input terminal										
VS	24	I	Vertical synchronization signal input terminal										
HS	25	I	Horizontal synchronization signal input terminal										
I	26	O	Image intensity output										
R	27	O	Red (R) output terminal of RGB image output		A4 (*1)								
G	28	O	Green (G) output terminal of RGB image output		A5 (*1)								
B	29	O	Blue (B) output terminal of RGB image output		A6 (*1)								
BL	30	O	Fast blanking control signal Switch TV image signal and caption/OSD image signal		A7 (*1)								
PWM0 to PWM9	31 to 40	O	PWM0 to 9 output terminal 15 V withstand		PWM0 to 8 : A8 to A16 (*1) PWM9 : "L" fixed								
Port 0	45 to 52	I/O	8-bit Input/output port Input/output can be specified in nibble units HOLD release input Interrupt input	Pull-up resistor Provided/not provided (in bit units)  Output Format CMOS/Nch-OD (in bit units)									
P00 to P07													
Port 1	1 to 8	I/O	8-bit Input/output port Input/output can be specified in a bit. Other function	Output Format CMOS/Nch-OD (in bit units)	D0 to D7 (*2)								
P10 to P17													
			<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30px;">P10</td> <td>SIO0 data output</td> </tr> <tr> <td>P11</td> <td>SIO0 data input / bus input / output</td> </tr> <tr> <td>P12</td> <td>SIO0 clock input / output</td> </tr> <tr> <td>P17</td> <td>Timer 1 (PWM) output</td> </tr> </table>	P10	SIO0 data output	P11	SIO0 data input / bus input / output	P12	SIO0 clock input / output	P17	Timer 1 (PWM) output		
P10	SIO0 data output												
P11	SIO0 data input / bus input / output												
P12	SIO0 clock input / output												
P17	Timer 1 (PWM) output												

## LC86P4332

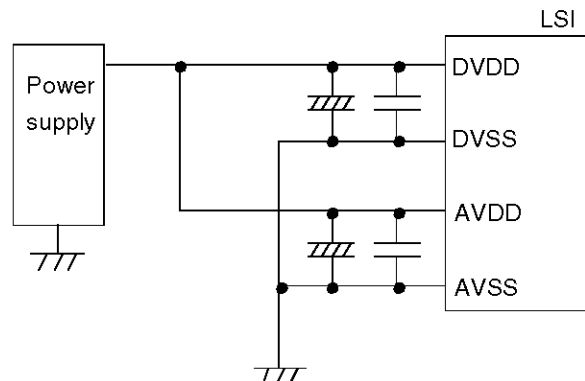
Pin name	Pin No.	I/O	Function Description	Option	PROM mode																																											
Port 7 P70 P71 to P73	41 42 to 44	I/O I	4-bit input port Other function <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">P70</td> <td>INT0 input / HOLD release input / Nch-transistor output for watchdog timer</td> </tr> <tr> <td>P71</td> <td>INT1 input / HOLD release input</td> </tr> <tr> <td>P72</td> <td>INT2 input / timer 0 event input</td> </tr> <tr> <td>P73</td> <td>INT3 input (noise rejection filter attached input / timer 0 event input</td> </tr> </table> Interrupt receiver format vector address <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th></th> <th>Rise</th> <th>Fall</th> <th>Rise/Fall</th> <th>H level</th> <th>L level</th> <th>Vector</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>03H</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>0BH</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>13H</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>1BH</td> </tr> </tbody> </table>	P70	INT0 input / HOLD release input / Nch-transistor output for watchdog timer	P71	INT1 input / HOLD release input	P72	INT2 input / timer 0 event input	P73	INT3 input (noise rejection filter attached input / timer 0 event input		Rise	Fall	Rise/Fall	H level	L level	Vector	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH	Pull-up resistor provided/ not provided (in bit units)	P70 : VPP (*3) P71 : DASEC (*4) P72 : $\overline{OE}$ (*5) P73 : $\overline{CE}$ (*6)
P70	INT0 input / HOLD release input / Nch-transistor output for watchdog timer																																															
P71	INT1 input / HOLD release input																																															
P72	INT2 input / timer 0 event input																																															
P73	INT3 input (noise rejection filter attached input / timer 0 event input																																															
	Rise	Fall	Rise/Fall	H level	L level	Vector																																										
INT0	enable	enable	disable	enable	enable	03H																																										
INT1	enable	enable	disable	enable	enable	0BH																																										
INT2	enable	enable	enable	disable	disable	13H																																										
INT3	enable	enable	enable	disable	disable	1BH																																										
Port 9 P90 to P93	13 to 16	I	4-bit input port Other function A/D converter input port (4 lines)	External RGB input	A0 to A3 (*3)																																											

- \*1 An → Address input
- \*2 Data I/O
- \*3 Power for programming
- \*4 Memory select input/output for data security
- \*5 OutputEnable input
- \*6 ChipEnable input

- Port status during reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	Input	Pull-up resistor OFF, ON after reset release
Port 1	Input	Programmable pull-up resistor OFF
Port 7	Input	Fixed pull-up resistor provided

\* AVDD and AVSS are the power supply terminals for the analog operation block. DVDD and DVSS are the power supply terminals for the digital operation block. Connect as shown in the following figure to reduce the noise influence.



## Specifications

### 1. Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit		
				V <sub>DD</sub> [V]	min	typ		max	
Supply voltage	V <sub>DDmax</sub>	DVDD, AVDD	DVDD = AVDD		-0.3		+7.0	V	
Input voltage	V <sub>I(1)</sub>	<ul style="list-style-type: none"> <li>• P71, 72, 73</li> <li>• Port 9</li> <li>• RES, HS, VS, CVIN</li> </ul>			-0.3		V <sub>DD</sub> +0.3		
Output voltage	V <sub>O(1)</sub>	R, G, B, BL, I, FILT			-0.3		V <sub>DD</sub> +0.3		
	V <sub>O(2)</sub>	PWM0 to PWM9			-0.3		+15		
Input/output voltage	V <sub>IO</sub>	Ports 0, 1, P70			-0.3		V <sub>DD</sub> +0.3		
High-level output current	Peak output current	I <sub>OPH(1)</sub>	Ports 0, 1	<ul style="list-style-type: none"> <li>• Pull-up MOS transistor output</li> <li>• At each pin</li> </ul>		-2			mA
		I <sub>OPH(2)</sub>	Ports 0, 1	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• At each pin</li> </ul>		-4			
		I <sub>OPH(3)</sub>	R, G, B, BL, I	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• At each pin</li> </ul>		-5			
	Total current	ΣI <sub>OA(1)</sub>	Port 1	The total of all pins		-10			
		ΣI <sub>OA(2)</sub>	Port 0	The total of all pins		-10			
		ΣI <sub>OA(3)</sub>	R, G, B, BL, I	The total of all pins		-15			
Low-level output current	Peak output current	I <sub>OPL(1)</sub>	Ports 0, 1	At each pin				20	
		I <sub>OPL(2)</sub>	P70	At each pin				30	
		I <sub>OPL(3)</sub>	<ul style="list-style-type: none"> <li>• R, G, B, BL, I</li> <li>• PWM0 to PWM9</li> </ul>	At each pin				5	
	Total current	ΣI <sub>OAL(1)</sub>	Port 0	The total of all pins					40
		ΣI <sub>OAL(2)</sub>	Port 1, P70	The total of all pins					40
		ΣI <sub>OAL(3)</sub>	R, G, B, BL, I	The total of all pins					15
		ΣI <sub>OAL(4)</sub>	PWM0 to PWM9	The total of all pins					30
	Maximum power dissipation	Pd max	DIP52S	Ta = -30 to +70°C				430	mW
Operating temperature range	Topr				-30		+70	°C	
Storage temperature range	Tstg				-55		+125		

\*DVSS and AVSS must be supplied the same voltage, V<sub>SS</sub>. V<sub>SS</sub> = DVSS = AVSS  
 DVDD and AVDD must be supplied the same voltage, V<sub>DD</sub>. V<sub>DD</sub> = DVDD = AVDD



## LC86P4332

### 2. Recommended Operating Range at Ta = -30°C to +70°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Operating supply voltage range	V <sub>DD</sub>	DVDD, AVDD	0.97 μs ≤ tCYC tCYC ≤ 1.02 μs		4.5		5.5	V
Hold voltage	V <sub>HD</sub>	DVDD, AVDD	RAMs and the registers hold data at HOLD mode.		2.0		5.5	
Input high-level voltage	V <sub>IH</sub> (1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	0.6V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (2)	• Port 1 (Schmitt) • P72, 73 • HS, VS	Output disable	4.5 to 5.5	0.75V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (3)	• P70 port input / interrupt • P71 • RES (Schmitt)	Output N-channel transistor OFF	4.5 to 5.5	0.75V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (4)	• P70 Watchdog timer input	Output N-channel transistor OFF	4.5 to 5.5	V <sub>DD</sub> -0.5		V <sub>DD</sub>	
	V <sub>IH</sub> (5)	Port 9 port input		4.5 to 5.5	0.7V <sub>DD</sub>		V <sub>DD</sub>	
Input low-level voltage	V <sub>IL</sub> (1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (2)	• Port 1 (Schmitt) • P72, 73 • HS, VS • Port 9	Output disable	4.5 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
	V <sub>IL</sub> (3)	• P70 port input / interrupt • P71 • RES (Schmitt)	N-channel transistor OFF	4.5 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
	V <sub>IL</sub> (4)	• P70 Watchdog timer input	N-channel transistor OFF	4.5 to 5.5	V <sub>SS</sub>		0.6V <sub>DD</sub>	
	V <sub>IL</sub> (5)	Port 9 port input		4.5 to 5.5	V <sub>SS</sub>		0.3V <sub>DD</sub>	
CVIN input amplitude	V <sub>CVIN</sub>	CVIN		5.0	1Vp-p -3dB	1Vp-p	1Vp-p +3dB	Vp-p *
Operation cycle time	tCYC(1)		OSD function	4.5 to 5.5	0.97	1	1.02	μs
	tCYC(2)		Except OSD function	4.5 to 5.5	0.97		40	

\* Vp-p : Peak-to-peak voltage

## LC86P4332

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 1.	4.5 to 5.5	11.76	12	12.24	MHz
	FmCF(2)		12.08 MHz (ceramic resonator oscillation) Refer to Figure 1.		11.84	12.08	12.32	
	FmLC	LC1, LC2	14.11 MHz (LC oscillation) Refer to Figure 2.	4.5 to 5.5		14.11		
	FmRC		RC oscillation	4.5 to 5.5	0.4	0.8	3.0	
Oscillation stable time period (Note 2)	tmsCF(1)	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 3.	4.5 to 5.5		0.02	0.2	ms
	tmsCF(2)		12.08 MHz (ceramic resonator oscillation) Refer to Figure 3.			0.02	0.2	

(Note 1) Refer to Table 1 and Table 2 for the oscillation constant.

(Note 2) The oscillation stable time period refers to the time it takes to oscillate stably after the following conditions.

1. Applying the first supply voltage.
  2. Release of the HOLD mode.
  3. Release of the stopping of the main-clock oscillation.
- Refer to Figure 3 for details.

## LC86P4332

### 3. Electrical Characteristics at Ta = -30°C to +70°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Input high-level current	I <sub>IH</sub> (1)	<ul style="list-style-type: none"> <li>Port 1</li> <li>Port 0 without pull-up MOS transistor</li> </ul>	<ul style="list-style-type: none"> <li>Output disable</li> <li>Pull-up MOS transistor OFF</li> <li>V<sub>IN</sub> = V<sub>DD</sub> (including the off-leak current of the output transistor)</li> </ul>	4.5 to 5.5			1	μA
	I <sub>IH</sub> (2)	<ul style="list-style-type: none"> <li>Port 7 without pull-up MOS transistor</li> <li>Port 9</li> <li><math>\overline{RES}</math></li> <li><math>\overline{HS}</math>, <math>\overline{VS}</math></li> </ul>	V <sub>IN</sub> = V <sub>DD</sub>	4.5 to 5.5			1	
Input low-level current	I <sub>IL</sub> (1)	<ul style="list-style-type: none"> <li>Port 1</li> <li>Port 0 without pull-up MOS transistor</li> </ul>	<ul style="list-style-type: none"> <li>Output disable</li> <li>Pull-up MOS transistor OFF</li> <li>V<sub>IN</sub> = V<sub>SS</sub> (including the off-leak current of the output transistor)</li> </ul>	4.5 to 5.5	-1			
	I <sub>IL</sub> (2)	<ul style="list-style-type: none"> <li>Port 7 without pull-up MOS transistor</li> <li>Port 9</li> </ul>	V <sub>IN</sub> = V <sub>SS</sub>	4.5 to 5.5	-1			
	I <sub>IL</sub> (3)	<ul style="list-style-type: none"> <li><math>\overline{RES}</math></li> <li><math>\overline{HS}</math>, <math>\overline{VS}</math></li> </ul>	V <sub>IN</sub> = V <sub>SS</sub>	4.5 to 5.5	-1			
Output high-level voltage	V <sub>OH</sub> (1)	CMOS output of ports 0, 1	I <sub>OH</sub> = -1.0 mA	4.5 to 5.5	V <sub>DD</sub> -1			V
	V <sub>OH</sub> (2)	R, G, B, BL, I	I <sub>OH</sub> = -0.1 mA	4.5 to 5.5	V <sub>DD</sub> -0.5			
Output low-level voltage	V <sub>OL</sub> (1)	Ports 0, 1	I <sub>OL</sub> = 10 mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (2)	Ports 0, 1	<ul style="list-style-type: none"> <li>I<sub>OL</sub> = 1.6 mA</li> <li>The total current of the ports 0,1 is not over 40 mA.</li> </ul>	4.5 to 5.5			0.4	
	V <sub>OL</sub> (3)	<ul style="list-style-type: none"> <li>R, G, B, BL, I</li> <li>PWM0 to PWM9</li> </ul>	<ul style="list-style-type: none"> <li>I<sub>OL</sub> = 3.0 mA</li> <li>The current of any unmeasured pin is not over 3 mA.</li> </ul>	4.5 to 5.5			0.4	
	V <sub>OL</sub> (4)	P70	I <sub>OL</sub> = 1 mA	4.5 to 5.5			0.4	
Pull-up MOS transistor resistance	R <sub>pu</sub>	<ul style="list-style-type: none"> <li>Ports 0, 1</li> <li>Port 7</li> </ul>	V <sub>OH</sub> = 0.9 V <sub>DD</sub>	4.5 to 5.5	13	38	80	kΩ
Output off-leakage current	I <sub>OFF</sub>	PWM0 to PWM9	V <sub>OUT</sub> = 13.5 V	4.5 to 5.5			5	μA
Hysteresis voltage	V <sub>HIS</sub>	<ul style="list-style-type: none"> <li>Ports 0, 1</li> <li>Port 7</li> <li><math>\overline{RES}</math></li> <li><math>\overline{HS}</math>, <math>\overline{VS}</math></li> </ul>	Output disable	4.5 to 5.5		0.1V <sub>DD</sub>		V

## LC86P4332

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Input clamp voltage	V <sub>CLMP</sub>	CVIN		5.0	2.3	2.5	2.7	V
Pin capacitance	CP	All pins	<ul style="list-style-type: none"> <li>• f = 1MHz</li> <li>• Unmeasured input pins are set to V<sub>SS</sub> level.</li> <li>• Ta = 25°C</li> </ul>	4.5 to 5.5		10		pF

### 4. Serial Input/Output Characteristics at Ta = -30°C to +70°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit				
				V <sub>DD</sub> [V]	min	typ		max			
Serial clock	Input clock	Cycle	tCKCY(1)	• SCK0	Refer to Figure 5.	4.5 to 5.5	2			tCYC	
		Low-level pulse width	tCKL(1)	• SCLK0							1
		High-level pulse width	tCKH(1)								1
	Output clock	Cycle	tCKCY(2)	• SCK0	<ul style="list-style-type: none"> <li>• Use a pull-up resistor (1 kΩ) when open drain output</li> <li>• Refer to Figure 5.</li> </ul>	4.5 to 5.5	2				
		Low-level pulse width	tCKL(2)	• SCLK0							1/2tCKCY
		High-level pulse width	tCKH(2)								1/2tCKCY
Serial input	Data set-up time	tICK	• SI0	<ul style="list-style-type: none"> <li>• Data set-up to SCK0 rising</li> <li>• Data hold from SCK0 rising</li> <li>• Refer to Figure 5.</li> </ul>	4.5 to 5.5	0.1			μs		
	Data hold time	tICKI								0.1	
Serial output	Output delay time (External serial clock)	tCKO(1)	• SO0	<ul style="list-style-type: none"> <li>• Use a pull-up resistor (1 kΩ) when open drain output.</li> <li>• Data set-up to SCK0 falling</li> <li>• Data hold from SCK0 falling</li> <li>• Refer to Figure 5.</li> </ul>	4.5 to 5.5			7/12tCYC +0.2	μs		
	Output delay time (Internal serial clock)	tCKO(2)								1/3tCYC +0.2	

## LC86P4332

### 5. Pulse Input Conditions at $T_a = -30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				$V_{DD}$ [V]	min	typ		max
High/low level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN	• Interrupt acceptable • Timer0-countable	4.5 to 5.5	1		tCYC	
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is set to 1/1)	• Interrupt acceptable • Timer0-countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is set to 1/16)	• Interrupt acceptable • Timer0-countable	4.5 to 5.5	32			
	tPIL(4)	$\overline{\text{RES}}$	Reset acceptable	4.5 to 5.5	200		$\mu\text{s}$	
	tPIH(5) tPIL(5)	$\overline{\text{HS}}$ , $\overline{\text{VS}}$	Display position controllable Each active edge of $\overline{\text{HS}}$ , $\overline{\text{VS}}$ must be more than 1tCYC. Refer to Figure 7.	4.5 to 5.5	10		tCYC	
Rise/fall time	tTHL tTLH	$\overline{\text{HS}}$	Refer to Figure 7.	4.5 to 5.5		500	ns	
Horizontal pull-in range	FH	$\overline{\text{HS}}$	The monitor point in Figure 10 is $1/2 V_{DD}$ .	4.5 to 5.5	15.23	15.73	16.23	kHz

### 6. A/D Converter Characteristics at $T_a = -30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				$V_{DD}$ [V]	min	typ		max
Resolution				4.5 to 5.5		5	bit	
Absolute precision			(Note 3)	4.5 to 5.5		$\pm 1/4$	$\pm 3/4$	LSB
Conversion time	tCAD	From Vref selection to when the result is produced	1 bit conversion time = 2tCYC	4.5 to 5.5		2		$\mu\text{s}$
Reference current	$I_{REF}$		(Regulate the ladder resistor)	4.5 to 5.5		1.0	2.0	mA
Analog input voltage range	$V_{AIN}$	AN0 to AN3		4.5 to 5.5	$V_{SS}$		$V_{DD}$	V
Analog port input current	$I_{AINH}$		$V_{AIN} = V_{DD}$	4.5 to 5.5			1	$\mu\text{A}$
	$I_{AINL}$		$V_{AIN} = V_{SS}$	4.5 to 5.5	-1			

(Note 3) Absolute precision excepts quantization error ( $\pm 1/2$  LSB).

## LC86P4332

### 7. Current Drain Characteristics at Ta = -30°C to +70°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Current drain during basic operation (Note 4)	I <sub>DDOP</sub> (1)	DVDD, AVDD	<ul style="list-style-type: none"> <li>• FmCF = 12 MHz or FmCF = 12.08 MHz when ceramic resonator oscillation</li> <li>• FmLC = 14.11 MHz when LC oscillation</li> <li>• System clock : when CF oscillation</li> <li>• Internal RC oscillation stops</li> </ul>	4.5 to 5.5		25	38	mA
Current drain in HALT mode (Note 4)	I <sub>DDHALT</sub> (1)	DVDD, AVDD	<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF = 12 MHz or FmCF = 12.08 MHz when ceramic resonator oscillation</li> <li>• FmLC = 0 Hz (when oscillation stops)</li> <li>• System clock : CF oscillation</li> <li>• Internal RC oscillation stops.</li> </ul>	4.5 to 5.5		5	10	mA
	I <sub>DDHALT</sub> (2)	DVDD, AVDD	<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF = 0 MHz (when oscillation stops)</li> <li>• FmLC = 0 Hz (when oscillation stops)</li> <li>• System clock : Internal RC</li> </ul>	4.5 to 5.5		600	1200	μA
Current drain in HOLD mode (Note 4)	I <sub>DDHOLD</sub>	DVDD, AVDD	<ul style="list-style-type: none"> <li>• HOLD mode</li> <li>• All oscillation stops.</li> </ul>	4.5 to 5.5		0.05	20	μA

(Note 4) The currents into the output transistors and the pull-up MOS transistors are ignored.

## LC86P4332

Oscillation type	Manufacturer	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33 pF	33 pF
12.08 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ021	33 pF	33 pF
		CST12.0MTW021	on chip	
	Kyocera	KBR-12.08M	33 pF	33 pF

\* Both C1 and C2 must use K rank ( $\pm 10\%$ ) and SL characteristics.

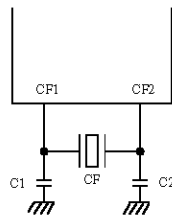
**Table 1. Ceramic Resonator Oscillation Guaranteed Constant (main-clock)**

Oscillation type	L	C3	C4
14.11 MHz LC oscillation	4.7 $\mu\text{H}$	33 pF	45 pF (Trimmer)
	4.7 $\mu\text{H} \pm 10\%$ (Variable)	33 pF	33 pF

\* See Figures 11 and 12.

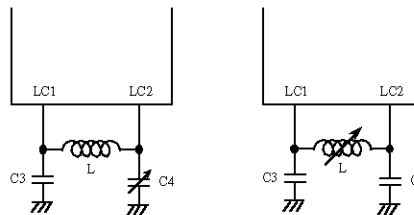
**Table 2. LC Oscillation Guaranteed Constant (OSD clock)**

- (Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
  - If you use other oscillators herein, we provide no guarantee for the characteristics.
  - Adjust the voltage of monitor point in Figure 10 to  $1/2 V_{DD} \pm 10\%$  by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.



main clock

**Figure 1 Ceramic Resonator Oscillation**



OSD clock

**Figure 2 LC Resonator Oscillation**

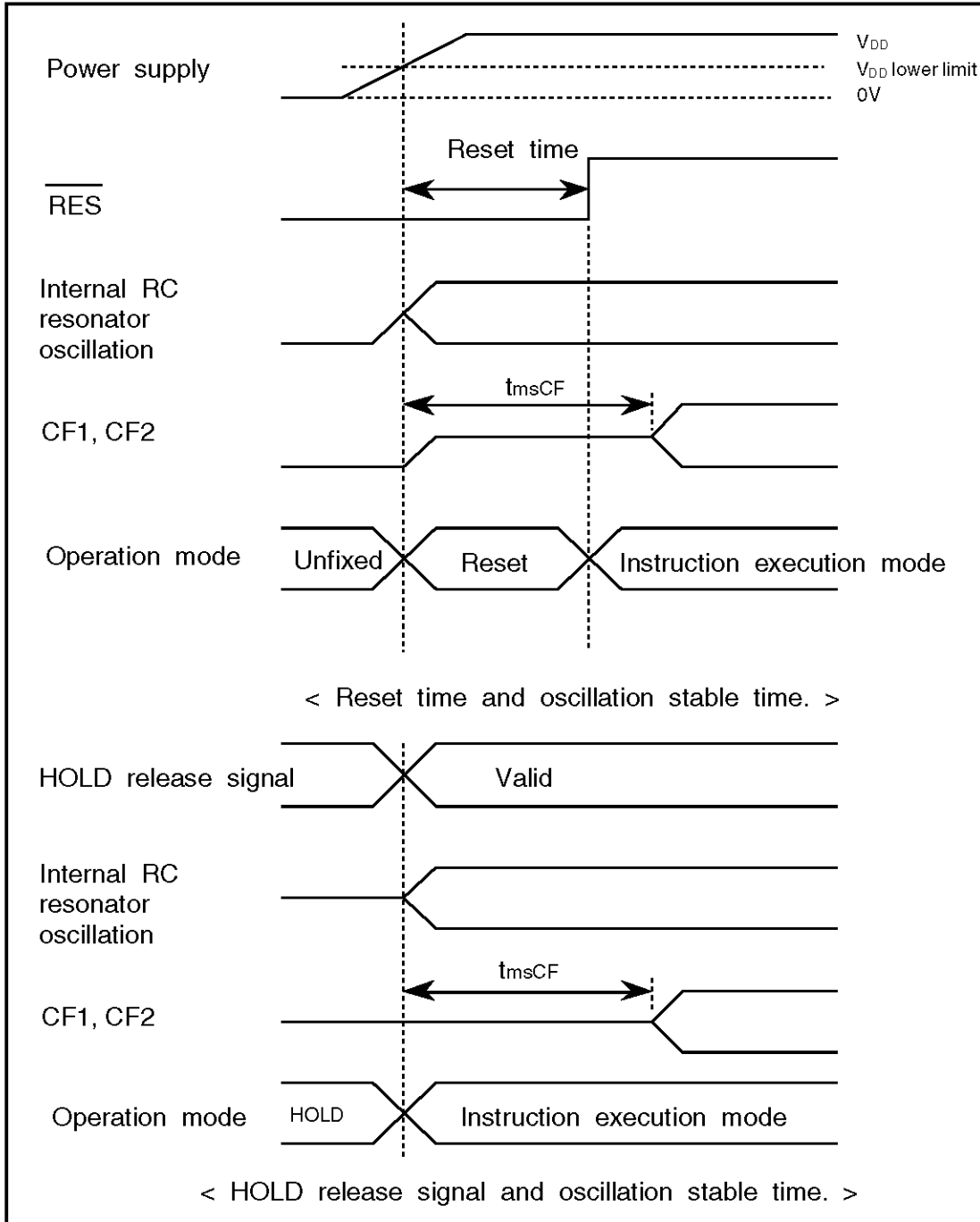
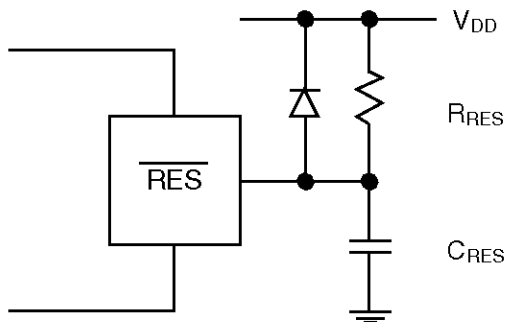


Figure 3 Oscillation Stable Time



(Note) Set the values of C<sub>RES</sub>, R<sub>RES</sub> so that the reset time is 200 μs or longer.

Figure 4 Reset Circuit



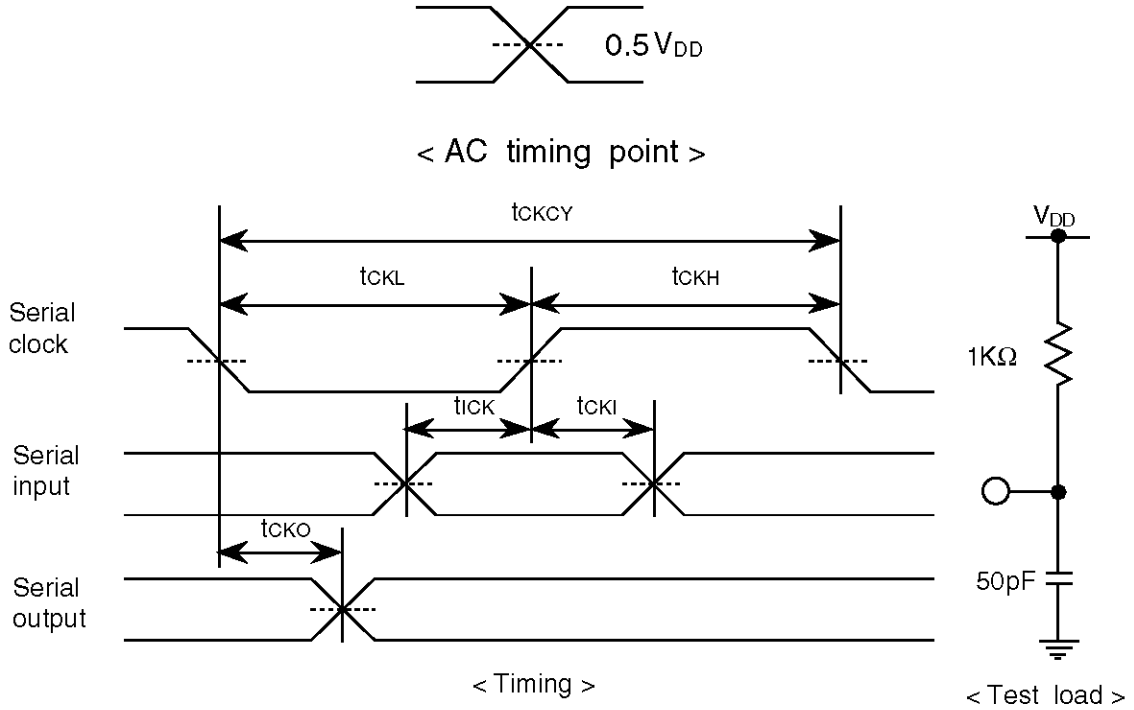


Figure 5 Serial Input/output Test Condition

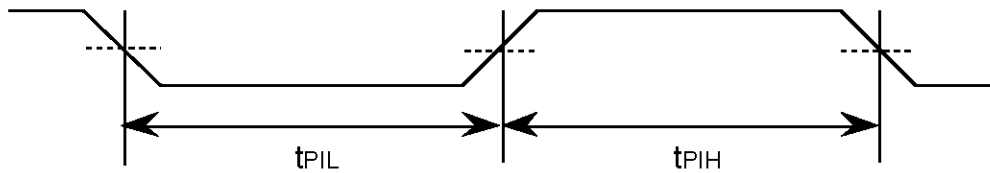


Figure 6 Pulse Input Timing Condition - 1

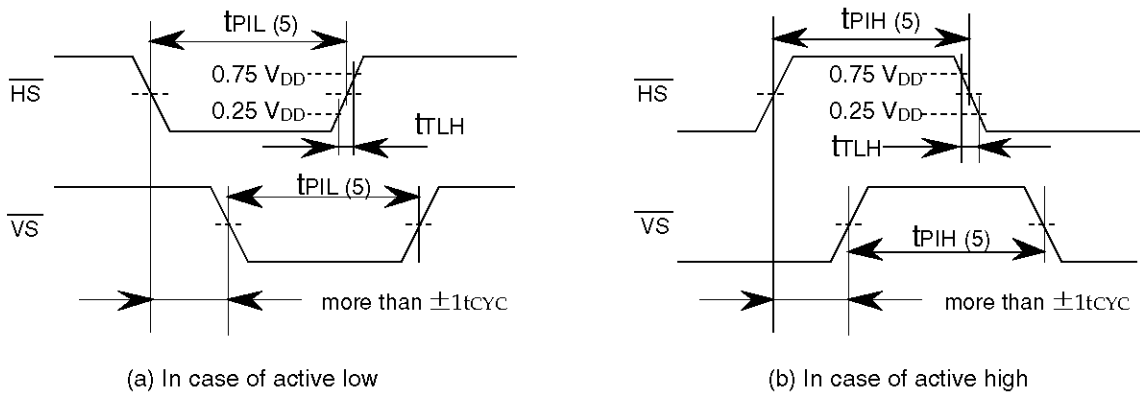


Figure 7 Pulse Input Timing Condition - 2

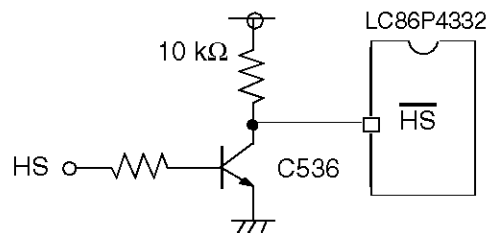


Figure 8 Recommended Interface Circuit

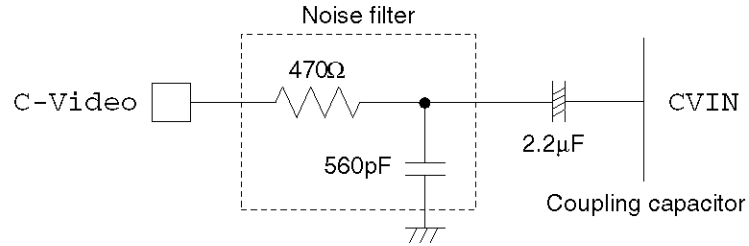


Figure 9 CVIN Recommended Circuit

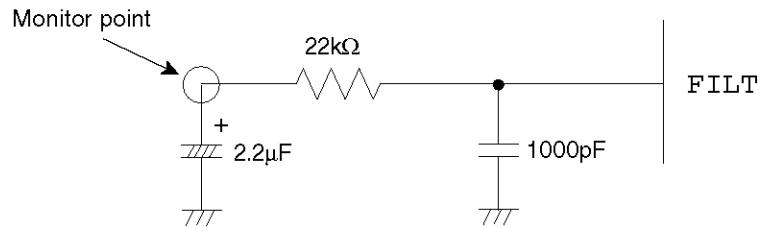


Figure 10 FILT Recommended Circuit

(Note) • Place the parts connected FILT terminal as close to the FILT as possible with the shortest pattern length on the board.

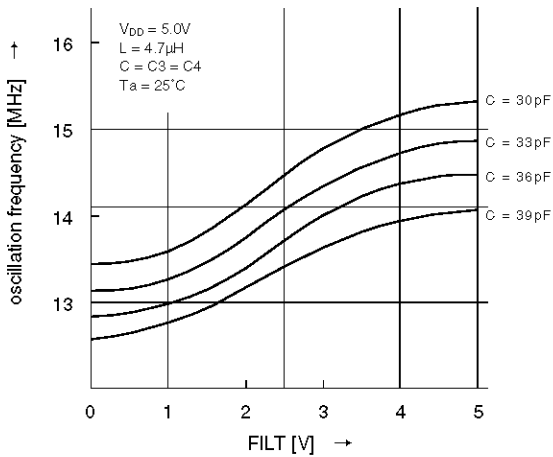


Figure 11 FILT-LC Oscillation Frequency(1)

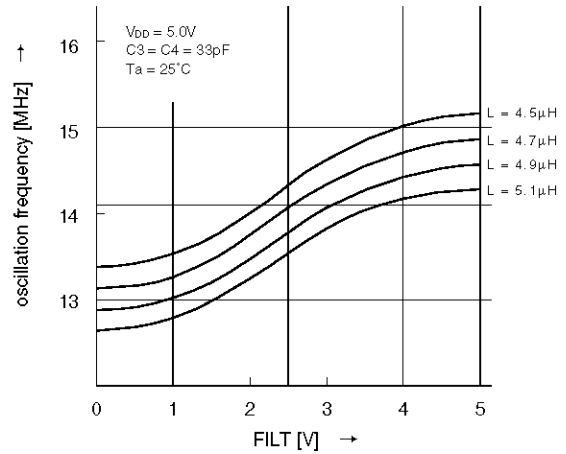


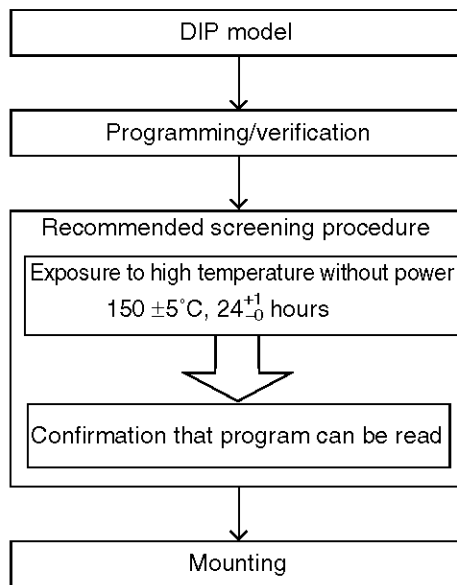
Figure 12 FILT-LC Oscillation Frequency(2)

**Requirements Prior to Mounting**

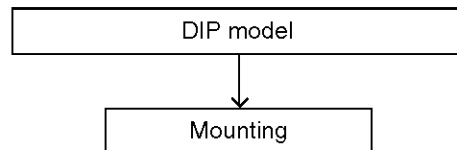
Notes on Handling

- The construction of one-time microcontrollers in which the PROM is not programmed precludes Sanyo from fully testing them before they are shipped. The screening procedure described below is recommended in order to attain higher reliability after programming the PROM.
- The nature of one-time microcontrollers in which the PROM is not programmed precludes us from fully testing them by writing all of the bits. Therefore, it is not possible for us to guarantee a write yield of 100%.
- Storage in moisture-proof packaging (unopened)  
While they are still in the moisture-proof packaging, these devices should be stored at a temperature of 30°C and a humidity of no more than 70%.
- After opening the moisture-proof packaging  
These devices should be mounted and soldered as soon as possible after the moisture-proof packaging is opened. Once the moisture-proof packaging is opened, the devices should be stored at a temperature of 30°C and a humidity of no more than 70% for no more than 96 hours.

- a. In the case of models that are programmed by the user (models that are shipped with the PROM not programmed)



- b. Requirements prior to mounting for models that are programmed by Sanyo (models that are shipped with the PROM already programmed)



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use
  - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of March, 1998. Specifications and information herein are subject to change without notice.