



SANYO Semiconductors

DATA SHEET

LC875832A

LC875824A

LC875816A

CMOS IC

ROM 32K/24K/16K byte, RAM 1024 byte on-chip

8-bit 1-chip Microcontroller

Overview

The SANYO LC875832A/24A/16A are 8-bit microcomputers that, centered around a CPU running at a minimum bus cycle time of 100ns, integrate on a single chip a number of hardware features such as 32K/24K/16K-byte ROM 1024-byte RAM, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO interface, a UART interface (full duplex), an 8-bit 11-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, ROM correction function, and a 23-source 10-vector interrupt feature.

Features

■ROM

- 32768 × 8-bits (LC875832A)
- 24576 × 8-bits (LC875824A)
- 16384 × 8-bits (LC875816A)

■RAM

- 1024 × 9 bits (LC875832A/24A/16A)

■Minimum Bus Cycle

- 100ns (10MHz) $V_{DD}=3.0$ to 3.6V
- 125ns (8MHz) $V_{DD}=2.5$ to 3.6V
- 500ns (2MHz) $V_{DD}=2.2$ to 3.6V

Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time

- 300ns (10MHz) $V_{DD}=3.0$ to 3.6V
- 375ns (8MHz) $V_{DD}=2.5$ to 3.6V
- 1.5 μ s (2MHz) $V_{DD}=2.2$ to 3.6V

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■ Ports

- Normal withstand voltage I/O ports
 - Ports whose I/O direction can be designated in 1-bit units 46 (P1n, P2n, P70 to P73, P80 to P86, PBn, PCn, PWM2, PWM3, XT2)
 - Ports whose I/O direction can be designated in 4-bit units 8 (P0n)
- Normal withstand voltage input ports 1 (XT1)
- Dedicated oscillator ports 2 (CF1, CF2)
- Reset pins 1 (RES)
- Power pins 6 (VSS1 to 3, VDD1 to 3)

■ Timers

- Timer 0 : 16-bit timer/counter with a capture register
 - Mode 0 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
 - Mode 1 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
 - Mode 2 : 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
 - Mode 3 : 16-bit counter (with a 16-bit capture register)
- Timer 1 : 16-bit timer/counter that supports PWM/toggle outputs
 - Mode 0 : 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter (with toggle outputs)
 - Mode 1 : 8-bit PWM with an 8-bit prescaler × 2-channels
 - Mode 2 : 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8-bits)
 - Mode 3 : 16-bit timer with an 8-bit prescaler (with toggle outputs) (the lower-order 8-bits can be used as PWM)
- Timer 4 : 8-bit timer with a 6-bit prescaler
- Timer 5 : 8-bit timer with a 6-bit prescaler
- Timer 6 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
 - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
 - 2) Interrupts programmable in 5 different time schemes

■ High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz)
- 2) Can generate output real-time

■ SIO

- SIO0 : 8-bit synchronous serial interface
 - 1) LSB first/MSB first mode selectable
 - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
 - 3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1 : 8-bit asynchronous/synchronous serial interface
 - Mode 0 : Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
 - Mode 1 : Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
 - Mode 2 : Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
 - Mode 3 : Bus mode 2 (start detect, 8 data bits, stop detect)

■ UART

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

LC875832A/24A/16A

■AD Converter : 8-bits × 11-channels

■PWM : Multifrequency 12-bit PWM × 2-channels

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

■Clock Output Function

- 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

■Interrupts

- 23 sources, 10 vector addresses
 - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer0/base timer1
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels : 512 levels (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions

- 16-bits × 8-bits (5 tCYC execution time)
- 24-bits × 16-bits (12 tCYC execution time)
- 16-bits ÷ 8-bits (8 tCYC execution time)
- 24-bits ÷ 16-bits (12 tCYC execution time)

■Oscillation Circuits

- RC oscillation circuit (internal) : For system clock
- CF oscillation circuit : For system clock, with internal Rf
- Crystal oscillation circuit : For low-speed system clock, with internal Rf

■System Clock Divider Function

- Can run on low current.
The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■ Standby Function

- HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) Canceled by a system reset or occurrence of an interrupt

- HOLD mode : Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC, and crystal oscillators automatically stop operation.
 - 2) There are three ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the lower level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0

- X'tal HOLD mode : Suspends instruction execution and the operation of the peripheral circuits except the base timer.
 - 1) The CF and RC oscillators automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are four ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established in the base timer circuit

■ ROM Correction Function

- Executes the correction program on detection of a match with the program counter value.
- Correction program area size : 128 bytes

■ Package Form

- QIP64E (14 × 14): Lead-free type
- TQFP64 (10 × 10): Lead-free type
- TQFP64J (10 × 10): Lead-free type
- TQFP64J (7 × 7): Lead-free type
- VQFN64 (10 × 10): Lead-free type

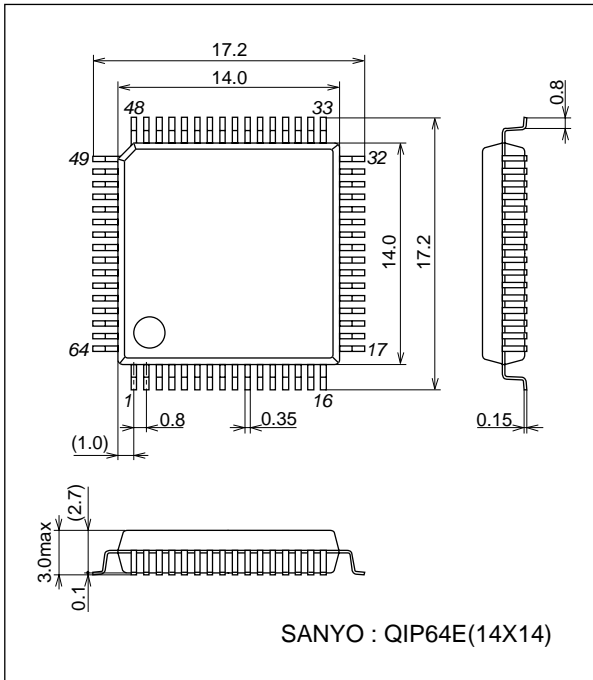
■ Development Tools

- Evaluation chip : LC87EV690
- Emulator : EVA62S + ECB876600D + SUB875800 + POD64QFP or POD64SQFP
(* Tools for VQFN64 (10 × 10), TQFP64J (7 × 7) version of PODs to be determined)

LC875832A/24A/16A

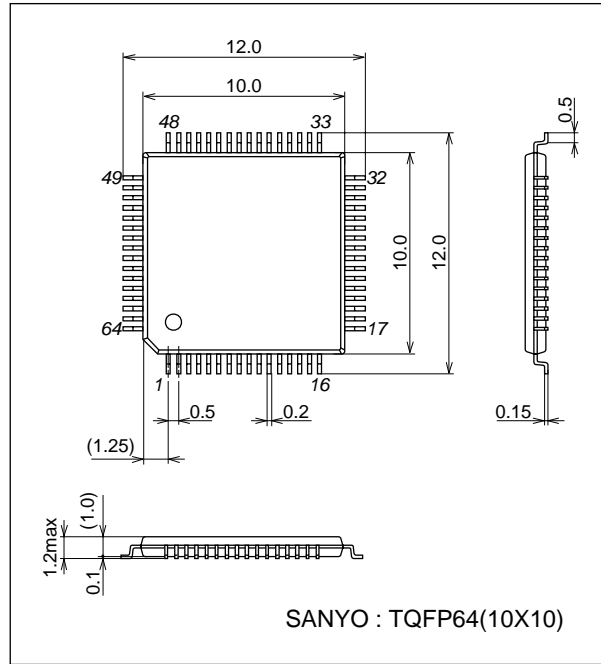
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unit : mm
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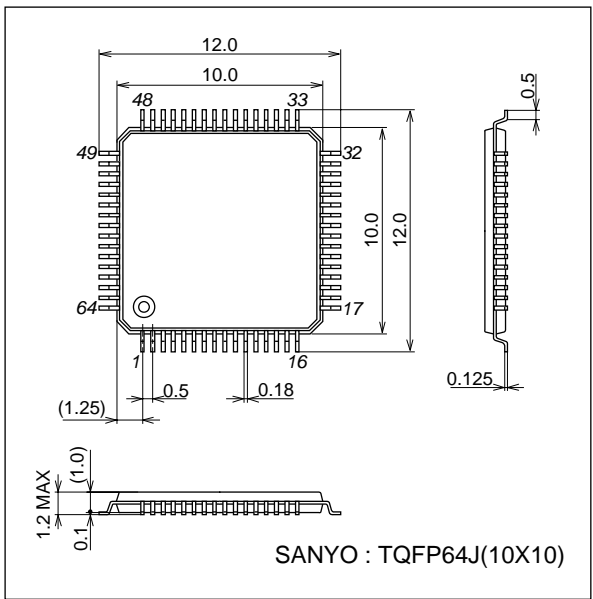
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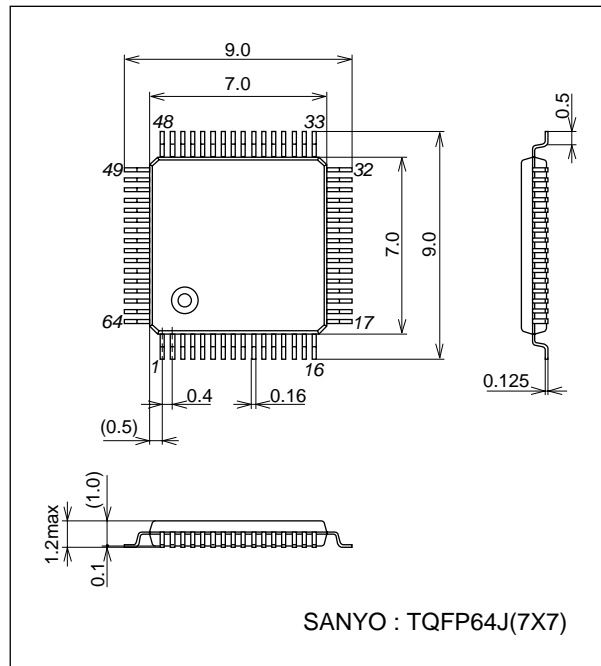
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Package Dimensions

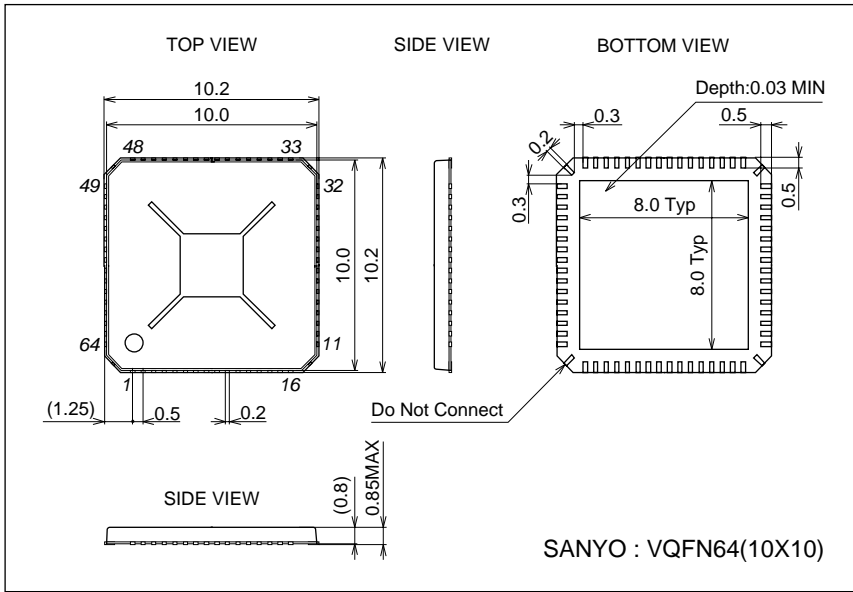
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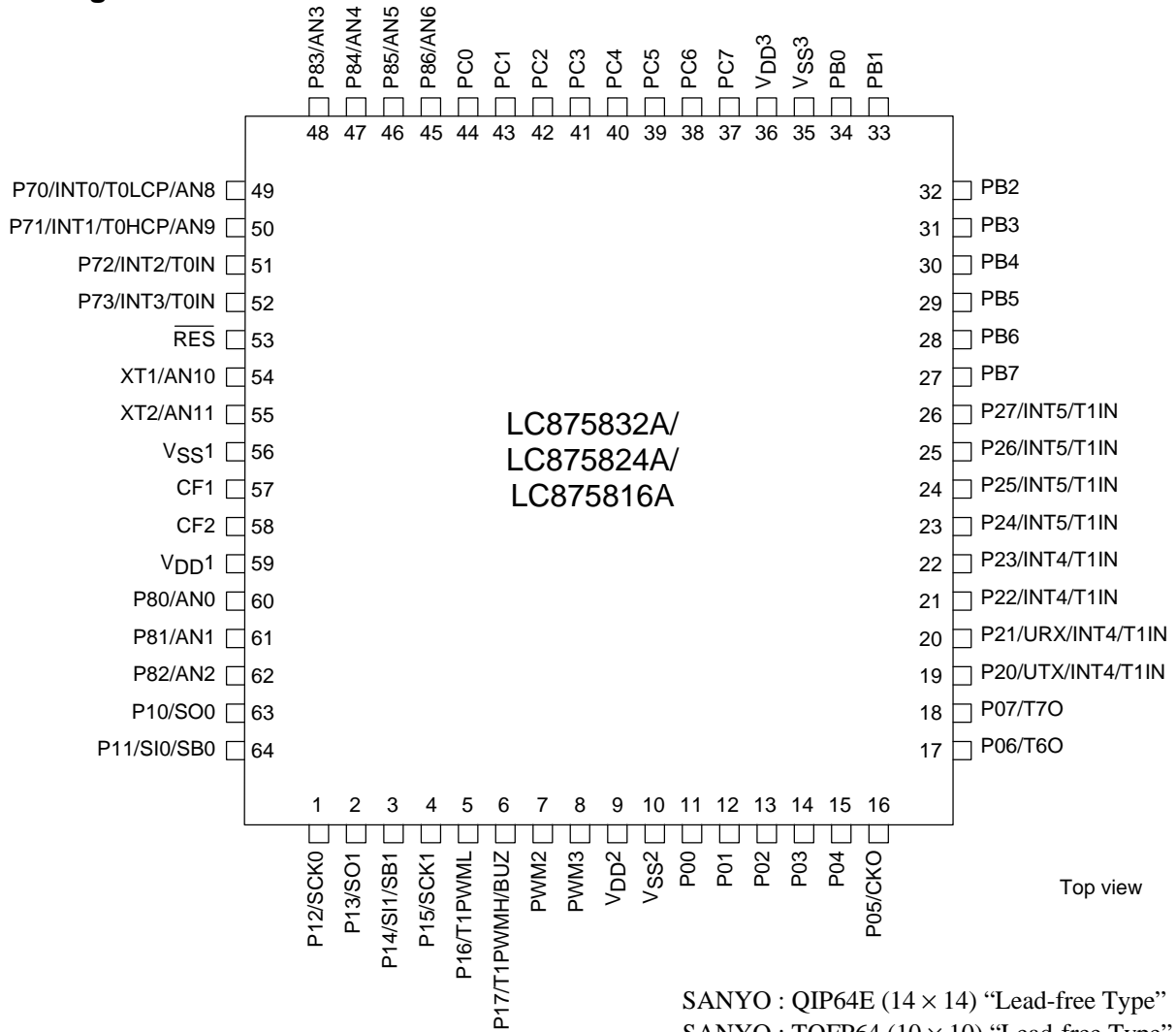
LC875832A/24A/16A

Package Dimensions

unit : mm
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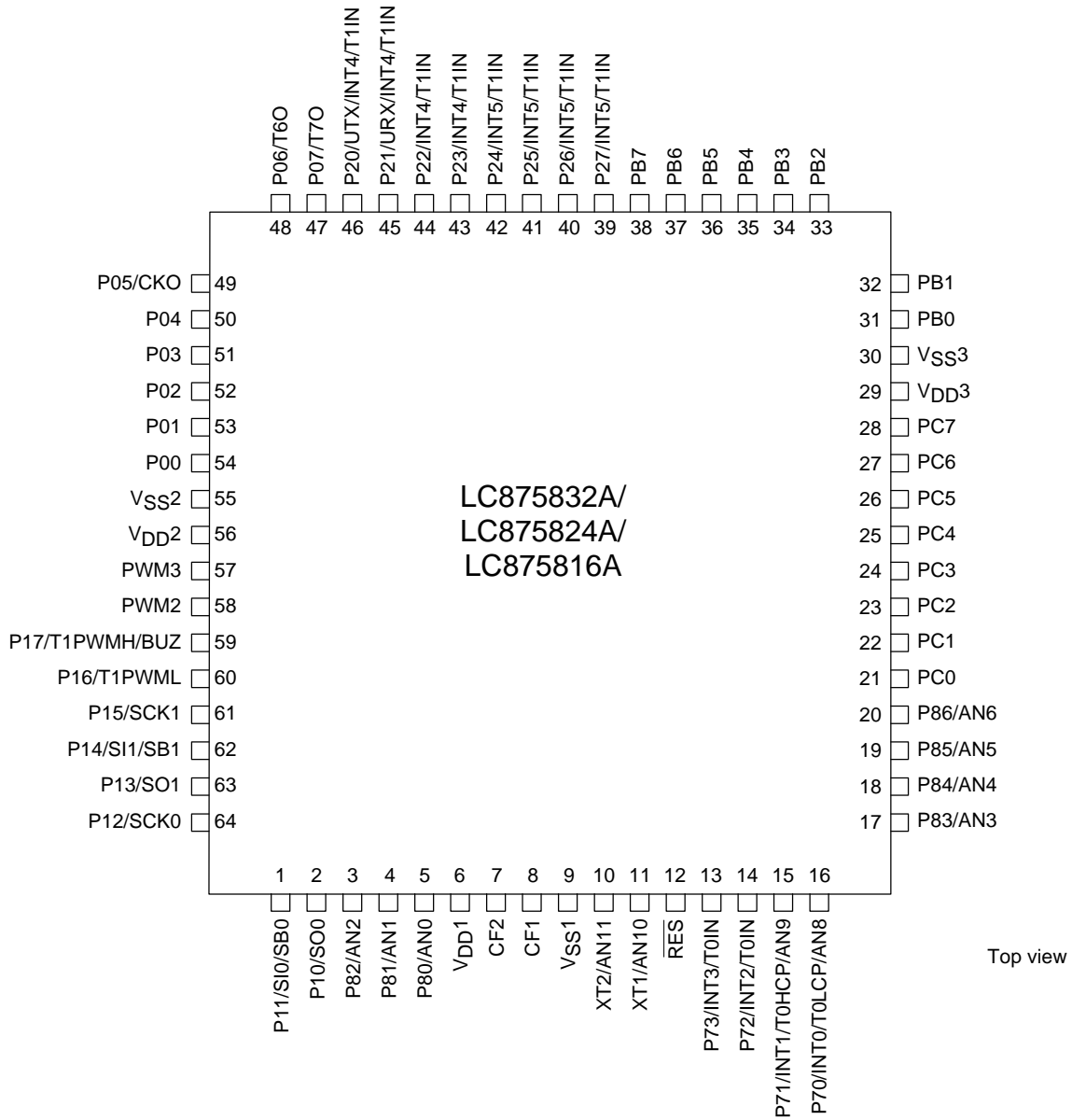


Pin Assignments



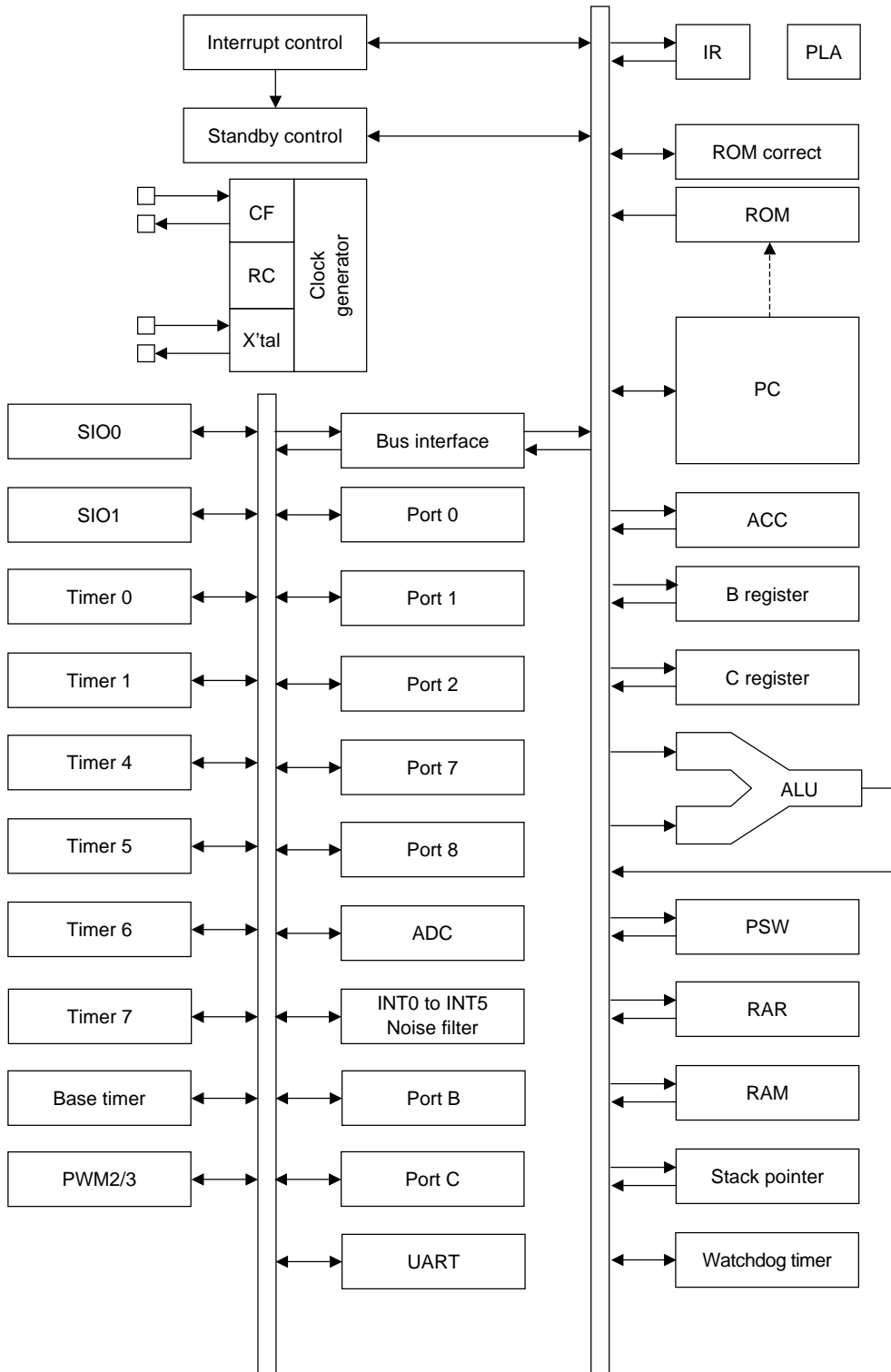
SANYO : QIP64E (14 × 14) “Lead-free Type”
 SANYO : TQFP64 (10 × 10) “Lead-free Type”
 SANYO : TQFP64J (10 × 10) “Lead-free Type”
 SANYO : TQFP64J (7 × 7) “Lead-free Type”

LC875832A/24A/16A



SANYO : VQFN64 (10 × 10) “Lead-free Type”

System Block Diagram



LC875832A/24A/16A

Pin Description

Pin Name	I/O	Description	Option																		
V _{SS} 1 V _{SS} 2 V _{SS} 3	-	-Power supply pin	No																		
V _{DD} 1 V _{DD} 2 V _{DD} 3	-	+Power supply pin	No																		
Port 0 P00 to P07	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 4-bit units • Pull-up resistors can be turned on and off in 4-bit units. • HOLD reset input • Port 0 interrupt input • Shared pins <ul style="list-style-type: none"> P05 : System clock output (system clock / can selected from sub clock) P06 : Timer 6 toggle output P07 : Timer 7 toggle output 	Yes																		
Port 1 P10 to P17	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions <ul style="list-style-type: none"> P10 : SIO0 data output P11 : SIO0 data input/bus I/O P12 : SIO0 clock I/O P13 : SIO1 data output P14 : SIO1 data input/bus I/O P15 : SIO1 clock I/O P16 : Timer 1PWML output P17 : Timer 1PWMH output/beeper output 	Yes																		
Port 2 P20 to P27	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions <ul style="list-style-type: none"> P20 : UART transmit P21 : UART receive P20 to P23 : INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input P24 to P27 : INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input <p>Interrupt acknowledge type</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT4</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT5</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table>		Rising	Falling	Rising & Falling	H level	L level	INT4	enable	enable	enable	disable	disable	INT5	enable	enable	enable	disable	disable	Yes
	Rising	Falling	Rising & Falling	H level	L level																
INT4	enable	enable	enable	disable	disable																
INT5	enable	enable	enable	disable	disable																

Continued on next page.

LC875832A/24A/16A

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Pin Name	I/O	Description	Option																														
Port 7 P70 to P73	I/O	<ul style="list-style-type: none"> • 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Shared pins AD converter input port : AN8 (P70), AN9 (P71) P70 : INTO input/HOLD reset input/timer 0L capture input/watchdog timer output P71 : INT1 input/HOLD reset input/timer 0H capture input P72 : INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/ High speed clock counter input P73 : INT3 input (with noise filter)/timer 0 event input/timer 0H capture input Interrupt acknowledge type <table border="1" style="margin-left: 20px; width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table>		Rising	Falling	Rising & Falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable	No
	Rising	Falling	Rising & Falling	H level	L level																												
INT0	enable	enable	disable	enable	enable																												
INT1	enable	enable	disable	enable	enable																												
INT2	enable	enable	enable	disable	disable																												
INT3	enable	enable	enable	disable	disable																												
Port 8 P80 to P86	I/O	<ul style="list-style-type: none"> • 7-bit I/O port • I/O specifiable in 1-bit units • Shared pins AD converter input : port : AN0 (P80) to AN6 (P86)	No																														
PWM2, PWM3	I/O	<ul style="list-style-type: none"> • PWM2 and PWM3 output ports • General-purpose I/O available 	No																														
Port B PB0 to PB7	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. 	Yes																														
Port C PC0 to PC7	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. 	Yes																														
$\overline{\text{RES}}$	Input	Reset pin	No																														
XT1	Input	<ul style="list-style-type: none"> • 32.768kHz crystal oscillator input pin • Shared pins General-purpose input port AD converter input port : AN10 Must be connected to V_{DD1} if not to be used.	No																														
XT2	I/O	<ul style="list-style-type: none"> • 32.768kHz crystal oscillator output pin • Shared pins General-purpose I/O port AD converter input port : AN11 Must be set for oscillation and kept open if not to be used.	No																														
CF1	Input	Ceramic resonator input pin	No																														
CF2	Output	Ceramic resonator output pin	No																														

LC875832A/24A/16A

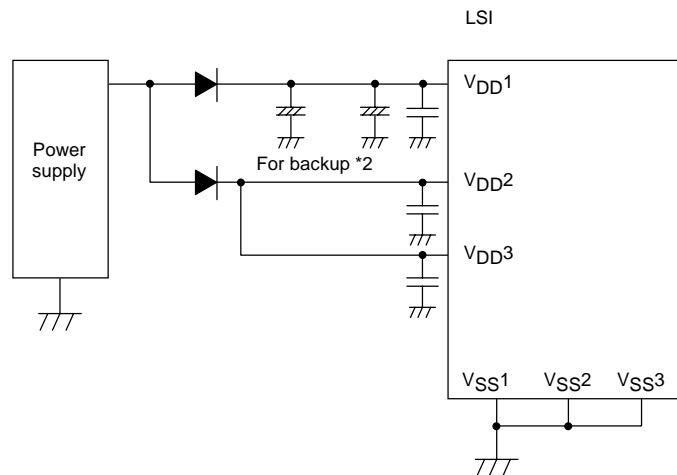
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1-bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P86	-	No	Nch-open drain	No
PWM2, PWM3	-	No	CMOS	No
PB0 to PB7	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PC0 to PC7	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

Note 1 : Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

*1 : Connect the IC as shown below to minimize the noise input to the V_{DD1} pin.
Be sure to electrically short the V_{SS1} , V_{SS2} , and V_{SS3} pins.



*2 : The internal memory is sustained by V_{DD1} . If none of V_{DD2} and V_{DD3} are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time.

Make sure that the port outputs are held at the low level in the HOLD backup mode.

LC875832A/24A/16A

Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				unit
				VDD [V]	min	typ	max	
Maximum supply voltage	VDD max	VDD1, VDD2, VDD3	VDD1=VDD2=VDD3		-0.3		+4.6	V
Input voltage	VI(1)	XT1, CF1			-0.3		VDD+0.3	
Input/output voltage	VIO(1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C PWM2, PWM3, XT2			-0.3		VDD+0.3	
High level output current	Peak output current (Note 1-1)	IOPH(1)	Ports 0, 1, 2, 7 Ports B, C PWM2, PWM3	CMOS output select Per 1 applicable pin		-4		mA
	Total output current	ΣIOAH(1)	Port 7	Total of all applicable pins		-10		
		ΣIOAH(2)	Port 1 PWM2, PWM3	Total of all applicable pins		-25		
		ΣIOAH(3)	Ports 0, 2	Total of all applicable pins		-25		
		ΣIOAH(4)	Port B	Total of all applicable pins		-25		
ΣIOAH(5)		Port C	Total of all applicable pins		-25			
Low level output current	Peak output current (Note 1-1)	IOPL(1)	P02 to P07 Ports 1, 2, 7, 8 Ports B, C PWM2, PWM3, XT2	Per 1 applicable pin			6	
		IOPL(2)	P00, P01	Per 1 applicable pin			15	
	Total output current	ΣIOAL(1)	Port 7 P83 to P86, XT2	Total of all applicable pins				10
		ΣIOAL(2)	P80 to P82	Total of all applicable pins				10
		ΣIOAL(3)	Port 1 PWM2, PWM3	Total of all applicable pins				25
		ΣIOAL(4)	Ports 0, 2	Total of all applicable pins				25
		ΣIOAL(5)	Port B	Total of all applicable pins				25
ΣIOAL(6)	Port C	Total of all applicable pins				25		
Power dissipation	Pd max	QIP64E (14×14)	Ta= -30 to +70°C				414	mW
		TQFP64 (10×10)				236		
		TQFP64J (10×10)				270		
		TQFP64J (7×7)				188		
		VQFN64 (10×10)				209		
Operating ambient temperature	Topr				-30		+70	°C
Storage ambient temperature	Tstg				-55		+125	

Note 1-1 : The average current per applicable pin must not exceed 1mA.

LC875832A/24A/16A

Allowable Operating Range at $T_a = -30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Operating supply voltage	$V_{DD}(1)$	$V_{DD1}=V_{DD2}=V_{DD3}$	$0.294\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		3.0		3.6	V
			$0.367\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		2.5		3.6	
			$1.47\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		2.2		3.6	
Memory sustaining supply voltage	VHD	$V_{DD1}=V_{DD2}=V_{DD3}$	RAM and register contents sustained in HOLD mode.		2.0		3.6	
High level input voltage	$V_{IH}(1)$	Ports 1, 2 P71 to P73 P70 port input /interrupt side		2.2 to 3.6	$0.3V_{DD} + 0.7$		V_{DD}	V
	$V_{IH}(2)$	Ports 0, 8, B, C PWM2, PWM3		2.2 to 3.6	$0.3V_{DD} + 0.7$		V_{DD}	
	$V_{IH}(3)$	Port 70 watchdog timer side		2.2 to 3.6	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	XT1, XT2, CF1, RES		2.2 to 3.6	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2 P71 to P73 P70 port input /interrupt side		2.2 to 3.6	V_{SS}		$0.2V_{DD}$	V
	$V_{IL}(2)$	Ports 0, 8, B, C PWM2, PWM3		2.2 to 3.6	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Port 70 watchdog timer side		2.2 to 3.6	V_{SS}		$0.8V_{DD} - 1.0$	
	$V_{IL}(4)$	XT1, XT2, CF1, RES		2.2 to 3.6	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-1)	tCYC			3.0 to 3.6	0.294		200	μs
				2.5 to 3.6	0.367		200	
				2.2 to 3.6	1.47		200	
External system clock frequency	FEXCF(1)	CF1	<ul style="list-style-type: none"> • CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty =$50 \pm 5\%$ 	3.0 to 3.6	0.1		10	MHz
				2.5 to 3.6	0.1		8	
				2.2 to 3.6	0.1		2	
				3.0 to 3.6	0.2		20	
				2.5 to 3.6	0.2		16	
				2.2 to 3.6	0.2		4	
Oscillation frequency range (Note 2-2)	FmCF(1)	CF1, CF2	10MHz ceramic oscillation mode See Fig. 1.	3.0 to 3.6		10		kHz
	FmCF(2)	CF1, CF2	8MHz ceramic oscillation mode See Fig. 1.	2.5 to 3.6		8		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation mode See Fig. 1.	2.2 to 3.6		4		
	FmRC		Internal RC oscillation	2.2 to 3.6	0.3	1.0	2.0	
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation mode See Fig. 2.	2.2 to 3.6		32.768		

Note 2-1 : Relationship between tCYC and oscillation frequency is $3/F_mCF$ at a division ratio of 1/1 and $6/F_mCF$ at a division ratio of 1/2.

Note 2-2 : See Tables 1 and 2 for the oscillation constants.

LC875832A/24A/16A

Electrical Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				VDD [V]	min	typ	max	unit
High level input current	I _{IH} (1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C RES PWM2, PWM3	Output disabled Pull-up resistor off V _{IN} =V _{DD} (Including output Tr's off leakage current)	2.2 to 3.6			1	μA
	I _{IH} (2)	XT1, XT2	For input port specification V _{IN} =V _{DD}	2.2 to 3.6			1	
	I _{IH} (3)	CF1	V _{IN} =V _{DD}	2.2 to 3.6			8	
Low level input current	I _{IL} (1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C RES PWM2, PWM3	Output disabled Pull-up resistor off V _{IN} =V _{SS} (Including output Tr's off leakage current)	2.2 to 3.6	-1			μA
	I _{IL} (2)	XT1, XT2	For input port specification V _{IN} =V _{SS}	2.2 to 3.6	-1			
	I _{IL} (3)	CF1	V _{IN} =V _{SS}	2.2 to 3.6	-8			
High level output voltage	V _{OH} (1)	Ports 0, 1, 2, 7 Ports B, C	I _{OH} = -0.4mA	3.0 to 3.6	V _{DD} -0.4			V
	V _{OH} (2)	PWM2, PWM3	I _{OH} = -0.2mA	2.2 to 3.6	V _{DD} -0.4			
	V _{OH} (3)	PWM2, PWM3	I _{OH} = -1.6mA	3.0 to 3.6	V _{DD} -0.4			
	V _{OH} (4)		I _{OH} = -0.8mA	2.2 to 3.6	V _{DD} -0.4			
Low level output voltage	V _{OL} (1)	Ports 0, 1, 2, 7, 8 Ports B, C	I _{OL} =1.6mA	3.0 to 3.6			0.4	V
	V _{OL} (2)	PWM2, PWM3 XT2	I _{OL} =0.8mA	2.2 to 3.6			0.4	
	V _{OL} (3)	P00, P01	I _{OL} =5mA	3.0 to 3.6			0.4	
	V _{OL} (4)		I _{OL} =2.5mA	2.2 to 3.6			0.4	
Pull-up resistance	R _{pu}	Ports 0, 1, 2, 7 Ports B, C	V _{OH} =0.9V _{DD}	2.2 to 3.6	25	50	200	kΩ
Hysteresis voltage	V _{HYS}	RES Ports 1, 2, 7		2.2 to 3.6		0.1		V
Pin capacitance	CP	All pins	For pins other than that under test : V _{IN} =V _{SS} f=1MHz Ta=25°C	2.2 to 3.6			10	pF

LC875832A/24A/16A

Serial Input/Output Characteristics at $T_a = -30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification				
						min	typ	max	unit	
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.2 to 3.6	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)							
	Output clock	Frequency	tSCK(2)	SCK0(P12)	<ul style="list-style-type: none"> • CMOS output selected • See Fig. 6. 	2.2 to 3.6	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
High level pulse width		tSCKH(2)	1/2				tCYC			
		tSCKHA(2)	<ul style="list-style-type: none"> • Continuous data transmission/reception mode • CMOS output selected • See Fig. 6. 					tSCKH(2) +2tCYC	tSCKH(2) +(10/3) tCYC	
Serial input	Data setup time	tsDI(1)	SB0(P11), SI0(P11)	<ul style="list-style-type: none"> • Must be specified with respect to rising edge of SIOCLK. • See Fig. 6. 	2.2 to 3.6	0.03				
	Data hold time	thDI(1)				2.2 to 3.6	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	<ul style="list-style-type: none"> • Continuous data transmission/reception mode • (Note 4-1-3) 	2.2 to 3.6			(1/3)tCYC +0.05	μs
			tdD0(2)				<ul style="list-style-type: none"> • Synchronous 8-bit mode • (Note 4-1-3) 	2.2 to 3.6		
	Output clock		tdD0(3)		(Note 4-1-3)	2.2 to 3.6			(1/3)tCYC +0.15	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans / rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

LC875832A/24A/16A

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification				
						min	typ	max	unit	
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.2 to 3.6	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	<ul style="list-style-type: none"> • CMOS output selected • See Fig. 6. 	2.2 to 3.6	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time	tsDI(2)	SB1(P14), SI1(P14)	<ul style="list-style-type: none"> • Must be specified with respect to rising edge of SIOCLK. • See Fig. 6. 	2.2 to 3.6	0.03				
	Data hold time	thDI(2)				2.2 to 3.6	0.03			
Serial output	Output delay time	tdD0(4)	SO1(P13), SB1(P14)	<ul style="list-style-type: none"> • Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6. 	2.2 to 3.6			(1/3)tCYC +0.05	μs	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

LC875832A/24A/16A

Pulse Input Conditions at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27)	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 or 1 are enabled. 	2.2 to 3.6	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. 	2.2 to 3.6	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. 	2.2 to 3.6	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. 	2.2 to 3.6	256			
	tPIL(5)	RES	Resetting is enabled.	2.2 to 3.6	200			

AD Converter Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to		3.0 to 3.6		8		bit
Absolute accuracy	ET	AN6(P86) AN8(P70)	(Note 6-1)	3.0 to 3.6			±1.5	LSB
Conversion time	TCAD	AN9(P71) AN10(XT1) AN11(XT2)	AD conversion time=32 × tCYC (when ADCR2=0) (Note 6-2)	3.0 to 3.6	31.36 (tCYC=0.980μs)		97.92 (tCYC=3.06μs)	μs
			AD conversion time=64 × tCYC (when ADCR2=1) (Note 6-2)	3.0 to 3.6	31.36 (tCYC=0.490μs)		97.92 (tCYC=1.53μs)	
Analog input voltage range	VAIN			3.0 to 3.6	V _{SS}		V _{DD}	V
Analog port input current	IAINH		VAIN=V _{DD}	3.0 to 3.6			1	μA
	IAINL		VAIN=V _{SS}	3.0 to 3.6	-1			

Note 6-1 : The quantization error (±1/2LSB) is excluded from the absolute accuracy value.

Note 6-2 : The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

LC875832A/24A/16A

Consumption Current Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				VDD [V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	VDD1 =VDD2 =VDD3	<ul style="list-style-type: none"> • FmCF=10MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 10MHz side • Internal RC oscillation stopped • 1/1 frequency division ratio 	3.0 to 3.6		3.7	8.3	mA
	IDDOP(2)		<ul style="list-style-type: none"> • CF1=20MHz external clock • FmX'tal=32.768kHz crystal oscillation mode • System clock set to CF1 side • Internal RC oscillation stopped • 1/2 frequency division ratio 	3.0 to 3.6		4.0	9.2	
	IDDOP(3)		<ul style="list-style-type: none"> • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped • 1/1 frequency division ratio 	3.0 to 3.6		2.9	6.8	
	IDDOP(4)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/1 frequency division ratio 	2.5 to 3.0		2.3	5.3	
	IDDOP(5)		<ul style="list-style-type: none"> • FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped • 1/2 frequency division ratio 	3.0 to 3.6		0.95	2.3	
	IDDOP(6)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/2 frequency division ratio 	2.2 to 3.0		0.66	1.8	
	IDDOP(7)		<ul style="list-style-type: none"> • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • 1/2 frequency division ratio 	3.0 to 3.6		0.29	1.3	
	IDDOP(8)		<ul style="list-style-type: none"> • 1/2 frequency division ratio 	2.2 to 3.0		0.2	0.96	
	IDDOP(9)		<ul style="list-style-type: none"> • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • 1/2 frequency division ratio 	3.0 to 3.6		11	38	
	IDDOP(10)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/2 frequency division ratio 	2.2 to 3.0		7.7	28	
HALT mode consumption current (Note 7-1)	IDDHALT(1)		HALT mode <ul style="list-style-type: none"> • FmCF=10MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 10MHz side • Internal RC oscillation stopped • 1/1 frequency division ratio 	3.0 to 3.6		1.2	2.9	mA
	IDDHALT(2)		<ul style="list-style-type: none"> • CF1=20MHz external clock • FmX'tal=32.768kHz crystal oscillation mode • System clock set to CF1 side • Internal RC oscillation stopped • 1/2 frequency division ratio 	3.0 to 3.6		1.7	3.9	
	IDDHALT(3)		HALT mode <ul style="list-style-type: none"> • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped • 1/1 frequency division ratio 	3.0 to 3.6		1.0	2.5	
	IDDHALT(4)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/1 frequency division ratio 	2.5 to 3.0		0.77	1.9	
	IDDHALT(5)		HALT mode <ul style="list-style-type: none"> • FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped • 1/2 frequency division ratio 	3.0 to 3.6		0.48	1.2	
	IDDHALT(6)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/2 frequency division ratio 	2.2 to 3.0		0.3	0.88	
	IDDHALT(7)		HALT mode <ul style="list-style-type: none"> • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • 1/2 frequency division ratio 	3.0 to 3.6		0.17	0.73	
	IDDHALT(8)		<ul style="list-style-type: none"> • 1/2 frequency division ratio 	2.2 to 3.0		0.12	0.56	

Note 7-1 : The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

LC875832A/24A/16A

Continued from preceding page.

Parameter	Symbol	Pin/remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(9)	V _{DD1} =V _{DD2} =V _{DD3}	<ul style="list-style-type: none"> • HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • 1/2 frequency division ratio 	3.0 to 3.6		7.6	26	μA
	IDDHALT(10)			2.2 to 3.0		4.7	18	
HOLD mode consumption current	IDDHOLD(1)	V _{DD1}	HOLD mode	3.0 to 3.6		0.04	8	
	IDDHOLD(2)			2.2 to 3.0		0.03	6	
Timer HOLD mode consumption current	IDDHOLD(3)		Timer HOLD mode	3.0 to 3.6		6.3	22	
	IDDHOLD(4)			2.2 to 3.0		3.8	15	

Note 7-1 : The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

UART (Full Duplex) Operating Conditions at Ta = -30°C to +70°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

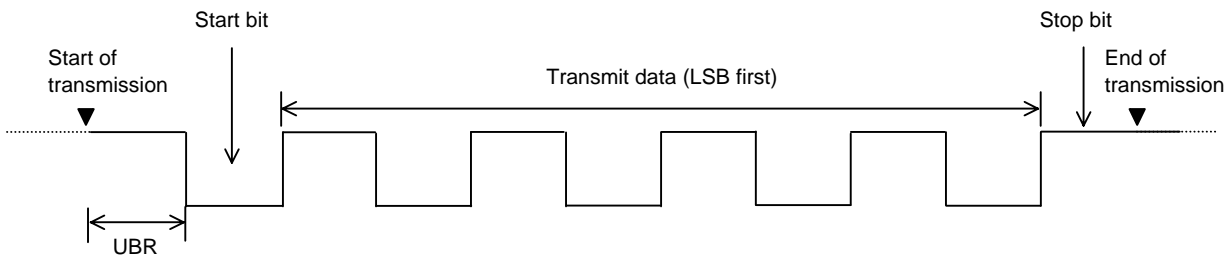
Parameter	Symbol	Pin/remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Transfer rate	UBR	UTX (P20), URX (P21)		2.2 to 3.6	16/3		8192/3	tCYC

Data length : 7, 8, and 9 bits (LSB first)

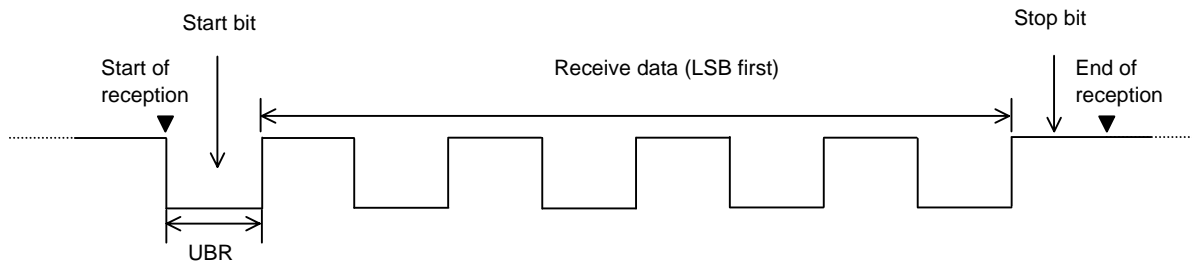
Stop bits : 1-bit (2-bit in continuous data transmission)

Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (first transmit data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (first receive data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant			Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rd1 [Ω]		typ [ms]	max [ms]	
10MHz	MURATA	CSTCE10M0G52-R0	(10)	(10)	470	3.0 to 3.6	0.05	0.25	Internal C1, C2
	KYOCERA	PBRC10.00HR	(10)	(10)	0	3.0 to 3.6	0.06	0.3	Internal C1, C2
8MHz	MURATA	CSTCE8M00G52-R0	(10)	(10)	1k	2.5 to 3.6	0.05	0.25	Internal C1, C2
	KYOCERA	PBRC8.00HR	(30)	(30)	0	2.5 to 3.6	0.07	0.35	Internal C1, C2
4MHz	MURATA	CSTCR4M00G53-R0	(15)	(15)	2.2k	2.2 to 3.6	0.05	0.25	Internal C1, C2
	KYOCERA	PBRC4.00HR	(30)	(30)	0	2.2 to 3.6	0.08	0.4	Internal C1, C2

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	SEIKO EPSON	MC-306	15	15	10M	510k	2.2 to 3.6	1.0	3.0	Applicable CL value =12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note : The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

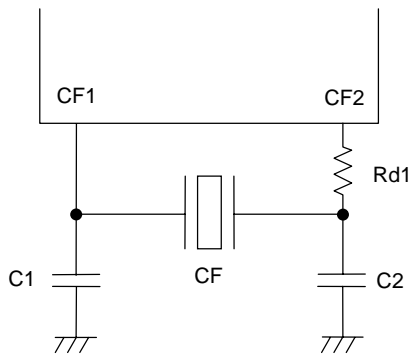


Figure 1 CF Oscillator Circuit

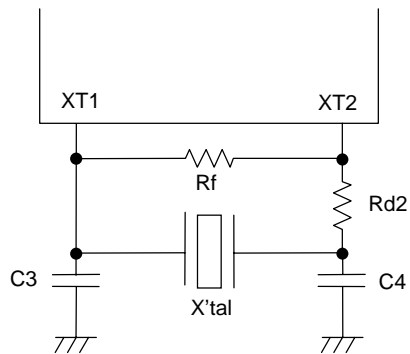


Figure 2 XT Oscillator Circuit

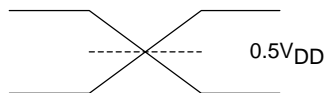
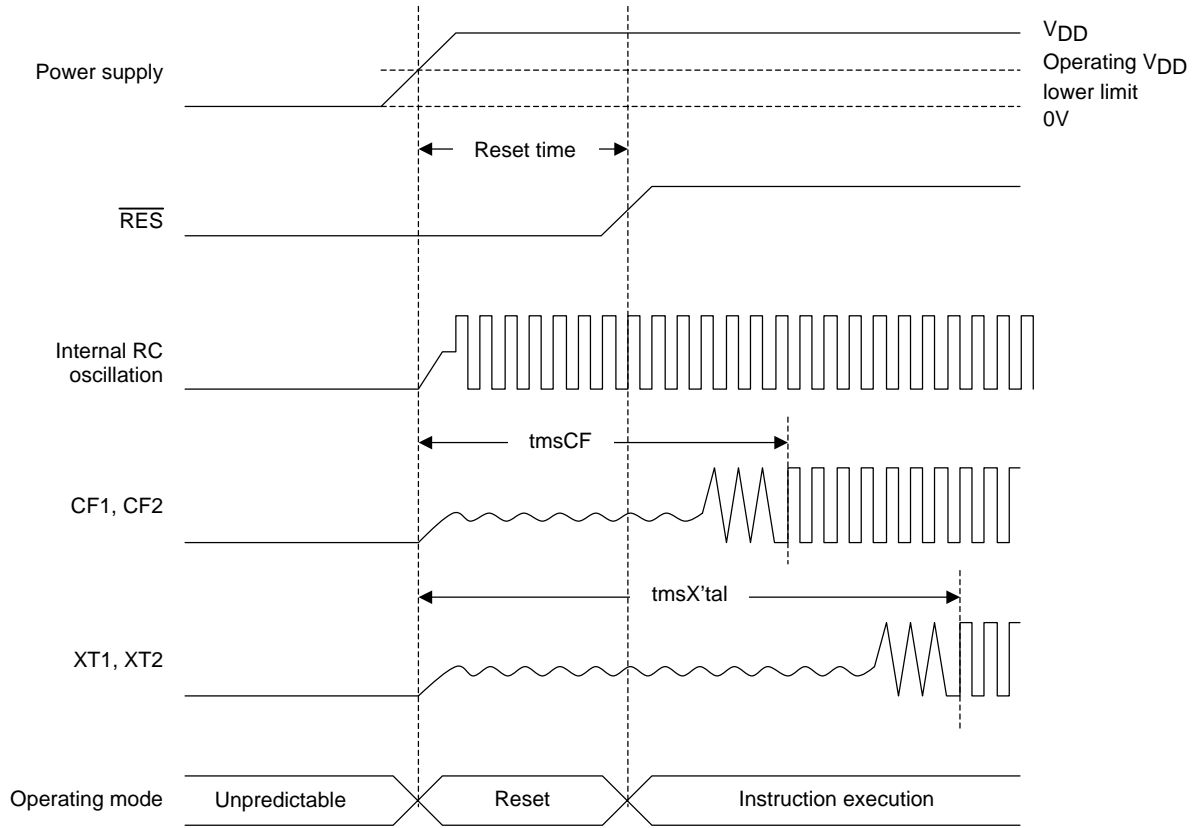
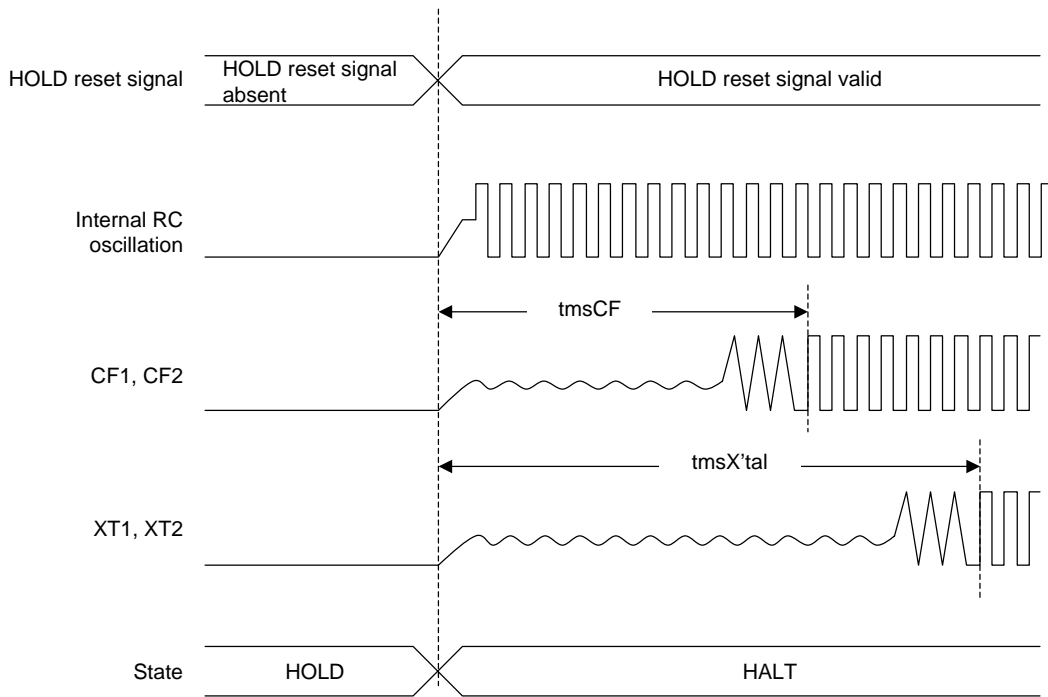


Figure 3 AC Timing Measurement Point

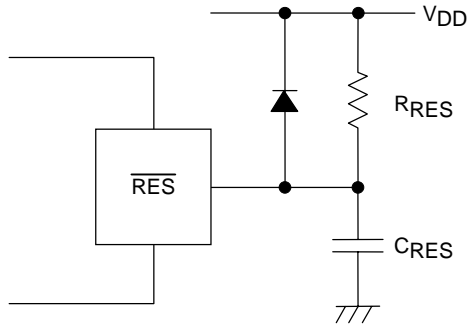


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note :
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of $200\mu s$ after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

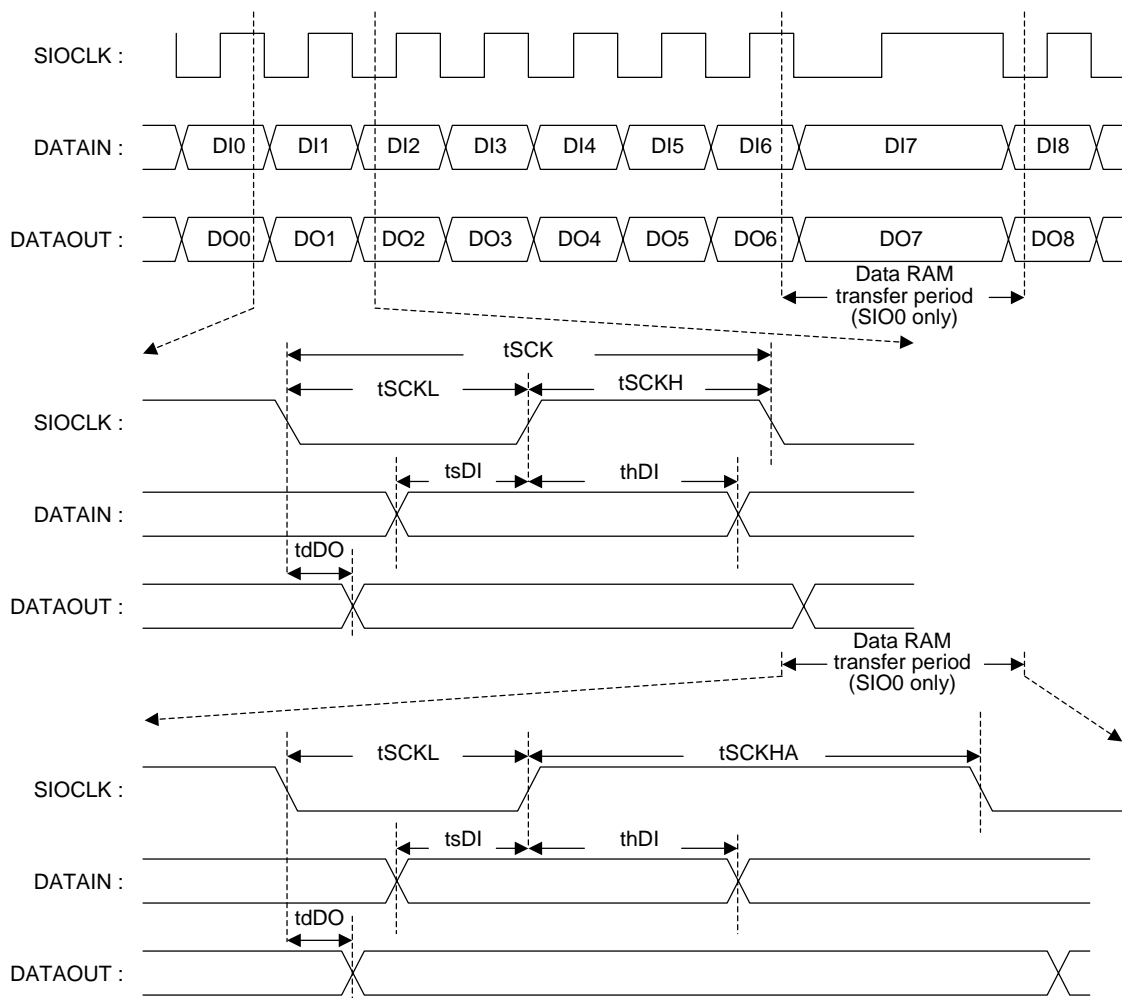


Figure 6 Serial I/O Output Waveforms

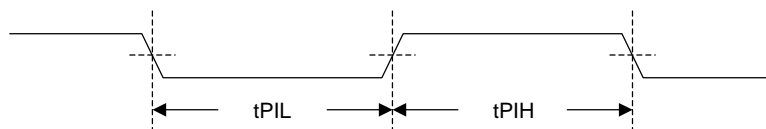


Figure 7 Pulse Input Timing Signal Waveform

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