



**SANYO Semiconductors**

# DATA SHEET

## LC875CC8A — CMOS IC LC875CB2A — ROM 128K/112K byte, RAM 4096 byte on-chip 8-bit 1-chip Microcontroller

### Overview

The SANYO LC875CC8A/B2A are 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrate on a single chip a number of hardware features such as 128K/112K-byte ROM, 4K-byte RAM, two sophisticated 16-bit timers/counters (may be divided into 8-bit timers), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, two synchronous SIO ports (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO port, two UART ports (full duplex), four 12-bit PWM channels, an 8-bit 15-channel AD converter, a high-speed clock counter, a system clock frequency divider, and a 29-source 10-vector interrupt feature.

### Features

#### ■ROM

- 131072 × 8 bits (LC875CC8A)
- 114688 × 8 bits (LC875CB2A)

#### ■RAM

- 4096 × 9 bits

#### ■Minimum Bus Cycle Time

- 83.3ns (12MHz)

Note: Bus cycle time indicates the speed to read ROM.

#### ■Minimum Instruction Cycle Time (tCYC)

- 250ns (12MHz)

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# LC875CC8A/B2A

## ■ Ports

- Normal withstand voltage I/O ports
  - Ports whose I/O direction can be designated in 1 bit units: 64 (P1n, P2n, P3n, P70 to P73, P8n, PAn, PBn, PCn, S2Pn, PWM0, PWM1, XT2)
  - Ports whose I/O direction can be designated in 2 bit units: 16 (PEn, PFn)
  - Ports whose I/O direction can be designated in 4 bit units: 8 (P0n)
- Normal withstand voltage input ports: 1 (XT1)
- Dedicated oscillator ports: 2 (CF1, CF2)
- Reset pin: 1 (RES)
- Power pins: 8 (VSS1 to VSS4, VDD1 to VDD4)

## ■ Timers

- Timer 0: 16-bit timer/counter with capture registers
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  - Mode 3: 16-bit counter (with 2 16-bit capture registers)
- Timer 1: 16-bit timer/counter that support PWM/ toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter (with toggle outputs)
  - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also from the lower-order 8 bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  - 1) The clock is selectable from the subclock (32.768 kHz crystal oscillator), system clock, and timer 0 prescaler output.
  - 2) Interrupts programmable in 5 different time schemes.

## ■ High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
- 2) Can generate output real time.

## ■ SIO

- SIO 0: 8 bit synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  - 3) Automatic continuous data transmission (1 to 256 bits)
- SIO 1: 8 bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (Half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- SIO2: 8 bit synchronous serial interface
  - 1) LSB first mode
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 Tcyc)
  - 3) Automatic continuous data transmission (1 to 32 bytes)

## ■ UART: 2 channels

- 1) Full duplex
- 2) 7/8/9 bit data bits selectable
- 3) 1 stop bit (2 bits in continuous transmission mode)
- 4) Built-in baudrate generator (with baudrates of 16/3 to 8192/3 tCYC)

## LC875CC8A/B2A

### ■AD Converter: 8 bits × 15 channels

- Analog reference voltage can selected from V<sub>DD1</sub> or V<sub>DD3</sub>.

### ■PWM: Multifrequency 12-bit PWM × 4 channels

### ■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- 1) Noise filtering function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
- 2) The noise filtering function is available for the INT3, T0IN, or T0HCP signal at P73. When P73 is read with an instruction, the signal level at that pin is read regardless of the availability of the noise filtering function.

### ■Watchdog Timer

- 1) External RC watchdog timer
- 2) Interrupt and reset signals selectable

### ■Interrupts

- 29 sources, 10 vector addresses
  - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector	Selectable Level	Interrupt Signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/Base timer
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/UART2 receive
8	0003BH	H or L	SIO1/SIO2/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

- Priority Level: X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

### ■Subroutine Stack Levels: 2048 levels maximum (the stack is allocated in RAM.)

### ■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

### ■Oscillation Circuits

- RC oscillator circuit (internal): For system clock
- CF oscillator circuit: For system clock with internal R<sub>f</sub>
- Crystal oscillator circuit: For low-speed system clock
- Multifrequency RC oscillator circuit (internal): For system clock

### ■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

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### ■ Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) Canceled by system reset or occurrence of interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The CF, RC, and crystal oscillators automatically stop operation.
  - 2) There are three ways of resetting the HOLD mode.
    - (1) Setting the Reset pin to the lower level
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    - (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  - 1) The CF and RC oscillators automatically stop operation.
  - 2) The state of crystal oscillation established when the HOLD mode is entered is retained.
  - 3) There are four ways of resetting the X'tal HOLD mode.
    - (1) Setting the Reset pin to the low level.
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level.
    - (3) Having an interrupt source established at port 0.
    - (4) Having an interrupt source established in the base timer circuit.

### ■ Package Form

- QIP100E(14×20): “Lead-free type”
- TQFP100(14×14): “Lead-free type”

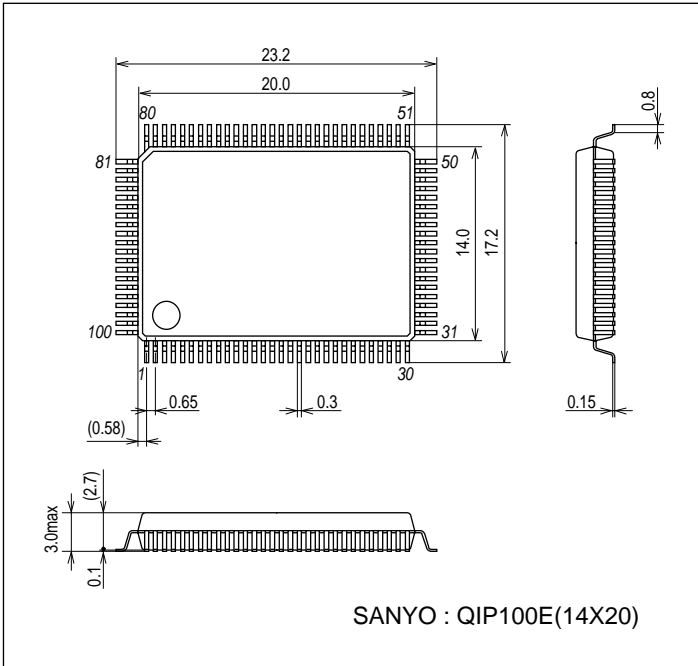
### ■ Development Tools

- Evaluation (EVA) chip : LC87EV690
- Emulator : EVA62S + ECB876600D + SUB875C00  
+ POD100QFP or POD100SQFP Type B  
: ICE-B877300 + SUB875C00 + POD100QFP or POD100SQFP Type B
- Flash version : LC87F5CC8A

**Package Dimensions**

unit : mm (typ)

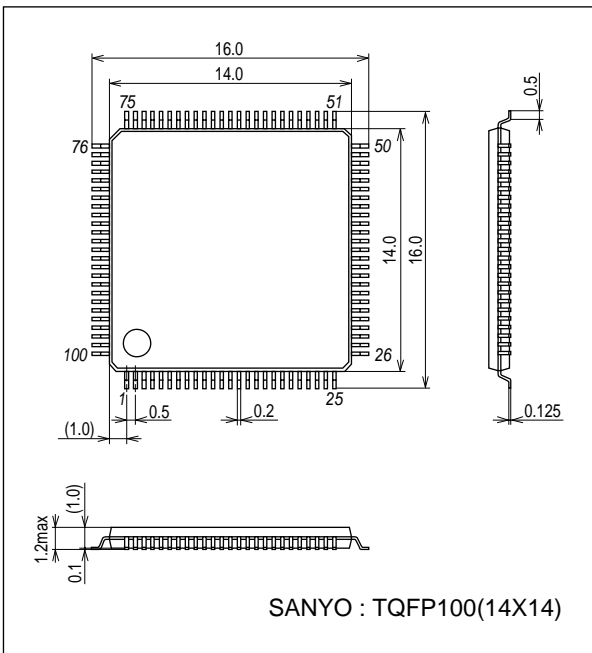
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**Package Dimensions**

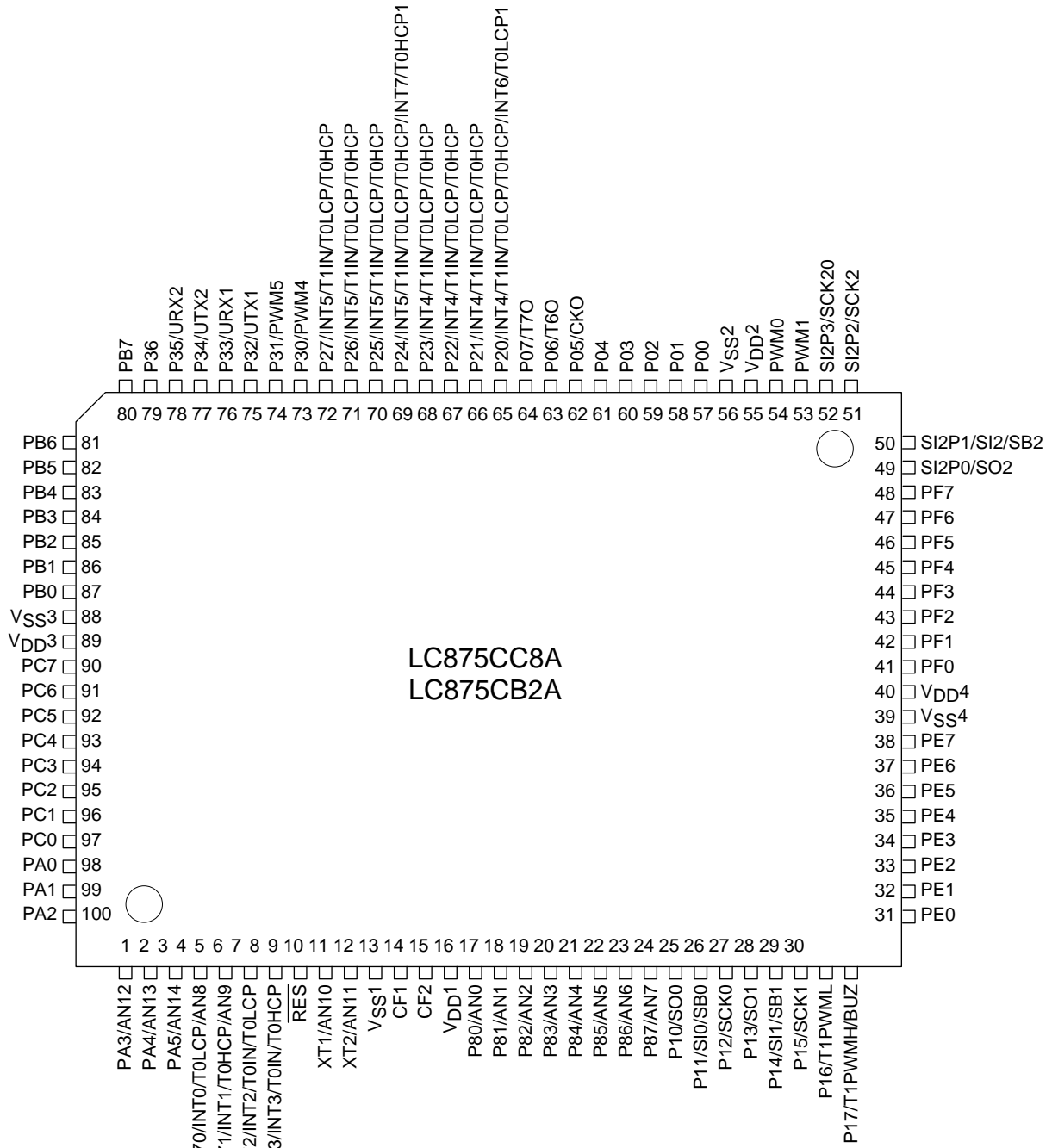
unit : mm (typ)

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## Pin Assignments



Top view

SANYO: QIP100E(14×20) “Lead-free Type”



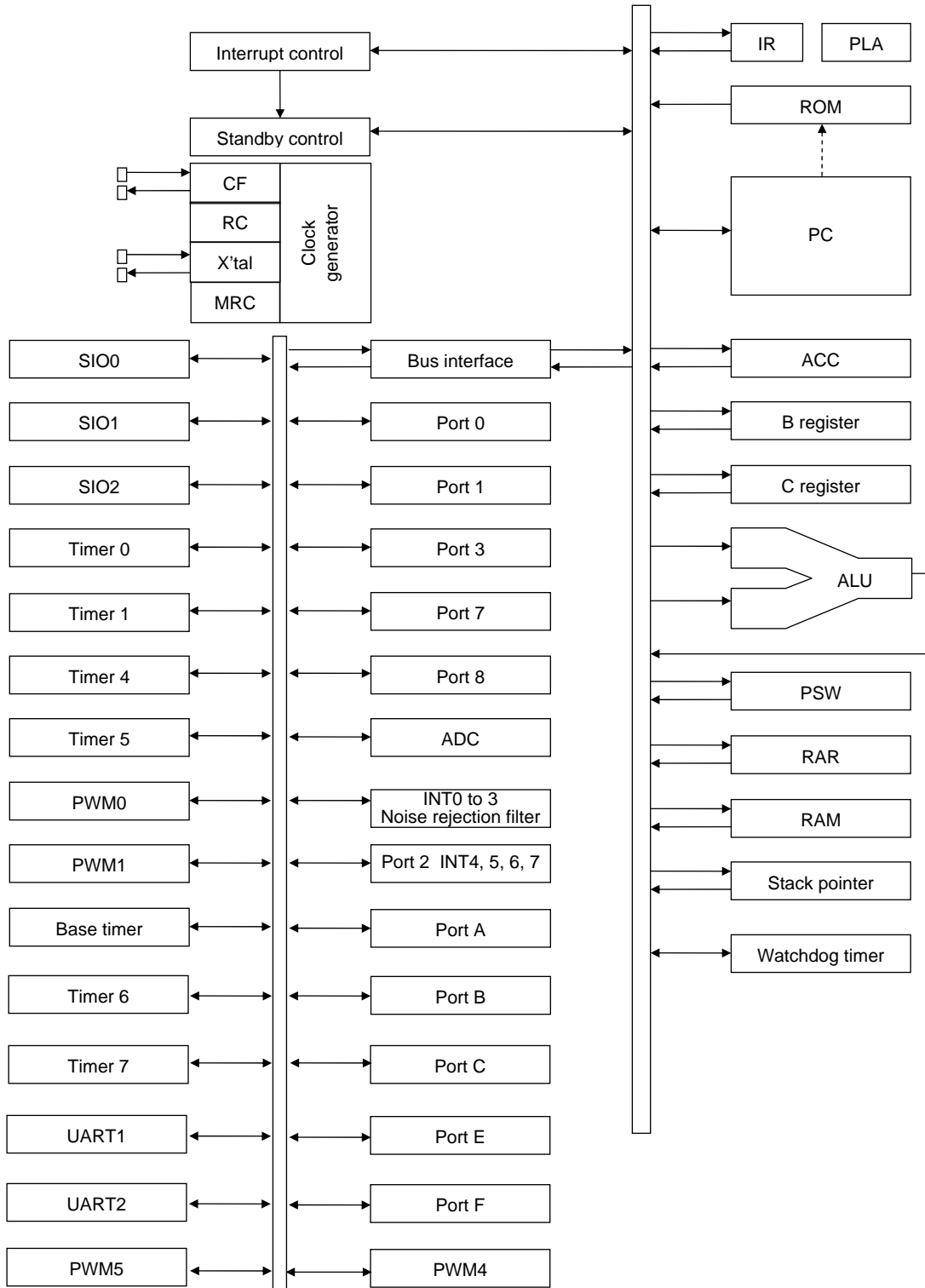
## LC875CC8A/B2A

QIP	NAME	TQFP
1	PA3/AN12	98
2	PA4/AN13	99
3	PA5/AN14	100
4	P70/INT0/T0LCP/AN8	1
5	P71/INT1/T0HCP/AN9	2
6	P72/INT2/T0IN/T0LCP	3
7	P73/INT3/T0IN/T0HCP	4
8	$\overline{\text{RES}}$	5
9	XT1/AN10	6
10	XT2/AN11	7
11	V <sub>SS</sub> 1	8
12	CF1	9
13	CF2	10
14	V <sub>DD</sub> 1	11
15	P80/AN0	12
16	P81/AN1	13
17	P82/AN2	14
18	P83/AN3	15
19	P84/AN4	16
20	P85/AN5	17
21	P86/AN6	18
22	P87/AN7	19
23	P10/SO0	20
24	P11/SI0/SB0	21
25	P12/SCK0	22
26	P13/SO1	23
27	P14/SI1/SB1	24
28	P15/SCK1	25
29	P16/T1PWML	26
30	P17/T1PWHM/BUZ	27
31	PE0	28
32	PE1	29
33	PE2	30
34	PE3	31
35	PE4	32
36	PE5	33
37	PE6	34
38	PE7	35
39	V <sub>SS</sub> 4	36
40	V <sub>DD</sub> 4	37
41	PF0	38
42	PF1	39
43	PF2	40
44	PF3	41
45	PF4	42
46	PF5	43
47	PF6	44
48	PF7	45
49	SI2P0/SO2	46
50	SI2P1/SI2/SB2	47

QIP	NAME	TQFP
51	SI2P2/SCK2	48
52	SI2P3/SCK20	49
53	PWM1	50
54	PWM0	51
55	V <sub>DD</sub> 2	52
56	V <sub>SS</sub> 2	53
57	P00	54
58	P01	55
59	P02	56
60	P03	57
61	P04	58
62	P05/CKO	59
63	P06/T6O	60
64	P07/T7O	61
65	P20/INT4/T1IN/T0LCP/T0HCP/ INT6/T0LCP1	62
66	P21/INT4/T1IN/T0LCP/T0HCP	63
67	P22/INT4/T1IN/T0LCP/T0HCP	64
68	P23/INT4/T1IN/T0LCP/T0HCP	65
69	P24/INT5/T1IN/T0LCP/T0HCP/ INT7/T0HCP1	66
70	P25/INT5/T1IN/T0LCP/T0HCP	67
71	P26/INT5/T1IN/T0LCP/T0HCP	68
72	P27/INT5/T1IN/T0LCP/T0HCP	69
73	P30/PWM4	70
74	P31/PWM5	71
75	P32/UTX1	72
76	P33/URX1	73
77	P34/UTX2	74
78	P35/URX2	75
79	P36	76
80	PB7	77
81	PB6	78
82	PB5	79
83	PB4	80
84	PB3	81
85	PB2	82
86	PB1	83
87	PB0	84
88	V <sub>SS</sub> 3	85
89	V <sub>DD</sub> 3	86
90	PC7	87
91	PC6	88
92	PC5	89
93	PC4	90
94	PC3	91
95	PC2	92
96	PC1	93
97	PC0	94
98	PA0	95
99	PA1	96
100	PA2	97



System Block Diagram



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## Pin Description

Pin Name	I/O	Function description	Option																														
V <sub>SS1</sub> , V <sub>SS2</sub> V <sub>SS3</sub> , V <sub>SS4</sub>	-	Power supply pin (-)	No																														
V <sub>DD1</sub> , V <sub>DD2</sub> V <sub>DD3</sub> , V <sub>DD4</sub>	-	Power supply pin (+)	No																														
Port 0 P00 to P07	I/O	<ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 4-bit units</li> <li>• Pull-up resistor can be turned on and off in 4-bit units</li> <li>• HOLD release input</li> <li>• Port 0 interrupt input</li> <li>• Pin functions                             <ul style="list-style-type: none"> <li>P05: System clock output</li> <li>P06: Timer 6 toggle output</li> <li>P07: Timer 7 toggle output</li> </ul> </li> </ul>	Yes																														
Port 1 P10 to P17	I/O	<ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistor can be turned on and off in 1-bit units</li> <li>• Pin functions                             <ul style="list-style-type: none"> <li>P10: SIO0 data output</li> <li>P11: SIO0 data input, bus I/O</li> <li>P12: SIO0 clock I/O</li> <li>P13: SIO1 data output</li> <li>P14: SIO1 data input, bus I/O</li> <li>P15: SIO1 clock I/O</li> <li>P16: Timer 1 PWML output</li> <li>P17: Timer 1 PWMH output, Beeper output</li> </ul> </li> </ul>	Yes																														
Port 2 P20 to P27	I/O	<ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistor can be turned on and off in 1-bit units</li> <li>• Pin functions                             <ul style="list-style-type: none"> <li>P20: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/INT6 input/timer 0L capture 1 input</li> <li>P21 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input</li> <li>P24: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input INT7 input/timer 0H capture 1 input</li> <li>P25 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input</li> </ul> </li> <li>• Interrupt acknowledge type                             <table border="1" style="margin-left: 20px; width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising/ Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT4</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT5</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT6</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT7</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table> </li> </ul>		Rising	Falling	Rising/ Falling	H level	L level	INT4	enable	enable	enable	disable	disable	INT5	enable	enable	enable	disable	disable	INT6	enable	enable	enable	disable	disable	INT7	enable	enable	enable	disable	disable	Yes
	Rising	Falling	Rising/ Falling	H level	L level																												
INT4	enable	enable	enable	disable	disable																												
INT5	enable	enable	enable	disable	disable																												
INT6	enable	enable	enable	disable	disable																												
INT7	enable	enable	enable	disable	disable																												
Port 3 P30 to P36	I/O	<ul style="list-style-type: none"> <li>• 7-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistor can be turned on and off in 1-bit units</li> <li>• Pin functions                             <ul style="list-style-type: none"> <li>P30: PWM4 output</li> <li>P31: PWM5 output</li> <li>P32: UART1 transmit</li> <li>P33: UART1 receive</li> <li>P34: UART2 transmit</li> <li>P35: UART2 receive</li> </ul> </li> </ul>	Yes																														

Continued on next page.

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Pin Name	I/O	Function description	Option																														
Port 7 P70 to P73	I/O	<ul style="list-style-type: none"> <li>• 4-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistor can be turned on and off in 1-bit units</li> <li>• Other functions</li> </ul> P70: INT0 input/HOLD release input/timer 0L capture input/output for watchdog timer P71: INT1 input/HOLD release input/timer 0H capture input P72: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input P73: INT3 input with noise filter/timer 0 event input/timer 0H capture input <ul style="list-style-type: none"> <li>• Interrupt acknowledge type</li> </ul> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising/ Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table> <ul style="list-style-type: none"> <li>• AD converter input port: AN8 (P70), AN9 (P71)</li> </ul>		Rising	Falling	Rising/ Falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable	No
	Rising	Falling	Rising/ Falling	H level	L level																												
INT0	enable	enable	disable	enable	enable																												
INT1	enable	enable	disable	enable	enable																												
INT2	enable	enable	enable	disable	disable																												
INT3	enable	enable	enable	disable	disable																												
Port 8 P80 to P87	I/O	<ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Other functions</li> </ul> P80 to P87: AD converter input port	No																														
Port A PA0 to PA5	I/O	<ul style="list-style-type: none"> <li>• 6-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistor can be turned on and off in 1-bit units</li> <li>• Shared functions</li> </ul> PA3 to PA5: AD converter input port	Yes																														
Port B PB0 to PB7	I/O	<ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistor can be turned on and off in 1-bit units</li> </ul>	Yes																														
Port C PC0 to PC7	I/O	<ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistor can be turned on and off in 1-bit units</li> </ul>	Yes																														
Port E PE0 to PE7	I/O	<ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 2-bit units</li> <li>• Pull-up resistor can be turned on and off in 1-bit units</li> </ul>	No																														
Port F PF0 to PF7	I/O	<ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 2-bit units</li> <li>• Pull-up resistor can be turned on and off in 1-bit units</li> </ul>	No																														
SIO2 Port SI2P0 to SI2P3	I/O	<ul style="list-style-type: none"> <li>• 4-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Shared functions:</li> </ul> SI2P0: SIO2 data output SI2P1: SIO2 data input, bus I/O SI2P2: SIO2 clock I/O SI2P3: SIO2 clock output	No																														
PWM0	I/O	<ul style="list-style-type: none"> <li>• PWM0 output port</li> <li>• General-purpose I/O available</li> </ul>	No																														
PWM1	I/O	<ul style="list-style-type: none"> <li>• PWM1 output port</li> <li>• General-purpose I/O available</li> </ul>	No																														
RES	I	Reset pin	No																														
XT1	I	<ul style="list-style-type: none"> <li>• Input terminal for 32.768kHz X'tal oscillation</li> <li>• Shared functions:</li> </ul> AN10: AD converter input port General-purpose input port Must be connected to VDD1 if not to be used.	No																														
XT2	I/O	<ul style="list-style-type: none"> <li>• Output terminal for 32.768kHz X'tal oscillation</li> <li>• Shared functions:</li> </ul> AN11: AD converter input port General-purpose I/O port Must be set for oscillation and kept open if not to be used.	No																														
CF1	I	Ceramic resonator input pin	No																														
CF2	O	Ceramic resonator output pin	No																														

## LC875CC8A/B2A

### Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

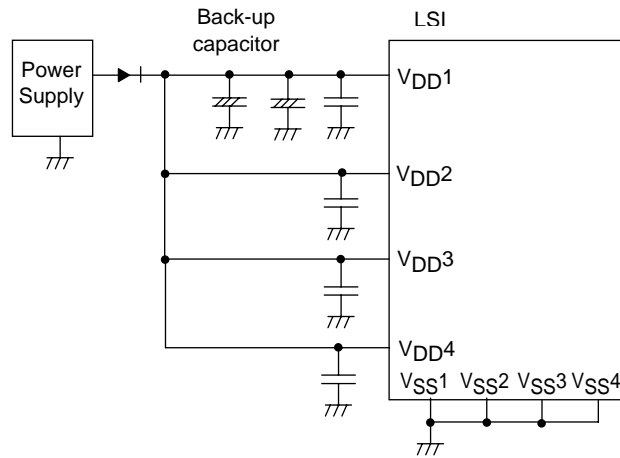
Port Name	Options Selected in Units of	Option Ttype	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	N-channel open drain	No
P10 to P17 P20 to P27 P30 to P36	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PA0 to PA5 PB0 to PB7 PC0 to PC7	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PE0 to PE7 PF0 to PF7	-	No	CMOS	Programmable
P70	-	No	N-channel open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	N-channel open drain	No
SI2P0, SI2P2 SI2P3 PWM0, PWM1	-	No	CMOS	No
SI2P1	-	No	CMOS (when selected as ordinary port) N-channel open drain (When SIO2 data is selected)	No
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz quartz oscillator N-channel open drain (when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to P03, P04 to P07).

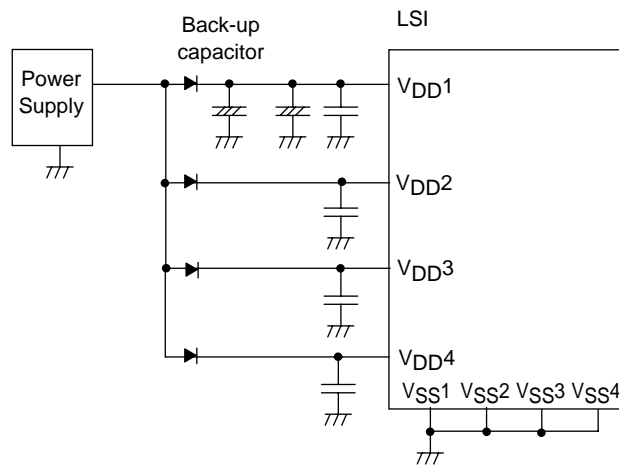
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- \*1: Make the following connection to minimize the noise input to the VDD1 pin and prolong the backup time.  
Be sure to electrically short the VSS1, VSS2, VSS3, and VSS4 pins.

(Example 1) When backup is active in the HOLD mode, the high level of the port outputs is supplied by the backup capacitors.



(Example 2) The high-level output at the ports is unstable when the HOLD mode backup is in effect.



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## Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				VDD[V]	min	typ	max	unit
Maximum supply voltage	VDD max	VDD1, VDD2, VDD3, VDD4	VDD1=VDD2=VDD3=VDD4		-0.3		+6.5	V
Input voltage	VI(1)	XT1, CF1			-0.3		VDD+0.3	
Input/Output voltage	VI(1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1, XT2			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3	CMOS output select per 1 application pin		-10		mA
		IOPH(2)	PWM0, PWM1	Per 1 application pin.		-20		
		IOPH(3)	P71 to P73	Per 1 application pin.		-5		
	Average output current (Note 1-1)	IOM(1)	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3	CMOS output select per 1 application pin		-7.5		
		IOM(2)	PWM0, PWM1	Per 1 application pin.		-15		
		IOM(3)	P71 to P73	Per 1 application pin.		-3		
	Total output current	ΣIOAH(1)	P71 to P73	Total of all applicable pins		-10		
		ΣIOAH(2)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-25		
		ΣIOAH(3)	Port 0	Total of all applicable pins		-25		
		ΣIOAH(4)	Port 0 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-45		
		ΣIOAH(5)	Ports 2, 3, B	Total of all applicable pins		-25		
		ΣIOAH(6)	Ports A, C	Total of all applicable pins		-25		
		ΣIOAH(7)	Ports 2, 3, A, B, C	Total of all applicable pins		-45		
	ΣIOAH(8)	Ports F	Total of all applicable pins		-25			
	ΣIOAH(9)	Ports 1, E	Total of all applicable pins		-25			
	ΣIOAH(10)	Ports 1, E, F	Total of all applicable pins		-45			

Note 1-1: Average output current is average of current in 100ms interval.

Continued on next page.

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Continued from preceding page.

Parameter	Symbol	Pins/Remarks	Conditions	Specification				unit
				V <sub>DD</sub> [V]	min	typ	max	
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin.			20	mA
		IOPL(2)	P00, P01	Per 1 application pin.			30	
		IOPL(3)	Ports 7, 8, XT2	Per 1 application pin.			10	
	Average output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin.			15	
		IOML(2)	P00, P01	Per 1 application pin.			20	
		IOML(3)	Ports 7, 8, XT2	Per 1 application pin.			7.5	
	Total output current	ΣIOAL(1)	Port 7, XT2	Total of all applicable pins			15	
		ΣIOAL(2)	Port 8	Total of all applicable pins			15	
		ΣIOAL(3)	Ports 7, 8, XT2	Total of all applicable pins			20	
		ΣIOAL(4)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins			45	
		ΣIOAL(5)	Port 0	Total of all applicable pins			45	
		ΣIOAL(6)	Port 0 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins			80	
ΣIOAL(7)		Ports 2, 3, B	Total of all applicable pins			45		
ΣIOAL(8)		Ports A, C	Total of all applicable pins			45		
ΣIOAL(9)		Ports 2, 3, A, B, C	Total of all applicable pins			80		
ΣIOAL(10)		Port F	Total of all applicable pins			45		
ΣIOAL(11)		Ports 1, E	Total of all applicable pins			45		
ΣIOAL(12)		Ports 1, E, F	Total of all applicable pins			80		
Maximum power dissipation	Pd max	QIP100E(14×20)	Ta=-30 to +70°C			444	mW	
		TQFP100(14×14)				345		
Operating ambient temperature	Topr				-30	70	°C	
Storage ambient temperature	Tstg				-55	125		

Note 1-1: Average output current is average of current in 100ms interval.

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**Allowable Operating Conditions** at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification					
				VDD[V]	min	typ	max	unit	
Operating supply voltage	VDD(1)	VDD1=VDD2 =VDD3=VDD4	0.245μs ≤ tCYC ≤ 200μs		2.8		5.5	V	
			0.367μs ≤ tCYC ≤ 200μs		2.5		5.5		
			1.47μs ≤ tCYC ≤ 200μs		2.2		5.5		
Memory sustaining supply voltage	VHD	VDD1=VDD2 =VDD3=VDD4	RAM and register contents in HOLD mode.		2.0		5.5		
High level input voltage	VIH(1)	Ports 1, 2, 3 SI2P0 to SI2P3 P71 to P73 P70 port input / interrupt side		2.2 to 5.5	0.3VDD +0.7		VDD	V	
	VIH(2)	Ports 0, 8 Ports A, B, C, E, F PWM0, PWM1		2.2 to 5.5	0.3VDD +0.7		VDD		
	VIH(3)	P70 Watchdog timer side		2.2 to 5.5	0.9VDD		VDD		
	VIH(4)	XT1, XT2, CF1, RES		2.2 to 5.5	0.75VDD		VDD		
Low level input voltage	VIL(1)	Ports 1, 2, 3 SI2P0 to SI2P3		4.0 to 5.5	VSS		0.1VDD +0.4	V	
	VIL(2)	P71 to P73 P70 port input/ interrupt side		2.2 to 4.0	VSS		0.2VDD		
	VIL(3)	Ports 0, 8 Ports A, B, C, E, F		4.0 to 5.5	VSS		0.15VDD +0.4		
	VIL(4)	PWM0, PWM1		2.2 to 4.0	VSS		0.2VDD		
	VIL(5)	Port 70 Watchdog timer side		2.2 to 5.5	VSS		0.8VDD -1.0		
	VIL(6)	XT1, XT2, CF1, RES		2.2 to 5.5	VSS		0.25VDD		
Instruction cycle time (Note 2-1)	tCYC			2.8 to 5.5	0.245		200	μs	
				2.5 to 5.5	0.367		200		
				2.2 to 5.5	1.470		200		
External system clock frequency	FEXCF(1)	CF1	<ul style="list-style-type: none"> <li>• CF2 pin open</li> <li>• System clock frequency division rate=1/1</li> <li>• External system clock duty =50±5%</li> </ul>	2.8 to 5.5	0.1		12	MHz	
				2.5 to 5.5	0.1		8		
				2.2 to 5.5	0.1		2		
				<ul style="list-style-type: none"> <li>• CF2 pin open</li> <li>• System clock frequency division rate=1/2</li> </ul>	2.8 to 5.5	0.2			24.4
					2.5 to 5.5	0.2			16
					2.2 to 5.5	0.2			4
Oscillation frequency range (Note 2-2)	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	2.8 to 5.5		12		MHz	
	FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		8			
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		4			
	FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0		
	FmMRC		Frequency variable RC oscillation source oscillation	2.2 to 5.5		16			
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation. See Fig. 2.	2.2 to 5.5		32.768			kHz

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-2: See tables 1 and 2 for the oscillation constants.



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## Electrical Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification				unit
				V <sub>DD</sub> [V]	min	typ	max	
High level input current	I <sub>IH</sub> (1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 RES PWM0, PWM1	Output disable Pull-up resistor OFF V <sub>IN</sub> =V <sub>DD</sub> (including the off-leak current of the output Tr.)	2.2 to 5.5			1	μA
	I <sub>IH</sub> (2)	XT1, XT2	Using as an input port V <sub>IN</sub> =V <sub>DD</sub>	2.2 to 5.5			1	
	I <sub>IH</sub> (3)	CF1	V <sub>IN</sub> =V <sub>DD</sub>	2.2 to 5.5			15	
Low level input current	I <sub>IL</sub> (1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 RES PWM0, PWM1	Output disable Pull-up resistor OFF V <sub>IN</sub> =V <sub>SS</sub> (including the off-leak current of the output Tr.)	2.2 to 5.5	-1			μA
	I <sub>IL</sub> (2)	XT1, XT2	Using as an input port V <sub>IN</sub> =V <sub>SS</sub>	2.2 to 5.5	-1			
	I <sub>IL</sub> (3)	CF1	V <sub>IN</sub> =V <sub>SS</sub>	2.2 to 5.5	-15			
High level output voltage	V <sub>OH</sub> (1)	Ports 0, 1, 2, 3	I <sub>OH</sub> =-1.0mA	4.5 to 5.5	V <sub>DD</sub> -1			V
	V <sub>OH</sub> (2)	Ports A, B, C, E, F	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (3)	SI2P0 to SI2P3	I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (4)	Ports 71, 72, 73	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (5)		I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (6)	PWM0, PWM1	I <sub>OH</sub> =-10mA	4.5 to 5.5	V <sub>DD</sub> -1.5			
	V <sub>OH</sub> (7)	P30, P31 (PWM4, 5 output mode)	I <sub>OH</sub> =-1.6mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (8)		I <sub>OH</sub> =-1.0mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
Low level output voltage	V <sub>OL</sub> (1)	Ports 0, 1, 2, 3	I <sub>OL</sub> =10mA	4.5 to 5.5			1.5	V
	V <sub>OL</sub> (2)	Ports A, B, C, E, F	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (3)	SI2P0 to SI2P3 PWM0, PWM1	I <sub>OL</sub> =1.0mA	2.2 to 5.5			0.4	
	V <sub>OL</sub> (4)	P00, P01	I <sub>OL</sub> =30mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (5)		I <sub>OL</sub> =5.0mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (6)		I <sub>OL</sub> =2.5mA	2.2 to 5.5			0.4	
	V <sub>OL</sub> (7)	Ports 7, 8, XT2	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (8)		I <sub>OL</sub> =1.0mA	2.2 to 5.5			0.4	
Pull-up resistation	R <sub>pu</sub> (1)	Ports 0, 1, 2, 3 Port 7	V <sub>OH</sub> =0.9V <sub>DD</sub>	4.5 to 5.5	15	35	80	kΩ
	R <sub>pu</sub> (2)	Ports A, B, C, E, F		2.2 to 5.5	15	35	150	
Hysteresis voltage	VHYS	RES Ports 1, 2, 7 SI2P0 to SI2P3		2.2 to 5.5		0.1V <sub>DD</sub>		V
Pin capacitance	CP	All pins	<ul style="list-style-type: none"> <li>• For pins other than that under test: V<sub>IN</sub>=V<sub>SS</sub></li> <li>• f=1MHz</li> <li>• Ta=25°C</li> </ul>	2.2 to 5.5		10		pF

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**Serial I/O Characteristics** at  $T_a = -30^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{SS1} = V_{SS2} = V_{SS3} = V_{SS4} = 0\text{V}$

## 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter		Symbol	Pins/ Remarks	Conditions	$V_{DD}[\text{V}]$	Specification				
						min	typ	max	unit	
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	<ul style="list-style-type: none"> <li>• See Fig. 6.</li> </ul>	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)	<ul style="list-style-type: none"> <li>• Continuous data transmission/reception mode</li> <li>• SIO2 is not in use simultaneous.</li> <li>• See Fig. 6.</li> <li>• (Note 4-1-2)</li> </ul>			4			
			tSCKHA(1b)				<ul style="list-style-type: none"> <li>• Continuous data transmission/reception mode</li> <li>• SIO2 is in use simultaneous.</li> <li>• See Fig. 6.</li> <li>• (Note 4-1-2)</li> </ul>	6		
	Output clock	Frequency	tSCK(2)	SCK0(P12)	<ul style="list-style-type: none"> <li>• CMOS output selected.</li> <li>• See Fig. 6.</li> </ul>	2.2 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2a)	<ul style="list-style-type: none"> <li>• Continuous data transmission/reception mode</li> <li>• SIO2 is not in use simultaneous.</li> <li>• CMOS output selected.</li> <li>• See Fig. 6.</li> </ul>			tSCKH(2) +2tCYC		tSCKH(2) +(10/3)tCYC	tCYC
tSCKHA(2b)		<ul style="list-style-type: none"> <li>• Continuous data transmission/reception mode</li> <li>• SIO2 is in use simultaneous.</li> <li>• CMOS output selected.</li> <li>• See Fig. 6.</li> </ul>	tSCKH(2) +2tCYC					tSCKH(2) +(16/3)tCYC		
Serial input	Data setup time		tsDI(1)	SIO(P11), SB0(P11)	<ul style="list-style-type: none"> <li>• Must be specified with respect to rising edge of SIOCLK</li> <li>• See fig. 6.</li> </ul>	2.2 to 5.5	0.03			
	Data hold Time	thDI(1)	0.03							
Serial output	Input clock	Output delay time	tdD0(1)	SIO(P10), SB0(P11),	<ul style="list-style-type: none"> <li>• Continuous data transmission/reception mode</li> <li>• (Note 4-1-3)</li> </ul>	2.2 to 5.5			(1/3)tCYC +0.05	$\mu\text{s}$
			tdD0(2)				<ul style="list-style-type: none"> <li>• Synchronous 8-bit mode.</li> <li>• (Note 4-1-3)</li> </ul>			
	tdD0(3)	<ul style="list-style-type: none"> <li>• (Note 4-1-3)</li> </ul>						(1/3)tCYC +0.05		

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIO0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

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## 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter		Symbol	Pins/ Remarks	Conditions	V <sub>DD</sub> [V]	Specification				
						min	typ	max	unit	
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected. • See Fig. 6.	2.2 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time	tsDI(2)	SI1(P14), SB1(P14)	• Must be specified with respect to rising edge of SIOCLK • See fig. 6.	2.2 to 5.5	0.03				
	Data hold time	thDI(2)				0.03				
Serial output	Output delay time	tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.2 to 5.5			(1/3)tCYC +0.05	μs	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

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## 3. SIO2 Serial I/O Characteristics (Note 4-3-1)

Parameter	Symbol	Pins/ Remarks	Conditions	Specification							
				V <sub>DD</sub> [V]	min	typ	max	unit			
Serial clock	Input clock	Frequency	tSCK(5)	SCK2 (SI2P2)	2.2 to 5.5				tCYC		
		Low level pulse width	tSCKL(5)								
		High level pulse width	tSCKH(5)								
			tSCKHA(5a)	<ul style="list-style-type: none"> <li>Continuous data transmission/reception mode of SIO0 is not in use simultaneous.</li> <li>See Fig. 6.</li> <li>(Note 4-3-2)</li> </ul>							
			tSCKHA(5b)							<ul style="list-style-type: none"> <li>Continuous data transmission/reception mode of SIO0 is in use simultaneous.</li> <li>See Fig. 6.</li> <li>(Note 4-3-2)</li> </ul>	
	Output clock	Frequency	tSCK(6)	SCK2 (SI2P2), SCK2O (SI2P3)	2.2 to 5.5				tSCK		
		Low level pulse width	tSCKL(6)								
		High level pulse width	tSCKH(6)								
			tSCKHA(6a)	<ul style="list-style-type: none"> <li>Continuous data transmission/reception mode of SIO0 is not in use simultaneous.</li> <li>CMOS output selected.</li> <li>See Fig. 6.</li> </ul>						tSCKH(6) + (5/3)tCYC	tSCKH(6) + (10/3)tCYC
			tSCKHA(6b)							<ul style="list-style-type: none"> <li>Continuous data transmission/reception mode of SIO0 is in use simultaneous.</li> <li>CMOS output selected.</li> <li>See Fig. 6.</li> </ul>	tSCKH(6) + (5/3)tCYC
Serial input	Data setup time	tsDI(3)	SI2(SI2P1), SB2(SI2P1)	2.2 to 5.5							
	Data hold time	thDI(3)									
Serial output	Output delay time	tdD0(5)	SO2(SI2P0), SB2(SI2P1)	2.2 to 5.5				(1/3)tCYC + 0.05	μs		

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input, a time from SI2RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

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### Pulse Input Conditions at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72) INT4(P20 to P23), INT5(P24 to P27), INT6(P20), INT7(P24)	<ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 or 1 are enabled.</li> </ul>	2.2 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (The noise rejection clock is selected to 1/32.)	<ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul>	2.2 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (The noise rejection clock is selected to 1/32.)	<ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul>	2.2 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (The noise rejection clock is selected to 1/128.)	<ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul>	2.2 to 5.5	256			
	tPIL(5)	RES	Reset acceptable	2.2 to 5.5	200			μs

### AD Converter Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Resolution	N	AN0(P80)		3.0 to 5.5		8		bit
Absolute precision	ET	to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2), AN12(PA3), AN13(PA4), AN14(PA5)	(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	11.74 (tCYC= 0.367μs)		97.92 (tCYC= 3.06μs)	μs
				3.0 to 5.5	31.36 (tCYC= 0.980μs)		97.92 (tCYC= 3.06μs)	
				4.5 to 5.5	15.68 (tCYC= 0.245μs)		97.92 (tCYC= 1.53μs)	
				3.0 to 5.5	31.36 (tCYC= 0.490μs)		97.92 (tCYC= 1.53μs)	
Analog input voltage range	VAIN			3.0 to 5.5	V <sub>SS</sub>		V <sub>DD</sub>	V
Analog port input current	I <sub>AINH</sub>		V <sub>AIN</sub> =V <sub>DD</sub>	3.0 to 5.5			1	μA
	I <sub>AINL</sub>		V <sub>AIN</sub> =V <sub>SS</sub>	3.0 to 5.5	-1			

Note 6-1: The quantization error (±1/2 LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the complete digital value corresponding to the analog input value is loaded in the required register.

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## Consumption Current Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/ Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	V <sub>DD1</sub> =V <sub>DD2</sub> =V <sub>DD3</sub> =V <sub>DD4</sub>	<ul style="list-style-type: none"> <li>• FmCF=12MHz ceramic oscillation mode</li> <li>• FmX'tal=32.768kHz by crystal oscillation mode</li> <li>• System clock set to 12MHz side</li> <li>• Internal RC oscillation stopped</li> <li>• Frequency variable RC oscillation stopped</li> <li>• 1/1 frequency division ratio.</li> </ul>	4.5 to 5.5		9.6	14	mA
	IDDOP(2)			2.8 to 4.5		4.8	8.5	
	IDDOP(3)			4.5 to 5.5		6.2	10	
	IDDOP(4)			2.5 to 4.5		3.2	6.5	
	IDDOP(5)			4.5 to 5.5		2.5	3	
	IDDOP(6)			2.2 to 4.5		1.2	2.5	
	IDDOP(7)			4.5 to 5.5		0.7	2	
	IDDOP(8)			2.2 to 4.5		0.3	1.5	
	IDDOP(9)			4.5 to 5.5		1.25	3	
	IDDOP(10)			2.2 to 4.5		0.75	2	
	IDDOP(11)			4.5 to 5.5		27	65	μA
	IDDOP(12)			2.2 to 4.5		12	45	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

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Parameter	Symbol	Pins/ Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3 =V <sub>DD</sub> 4	<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=12MHz ceramic oscillation mode</li> <li>• FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	4.5 to 5.5		3.3	6	mA
	IDDHALT(2)		<ul style="list-style-type: none"> <li>• System clock set to 12MHz side</li> <li>• Internal RC oscillation stopped</li> <li>• Frequency variable RC oscillation stopped</li> <li>• 1/1 frequency division ratio.</li> </ul>	2.8 to 5.5		1.6	3.5	
	IDDHALT(3)		<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=8MHz ceramic oscillation mode</li> <li>• FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	4.5 to 5.5		2.3	4.5	
	IDDHALT(4)		<ul style="list-style-type: none"> <li>• System clock set to 8MHz side</li> <li>• Internal RC oscillation stopped</li> <li>• Frequency variable RC oscillation stopped</li> <li>• 1/1 frequency division ratio.</li> </ul>	2.5 to 5.5		0.98	2.5	
	IDDHALT(5)		<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=4MHz ceramic oscillation mode</li> <li>• FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	4.5 to 5.5		1.2	2.0	
	IDDHALT(6)		<ul style="list-style-type: none"> <li>• System clock set to 4MHz side</li> <li>• Internal RC oscillation stopped</li> <li>• Frequency variable RC oscillation stopped</li> <li>• 1/2 frequency division ratio.</li> </ul>	2.2 to 4.5		0.6	1.5	
	IDDHALT(7)		<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz(oscillation stopped)</li> <li>• FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	4.5 to 5.5		0.3	1	
	IDDHALT(8)		<ul style="list-style-type: none"> <li>• System clock set to internal RC oscillation</li> <li>• Frequency variable RC oscillation stopped</li> <li>• 1/2 frequency division ratio.</li> </ul>	2.2 to 4.5		0.14	0.5	
	IDDHALT(9)		<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz(oscillation stopped)</li> <li>• FmX'al=32.768kHz by crystal oscillation mode.</li> </ul>	4.5 to 5.5		1.0	2.5	
	IDDHALT(10)		<ul style="list-style-type: none"> <li>• System clock set to 1MHz with frequency variable RC oscillation</li> <li>• Internal RC oscillation stopped</li> <li>• 1/2 frequency division ratio.</li> </ul>	2.2 to 4.5		0.5	1.8	
	IDDHALT(11)		<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz(oscillation stopped)</li> <li>• FmX'al=32.768kHz by crystal oscillation mode.</li> </ul>	4.5 to 5.5		17	55	
	IDDHALT(12)		<ul style="list-style-type: none"> <li>• System clock set to 32.768kHz side.</li> <li>• Internal RC oscillation stopped</li> <li>• Frequency variable RC oscillation stopped</li> <li>• 1/2 frequency division ratio.</li> </ul>	2.2 to 4.5		5	30	
Current drain during HOLD mode	IDDHOLD(1)	V <sub>DD</sub> 1	<ul style="list-style-type: none"> <li>• HOLD mode</li> <li>• CF1=V<sub>DD</sub> or open (External clock mode)</li> </ul>	4.5 to 5.5		0.02	10	μA
	IDDHOLD(2)		<ul style="list-style-type: none"> <li>• Timer HOLD mode</li> <li>• CF1=V<sub>DD</sub> or open(External clock mode)</li> </ul>	2.2 to 4.5		0.008	8	
Current drain during time-base clock HOLD mode	IDDHOLD(3)		<ul style="list-style-type: none"> <li>• Timer HOLD mode</li> <li>• CF1=V<sub>DD</sub> or open(External clock mode)</li> </ul>	4.5 to 5.5		14	40	
	IDDHOLD(4)		<ul style="list-style-type: none"> <li>• FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	2.2 to 4.5		3.2	2.5	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

**UART(Full Duplex) Operating Conditions**

at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

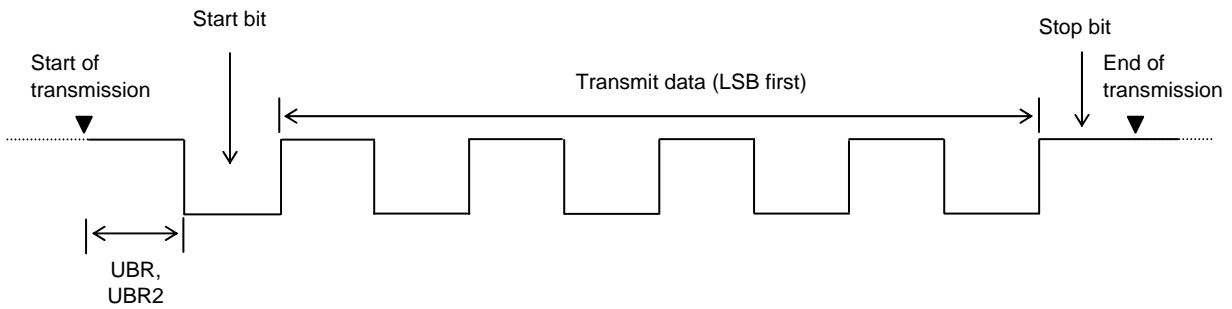
Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Clock rate	UBR, UBR2	UTX1(P32), RTX1(P33), UTX2(P33), RTX2(P34)		2.2 to 5.5	16/3		8192/3	tCYC

Data length: 7,8,and 9 bits (LSB first)

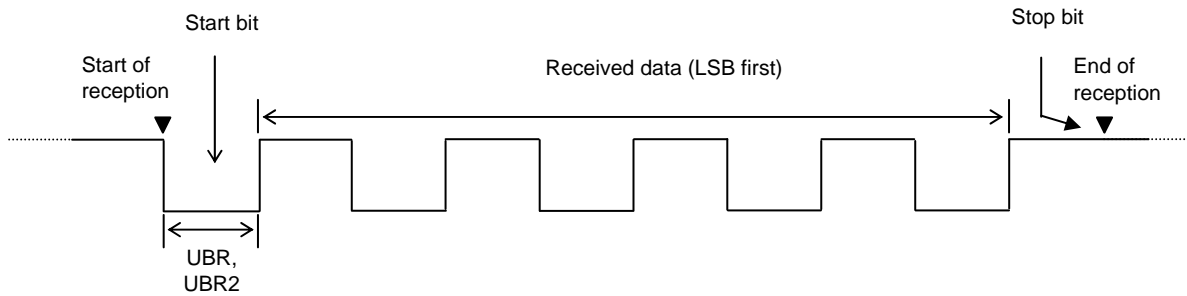
Stop bits: 1 bit (2-bit in continuous data transmission)

Parity bits: Non

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)

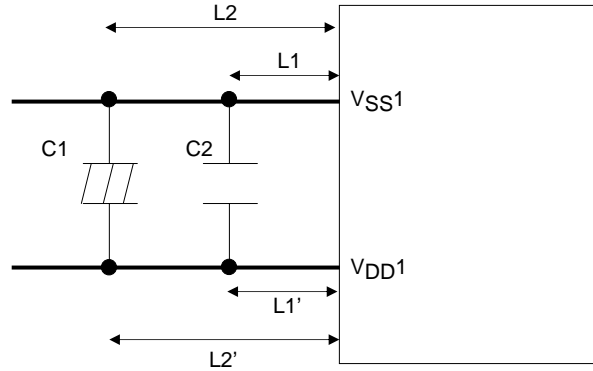




**VDD1, VSS1 Terminal Condition**

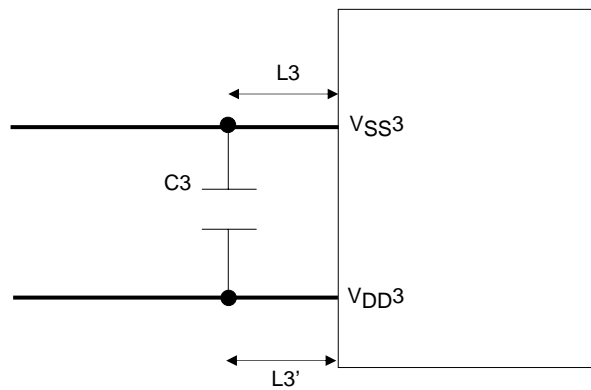
It is necessary to place capacitors between VDD1 and VSS1 as described below.

- Place capacitors as close to VDD1 and VSS1 as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal ( $L1 = L1'$ ,  $L2 = L2'$ ).
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
- Capacitance of C2 must be more than  $0.1\mu\text{F}$ .
- Use thicker pattern for VDD1 and VSS1.

**VDD3, VSS3 Terminal Condition**

It is necessary to place capacitors between VDD3 and VSS3 as described below.

- Place capacitors as close to VDD3 and VSS3 as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal ( $L3 = L3'$ ).
- Capacitance of C3 must be more than  $0.1\mu\text{F}$ .
- Use thicker pattern for VDD3 and VSS3.



## Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1. Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	OPEN	470	2.8 to 5.5	0.05	0.15	Internal C1, C2
8MHz		CSTCE8M00G52-R0	(10)	(10)	OPEN	2.2k	2.7 to 5.5	0.05	0.15	Internal C1, C2
		CSTLS8M00G53-B0	(15)	(15)	OPEN	680	2.5 to 5.5	0.05	0.15	Internal C1, C2
4MHz		CSTCR4M00G53-R0	(15)	(15)	OPEN	3.3k	2.2 to 5.5	0.05	0.15	Internal C1, C2
		CSTLS4M00G53-R0	(15)	(15)	OPEN	3.3k	2.2 to 5.5	0.05	0.15	Internal C1, C2

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the operating voltage lower limit (see Fig 4).

## Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2. Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	SEIKO EPSON	MC-306	18	18	OPEN	560k	2.2 to 5.5	1.3	3.0	Applicable CL Value=12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Fig 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

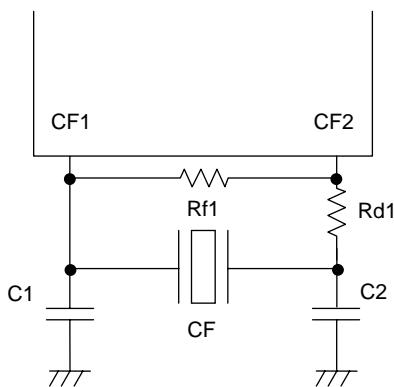


Figure 1 Ceramic oscillation circuit

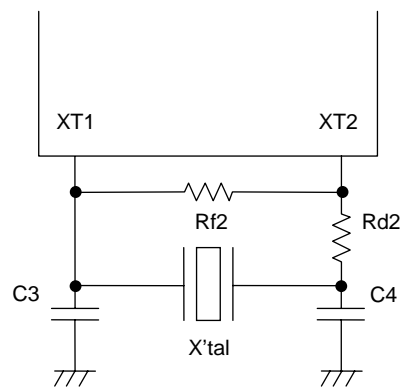


Figure 2 Crystal oscillation circuit

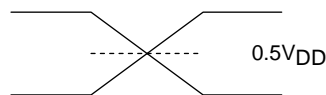
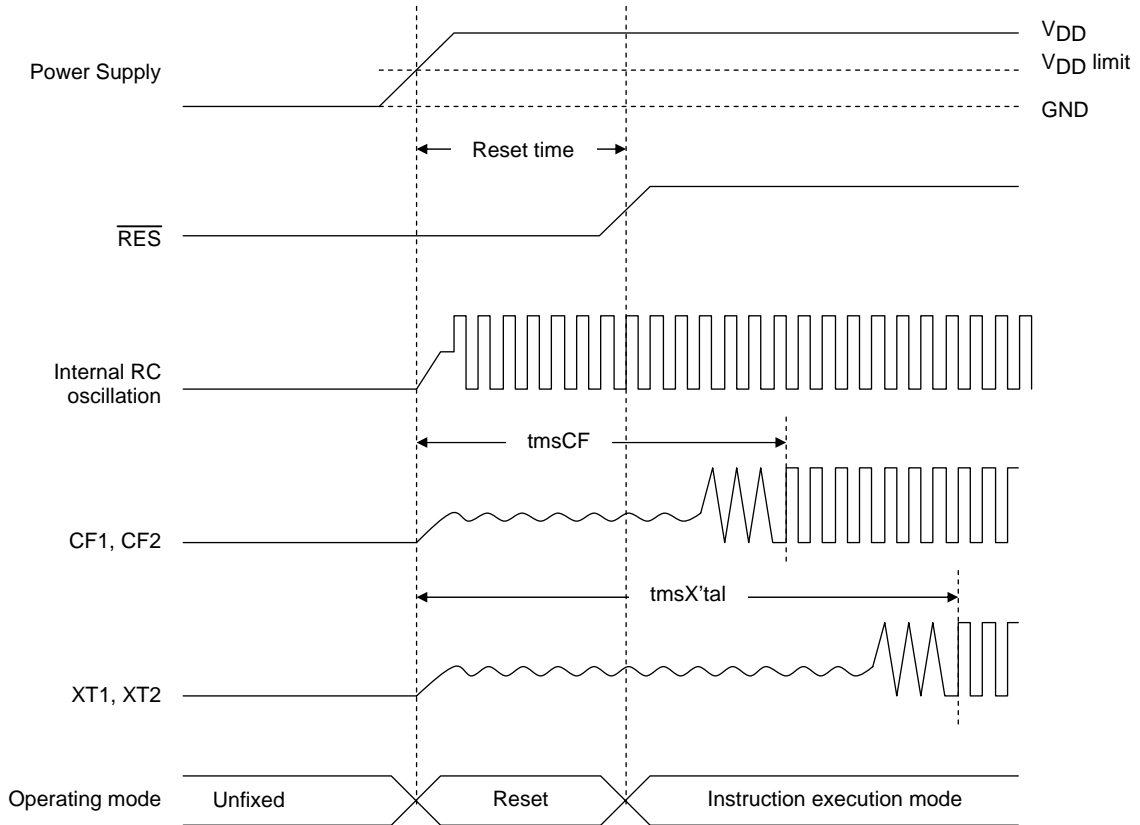
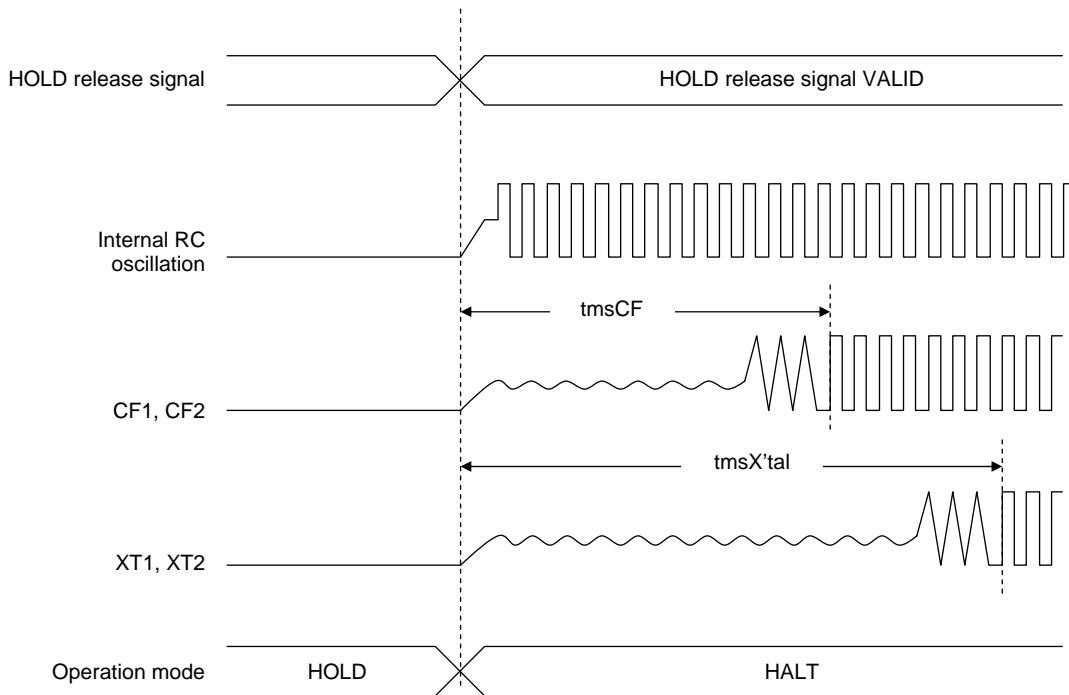


Figure 3 AC timing point

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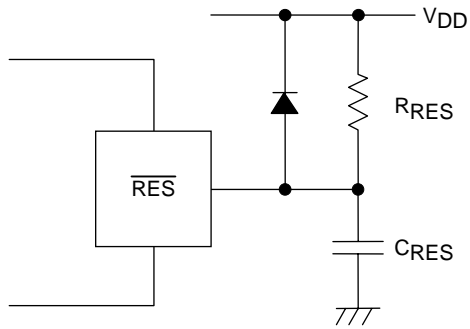


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



Note :  
 Select  $C_{RES}$  and  $R_{RES}$  value to assure that at least  $200\mu s$  reset time is generated after the  $V_{DD}$  becomes higher than the minimum operating voltage.

Figure 5 Reset Circuit

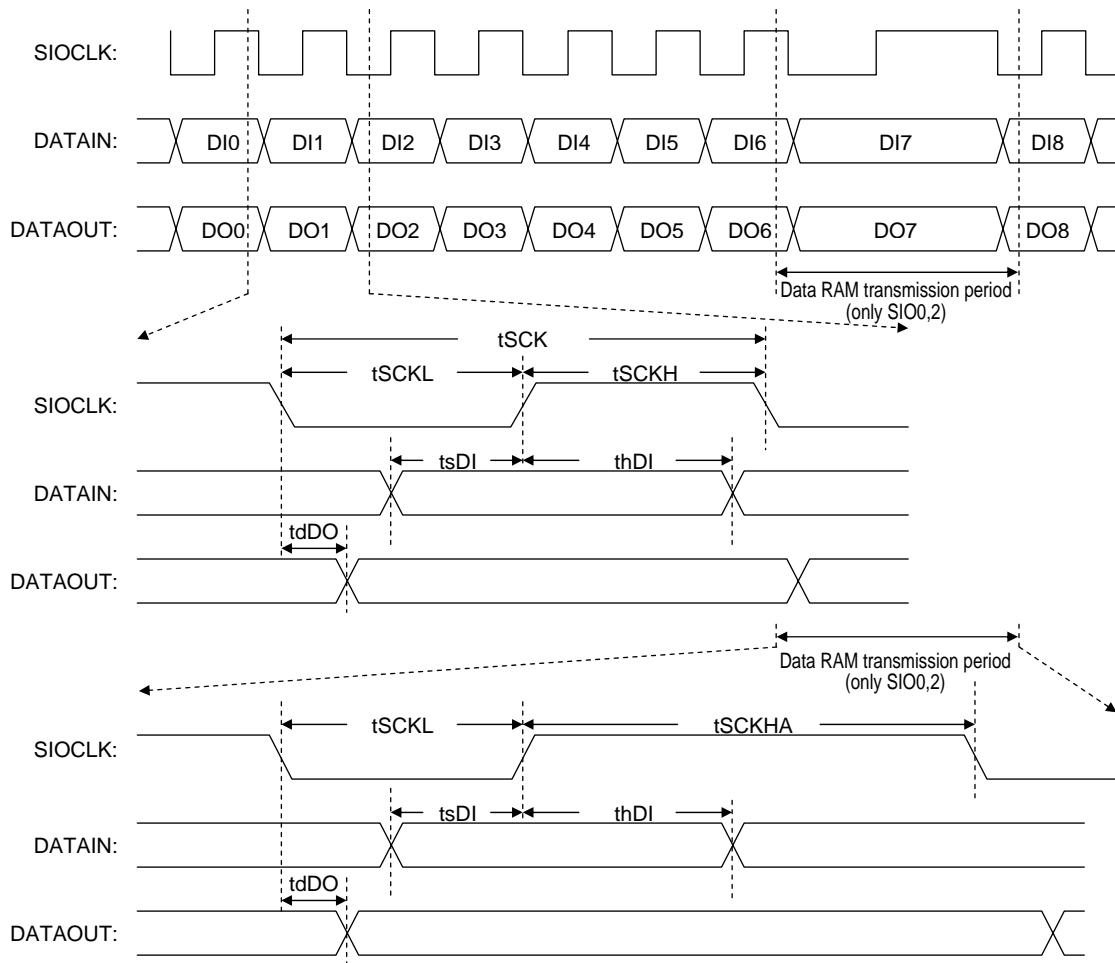


Figure 6 Serial I/O Waveforms

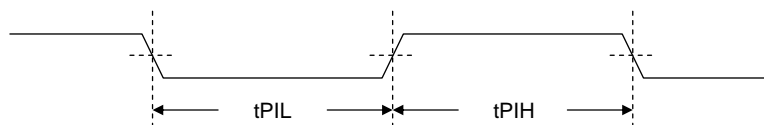


Figure 7 Pulse Input Timing Condition

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