Ordering number : ENA1828

SANYO Semiconductors
DATA SHEET

LC87F0808A — CMOS IC 8K-byte FROM and 256-byte RAM integrated 8-bit 1-chip Microcontroller

Overview

The SANYO LC87F0808A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 50.0ns, integrates on a single chip a number of hardware features such as 8K-byte flash ROM (On-board-programmable), 256-byte RAM, an On-chip-debugger, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), two 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface, an asynchronous/synchronous SIO interface, a UART interface (full duplex), motor control PWM , a 10/8-bit 10-channel AD converter, a system clock frequency divider, an internal reset and a 21-source 10-vector interrupt feature.
This microcomputer is suitable for small motor control equipment.

Features

■Flash ROM
- Capable of On-board-programming with wide range (3.3 to 5.5V) of voltage source.
- Block-erasable in 128 byte units
- Writable in 2-byte units
- 8192 × 8 bits

■RAM
- 256 × 9 bits

■Minimum Bus Cycle
- 50.0ns (20MHz at V_{DD}=3.3V to 5.5V)
  Note: The bus cycle time here refers to the ROM read speed.

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■Ports

- Normal withstand voltage I/O ports
  Ports I/O direction can be designated in 1-bit units — 20 (P1n, P20, P21, P30 to P35, P70 to P73)
  Ports I/O direction can be designated in 4-bit units — 8 (P0n)
- Dedicated oscillator ports/input ports — 2 (CF1/XT1, CF2/XT2)
- Reset pin — 1 ($\overline{\text{RES}}$)
- On-chip Debugger pin — 1 (OWP0)
- Power pins — 4 ($V_{SS}1$, $V_{SS}2$, $V_{DD}1$, $V_{DD}2$)

■Timers

- Timer 0: 16-bit timer/counter with a capture register.
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM)
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts are programmable in 5 different time schemes
  3) The base timer is unavailable when the CF oscillator circuit is selected

■SIO

- SIO0: 8-bit Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle=4/3tCYC)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART

- Full Duplex
- 7/8/9 bit data bits selectable
- 1 Stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

■AD Converter: 10 bits/8 bits × 10 channels (internal: 2 channels)

- 10/8 bits AD converter resolution selectable
- Auto start function (It links an interrupt factor of MCPWM)

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
- Noise rejection function (noise filter time constant selectable from 1 tCYC/32 tCYC/128 tCYC)

■Clock Output Function
- Can generate clock outputs with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock selected as the system clock.
- Can generate the source clock for the subclock

■Analog Comparator / Amplifier × 2 channels
- Analog comparator / amplifier selectable (each channel)
- Analog comparator Interrupt

■MCPWM: Motor Control 12-bit PWM × 6 channels
- Dead time is programmable.
- Forced stop is possible by the output of the analog comparator and the INT terminals.
- Edge-aligned / center-aligned selectable

■Watchdog Timer
- Can generate the internal reset signal on a timer overflow monitored by the WDT-dedicated low-speed RC oscillation clock (30kHz).
- Allows selection of continue, stop, or hold mode operation of the counter on entry into the HALT/HOLD mode.

■Interrupts
- 21 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/Base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit/MCPWM
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/CMP1/CMP2

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 128levels (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- Internal oscillation circuits

  Medium-speed RC oscillation circuit: For system clock (1MHz)
  High-speed RC oscillation circuit: For system clock (20MHz)
  Low-speed RC oscillation circuit: For watch dog timer (30kHz)

- External oscillation circuits

  Hi-speed CF oscillation circuit: For system clock, with internal Rf
  Low speed crystal oscillation circuit: For low-speed system clock, with internal Rf

  1) The CF and crystal oscillation circuits share the same pins. The active circuit is selected under program control.
  2) The CF and the crystal oscillation circuits stop operating in the system reset state and start oscillating when the oscillation is enabled with an instruction.

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 150ns, 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs and 38.4µs (at a main clock rate of 20MHz).

■Internal Reset Function

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are three ways of resetting the HALT mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC and crystal oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Having an interrupt source established at either INT0, INT1, INT2 or INT4
         * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0.
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF and RC oscillator automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) System resetting by watchdog timer or low-voltage detection.
     (3) Having an interrupt source established at either INT0, INT1, INT2 or INT4
         * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0.
     (5) Having an interrupt source established in the base timer circuit.
     Note: Available only when X’tal oscillation is selected.

■On-chip Debugger
- Supports software debugging with the IC mounted on the target board.

■Data Security Function (flash versions only)
- Protects the program data stored in flash memory from unauthorized read or copy.
  Note: This data security function does not necessarily provide absolute data security.

■Package Form
- QFP36 (7×7): Lead-/Halogen-free type

■Development Tools
- On-chip debugger: TCB87 type C + LC87F0808A

■Programming Boards

Package	Programming boards
QFP36(7×7)	W87F24Q

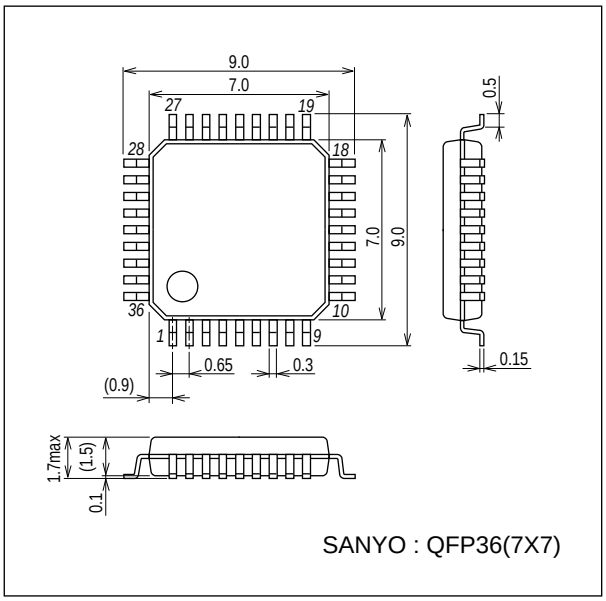
■Flash ROM Programmer

Maker		Model	Supported Version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev 03.28 or later	87f008SU (3B247)
	Gang Programmer	AF9723/AF9723B(Main body) (Including Ando Electric Co., Ltd. models)	-	-
		AF9833(Unit) (Including Ando Electric Co., Ltd. models)	-	-
Sanyo	Single/Gang Programmer	SKK/SKK Type B (SanyoFWS)	Application Version 1.06 or later Chip Data Version 2.26 or later	LC87F0808
	Gang Programmer	SKK-4G (SanyoFWS)		
	In-circuit/Gang Programmer	SKK-DBG Type C (SanyoFWS)	Application Version 1.06 or later Chip Data Version 2.31 or later	

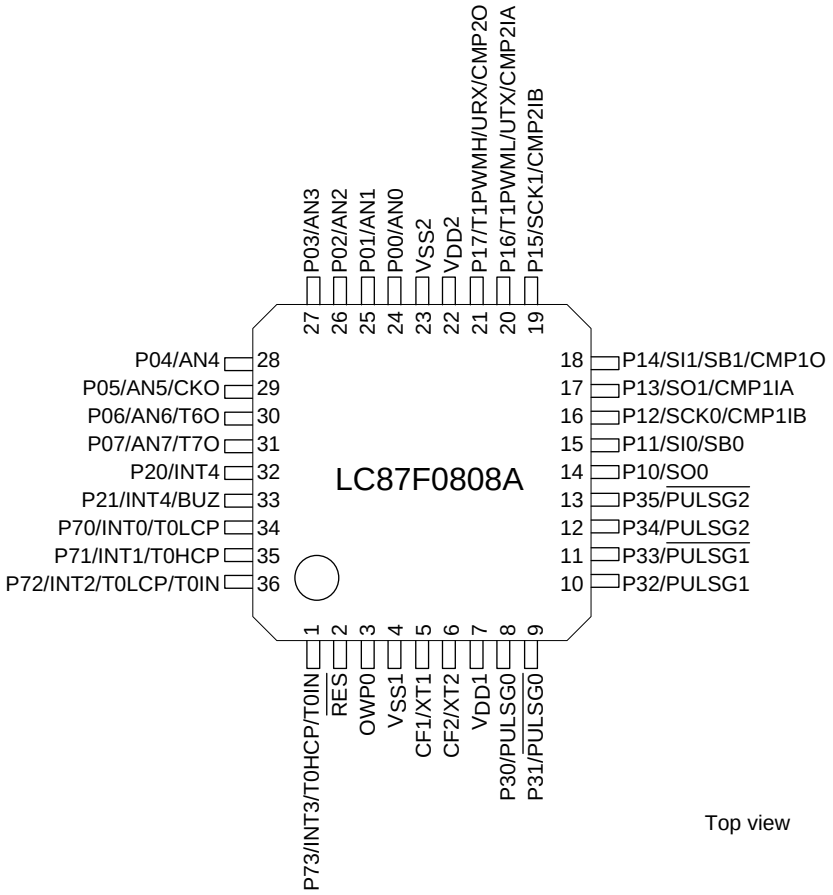
For information about AF-Series:
Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

Package Dimensions

unit : mm (typ)
3162C



Pin Assignment

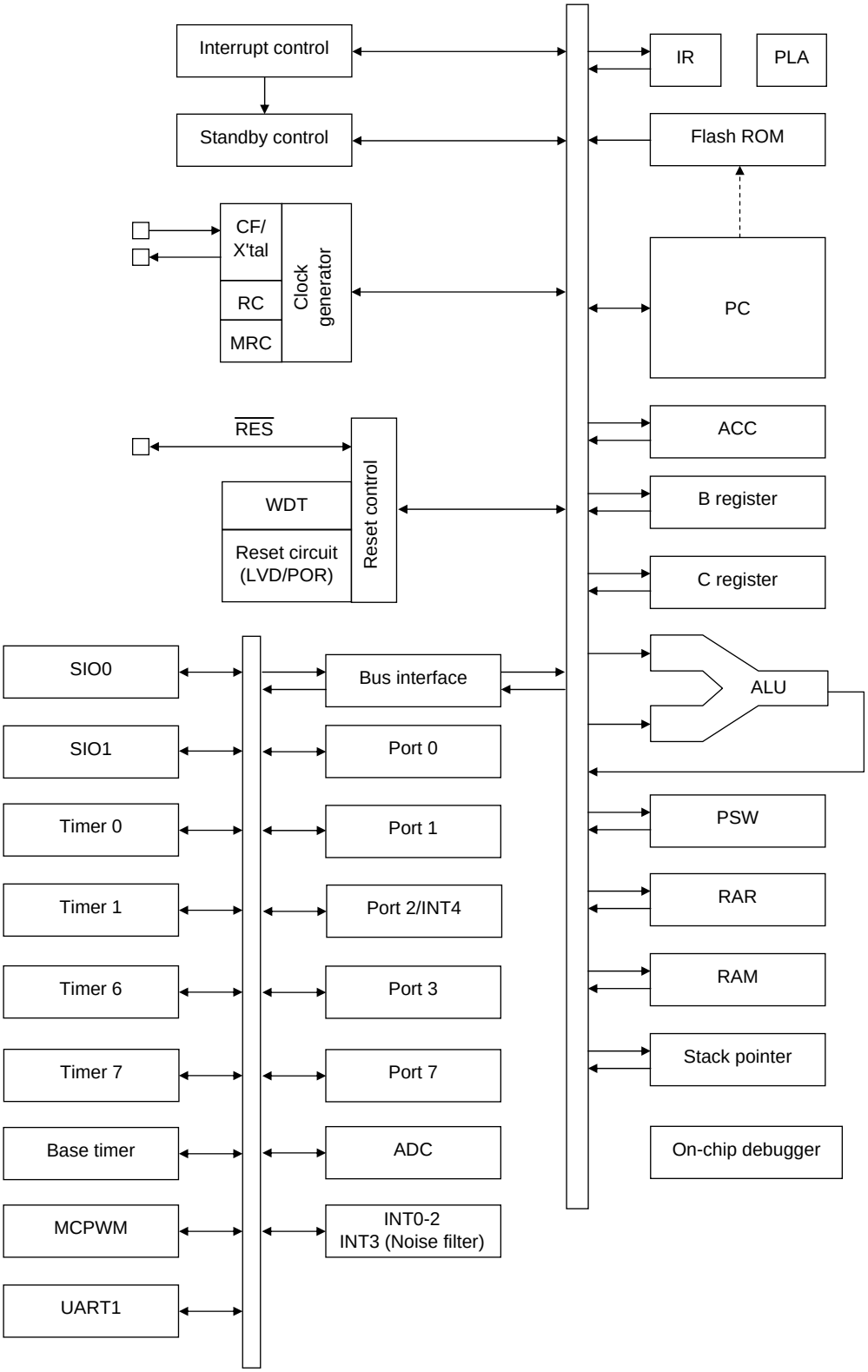


SANYO: QFP36 (7×7) “Lead-/Halogen-free Type”

QFP36	NAME
1	P73/INT3/T0HCP/T0IN
2	$\overline{RES}$
3	OWP0
4	$V_{SS}1$
5	CF1/XT1
6	CF2/XT2
7	$V_{DD}1$
8	P30/PULSG0
9	P31/$\overline{PULSG0}$
10	P32/PULSG1
11	P33/$\overline{PULSG1}$
12	P34/PULSG2
13	P35/$\overline{PULSG2}$
14	P10/SO0
15	P11/SI0/SB0
16	P12/SCK0/CMP1IB(+)
17	P13/SO1/CMP1IA(-)
18	P14/SI1/SB1/CMP1O

QFP36	NAME
19	P15/SCK1/CMP2IB(+)
20	P16/T1PWML/UTX/CMP2IA(-)
21	P17/T1PWMH/URX/CMP2O
22	$V_{DD}2$
23	$V_{SS}2$
24	P00/AN0
25	P01/AN1
26	P02/AN2
27	P03/AN3
28	P04/AN4
29	P05/AN5/CKO
30	P06/AN6/T6O
31	P07/AN7/T7O
32	P20/INT4
33	P21/INT4/BUZ
34	P70/INT0/T0LCP
35	P71/INT1/T0HCP
36	P72/INT2/T0LCP/T0IN

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$,$V_{SS}2$</td><td>-</td><td>- Power supply pins</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$</td><td>-</td><td>+ Power supply pins</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistors can be turned on and off in 4-bit units.
• HOLD reset input
• Port 0 interrupt input
• Pin functions
P05: System clock output
P06: Timer 6 toggle output
P07: Timer 7 toggle output
P00 (AN0) to P07 (AN7): AD converter input</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input / bus I/O
P15: SIO1 clock I/O
P16: Timer 1 PWML output / UART transmit
P17: Timer 1 PWMH output / UART receive
P12 to P17: analog comparator / amplifier I/O pins
P12: CMP1(+) input / AMP1(+) input
P13: CMP1(-) input / AMP1(-) input
P14: CMP1 output / AMP1 output
P15: CMP2(+) input / AMP2(+) input
P16: CMP2(-) input / AMP2(-) input
P17: CMP2 output / AMP2 output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P21</td><td>I/O</td><td>• 2-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P21: Beeper output
P20 to P21: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P35</td><td>I/O</td><td>• 6-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P30 to p35 : motor control PWM output pins
P30: PULSG0 output
P31: $\overline{\text{PULSG0}}$ output
P32: PULSG1 output
P33: $\overline{\text{PULSG1}}$ output
P34: PULSG2 output
P35: $\overline{\text{PULSG2}}$ output</td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P70: INT0 input/HOLD reset input/timer 0L capture input
P71: INT1 input/HOLD reset input/timer 0H capture input
P72: INT2 input/HOLD reset input/timer 0 event input / timer 0L capture input
P73: INT3 input (with noise filter)/ timer 0 event input/timer 0H capture input
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>OWP0</td><td>I/O</td><td>On-chip debugger (exclusive pin)</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset input/internal reset output</td><td>No</td></tr>
<tr><td>CF1/XT1</td><td>I</td><td>• Ceramic resonator or 32.768kHz crystal oscillator input pin
• Pin function
General-purpose input port</td><td>No</td></tr>
<tr><td>CF2/XT2</td><td>I/O</td><td>• Ceramic resonator or 32.768kHz crystal oscillator output pin
• Pin function
General-purpose input port</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P21	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P35	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70 to P73	-	No	CMOS	Programmable

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low-and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

User Option Table

Option name	Option to be applied on	Flash-rom version	Option selected in units of	Option selection
Port output type	P00 to P07	○	1 bit	CMOS
				Nch-open drain
	P10 to P17	○	1 bit	CMOS
				Nch-open drain
	P20 to P21	○	1 bit	CMOS
				Nch-open drain
	P30 to P35	○	1 bit	CMOS
				Nch-open drain
Program start address	-	○	-	00000h
				01E00h
Protect area (Note 1)	-	○	-	00000h to 01BFFh
				01C00h to 01EFFh
Low-voltage detection reset function	Detect function	○	-	Enable: Use
				Disable: Not Used
	Detect level	○	-	7-level
Power-on reset function	Power-On reset level	○	-	8-level

(Note 1) This option selects the area to be write protected at the time of the On-board writing.

Recommended Unused Pin Connections

Port Name	Recommended unused pin connections	
	Board	Software
P00 to P07	Open	Output low
P10 to P17	Open	Output low
P20 to P21	Open	Output low
P30 to P35	Open	Output low
P70 to P73	Open	Output low
CF1/XT1	Pulled low with a 100kΩ resistor or less	General-purpose input port
CF2/XT2	Pulled low with a 100kΩ resistor or less	General-purpose input port

On-chip Debugger Pin Connection Requirements

OWP0 of the On-chip-debugger terminal must add pull-down resistor of 100kΩ.
The connection with TCB87 Type C are OWP0/V_{DD}/V_{SS}

Note: Be sure to electrically short-circuit between the $V_{SS}1$ and $V_{SS}2$ pins and between the $V_{DD}1$ and $V_{DD}2$ pins.

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$			-0.3		+6.5	V
Input voltage		V_I	CF1			-0.3		V_{DD}+0.3	V
Input/output voltage		V_{IO}	CF2 Ports 0, 1, 2, 3 Port 7			-0.3		V_{DD}+0.3	V
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-10			mA
		IOPH(2)	Port7	Per 1 applicable pin		-5			mA
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-7.5			mA
		IOMH(2)	Port7	Per 1 applicable pin		-3			mA
	Total output current	ΣIOAH(1)	Ports 0, 2, 7	Total of all applicable pins		-25			mA
		ΣIOAH(2)	Ports 1, 3	Total of all applicable pins		-25			mA
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2, 3	Per 1 applicable pin				20	mA
		IOPL(2)	P00, P01	Per 1 applicable pin				30	mA
		IOPL(3)	Port 7	Per 1 applicable pin				10	mA
	Mean output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2, 3	Per 1 applicable pin				15	mA
		IOML(2)	P00, P01	Per 1 applicable pin				20	mA
		IOML(3)	Port 7	Per 1 applicable pin				7.5	mA
	Total output current	ΣIOAL(1)	Ports 0, 2, 7	Total of all applicable pins				45	mA
		ΣIOAL(2)	Ports 1, 3	Total of all applicable pins				45	mA
Power Dissipation		Pd max(1)	QFP36(7×7)	Ta=-40 to +85°C Package only				115	mW
		Pd max(2)		Ta=-40 to +85°C Package with thermal resistance board (Note 1-2)				244	mW
Operating ambient Temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	°C

Note 1-1: The mean output current is a mean value measured over 100ms.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6tmm, glass epoxy) is used.

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage	V_{DD}	$V_{DD}1$, $V_{DD}2$	0.142µs ≤ tCYC ≤ 200µs		3.3		5.5	V
Memory sustaining supply voltage	VHD	$V_{DD}1$, $V_{DD}2$	RAM and register contents sustained in HOLD mode.		2.0			
High level input voltage	$V_{IH}(1)$	Ports 1, 2, 3, 7		3.3 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}(2)$	Ports 0		3.3 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}(3)$	CF1, CF2, $\overline{RES}$		3.3 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 3, 7		4.0 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
				3.3 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Ports 0		4.0 to 5.5	V_{SS}		$0.15V_{DD}+0.4$	
				3.3 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	CF1, CF2, $\overline{RES}$		3.3 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-1)	tCYC			3.3 to 5.5	0.142		200	µs
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	3.3 to 5.5	0.1		20	MHz
Oscillation frequency range (Note 2-2)	FmCF(1)	CF1, CF2	20MHz ceramic oscillation See Fig. 1.	3.3 to 5.5		20		
	FmCF(2)	CF1, CF2	10MHz ceramic oscillation See Fig. 1.	3.3 to 5.5		10		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	3.3 to 5.5		4		
	FmMRC		Internal High-speed RC oscillation. 1/2 frequency division ration. (RCCTD=0) (Note 2-3)	3.3 to 5.5	19.0	20.0	21.0	
	FmRC		Internal medium-speed RC oscillation	3.3 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation	3.3 to 5.5	15	30	60	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 1.	3.3 to 5.5		32.768		

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-2: See Tables 1 and 2 for the oscillation constants.

Note 2-3: When switching the system clock, allow an oscillation stabilization time of 100µs or longer after the high-speed RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	3.3 to 5.5			1	µA
	$I_{IH}(2)$	CF1, CF2	$V_{IN}=V_{DD}$	3.3 to 5.5			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	3.3 to 5.5	-1			
	$I_{IL}(2)$	CF1, CF2	$V_{IN}=V_{SS}$	3.3 to 5.5	-15			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 7	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.35mA	3.3 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$	Port 3	I_{OH}=-6mA	4.5 to 5.5	V_{DD}-1			
	$V_{OH}(4)$		I_{OH}=-1.4mA	3.3 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.4mA	3.3 to 5.5			0.4	
	$V_{OL}(3)$	Port 7	I_{OL}=1.4mA	3.3 to 5.5			0.4	
	$V_{OL}(4)$	P00, P01	I_{OL}=25mA	4.5 to 5.5			1.5	
	$V_{OL}(5)$		I_{OL}=4mA	3.3 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Port 7	$V_{OH}=0.9V_{DD}$ When Port 0 selected low-impedance pull-up.	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)	Port 0	$V_{OH}=0.9V_{DD}$ When Port 0 selected high-impedance pull-up.	3.3 to 5.5	100	210	400	
Hysteresis voltage	VHYS	Ports 1, 2, 3, 7 $\overline{RES}$	When Port 2 selected INT4.	3.3 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	3.3 to 5.5		10		pF

Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 5.	3.3 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 5.	3.3 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	3.3 to 5.5	0.05			µs
	Data hold time		thDI(1)				0.05			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-2)	3.3 to 5.5			(1/3)tCYC +0.08	
			tdD0(2)		• Synchronous 8-bit mode (Note 4-1-2)				1tCYC +0.08	
	Output clock		tdD0(3)		(Note 4-1-2)				(1/3)tCYC +0.08	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 5.

SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 5.	3.3 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 5.	3.3 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	3.3 to 5.5	0.05			µs
	Data hold time		thDI(2)				0.05			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 5.	3.3 to 5.5			(1/3)tCYC +0.08	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P21)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	3.3 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	3.3 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are nabled.	3.3 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	3.3 to 5.5	256			
	tPIL(5)	$\overline{RES}$	• Resetting is enabled.	3.3 to 5.5	200			µs

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = 0V$

10bits AD Converter Mode/Ta = -40°C to +85°C

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(AMP1O) AN9(AMP2O)		3.3 to 5.5		10		bit
Absolute accuracy	ET		(Note 6-1)	3.3 to 5.5			±16	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	3.3 to 5.5	8.5		59.5	µs
Analog input voltage range	VAIN			3.3 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.3 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.3 to 5.5	-1			

8bits AD Converter Mode/Ta = -40°C to +85°C

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(AMP1O) AN9(AMP2O)		3.3 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.3 to 5.5			±1.5	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	3.3 to 5.5	2.9		20	µs
Analog input voltage range	VAIN			3.3 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.3 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.3 to 5.5	-1			

Conversion time calculation formulas:

10bits AD Converter Mode: TCAD (Conversion time) = ((42/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD (Conversion time) = ((28/(AD division ratio))+2)× (1/3)×tCYC

External oscillation (FmCF)	Operating supply voltage range (V_{DD})	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)		AD conversion time (TCAD)	
				10bit AD	8bit AD	10bit AD	8bit AD
CF-20MHz	3.3V to 5.5V	1/1	150ns	1/4	1/2	8.5µs	2.9µs
CF-10MHz	3.3V to 5.5V	1/1	300ns	1/4	1/2	17µs	5.8µs
CF-4MHz	3.3V to 5.5V	1/1	750ns	1/4	1/2	42.5µs	14.5µs

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 10-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 10-bit conversion mode.

Power-on Reset (POR) Characteristics at Ta = -40°C to +85°C, $V_{SS}1=V_{SS}2=0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				Option selected voltage	min	typ	max	unit
POR release voltage	PORRL		• Select from option. (Note 7-1)	1.67V	1.55	1.67	1.79	V
				1.97V	1.85	1.97	2.09	
				2.07V	1.95	2.07	2.19	
				2.37V	2.25	2.37	2.49	
				2.57V	2.45	2.57	2.69	
				2.87V	2.75	2.87	2.99	
				3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	
Detection voltage unknown state	POUKS		• See Fig. 7. (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS		• Power supply rise time from 0V to 1.6V.				100	ms

Note7-1: The POR release level can be selected out of 8 levels only when the LVD reset function is disabled.

Note7-2: POR is in an unknown state before transistors start operation.

Low Voltage Detection Reset (LVD) Characteristics at Ta = -40°C to +85°C, $V_{SS}1=V_{SS}2=0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				Option selected voltage	min	typ	max	unit
LVD reset voltage (Note 8-2)	LVDET		• Select from option. (Note 8-1) (Note 8-3) • See Fig. 8.	1.91V	1.81	1.91	2.01	V
				2.01V	1.91	2.01	2.11	
				2.31V	2.21	2.31	2.41	
				2.51V	2.41	2.51	2.61	
				2.81V	2.71	2.81	2.91	
				3.79V	3.69	3.79	3.89	
				4.28V	4.18	4.28	4.38	
LVD hysteresys width	LVHYS			1.91V		55		mV
				2.01V		55		
				2.31V		55		
				2.51V		55		
				2.81V		60		
				3.79V		65		
				4.28V		65		
Detection voltage unknown state	LVUKS		• See Fig. 8. (Note 8-4)			0.7	0.95	V
Low voltage detection minimum width (Reply sensitivity)	TLVDW		• LVDET-0.5V • See Fig. 9.		0.2			ms

Note8-1: The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.

Note8-2: LVD reset voltage specification values do not include hysteresis voltage.

Note8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4: LVD is in an unknown state before transistors start operation.

Comparator, Operational Amplifiers Characteristics at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=0V$

Function	Parameter	Symbol	Pin/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
CMP1, 2	Input common-mode voltage (Note9-1)	VCMIN	CMP1IA, CMP1IB CMP2IA, CMP2IB		3.3 to 5.5	V_{SS}		V_{DD}-1.5V	V
	Offset voltage	VOFF(1)	CMP1IA, CMP1IB CMP2IA, CMP2IB	Input common-mode voltage range	3.3 to 5.5			20	mV
	CMP response speed	tCRT	CMP1O CMP2O	• Input common-mode voltage range • Input amplitude=100mV • Over drive=50mV	3.3 to 5.5		200		ns
AMP1, 2	AMP input voltage (Note9-1)	VAMIN	CMP1IA, CPM2IA		3.3 to 5.5	V_{SS}		V_{DD}-1.5V	V
	Input offset voltage	VOPOFF	CMP1IA, CMP1IB CMP2IA, CMP2IB	Input common-mode voltage range	3.3 to 5.5			20	mV
	Slew rate	SR	CMP1O CMP2O	50pF	5.0		3		V/µs
	Output current	Source	IoSource	CMP1IA,CMP1IB(+)=1V CMP2IA,CMP2IB(-)=0V CMP1O,CMP2O=V_{DD}-1.5V	5.0	2.5	3.5		mA
		Sink	IoSink	CMP1IA,CMP1IB(+)=0V CMP2IA,CMP2IB(-)=1V CMP1O,CMP2O=V_{DD}+0.5V	5.0	0.3	0.35		mA

Note9-1: When V_{DD}=5V, input voltage is effective from 0 to 3.5V.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 10-1) (Note 10-2)	IDDOP(1)	$V_{DD}1$, $V_{DD}2$	• FmCF=20MHz ceramic oscillation mode • System clock set to 20MHz side • All internal RC oscillation stopped. • 1/1 frequency division ratio	3.3 to 5.5		10	12.5	mA
	IDDOP(2)		• FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • All internal RC oscillation stopped. • 1/1 frequency division ratio	3.3 to 5.5		3	4.1	
	IDDOP(3)		• FsX'tal=32.768kHz crystal oscillation mode • Internal medium speed RC oscillation stopped. • System clock set to internal high speed RC oscillation (20MHz). • 1/1 frequency division ratio	3.3 to 5.5		9.2	11	
	IDDOP(4)		• FsX'tal=32.768kHz crystal oscillation mode • Internal high speed RC oscillation stopped. • System clock set to internal medium speed RC oscillation. • 1/2 frequency division ratio	3.3 to 5.5		0.5	0.7	
	IDDOP(5)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz crystal oscillation. • All internal RC oscillation stopped. • 1/1 frequency division ratio	3.3 to 5.5		32	74	µA
HALT mode consumption current (Note 10-1) (Note 10-2)	IDDHALT(1)	$V_{DD}1$, $V_{DD}2$	• HALT mode • FmCF=20MHz ceramic oscillation mode • System clock set to 20MHz side • All internal RC oscillation stopped. • 1/1 frequency division ratio	3.3 to 5.5		4.7	5.8	mA
	IDDHALT(2)		• HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • All internal RC oscillation stopped. • 1/1 frequency division ratio	3.3 to 5.5		1.5	2.3	
	IDDHALT(3)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal medium speed RC oscillation stopped. • System clock set to internal high speed RC oscillation (20MHz). • 1/1 frequency division ratio	3.3 to 5.5		4	5	
	IDDHALT(4)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal high speed RC oscillation stopped. • System clock set to internal medium speed RC oscillation. • 1/2 frequency division ratio	3.3 to 5.5		0.3	0.45	
	IDDHALT(5)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz crystal oscillation. • All internal RC oscillation stopped. • 1/1 frequency division ratio	3.3 to 5.5		16	60	µA

Note10-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note10-2: The consumption current values do not include operational current of LVD function if not specified.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HOLD mode consumption current (Note 10-1) (Note 10-2) (Note 10-3)	IDDHOLD(1)	$V_{DD}1$, $V_{DD}2$	HOLD mode • CF1=V_{DD} or open (External clock mode)	3.3 to 5.5		0.03	32	µA
	IDDHOLD(2)		HOLD mode • CF1=V_{DD} or open (External clock mode) • LVD option selected	3.3 to 5.5		3	35	

Note10-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.
Note10-2: The consumption current values do not include operational current of LVD function if not specified.
Note10-3: The amplifier / comparator circuit operates in the HOLD mode.

F-ROM Programming Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

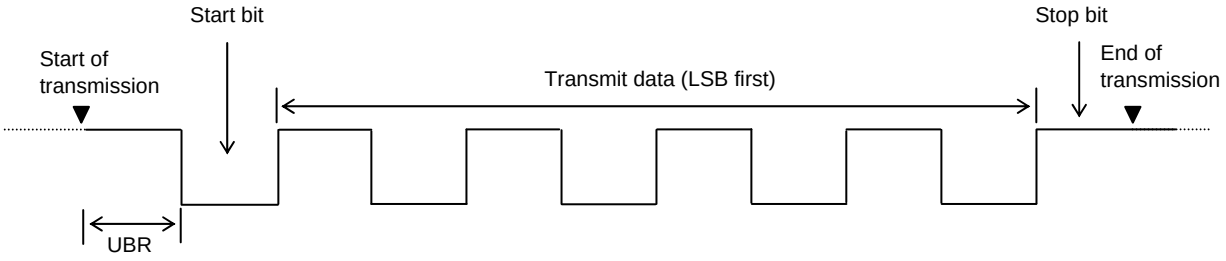
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$, $V_{DD}2$	• Only current of the flash block.	3.3 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing time	3.3 to 5.5		20	30	ms
	tFW(2)		• Programming time			40	60	µs

UART (Full Duplex) Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

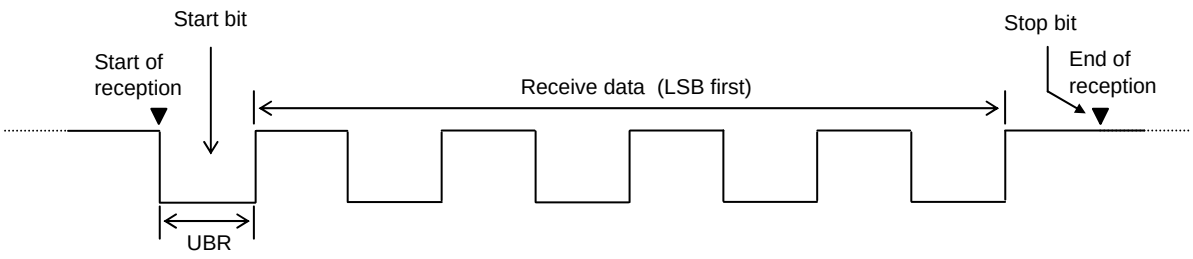
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	UTX(P16) URX(P17)		3.3 to 5.5	16/3		8192/3	tCYC

Data length : 7/8/9 bits (LSB first)
Stop bits : 1 bit (2-bit in continuous data transmission)
Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator
■MURATA

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
20MHz	SMD	CSTCE20M0G51-R0	(5)	(5)	Open	470	3.3 to 5.5	0.02		Internal C1,C2
	LEAD	CSTLS20M0G52-B0	(5)	(5)	Open	330	3.3 to 5.5	0.06		
10MHz	SMD	CSTCE10M0G52-R0	(10)	(10)	Open	470	3.3 to 5.5	0.02		
	LEAD	CSTLS10M0G53-B0	(15)	(15)	Open	680	3.3 to 5.5	0.02		
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	3.3 to 5.5	0.04		
	LEAD	CSTLS4M00G53-B0	(15)	(15)	Open	1.5k	3.3 to 5.5	0.03		

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 3).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator
■EPSON TOYOCOM

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [s]	max [s]	
32.768kHz	SMD	MC-306	8	8	Open	330k	3.3 to 5.5	1.0	4.0	Applicable CL value = 7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 3).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

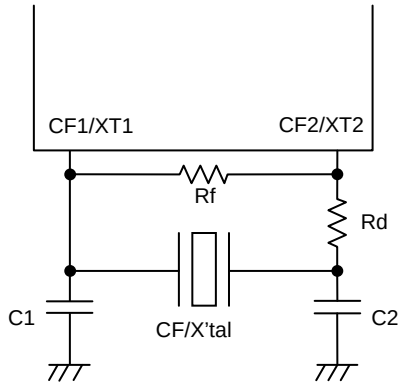


Figure 1 CF and XT Oscillator Circuit

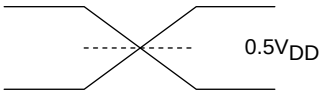
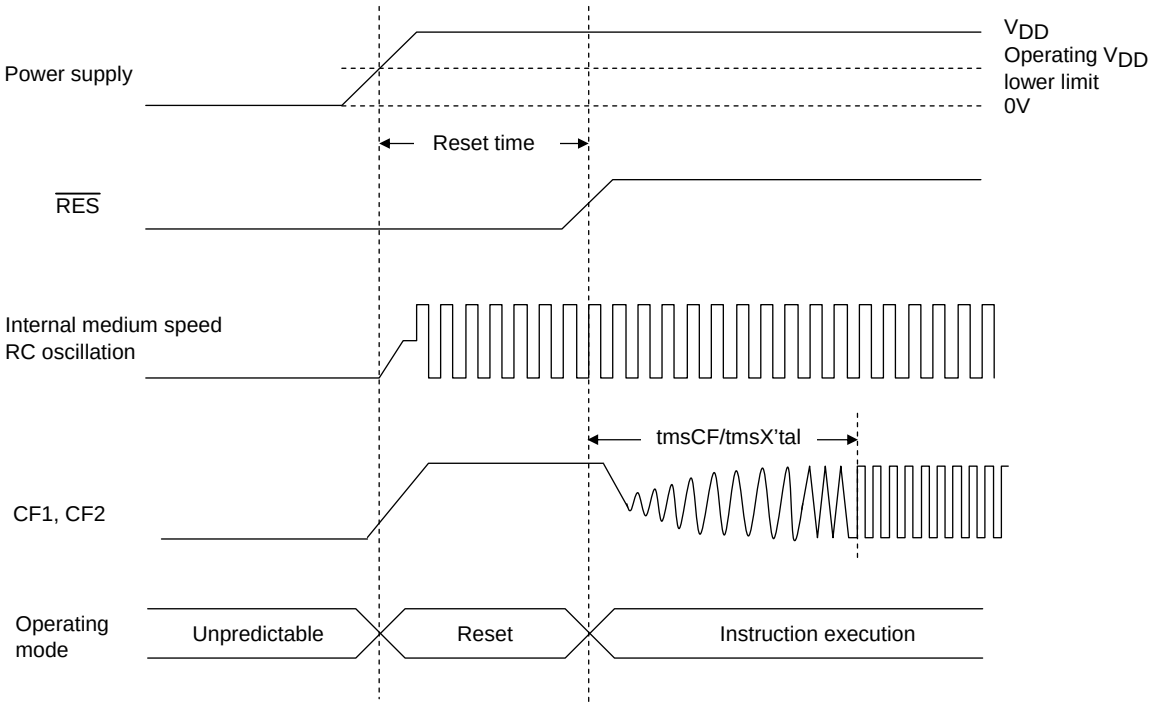
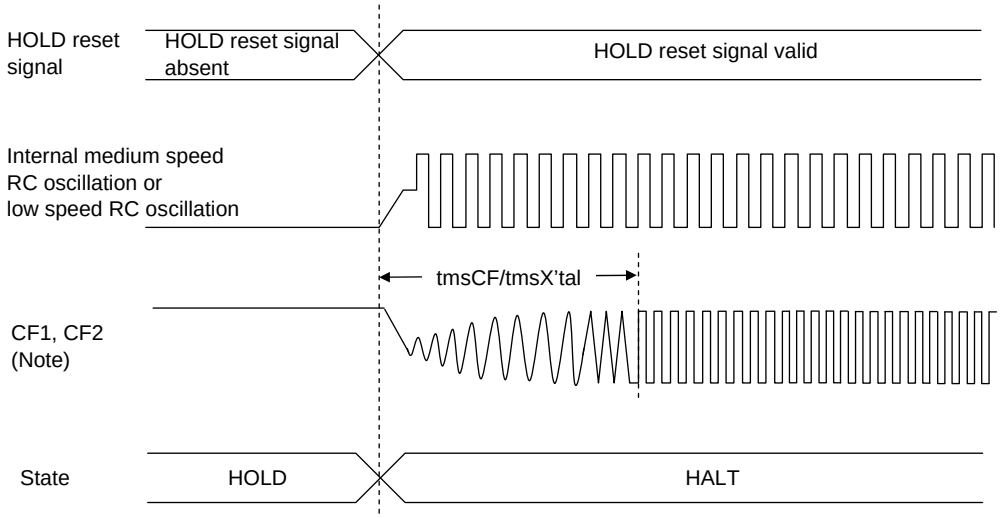


Figure 2 AC Timing Measurement Point



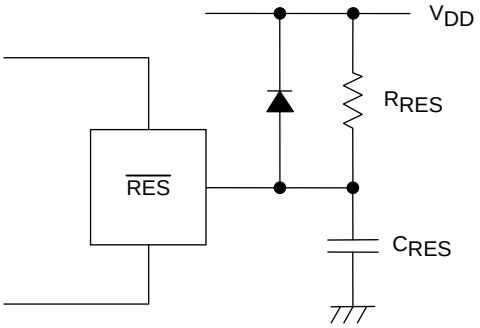
Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Note: External oscillation circuit is selected.

Figure 3 Oscillation Stabilization Times



Note:
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information.

Figure 4 Reset Circuit

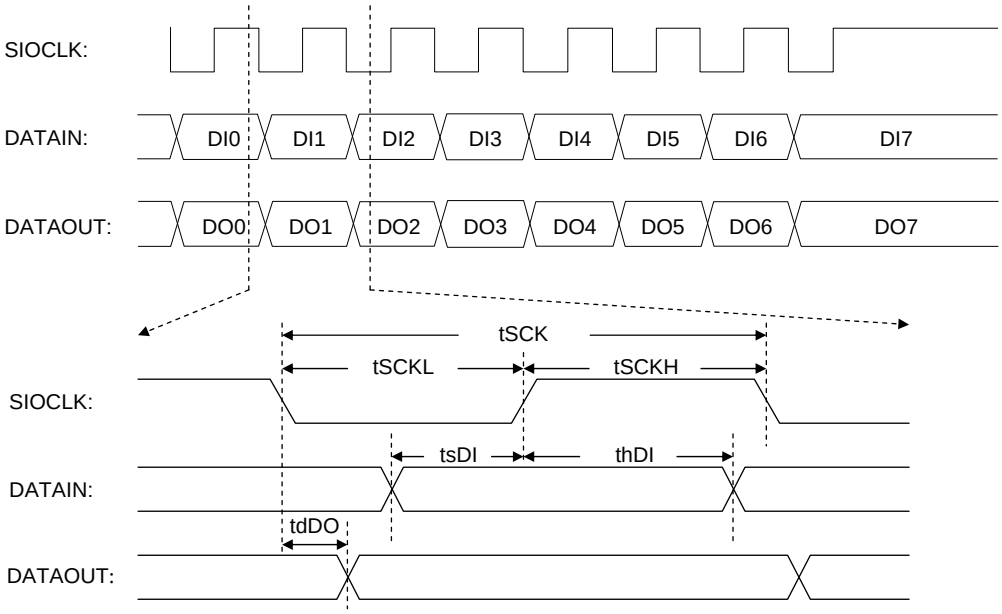


Figure 5 Serial I/O Output Waveforms

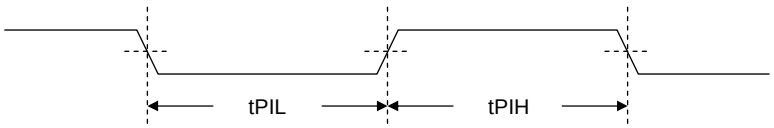


Figure 6 Pulse Input Timing Signal Waveform

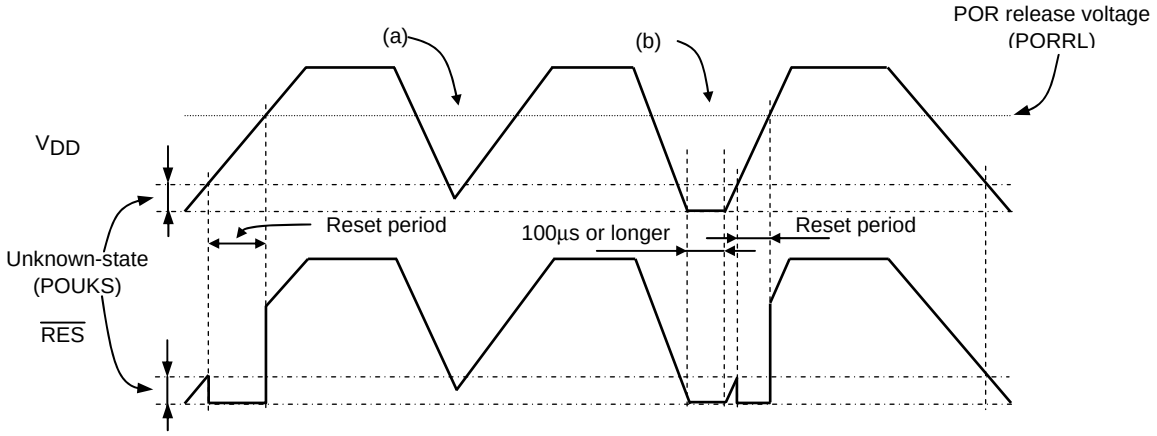


Figure 7 Waveform observed when only POR is used (LVD not used)
(RESET pin: Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

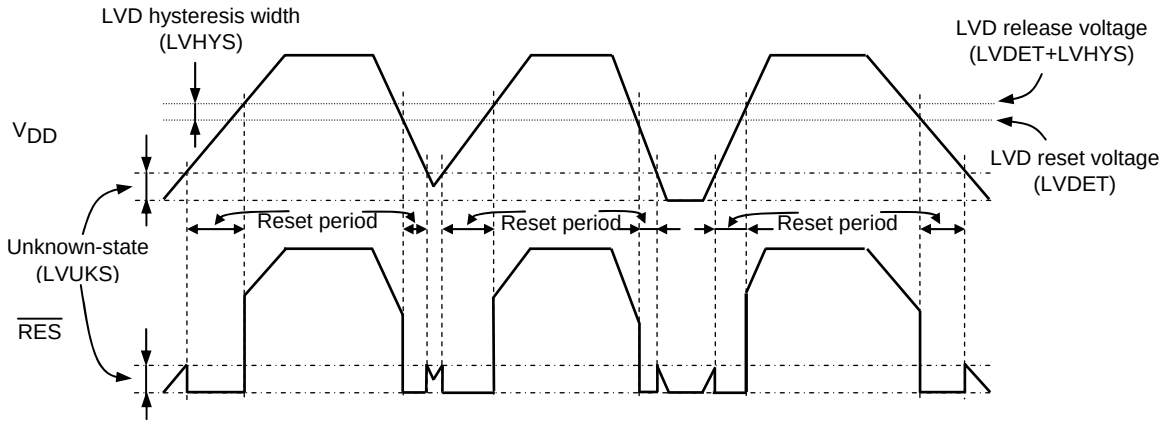


Figure 8 Waveform observed when both POR and LVD functions are used
(RESET pin: Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

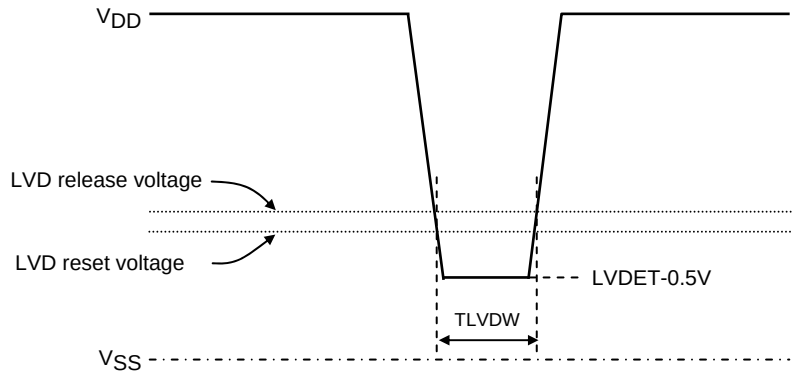


Figure 9 Low voltage detection minimum width
(Example of momentary power loss/Voltage variation waveform)