

SANYO Semiconductors **DATA SHEET**

LC87F1364A-

CMOS IC FROM 64K byte, RAM 1K byte on-chip

8-bit 1-chip Microcontroller with Low-speed USB

Overview

The SANYO LC87F1364A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 166ns, integrates on a single chip a number of hardware features such as 64K-byte flash ROM (onboard programmable), 1024-byte RAM, an on-chip debugger, a sophisticated 16-bit timers/counters (may be divided into 8-bit timers), 16-bit timers (may be divided into 8-bit timers or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmit/receive function), an asynchronous/synchronous SIO interface, a UART interface (full duplex), a USB (Low-Speed) interface, two 12-bit PWM channels, an 8-bit 9-channel AD converter, and a 29-source 10-vector address interrupt feature.

Features

- ■Flash ROM
 - Block-erasable in 128-byte units
 - 65536×8 bits
- ■Minimum Bus Cycle Time
 - 166ns (CF = 6MHz)

Note: The bus cycle time here refers to the ROM read speed.

- ■Minimum Instruction Cycle Time (tCYC)
 - 500ns (CF = 6MHz)
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SANYO Semiconductor Co., Ltd.

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■Ports

• I/O ports

Ports whose I/O direction can be designated in 1 bit units 9 (P1n, P70)

Ports whose I/O direction can be designated in 4 bit units 8 (P0n)

• USB ports 2 (D+, D-)

USB ports
 Dedicated oscillator ports
 Reset pins
 (XT1, XT2)
 (RES)

 \bullet Power pins 1 (V_{SS}1, V_{DD}1)

■Timers

• Timer 0: 16-bit timer/counter with a capture register.

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture registers) \times 2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture registers)

+ 8-bit counter (with an 8-bit capture register)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)

Mode 3: 16-bit counter (with a 16-bit capture register)

• Timer 1: 16-bit timer that supports PWM/toggle output capabilities)

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) \times 2 channels

Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels

Mode 2: 16-bit timer with an 8-bit prescaler (with toggle output)

(The lower-order 8 bits can be used as a timer with toggle output.)

Mode 3: 16-bit timer with an 8-bit prescaler (with toggle output)

(The lower-order 8 bits can be used as PWM.)

- Base timer
 - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
 - 2) Interrupts programmable in 5 different time schemes
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler
- Timer 7: 8-bit timer with a 6-bit prescaler

■SIO

- SIO0: Synchronous serial interface
 - 1) LSB first/MSB first mode selectable
 - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3tCYC)
 - 3) Automatic continuous data transmission (1 to 256 bits)
- SIO1: 8-bit asynchronous/synchronous serial interface

Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)

Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)

Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)

Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■Full Duplex UART

- UART1
 - 1) Data length: 7/8/9 bits selectable
 - 2) Stop bits: 1 bit (2 bits in continuous transmission mode)
 - 3) Baud rate: 16/3 to 8192/3 tCYC
- ■AD Converter: 8 bits × 9 channels
- ■PWM: Multifrequency 12-bit PWM × 2 channels

■USB Controller

- USB Specification rev. 1.1 (Low-Speed) compatible
- Supports a maximum of 2 user-defined endpoints.

En	dpoint	EP0	EP1	EP2
Transfer Tune	Control	enable	enable	-
Transfer Type	Interrupt	-	enable	enable
Max.	payload	8	8	8

■Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

■Interrupts

- 29 sources, 10 vector addresses
 - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/USB bus active
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	ТОН
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/USB bus reset/USB suspend/UART1 receive
8	0003BH	H or L	SIO1/USBERR/USBPOV/USBENP/USBNAK/ USBSTL/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/PWM0/PWM1/T4/T5

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- ■Subroutine Stack Levels: 512 levels (the stack is allocated in RAM.)
- ■High-speed Multiplication/Division Instructions

16 bits × 8 bits
24 bits × 16 bits
16 bits ÷ 8 bits
24 bits ÷ 16 bits
24 bits ÷ 16 bits
16 tCYC execution time)
25 tCYC execution time
26 tCYC execution time
27 tCYC execution time
28 tCYC execution time
29 tcYC execution time
20 tcYC execution time

■Oscillation Circuits

• RC oscillation circuit (internal): For system clock

CF oscillation circuit:
 Crystal oscillation circuit:
 PLL circuit (internal):
 For system clock, USB interface
 For system clock, USB interface

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The PLL base clock generator, CF, RC and crystal oscillators automatically stop operation.
 - 2) There are four ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the lower level.
 - (2) Setting at least one of the INT0, INT1, and INT2 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an bus active interrupt source established in the USB interface circuit
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
 - 1) The PLL base clock generator, CF and RC oscillator automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are five ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, and INT2 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established in the base timer circuit
 - (5) Having an bus active interrupt source established in the USB interface circuit

■Package Form

• MFP24S(300mil): Lead-free type

■Development Tools

• On-chip debugger: TCB87 type-A or TCB87 type-B + LC87F1364A

■Flash ROM Programming Boards

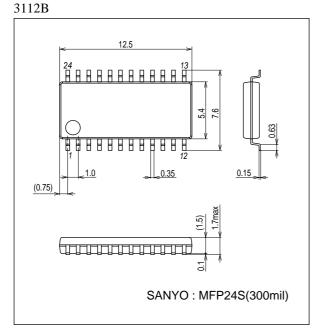
Package	Programming boards
MFP24S(300mil)	W87F5300M

■Recommended EPROM Programmer

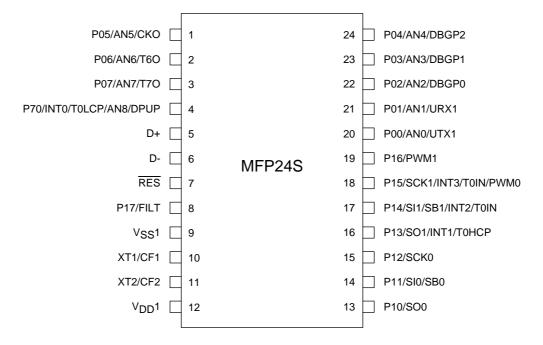
Maker	Model	Supported version	Device
Flash Support Group, Inc.	AF9708/AF9709/AF9709B	After 02.40	LC87F1364A
(Single)	(including product of Ando Electric Co.,Ltd)	Aitel 02.40	LC8/F1304A
SANYO	SKK(SANYO FWS)	Application Version: After 1.03 Chip Data Version: After 2.01	LC87F1364

Package Dimensions

unit: mm (typ)



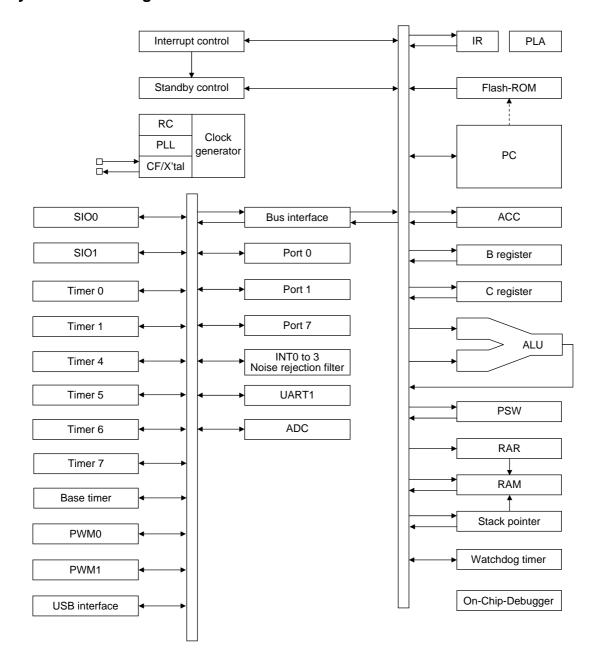
Pin Assignment



Top view

MFP	NAME
1	P05/AN5/CKO
2	P06/AN6/T6O
3	P07/AN7/T7O
4	P70/INT0/T0LCP/AN8/DPUP
5	D+
6	D-
7	RES
8	P17/FILT
9	V _{SS} 1
10	XT1/CF1
11	XT2/CF2
12	V _{DD} 1
13	P10/SO0
14	P11/SI0/SB0
15	P12/SCK0
16	P13/SO1/INT1/T0HCP
17	P14/SI1/SB1/INT2/T0IN
18	P15/SCK1/INT3/T0IN/PWM0
19	P16/PWM1
20	P00/AN0/UTX1
21	P01/AN1/URX1
22	P02/AN2/DBGP0
23	P03/AN3/DBGP1
24	P04/AN4/DBGP2

System Block Diagram



Pin Description

Pin Name	I/O			Des	cription			Option	
V _{SS} 1	-	- power supply p	in					No	
V _{DD} 1	-	+ power supply p	+ power supply pin						
Port 0	I/O	• 8-bit I/O port							
P00 to P07	- "	I/O specifiable i	n 4 bit units					Yes	
1 00 10 1 07		Pull-up resistors		on and off in 4 b	oit units.				
		HOLD reset inp							
		Port 0 interrupt	input						
		• Pin functions							
		P00: AN0 (ADC	input)/UART1	transmit					
		P01: AN1 (ADC	input)/UART1	receive					
		P02: AN2 (ADC	input)/For On-	Chip-Debugger					
		P03: AN3 (ADC	input)/For On-	Chip-Debugger					
		P04: AN4 (ADC	input)/For On-	Chip-Debugger					
		P05: AN5 (ADC		=					
		P06: AN6 (ADC							
		P07: AN7 (ADC	input)/timer 7 t	oggle outputs					
Port 1	I/O	• 8-bit I/O port	410 0					Yes	
P10 to P17		I/O specifiable i							
		Pull-up resistor: Dia functions	s can be turned	on and off in 1 t	oit units.				
		Pin functions P10: SIO0 data	output						
		P10: SIO0 data P11: SIO0 data	•						
			•						
			P12: SIO0 clock I/O P13: SIO1 data output/INT1 input/HOLD reset input/timer OH capture input						
					reset input/timer	•	mer OL canture		
			input bus it Offi	112 IIIput 110EB	reset input times	o event inputti	ner OE captare		
		input P15: SIO1 clock I/O/INT3 input (with noise filter)/timer 0 event input/timer OH capture input							
		/PWM 0 o	· ·	(,,	par	pta.opat		
		P16: Timer 1 PWML output/PWM 1 output							
		P17: Timer 1 PWMH output/beeper output/Internal PLL filter pin							
		Interrupt acknow							
			Dist	E.W.	Rising &				
			Rising	Falling	Falling	H level	L level		
		INT1	enable	enable	disable	enable	enable		
		INT2	enable	enable	enable	disable	disable		
		INT3	enable	enable	enable	disable	disable		
Port 7	I/O	• 1 bit I/O port						No	
	- 1/0	1-bit I/O portI/O specifiable i	n 1 hit unite					NO	
P70		Pull-up resistors		on and off in 1 h	nit units				
		Shared pins	o dan bo tamba	on and on in the	nt dinto.				
			/HOLD reset in	out/timer 0L capt	ure input/watchd	og timer output/	AN8 (ADC input) /		
			oull-up resistor		are input materia	ogo. oatpat.	(* 1.20pat) /		
		Interrupt acknow	•						
					Rising &				
			Rising	Falling	Falling	H level	L level		
		INT0	enable	enable	disable	enable	enable		
RES	1	Reset pin		rool II				No	
XT1	1	Ceramic oscillato						No	
XT2	I/O	Ceramic oscillato		68kHz crystal os	cillator output pir	1		No	
D-	1/0	USB data I/O pin						No	
D+	I/O	USB data I/O pin	D+					No	

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
XT1	-	No	Input only	No
XT2	-	No	32.768kHz crystal oscillator output	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4 bit units (P00 to 03, P04 to 07).

USB Reference Power Option

When a voltage 4.5V to 5.5V is supplied to $V_{DD}1$ and the internal USB reference voltage circuit is activated, the H output level of the USB Port is 3.0V to 3.6V (the H output level of the ports except the USB Port is the $V_{DD}1$ voltage level, however). The active/inactive state of the reference voltage circuit can be determined by option settings.

According to the voltage to be supplied to V_{DD}1, make option settings as shown below.

V[OD1 voltage (V)		3.0 to 3.6		
Option setting	USB Regulator	USE	USE	USE	NONUSE
	USB Regulator in HOLD mode	USE	NONUSE	NONUSE	NONUSE
	USB Regulator in HALT mode	USE	NONUSE	USE	NONUSE
Reference voltage circuit state	Normal state	active	active	active	inactive
	HOLD mode	active	inactive	inactive	inactive
	HALT mode	active	inactive	active	inactive
		(1)	(2)	(3)	(4)

- When the USB reference voltage circuit is made inactive, the H output level of the USB Port becomes the V_{DD}1 voltage level.
- Use the setting (2) or (3) to make the reference voltage circuit inactive in HOLD or HALT mode.
- \bullet When the reference voltage circuit is activated, the current drain increases by approximately $100\mu A$ compared with when the reference voltage circuit is inactive.

Absolute Maximum Ratings at $Ta = 25^{\circ}C$, $V_{SS}1 = 0V$

Parameter		Cumbal	Pin/Remarks	Conditions		Specification			
	Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	D[V] min typ max		unit	
Maximum supply V _{DD} max V _{DD} 1 V _{DD} 1 voltage		V _{DD} 1		-0.3		+6.5			
Inp	ut voltage	V _I (1)	XT1, XT2			-0.3		V _{DD} +0.3	V
	ut/output tage	V _{IO} (1)	Ports 0, 1, 7			-0.3		V _{DD} +0.3	
ent	Peak output current	IOPH(1)	Ports 0, 1	When CMOS output type is selected Per 1 applicable pin		-10			
Surre		IOPH(2)	PWM0, PWM1	Per 1 applicable pin		-20			
High level output current	Average output current (Note 2)	IOMH(1)	Ports 0, 1	When CMOS output type is selected Per 1 applicable pin		-7.5			
jh le		IOMH(2)	PWM0, PWM1	Per 1 applicable pin		-15			
Hi	Total output current	ΣΙΟΑΗ(1)	Ports 0, 1 PWM0, PWM1 D+, D-	Total of all applicable pins		-50			mA
rent	Peak output current	IOPL(1)	P00 to P05 Ports 1, P70 PWM0, PWM1	Per 1 applicable pin				20	
t cur		IOPL(2)	P06, 07	Per 1 applicable pin				30	
Low level output current	Average output current (Note 2)	IOML(1)	P00 to P05 Ports 1, P70 PWM0, PWM1	Per 1 applicable pin				15	
νo		IOML(2)	P06, 07	Per 1 applicable pin				20	
_	Total output current	ΣIOAL(1)	Ports 0, 1, P70 PWM0, PWM1 D+, D-	Total of all applicable pins				75	
	owable power sipation	Pd max	MFP24S	Ta=-20 to +70°C					mW
	erating ambient mperature	Topr				-20		+70	°C
	rage ambient nperature	Tstg				-55		+125	

Note 2: The mean output current is a mean value measured over 100ms.

Allowable Operating Conditions at $Ta = -20^{\circ}C$ to $+70^{\circ}C,~V_{SS}1 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions			Specific	ation	
Farameter	Symbol	FIII/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Operating supply voltage	V _{DD} (1)	V _{DD} 1	0.490µs ≤ tCYC ≤ 200µs Except for onboard programming (Note 3)		2.5		5.5	
	V _{DD} (2)		0.490µs ≤ tCYC ≤ 200µs internal PLL oscillation		4.5		5.5	
Memory sustaining supply voltage	VHD	V _{DD} 1	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	V _{IH} (1)	Port 1 P70 port input /interrupt side		2.5 to 5.5	0.3V _{DD} +0.7		V_{DD}	
	V _{IH} (2)	Port 70 watchdog timer side		2.5 to 5.5	0.9V _{DD}		V_{DD}	V
	V _{IH} (3)	XT1, XT2, RES		2.5 to 5.5	0.75V _{DD}		V_{DD}	
Low level input voltage	V _{IL} (1)	Port 1 P70 port input		4.0 to 5.5	V _{SS}		0.1V _{DD} +0.4	
		/interrupt side		2.5 to 4.0	V _{SS}		0.2V _{DD}	
	V _{IL} (2)	Port 0		4.0 to 5.5	V _{SS}		0.15V _{DD} +0.4	
				2.5 to 4.0	V _{SS}		0.2V _{DD}	
	V _{IL} (3)	Port 70 watchdog timer side		2.5 to 5.5	V _{SS}		0.8V _{DD} -1.0	
	V _{IL} (4)	XT1, XT2, RES		2.5 to 5.5	V _{SS}		0.25V _{DD}	
Instruction cycle time (Note 4)	tCYC			2.5 to 5.5	0.490		200	μs
External system clock frequency	FEXCF(1)	XT1	XT2 pin open System clock frequency division ratio=1/1 External system clock duty =50±5%	2.5 to 5.5	0.1		6	MHz
			XT2 pin open System clock frequency division ratio=1/2	2.5 to 5.5	0.1		12	
Oscillation frequency	FmCF	XT1, XT2	6MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		6		MHz
range	FmRC		Internal RC oscillation	2.5 to 5.5	0.3	1.0	2.0	
(Note 5)	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.5 to 5.5		32.768		kHz

Note 3: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 4: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 5: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at $Ta = -20^{\circ}C$ to $+70^{\circ}C$, $V_{SS}1 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions			Specifica	ation	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High level input current	I _{IH} (1)	Ports 0, 1 Port 70 RES	Output disabled Pull-up resistor off VIN=VDD (Including output Tr's off leakage current)	2.5 to 5.5			1	
	I _{IH} (2)	XT1, XT2	V _{IN} =V _{DD}	2.5 to 5.5			1	,
Low level input current	I _{IL} (1)	Ports 0, 1 Port 70 RES	Output disabled Pull-up resistor off VIN=VSS (Including output Tr's off leakage current)	2.5 to 5.5	-1			μА
	I _{IL} (2)	XT1, XT2	V _{IN} =V _{SS}	2.5 to 5.5	-1			
High level output	V _{OH} (1)	Ports 0, 1	I _{OH} =-1mA	4.5 to 5.5	V _{DD} -1			
voltage	V _{OH} (2)		I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (3)		I _{OH} =-0.2mA	2.5 to 5.5	V _{DD} -0.4			
	V _{OH} (4)	PWM0, PWM1	I _{OH} =-10mA	4.5 to 5.5	V _{DD} -1.5			
	V _{OH} (5)	P05 (CK0 when	I _{OH} =-1.6mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (6)	using system clock output function)	I _{OH} =-1mA	2.5 to 5.5	V _{DD} -0.4			V
Low level output	V _{OL} (1)	Ports 0, 1	I _{OL} =10mA	4.5 to 5.5			1.5	
voltage	V _{OL} (2)	Port 70	I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (3)	PWM0, PWM1	I _{OL} =1mA	2.5 to 5.5			0.4	
	V _{OL} (4)	P06, P07	I _{OL} =30mA	4.5 to 5.5			1.5	
	V _{OL} (5)		I _{OL} =5mA	3.0 to 5.5			0.4	
	V _{OL} (6)		I _{OL} =2.5mA	2.5 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1	V _{OH} =0.9V _{DD}	4.5 to 5.5	15	35	80	
	Rpu(2)	Port 70		2.5 to 5.5	18	50	150	kΩ
Hysteresis voltage	VHYS	RES Port 1 Port 70		2.5 to 5.5		0.1V _{DD}		٧
Pin capacitance	СР	All pins	For pins other than that under test: VIN=VSS F=1MHz Ta=25°C	2.5 to 5.5		10		pF

Serial I/O Characteristics at Ta = -20°C to +70°C, $V_{SS}1 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

) aramatar	Cumbal	Pin	Conditions			Specif	ication	
	F	Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
		Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.		2			
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
	Input clock		tSCKHA(1a)		Continuous data transmission/reception mode USB is not in use simultaneous. See Fig. 6. (Note 4-1-2)	2.7 to 5.5	4			tCYC
lock			tSCKHA(1b)		Continuous data transmission /reception mode USB is in use simultaneous. See Fig.6. (Note 4-1-2)		7			
Serial clock		Frequency	tSCK(2)	SCK0(P12)	CMOS output selected See Fig.6.		4/3			
		Low level pulse width	tSCKL(2)					1/2		tSCK
		High level pulse width	tSCKH(2)					1/2		100.1
	Output clock		tSCKHA(2a)		Continuous data transmission /reception mode USB is not in use simultaneous. CMOS output selected See Fig.6.	2.7 to 5.5	tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
			tSCKHA(2b)		Continuous data transmission /reception mode USB is in use simultaneous. CMOS output selected See Fig.6.		tSCKH(2) +2tCYC		tSCKH(2) +(19/3) tCYC	
erial input	Da	ta setup time	tsDI(1)	SB0(P11), SI0(P11)	Must be specified with respect to rising edge of SIOCLK. See Fig.6.	2.7 to 5.5	0.03			
Serial	Da	ta hold time	thDI(1)			2.7 to 5.5	0.03			
	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	Continuous data transmission /reception mode (Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	μs
Serial output	lnp		tdD0(2)		Synchronous 8-bit mode (Note 4-1-3)	2.7 to 5.5			1tCYC +0.05	
Serial	Output clock		tdD0(3)		(Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig.6.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIORUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

	-	Parameter	Cumbal	Pin	CondiPtions			Specif	ication	
	ŀ	Parameter	Symbol	/Remarks	CondiPtions	V _{DD} [V]	min	typ	max	unit
	ķ	Frequency	requency tSCK(3) SCK1(P15) See Fig.6.			2				
	Input clock	Low level pulse width	tSCKL(3)			2.7 to 5.5	1			
Slock		High level pulse width	tSCKH(3)				1			tCYC
Serial clock	×	Frequency	tSCK(4)	SCK1(P15)	CMOS output selected See Fig.6.		2			
	Output clock	Low level pulse width	tSCKL(4)			2.7 to 5.5		1/2		
	Oui	High level pulse width	0 ()							tSCK
Serial input	Da	ta setup time	tsDI(2)	SB1(P14), SI1(P14)	Must be specified with respect to rising edge of SIOCLK. See Fig.6.	2.7 to 5.5	0.03			
Serial	Da	ta hold time	thDI(2)			2.7 to 5.5	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig.6.	2.7 to 5.5			(1/3)tCYC +0.05	μѕ

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -20°C to +70°C, $V_{SS}1 = 0V$

Parameter	Symbol Pin/Remarks		Conditions		Specification					
Farameter			Conditions	V _{DD} [V]	min	typ	max	unit		
High/low level pulse width	tP1H(1) tP1L(1)	INT0(P70), INT1(P13), INT2(P14),	Interrupt source flag can be set. Event inputs for timer 0 or 1 are enabled.	2.5 to 5.5	1					
	tPIH(2) tPIL(2)	INT3(P15) when noise filter time constant is 1/1	Interrupt source flag can be set. Event inputs for timer 0 are enabled.	2.5 to 5.5	2			40.70		
	tPIH(3) tPIL(3)	INT3(P15) when noise filter time constant is 1/32	Interrupt source flag can be set. Event inputs for timer 0 are enabled.	2.5 to 5.5	64			tCYC		
	tPIH(4) INT3(P15) when • Interrupt source flag can be set.		2.5 to 5.5	256						
	tPIL(5)	RES	Resetting is enabled.	2.5 to 5.5	200			μs		

AD Converter Characteristics at $Ta = -20^{\circ}C$ to $+70^{\circ}C$, $V_{SS}1 = 0V$

D	Symbol	Dia /Damanda	O and distance		Specification			
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P00) to		3.0 to 5.5		8		bit
Absolute accuracy	ET	AN7(P07), AN8(P70)	(Note 6)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time = 32×tCYC (when ADCR2=0) (Note 7)	4.5 to 5.5	15.68 (tCYC= 0.49μs)		97.92 (tCYC= 3.06μs)	
				3.0 to 5.5	31.36 (tCYC= 0.98μs)		97.92 (tCYC= 3.06μs)	
			AD conversion time = 64×tCYC (when ADCR2=1) (Note 7)	4.5 to 5.5	31.36 (tCYC= 0. 49μs)		97.92 (tCYC= 1.53μs)	μs
				3.0 to 5.5	31.36 (tCYC= 0. 49μs)		97.92 (tCYC= 1.53μs)	
Analog input voltage range	VAIN			3.0 to 5.5	V _{SS}		V _{DD}	V
Analog port	IAINH]	VAIN=V _{DD}	3.0 to 5.5			1	
input current	IAINL	1	VAIN=V _{SS}	3.0 to 5.5	-1			μΑ

Note 6: The quantization error $(\pm 1/2LSB)$ is excluded from the absolute accuracy value.

Note 7: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

Consumption Current Characteristics at Ta = -20 °C to +70 °C, $V_{SS}1 = 0V$

Parameter	Symbol	Pin	Conditions			Specif	ication	
Farameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	Max	unit
Normal mode consumption	IDDOP(1)	V _{DD} 1	FmCF=6MHz ceramic oscillation mode System clock set to 6MHz side	4.5 to 5.5		5.3	13	
current (Note 8)	IDDOP(2)		Internal RC oscillation stopped 1/1 frequency division ration	2.5 to 4.5		3.5	9.6	
	IDDOP(3)		FsX'tal=32.768kHz crystal oscillation mode System clock set to PLL clock side Internal RC oscillation stopped 1/1 frequency division ration	4.5 to 5.5		6.7	17	mA
	IDDOP(4)		FsX'tal=32.768kHz crystal oscillation mode System clock set to internal RC oscillation	4.5 to 5.5		0.67	3.1	
	IDDOP(5)		Internal PLL oscillation stopped 1/2 frequency division ration	2.5 to 4.5		0.43	2.3	
	IDDOP(6)		FsX'tal=32.768kHz crystal oscillation mode System clock set to 32.768kHz side Internal RC oscillation stopped	4.5 to 5.5		120	380	μА
	IDDOP(7)		Internal PLL oscillation stopped Internal PLL oscillation stopped 1/2 frequency division ration	2.5 to 4.5		79	290	μΛ
HALT mode consumption	IDDHALT(1)		HALT mode FmCF=6MHz ceramic scillation mode	4.5 to 5.5		2.0	5.4	
current (Note 8)	IDDHALT(2)		System clock set to 6MHz side Internal RC oscillation stopped 1/1 frequency division ration	2.5 to 4.5		1.2	3.6	
	IDDHALT(3)		HALT mode FsX'tal=32.768kHz crystal oscillation mode System clock set to PLL clock side Internal RC oscillation stopped 1/1 frequency division ration			3.6	9.6	mA
	IDDHALT(4)		HALT mode FsX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		0.33	1.6	
	IDDHALT(5)	-	System clock set to internal RC oscillation Internal PLL oscillation stopped 1/2 frequency division ration	2.5 to 4.5		0.19	1.1	
	IDDHALT(6)		HALT mode FsX'tal=32.768kHz crystal oscillation mode System clock set to 32.768kHz side	4.5 to 5.5		30	130	
	IDDHALT(7)		Internal RC oscillation stopped Internal PLL oscillation stopped 1/2 frequency division ration			12	73	
HOLD mode	IDDHOLD(1)		HOLD mode	4.5 to 5.5		0.04	13	μΑ
consumption current	IDDHOLD(2)	1	• XT1=V _{DD} or open (External clock mode)			0.02	9.8	
Timer HOLD mode	IDDHOLD(3)		Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		27	120	
consumption current	IDDHOLD(4)			2.5 to 4.5		9.6	66	

Note 8: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

USB Characteristics and Timing at Ta = -20 °C to +70 °C, $V_{SS}1 = 0V$

Dozomotor	Parameter Symbol Conditions		Specification				
Parameter	Symbol	min typ		typ	max	unit	
High level output	VOH(USB)	• 15kΩ±5% to GND	2.8		3.6	٧	
Low level output	V _{OL}	• 1.5kΩ±5% to 3.6V			0.3	V	
Output signal crossover voltage	VCRS		1.3		2.0	V	
Differential input sensitivity	V _{DI}	• (D+)-(D-)	0.2			V	
Differential input common mode range	Vсм		0.8		2.5	V	
High level input	V _{IH(USB)}		2.0			٧	
Low level input	V _{IL(USB)}				0.8	V	
USB data rise time	t _R		75		300	ns	
USB data fall time	tF		75		300	ns	
Rise/fall time	t _{RFM}	• t _R /t _F	80		125	%	

F-ROM Write Characteristics at $Ta = +10^{\circ}C$ to $+55^{\circ}C$, $V_{SS}1 = 0V$

				. ~~				
Doromotor	Cumbal	Din	Conditions			Specifica	ation	
Parameter	ameter Symbol Pin		Conditions V _{DD} [V]		min	typ	max	unit
Onboard programming current	IDDFW(1)	V _{DD} 1	128-byte programming Erasing current included	3.0 to 5.5		25	40	mA
Programming time	tFW(1)		128-byte programming Erasing current included Time for setting up 128-byte data excluded.	3.0 to 5.5		22.5	45	mS

Characteristics of a Sample External Clock Oscillation Circuit

Given below are the characteristics of a sample external clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample External Clock Oscillator Circuit with a Crystal Oscillator

Nominal	Vendor			Circuit (Constant		Operating Voltage		lation tion Time	Develo	
Frequency	Name	Oscillator Name	C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]	Range [V]	typ [s]	max [s]	Remarks	
32.768kHz	EPSON TOYOCOM	MC-306	22	22	Open	820k	2.5 to 5.5	1.3	3	Applicable CL value=12.5pF	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

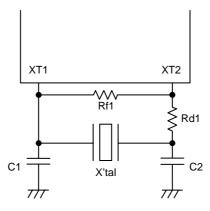


Figure 1 Crystal Oscillation Circuit

Table 2 Characteristics of a Sample External Clock Oscillator Circuit with a CF Oscillator

Nominal	Vendor	endor Oscillator Name		Circuit (Constant		Operating Voltage		lation tion Time	Damada
Frequency	Name	Oscillator Name	C3	C4	Rf2	Rd2	Range	typ	max	Remarks
			[pF]	[pF]	$[\Omega]$	$[\Omega]$	[V]	[ms]	[ms]	
6MHz	MURATA	CSTCR6M00G15***-R0	(39)	(39)	Open	1k	2.5 to 5.5	0.1	0.5	Built in C3, C4

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

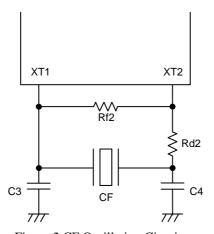
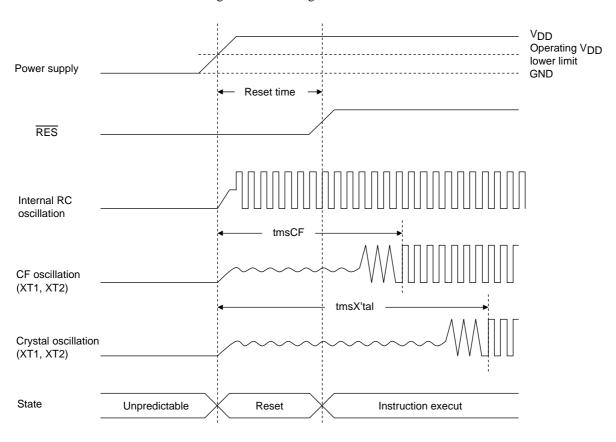


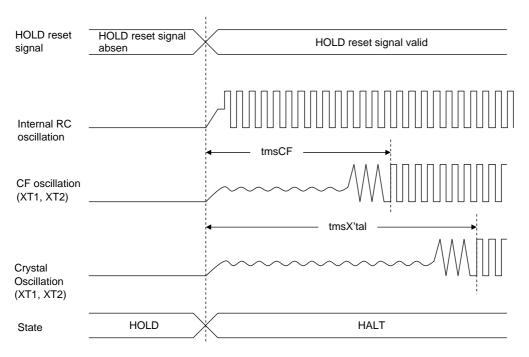
Figure 2 CF Oscillation Circuit



Figure 3 AC Timing Measurement Point

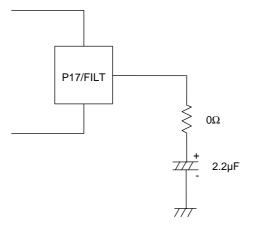


Reset Time and Oscillation Stabilization Time



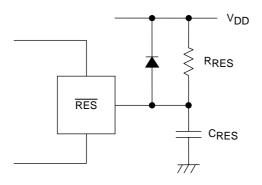
HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



When using the internal PLL circuit to generate the 6MHz clock for USB or system clock, it is necessary to connect a filter circuit such as that shown to the left to the P17/FILT pin..

Figure 5 Filter Circuit for the Internal PLL Circuit



Note:

Determine the value of CRES and RRES so that the reset signal is present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 6 Reset Circuit

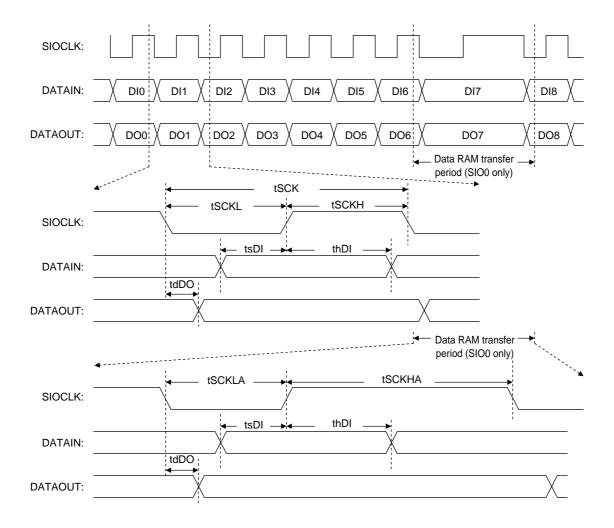


Figure 7 Serial Input/Output Waveforms

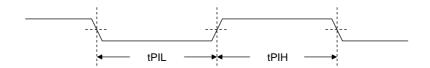


Figure 8 Pulse Input Timing Signal Waveform

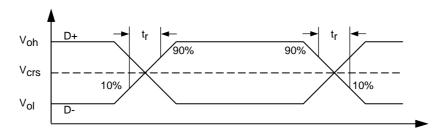


Figure 9 USB Data Signal Timing and Voltage Level

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