



SANYO Semiconductors

DATA SHEET

LC87F1D64A

CMOS IC

FROM 64K byte, RAM 4K byte on-chip

8-bit 1-chip Microcontroller with Full-Speed USB

Overview

The SANYO LC87F1D64A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 62.5ns, integrates on a single chip a number of hardware features such as 64K-byte flash ROM (onboard programmable), 4096-byte RAM, an on-chip debugger, a sophisticated 16-bit timers/counters (may be divided into 8-bit timers), 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), two 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, two synchronous SIO interface (with automatic block transmit/ receive function), an asynchronous/synchronous SIO interface, a UART interface (full duplex), a Full-Speed USB interface (function controller), 12-channel 12-bit A/D converter with 12-/8-bit resolution selector, two 12-bit PWM channels, a system clock frequency divider, an infrared remote control receiver circuit, and a 30-source 10-vector address interrupt feature.

Features

■Flash ROM

- Capable of on-board-programming with wide range, 3.0 to 5.5V, of voltage source.
- Block-erasable in 128 byte units
- Writes data in 2-byte units
- 65536 × 8 bits

■RAM

- 4096 × 9 bits

■Minimum Bus Cycle

- 62.5ns (CF=16MHz)

Note: The bus cycle time here refers to the ROM read speed.

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SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LC87F1D64A

■ Minimum Instruction Cycle Time

- 188ns (CF=16MHz)

■ Ports

- I/O ports

Ports whose I/O direction can be designated in 1 bit units 28 (P10 to P17, P20 to P27, P30 to P34, P70 to P73, PWM0, PWM1, XT2)

Ports whose I/O direction can be designated in 4 bit units 8 (P00 to P07)

- USB ports 2 (D+, D-)
- Dedicated oscillator ports 2 (CF1, CF2)
- Input-only port (also used for oscillation) 1 (XT1)
- Reset pins 1 (RES)
- Power pins 6 (VSS1 to 3, VDD1 to 3)

■ Timers

- Timer 0: 16-bit timer/counter with a capture register.

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)

Mode 3: 16-bit counter (with a 16-bit capture register)

- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)

Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels

Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)

Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)

- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)

- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)

- Base timer

1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.

2) Interrupts programmable in 5 different time schemes

■ SIO

- SIO0: Synchronous serial interface

1) LSB first/MSB first mode selectable

2) Transfer clock cycle: 4/3 to 512/3 tCYC

3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)

- SIO1: 8-bit asynchronous/synchronous serial interface

Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)

Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)

Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)

Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

- SIO4: Synchronous serial interface

1) LSB first/MSB first mode selectable

2) Transfer clock cycle: 4/3 to 1020/3 tCYC

3) Automatic continuous data transmission (1 to 4096 bytes, specifiable in 1 byte units, suspension and resumption of data transmission possible in 1 byte or 2 bytes units)

4) Auto-start-on-falling-edge function

5) Clock polarity selectable

6) CRC16 calculator circuit built in

■ Full Duplex UART

- UART1
 - 1) Data length: 7/8/9 bits selectable
 - 2) Stop bits: 1 bit (2 bits in continuous transmission mode)
 - 3) Baud rate: 16/3 to 8192/3 tCYC
- UART2
 - 1) Data length: 7/8/9 bits selectable
 - 2) Stop bits: 1 bit (2 bits in continuous transmission mode)
 - 3) Baud rate: 16/3 to 8192/3 tCYC

■ AD Converter: 12 bits × 12 channels

- 12/8 bits AD converter resolution selectable

■ PWM: Multifrequency 12-bit PWM × 2 channels

■ Infrared Remote Control Receiver Circuit

- 1) Noise reduction function
(noise filter time constant: Approx. 120μs, when the 32.768kHz crystal oscillator is selected as the reference voltage source.)
- 2) Supports data encoding systems such as PPM (Pulse Position Modulation) and Manchester encoding
- 3) X'tal HOLD mode release function

■ USB Interface (function controller)

- Compliant with USB 2.0 Full-Speed
- Supports a maximum of 4 user-defined endpoints.

Endpoint		EP0	EP1	EP2	EP3	EP4
Transfer Type	Control	○	-	-	-	-
	Bulk	-	○	○	○	○
	Interrupt	-	○	○	○	○
	Isochronous	-	○	○	○	○
Max. payload		64	64	64	64	64

■ Watchdog Timer

- External RC watchdog timer
 - 1) Interrupt and reset signals selectable
- Internal counter watchdog timer
 - 1) Generates an internal reset signal on overflow occurring in a timer that runs on a dedicated low-speed RC oscillator clock (30kHz).
 - 2) Three operating modes are selectable: continues counting, stops counting, or retains count when the CPU

■ Clock Output Function

- 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

■ Interrupts

- 30 sources, 10 vector addresses
 - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/USB bus active/remote control receiver
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/USB bus reset/USB suspend/UART1 receive/UART2 receive
8	0003BH	H or L	SIO1/USB endpoint/USB-SOF/SIO4/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/PWM0/PWM1

- Priority Level: X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■ Subroutine Stack Levels: 2048 levels (the stack is allocated in RAM.)

■ High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■ Oscillation Circuits

- RC oscillation circuit (internal): For system clock (1MHz)
- Low-speed RC oscillation circuit (internal): For watchdog timer (30kHz)
- CF oscillation circuit: For system clock
- Crystal oscillation circuit: For system clock, time-of-day clock
- PLL circuit (internal): For USB interface (see Fig.5)

■ Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) There are three ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Reset generated by watchdog timer
 - (3) Interrupt generation
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The PLL base clock generator, CF, RC and crystal oscillators automatically stop operation.
 - 2) There are five ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the lower level.
 - (2) Reset generated by watchdog timer
 - (3) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (4) Having an interrupt source established at port 0
 - (5) Having an bus active interrupt source established in the USB interface circuit

Continued on next page.

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- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer and the infrared remote control receiver circuit.
 - 1) The PLL base clock generator, CF and RC oscillator automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are seven ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Reset generated by watchdog timer
 - (3) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (4) Having an interrupt source established at port 0
 - (5) Having an interrupt source established in the base timer circuit
 - (6) Having a bus active interrupt source established in the USB interface circuit
 - (7) Having an interrupt source established in the infrared remote control receiver circuit

■ Package Form

- TQFP48J(7×7): Lead-/Halogen-free type

■ Development Tools

- On-chip debugger: TCB87 type B + LC87F1D64A

■ Flash ROM Programming Boards

Package	Programming boards
TQFP48J(7×7)	W87F55256SQ

■ Flash ROM Programmer

Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9708 AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev.03.06 or later	LC87F1D64A
		AF9101/AF9103 (main body) (FSG models)	(Note 2)	
Flash Support Group, Inc. (FSG) + SANYO (Note 1)	In-circuit Programmer	SIB87 (Inter Face Driver) (SANYO model)		
		SANYO	Single/Gang Programmer	SKK/SKK Type B (SANYO FWS)
	In-circuit/Gang Programmer	SKK-DBG Type B (SANYO FWS)	Chip Data Version 2.15 or later	

Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from SANYO (SIB87) together can give a PC-less, standalone on-board-programming capabilities.

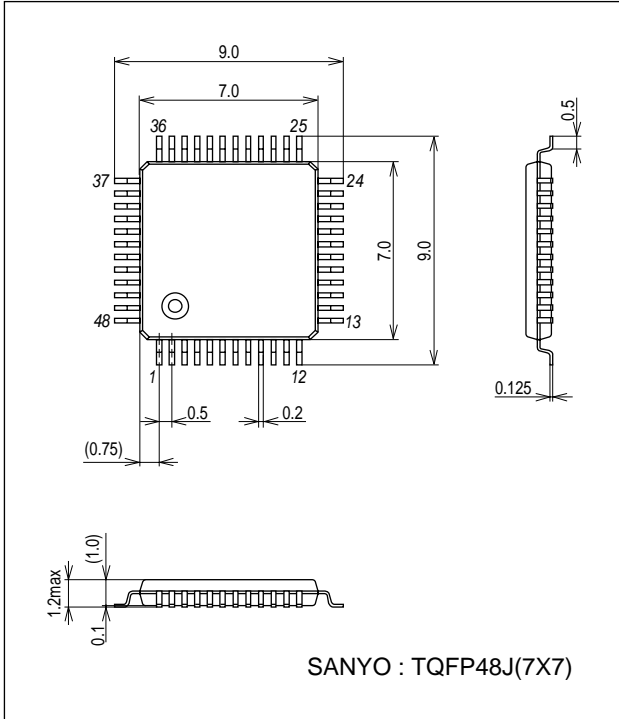
Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or SANYO for the information.

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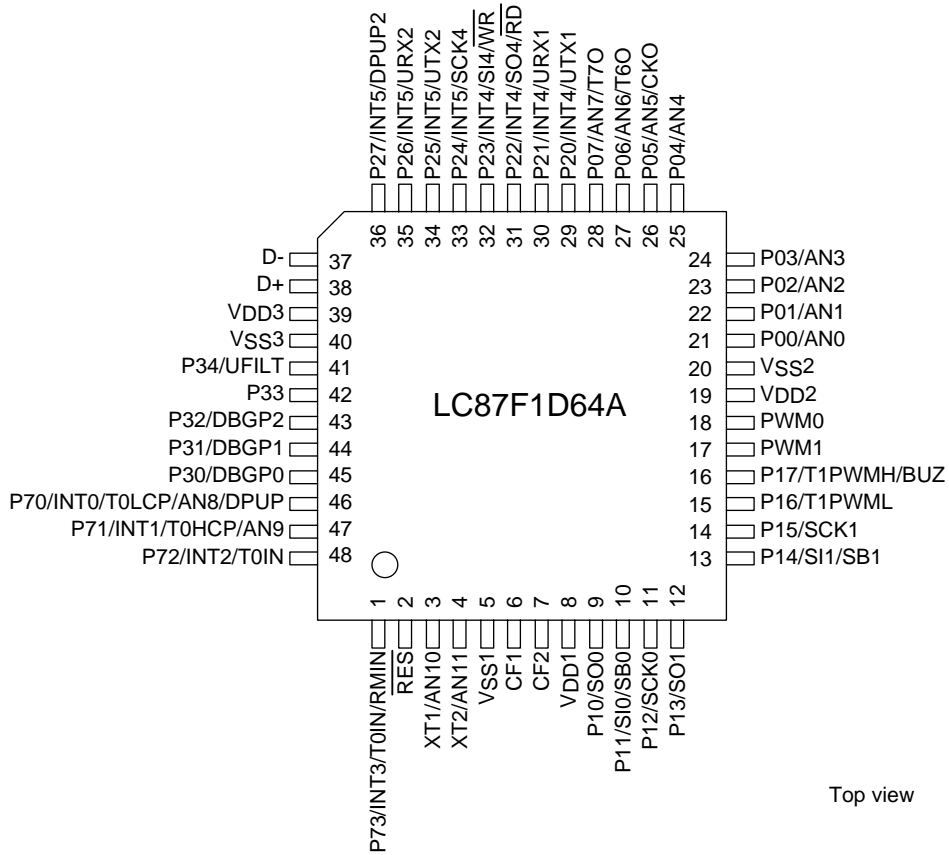
Package Dimensions

unit : mm (typ)

3288



Pin Assignment



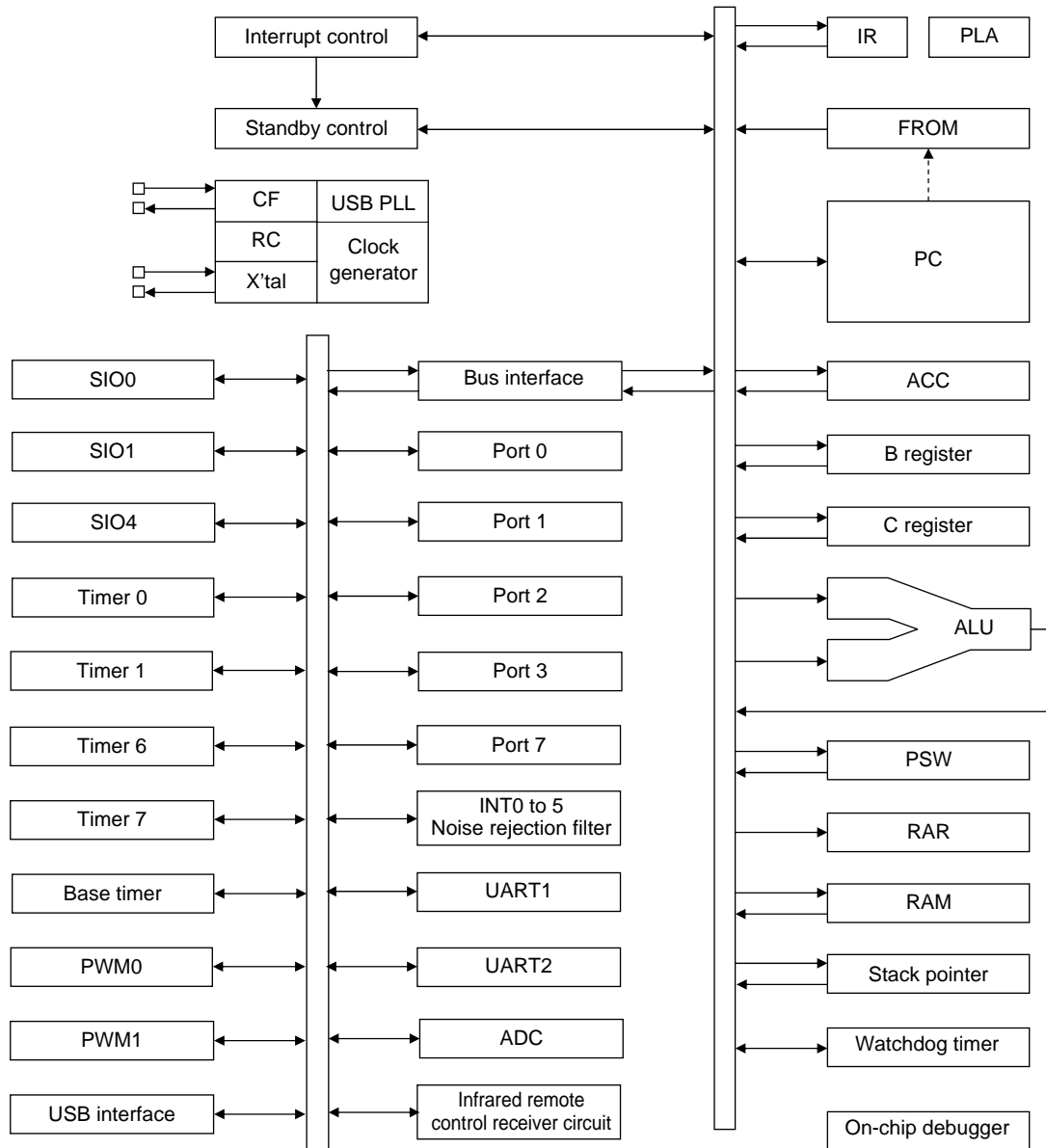
SANYO: TQFP48J(7×7) “Lead-/ Halogen-free Type”

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TQFP48J	NAME
1	P73/INT3/T0IN/RMIN
2	$\overline{\text{RES}}$
3	XT1/AN10
4	XT2/AN11
5	V _{SS1}
6	CF1
7	CF2
8	V _{DD1}
9	P10/SO0
10	P11/SI0/SB0
11	P12/SCK0
12	P13/SO1
13	P14/SI1/SB1
14	P15/SCK1
15	P16/T1PWML
16	P17/T1PVMH/BUZ
17	PWM1
18	PWM0
19	V _{DD2}
20	V _{SS2}
21	P00/AN0
22	P01/AN1
23	P02/AN2
24	P03/AN3

TQFP48J	NAME
25	P04/AN4
26	P05/AN5/CKO
27	P06/AN6/T6O
28	P07/AN7/T7O
29	P20/INT4/UTX1
30	P21/INT4/URX1
31	P22/INT4/SO4/ $\overline{\text{RD}}$
32	P23/INT4/SI4/ $\overline{\text{WR}}$
33	P24/INT5/SCK4
34	P25/INT5/UTX2
35	P26/INT5/URX2
36	P27/INT5/DPUP2
37	D-
38	D+
39	V _{DD3}
40	V _{SS3}
41	P34/UFILT
42	P33
43	P32/DBGP2
44	P31/DBGP1
45	P30/DBGP0
46	P70/INT0/T0LCP/AN8/DPUP
47	P71/INT1/T0HCP/AN9
48	P72/INT2/T0IN

System Block Diagram



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Pin Description

Pin Name	I/O	Description	Option																		
V _{SS1} , V _{SS2} , V _{SS3}	-	-power supply pin	No																		
V _{DD1} , V _{DD2}	-	+power supply pin	No																		
V _{DD3}	-	USB reference voltage pin	Yes																		
Port 0 P00 to P07	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 4-bit units • Pull-up resistors can be turned on and off in 4-bit units. • HOLD reset input • Port 0 interrupt input • Pins functions AD converter input port: AN0 to AN7 (P00 to P07) P05: System Clock Output P06: Timer 6 toggle outputs P07: Timer 7 toggle outputs	Yes																		
Port 1 P10 to P17	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P10: SIO0 data output P11: SIO0 data input/bus I/O P12: SIO0 clock I/O P13: SIO1 data output P14: SIO1 data input/bus I/O P15: SIO1 clock I/O P16: Timer 1 PWML output P17: Timer 1 PWMH output/beeper output	Yes																		
Port 2 P20 to P27	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P20 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input P24 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input P20: UART1 transmit P21: UART1 receive P22: SIO4 data I/O/parallel interface \overline{RD} output P23: SIO4 data I/O/parallel interface \overline{WR} output P24: SIO4 clock I/O P25: UART2 transmit P26: UART2 receive P27: D+ 1.5k Ω pull-up resistor connect pin Interrupt acknowledge type <table border="1" style="margin-left: 20px; margin-top: 10px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT4</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT5</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table>		Rising	Falling	Rising & Falling	H level	L level	INT4	enable	enable	enable	disable	disable	INT5	enable	enable	enable	disable	disable	Yes
	Rising	Falling	Rising & Falling	H level	L level																
INT4	enable	enable	enable	disable	disable																
INT5	enable	enable	enable	disable	disable																

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Pin Name	I/O	Description	Option																														
Port 3 P30 to P34	I/O	<ul style="list-style-type: none"> • 5-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P34: USB interface PLL filter pin (see Fig.5) On-chip debugger pins: DBG P0 to DBG P2 (P30 to P32)	Yes																														
Port 7 P70 to P73	I/O	<ul style="list-style-type: none"> • 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output/ D+ 1.5kΩ pull-up resistor connect pin P71: INT1 input/HOLD reset input/timer 0H capture input P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/ high speed clock counter input P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input/ infrared remote control receiver input AD converter input port: AN8(P70), AN9(P71) Interrupt acknowledge type <table border="1" style="margin-left: 20px; width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table>		Rising	Falling	Rising & Falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable	No
	Rising	Falling	Rising & Falling	H level	L level																												
INT0	enable	enable	disable	enable	enable																												
INT1	enable	enable	disable	enable	enable																												
INT2	enable	enable	enable	disable	disable																												
INT3	enable	enable	enable	disable	disable																												
PWM0 PWM1	I/O	<ul style="list-style-type: none"> • PWM0 and PWM1 output port • General-purpose input port 	No																														
D-	I/O	<ul style="list-style-type: none"> • USB data I/O pin D- • General-purpose I/O port 	No																														
D+	I/O	<ul style="list-style-type: none"> • USB data I/O pin D+ • General-purpose I/O port 	No																														
$\overline{\text{RES}}$	Input	Reset pin	No																														
XT1	Input	<ul style="list-style-type: none"> • 32.768kHz crystal oscillator input pin • Pin functions General-purpose input port AD converter input port: AN10 Must be connected to V_{DD1} if not to be used.	No																														
XT2	I/O	32.768kHz crystal oscillator output pin <ul style="list-style-type: none"> • Pin functions General-purpose I/O port AD converter input port: AN11 Must be set for oscillation and kept open if not to be used.	No																														
CF1	Input	Ceramic resonator input pin	No																														
CF2	Output	Ceramic resonator output pin	No																														

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Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17 P20 to P27 P30 to P34	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
PWM0, PWM1	-	No	CMOS	No
D+, D-	-	No	CMOS	No
XT1	-	No	Input only	No
XT2	-	No	32.768kHz crystal oscillator output (N channel open drain when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

User Option Table

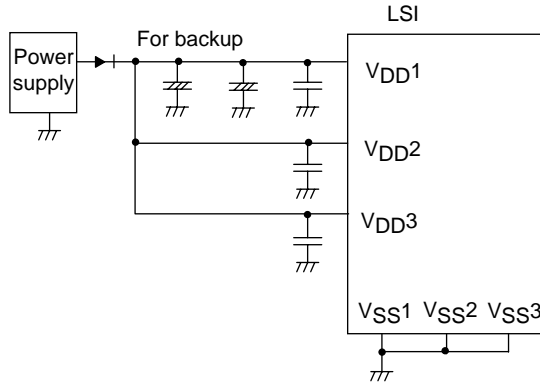
Option Name	Option to be Applied on	Flash-ROM Version	Option Selected in Units of	Option Selection	
Port output type	P00 to P07	○	1 bit	CMOS	
				Nch-open drain	
	P10 to P17	○	1 bit	CMOS	
				Nch-open drain	
	P20 to P27	○	1 bit	CMOS	
				Nch-open drain	
P30 to P34	○	1 bit	CMOS		
			Nch-open drain		
Program start address	-	○	-	00000h	
				0FE00h	
USB Regulator	USB Regulator	○	-	USE	
				NONUSE	
	USB Regulator (at HOLD mode)	○	-	-	USE
					NONUSE
	USB Regulator (at HALT mode)	○	-	-	USE
					NONUSE

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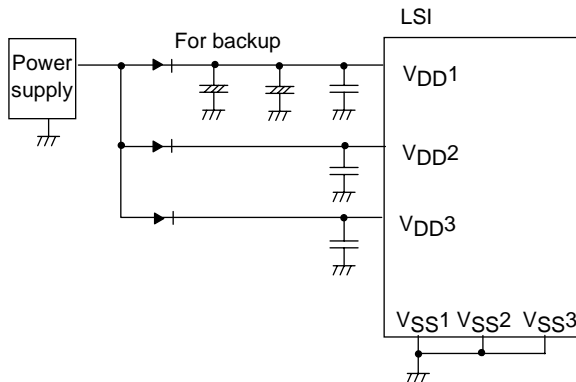
Power Pin Treatment

Connect the IC as shown below to minimize the noise input to the V_{DD1} pin. Be sure to electrically short the V_{SS1} , V_{SS2} , and V_{SS3} pins.

Example 1: When the microcontroller is in the backup state in the HOLD mode, the power to sustain the high level of output ports is supplied by their backup capacitors.



Example 2: The high level output at ports is not sustained and unstable in the HOLD backup mode.



USB Reference Power Option

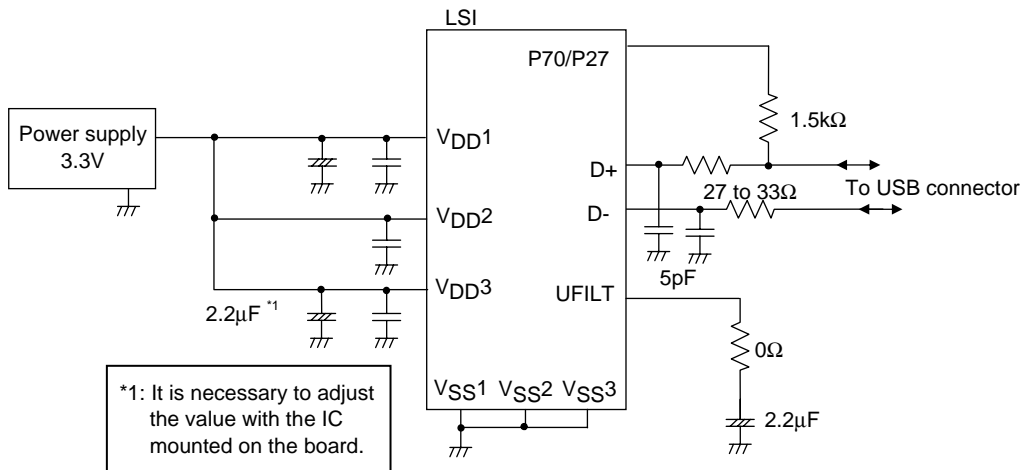
When a voltage 4.5 to 5.5V is supplied to VDD1 and the internal USB reference voltage circuit is activated, the reference voltage for USB port output is generated. The active/inactive state of reference voltage circuit can be switched by the option select. The procedure for marking the option selection is described below.

		(1)	(2)	(3)	(4)
Option select	USB Regulator	USE	USE	USE	NONUSE
	USB Regulator at HOLD mode	USE	NONUSE	NONUSE	NONUSE
	USB Regulator at HALT mode	USE	NONUSE	USE	NONUSE
Reference voltage circuit state	Normal state	active	active	active	inactive
	HOLD mode	active	inactive	inactive	inactive
	HALT mode	active	inactive	active	inactive

- When the USB reference voltage circuit is made inactive, the level of the reference voltage for USB port output is equal to VDD1.
- Selection (2) or (3) can be used to set the reference voltage circuit inactive in HOLD or HALT mode.
- When the reference voltage circuit is activated, the current drain increase by approximately 100μA compared with when the reference voltage circuit is inactive.

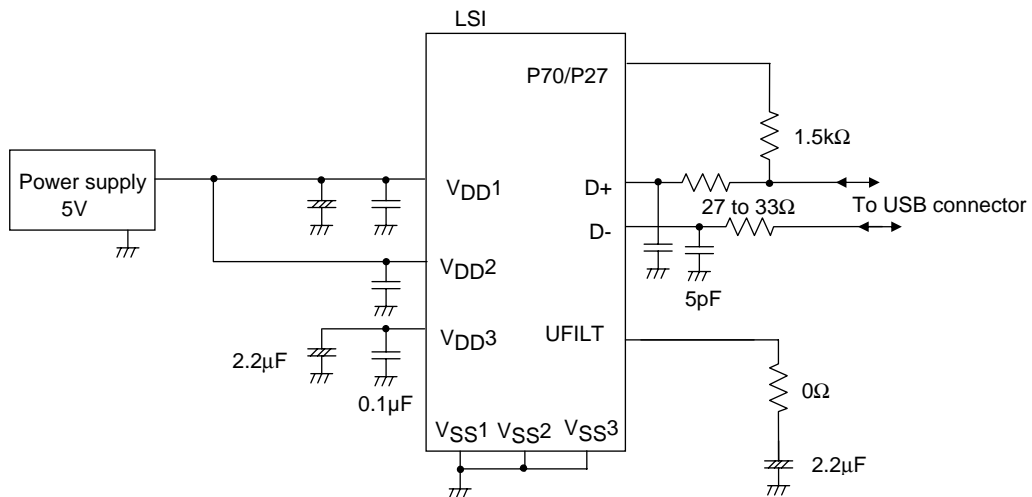
Example 1: VDD1=VDD2=3.3V

- Inactivating the reference voltage circuit (selection (4)).
- Connecting VDD3 to VDD1 and VDD2.



Example 2: VDD1=VDD2=5.0V

- Activating the reference voltage circuit (selection (1)).
- Isolating VDD3 from VDD1 and VDD2, and connecting capacitor between VDD3 and VSS.



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Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				unit
				V _{DD} [V]	min	typ	max	
Maximum supply voltage	V _{DD} max	V _{DD} 1, V _{DD} 2, V _{DD} 3	V _{DD} 1=V _{DD} 2=V _{DD} 3		-0.3		+6.5	V
Input voltage	V _I (1)	XT1, CF1			-0.3		V _{DD} +0.3	
Input/output voltage	V _{IO} (1)	Ports 0, 1, 2, 3, 7 PWM0, PWM1, XT2			-0.3		V _{DD} +0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		-10		mA
		IOPH(2)	PWM0, PWM1	Per 1 applicable pin		-20		
		IOPH(3)	Port 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		-5		
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		-7.5		
		IOMH(2)	PWM0, PWM1	Per 1 applicable pin		-15		
		IOMH(3)	Port 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		-3		
	Total output current	ΣIOAH(1)	Ports 0, 2	Total of all applicable pins		-25		
		ΣIOAH(2)	Port 1 PWM0, PWM1	Total of all applicable pins		-25		
		ΣIOAH(3)	Ports 0, 1, 2 PWM0, PWM1	Total of all applicable pins		-45		
		ΣIOAH(4)	Port 3 P71 to P73	Total of all applicable pins		-10		
ΣIOAH(5)		D+, D-	Total of all applicable pins		-25			
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin			20	
		IOPL(2)	P00, P01	Per 1 applicable pin			30	
		IOPL(3)	Ports 3, 7, XT2	Per 1 applicable pin			10	
	Average output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin			15	
		IOML(2)	P00, P01	Per 1 applicable pin			20	
		IOML(3)	Ports 3, 7, XT2	Per 1 applicable pin			7.5	
	Total output current	ΣIOAL(1)	Ports 0, 2	Total of all applicable pins			45	
		ΣIOAL(2)	Port 1 PWM0, PWM1	Total of all applicable pins			45	
		ΣIOAL(3)	Ports 0, 1, 2 PWM0, PWM1	Total of all applicable pins			80	
		ΣIOAL(4)	Ports 3, 7, XT2	Total of all applicable pins			15	
ΣIOAL(5)		D+, D-	Total of all applicable pins			25		
Allowable power Dissipation	Pd max	TQFP48J(7×7)	Ta=-30 to +70°C				190	mW
Operating ambient Temperature	Topr				-30		+70	°C
Storage ambient temperature	Tstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

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Allowable Operating Conditions at Ta = -30°C to +70°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				unit
				V _{DD} [V]	min	typ	max	
Operating supply voltage (Note 2-1)	V _{DD} (1)	V _{DD1} =V _{DD2} =V _{DD3}	0.183μs≤tCYC≤200μs		3.0		5.5	V
			0.183μs≤tCYC≤0.383μs USB circuit active		3.0		5.5	
			0.367μs≤tCYC≤200μs Except for onboard programming		2.7		5.5	
Memory sustaining supply voltage	V _H D	V _{DD1} =V _{DD2} =V _{DD3}	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	V _{IH} (1)	Ports 0, 1, 2, 3 P71 to P73 P70 port input/ interrupt side PWM0, PWM1		2.7 to 5.5	0.3V _{DD} +0.7		V _{DD}	
	V _{IH} (2)	Port 70 watchdog timer side		2.7 to 5.5	0.9V _{DD}		V _{DD}	
	V _{IH} (3)	XT1, XT2, CF1, $\overline{\text{RES}}$		2.7 to 5.5	0.75V _{DD}		V _{DD}	
Low level input voltage	V _{IL} (1)	Ports 1, 2, 3 P71 to P73		4.0 to 5.5	V _{SS}		0.1V _{DD} +0.4	
	V _{IL} (2)	P70 port input/ interrupt side		2.7 to 4.0	V _{SS}		0.2V _{DD}	
	V _{IL} (3)	Port 0 PWM0, PWM1		4.0 to 5.5	V _{SS}		0.15V _{DD} +0.4	
	V _{IL} (4)			2.7 to 4.0	V _{SS}		0.2V _{DD}	
	V _{IL} (5)	Port 70 watchdog timer side		2.7 to 5.5	V _{SS}		0.8V _{DD} -1.0	
	V _{IL} (6)	XT1, XT2, CF1, $\overline{\text{RES}}$		2.7 to 5.5	V _{SS}		0.25V _{DD}	
Instruction cycle time (Note 2-2)	tCYC			3.0 to 5.5	0.183		200	μs
			USB circuit active	3.0 to 5.5	0.183		0.383	
			Except for onboard programming	2.7 to 5.5	0.367		200	
External system clock frequency	FEXCF(1)	CF1	<ul style="list-style-type: none"> • CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty =50±5% 	3.0 to 5.5	0.1		16	MHz
			<ul style="list-style-type: none"> • CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty =50±5% 	2.7 to 5.5	0.1		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	16MHz ceramic oscillation See Fig. 1.	3.0 to 5.5		16		MHz
	FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.7 to 5.5		8		
	FmRC		Internal RC oscillation	2.7 to 5.5	0.3	1.0	2.0	
	FmSLRC		Internal low-speed RC oscillation	2.7 to 5.5	15	30	60	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.7 to 5.5		32.768		

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

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Electrical Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				unit
				VDD[V]	min	typ	max	
High level input current	I _{IH} (1)	Ports 0, 1, 2, 3 Port 7 $\overline{\text{RES}}$ PWM0, PWM1 D+, D-	Output disabled Pull-up resistor off V _{IN} =V _{DD} (Including output Tr's off leakage current)	2.7 to 5.5			1	μA
	I _{IH} (2)	XT1, XT2	For input port specification V _{IN} =V _{DD}	2.7 to 5.5			1	
	I _{IH} (3)	CF1	V _{IN} =V _{DD}	2.7 to 5.5			15	
Low level input current	I _{IL} (1)	Ports 0, 1, 2, 3 Port 7 $\overline{\text{RES}}$ PWM0, PWM1 D+, D-	Output disabled Pull-up resistor off V _{IN} =V _{SS} (Including output Tr's off leakage current)	2.7 to 5.5	-1			μA
	I _{IL} (2)	XT1, XT2	For input port specification V _{IN} =V _{SS}	2.7 to 5.5	-1			
	I _{IL} (3)	CF1	V _{IN} =V _{SS}	2.7 to 5.5	-15			
High level output voltage	V _{OH} (1)	Ports 0, 1, 2, 3 P71 to P73	I _{OH} =-1mA	4.5 to 5.5	V _{DD} -1			V
	V _{OH} (2)		I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (3)		I _{OH} =-0.2mA	2.7 to 5.5	V _{DD} -0.4			
	V _{OH} (4)	PWM0, PWM1 P05 (CK0 when using system clock output function)	I _{OH} =-10mA	4.5 to 5.5	V _{DD} -1.5			
	V _{OH} (5)		I _{OH} =-1.6mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (6)		I _{OH} =-1mA	2.7 to 5.5	V _{DD} -0.4			
Low level output voltage	V _{OL} (1)	P00, P01	I _{OL} =30mA	4.5 to 5.5			1.5	V
	V _{OL} (2)		I _{OL} =5mA	3.0 to 5.5			0.4	
	V _{OL} (3)		I _{OL} =2.5mA	2.7 to 5.5			0.4	
	V _{OL} (4)	Ports 0, 1, 2 PWM0, PWM1 XT2	I _{OL} =10mA	4.5 to 5.5			1.5	
	V _{OL} (5)		I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (6)		I _{OL} =1mA	2.7 to 5.5			0.4	
	V _{OL} (7)	Ports 3, 7	I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (8)		I _{OL} =1mA	2.7 to 5.5			0.4	
Pull-up resistance	R _{pu} (1)	Ports 0, 1, 2, 3	V _{OH} =0.9V _{DD}	4.5 to 5.5	15	35	80	kΩ
	R _{pu} (2)	Port 7		2.7 to 5.5	18	50	150	
Hysteresis voltage	V _{HYS}	$\overline{\text{RES}}$ Ports 1, 2, 3, 7		2.7 to 5.5		0.1V _{DD}		V
Pin capacitance	CP	All pins	For pins other than that under test: V _{IN} =V _{SS} f=1MHz Ta=25°C	2.7 to 5.5		10		pF

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Serial I/O Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification					
					min	typ	max	unit		
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	2.7 to 5.5	See Fig.8.	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)	<ul style="list-style-type: none"> Continuous data transmission/reception mode USB nor SIO4 are not in use simultaneous. See Fig.8. (Note 4-1-2) 			4			
			tSCKHA(1b)	<ul style="list-style-type: none"> Continuous data transmission/reception mode USB is in use simultaneous. SIO4 is not in use simultaneous. See Fig.8. (Note 4-1-2) 			7			
	tSCKHA(1c)	<ul style="list-style-type: none"> Continuous data transmission/reception mode USB and SIO4 are in use simultaneous. See Fig.8. (Note 4-1-2) 	9							
	Output clock	Frequency	tSCK(2)	SCK0(P12)	2.7 to 5.5	<ul style="list-style-type: none"> CMOS output selected See Fig.8. 	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2a)	<ul style="list-style-type: none"> Continuous data transmission/reception mode USB nor SIO4 are not in use simultaneous. CMOS output selected See Fig.8. 			tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	
tSCKHA(2b)		<ul style="list-style-type: none"> Continuous data transmission/reception mode USB is in use simultaneous. SIO4 is not in use simultaneous. CMOS output selected See Fig.8. 	tSCKH(2) +2tCYC				tSCKH(2) +(19/3) tCYC			
tSCKHA(2c)	<ul style="list-style-type: none"> Continuous data transmission/reception mode USB and SIO4 are in use simultaneous. CMOS output selected See Fig.8. 	tSCKH(2) +2tCYC		tSCKH(2) +(25/3) tCYC						

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIORUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

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Continued from preceding page.

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V _{DD} [V]	min	typ	max	unit
Serial input	Data setup time	tsDI(1)	SB0(P11), SI0(P11)	<ul style="list-style-type: none"> • Must be specified with respect to rising edge of SIOCLK. • See Fig.8. 	2.7 to 5.5	0.03			
	Data hold time	thDI(1)							
Serial output	Input clock	tdD0(1)	SO0(P10), SB0(P11)	<ul style="list-style-type: none"> • Continuous data transmission/reception mode • (Note 4-1-3) 	2.7 to 5.5			(1/3)tCYC +0.05	μs
		tdD0(2)		<ul style="list-style-type: none"> • Synchronous 8-bit mode • (Note 4-1-3) 				1tCYC +0.05	
	Output clock	tdD0(3)		(Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig.8.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter		Symbol	Pin/Remarks	Conditions	Specification					
					V _{DD} [V]	min	typ	max	unit	
Serial clock	Input clock	Frequency	SCK1(P15)	See Fig.8.	2.7 to 5.5	2			tCYC	
		Low level pulse width				tSCKL(3)	1			
		High level pulse width				tSCKH(3)	1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	<ul style="list-style-type: none"> • CMOS output selected • See Fig.8. 	2.7 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time	tsDI(2)	SB1(P14), SI1(P14)	<ul style="list-style-type: none"> • Must be specified with respect to rising edge of SIOCLK. • See Fig.8. 	2.7 to 5.5	0.03				
	Data hold time	thDI(2)								
Serial output	Output delay time	tdD0(4)	SO1(P13), SB1(P14)	<ul style="list-style-type: none"> • Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig.8. 	2.7 to 5.5			(1/3)tCYC +0.05	μs	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

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3. SIO4 Serial I/O Characteristics (Note 4-3-1)

	Parameter	Symbol	Pin/ Remarks	Conditions	Specification					
					V _{DD} [V]	min	typ	max	unit	
Serial clock	Input clock	Frequency	tSCK(5)	SCK4(P24)	See Fig.8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(5)				1			
		High level pulse width	tSCKH(5)				1			
			tSCKHA(5a)	<ul style="list-style-type: none"> • USB nor continuous data transmission/reception mode Of SIO0 are not in use simultaneous. • See Fig.8. • (Note 4-3-2) 			4			
		tSCKHA(5b)	<ul style="list-style-type: none"> • USB is in use simultaneous. • Continuous data transmission/ reception mode of SIO0 is not in use simultaneous. • See Fig.8. • (Note 4-3-2) 				7			
	tSCKHA(5c)	<ul style="list-style-type: none"> • USB and continuous data transmission/ reception mode of SIO0 are in use simultaneous. • See Fig.8. • (Note 4-3-2) 	10							
	Output clock	Frequency	tSCK(6)	SCK4(P24)	<ul style="list-style-type: none"> • CMOS output selected • See Fig.8. 	2.7 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(6)				1/2			
		High level pulse width	tSCKH(6)				1/2			
			tSCKHA(6a)	<ul style="list-style-type: none"> • USB nor continuous data transmission/reception mode of SIO0 are not in use simultaneous. • CMOS output selected • See Fig.8. 			tSCKH(6) +(5/3) tCYC		tSCKH(6) +(10/3) tCYC	
tSCKHA(6b)		<ul style="list-style-type: none"> • USB is in use simultaneous. • Continuous data transmission/ reception mode of SIO0 is not in use simultaneous. • CMOS output selected • See Fig.8. 	tSCKH(6) +(5/3) tCYC				tSCKH(6) +(19/3) tCYC	tCYC		
tSCKHA(6c)	<ul style="list-style-type: none"> • USB and continuous data transmission/reception mode of SIO0 are in use simultaneous. • CMOS output selected • See Fig.8. 	tSCKH(6) +(5/3) tCYC		tSCKH(6) +(28/3) tCYC	tCYC					
Serial input	Data setup time	tsDI(3)	SO4(P22), SI4(P23)	<ul style="list-style-type: none"> • Must be specified with respect to rising edge of SIOCLK. • See Fig.8. 	2.7 to 5.5	0.03			μs	
	Data hold time	thDI(3)					2.7 to 5.5	0.03		
Serial output	Output delay time	tdD0(5)	SO4(P22), SI4(P23)	<ul style="list-style-type: none"> • Must be specified with respect to rising edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig.8. 	2.7 to 5.5			(1/3)tCYC +0.05	μs	

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input in continuous trans/rec mode, a time from SI4RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

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Pulse Input Conditions at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27)	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 or 1 are enabled. 	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. 	2.7 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. 	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. 	2.7 to 5.5	256			
	tPIL(5)	RMIN(P73)	Recognized by the infrared remote control receiver circuit as a signal	2.7 to 5.5	4			RMCK (Note 5-1)
	tPIL(6)	$\overline{\text{RES}}$	Resetting is enabled.	2.7 to 5.5	200			μs

Note 5-1: Represents the period of the reference clock (1 tCYC to 128 tCYC or the source frequency of the subclock) for the infrared remote control receiver circuit.

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AD Converter Characteristics at Ta= -30°C to +70°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

<12-bits AD Converter Mode>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2)		3.0 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±16	LSB
Conversion time	TCAD		See conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		115	μs
				3.0 to 5.5	64		115	
			AD division ratio=1/16	3.0 to 5.5	50		115	
Analog input voltage range	VAIN			3.0 to 5.5	V _{SS}		V _{DD}	V
Analog port input current	IAINH	VAIN=V _{DD}	3.0 to 5.5			1	μA	
	IAINL	VAIN=V _{SS}	3.0 to 5.5	-1				

<8-bits AD Converter Mode>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		See conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	20		90	μs
				3.0 to 5.5	40		90	
			AD division ratio=1/16	3.0 to 5.5	31		90	
Analog input voltage range	VAIN			3.0 to 5.5	V _{SS}		V _{DD}	V
Analog port input current	IAINH	VAIN=V _{DD}	3.0 to 5.5			1	μA	
	IAINL	VAIN=V _{SS}	3.0 to 5.5	-1				

<Conversion time calculation formulas>

12-bits AD Converter Mode: TCAD (Conversion time) = ((52/(AD division ratio))+2) × (1/3) × tCYC

8-bits AD Converter Mode: TCAD (Conversion time) = ((32/(AD division ratio))+2) × (1/3) × tCYC

<Recommended Operating Conditions>

External oscillator FmCF[MHz]	Supply Voltage Range V _{DD} [V]	System Clock Division (SYSDIV)	Cycle Time tCYC [ns]	AD Frequency Division Ratio (ADDIV)	Conversion Time (TCAD)[μs]	
					12-bit AD	8-bit AD
16	3.0 to 5.5	1/1	187.5	1/16	52.125	32.125
12	4.0 to 5.5	1/1	250	1/8	34.8	21.5
	3.0 to 5.5	1/1	250	1/16	69.5	42.8
8	4.0 to 5.5	1/1	375	1/8	52.25	32.25
	3.0 to 5.5	1/1	375	1/16	104.25	64.25

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

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Consumption Current Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification					
				V _{DD} [V]	min	typ	max	unit	
Normal mode consumption current (Note 7-1)	IDDOP(1)	V _{DD1} =V _{DD2} =V _{DD3}	<ul style="list-style-type: none"> • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ration 	4.5 to 5.5		9.9	25	mA	
	IDDOP(2)		<ul style="list-style-type: none"> • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ration 	3.0 to 3.6		5.7	14		
	IDDOP(3)		<ul style="list-style-type: none"> • FmCF=16MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 16MHz side • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ration 	4.5 to 5.5		12	30		
	IDDOP(4)		<ul style="list-style-type: none"> • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ration 	3.0 to 3.6		6.8	17		
	IDDOP(5)		<ul style="list-style-type: none"> • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation mode • Internal RC oscillation stopped • USB circuit active • 1/1 frequency division ration 	4.5 to 5.5		14	35		
	IDDOP(6)		<ul style="list-style-type: none"> • Internal PLL oscillation mode • Internal RC oscillation stopped • USB circuit active • 1/1 frequency division ration 	3.0 to 3.6		7.7	19		
	IDDOP(7)		<ul style="list-style-type: none"> • FmCF=16MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 16MHz side • Internal PLL oscillation mode • Internal RC oscillation stopped • USB circuit active • 1/1 frequency division ration 	4.5 to 5.5		16	40		
	IDDOP(8)		<ul style="list-style-type: none"> • Internal PLL oscillation mode • Internal RC oscillation stopped • USB circuit active • 1/1 frequency division ration 	3.0 to 3.6		8.8	22		
	IDDOP(9)		<ul style="list-style-type: none"> • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side • Internal RC oscillation stopped • 1/2 frequency division ration 	4.5 to 5.5		6.8	16		
	IDDOP(10)		<ul style="list-style-type: none"> • System clock set to 6MHz side • Internal RC oscillation stopped • 1/2 frequency division ration 	3.0 to 3.6		4.1	9.7		
	IDDOP(11)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/2 frequency division ration 	2.7 to 3.0		3.5	7.9		
	IDDOP(12)		<ul style="list-style-type: none"> • FmCF=16MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped • 1/2 frequency division ration 	4.5 to 5.5		8.2	20		
	IDDOP(13)		<ul style="list-style-type: none"> • System clock set to 8MHz side • Internal RC oscillation stopped • 1/2 frequency division ration 	3.0 to 3.6		4.7	12		
	IDDOP(14)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/2 frequency division ration 	2.7 to 3.0		4.0	9.2		
	IDDOP(15)		<ul style="list-style-type: none"> • FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • 1/2 frequency division ration 	4.5 to 5.5		0.73	3.5		
	IDDOP(16)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • 1/2 frequency division ration 	3.0 to 3.6		0.43	1.9		
	IDDOP(17)		<ul style="list-style-type: none"> • System clock set to internal RC oscillation • 1/2 frequency division ration 	2.7 to 3.0		0.37	1.5		
	IDDOP(18)		<ul style="list-style-type: none"> • FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • 1/2 frequency division ration 	4.5 to 5.5		45	174		μA
	IDDOP(19)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • 1/2 frequency division ration 	3.0 to 3.6		18	86		
	IDDOP(20)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/2 frequency division ration 	2.7 to 3.0		14	63		
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V _{DD1} =V _{DD2} =V _{DD3}	<ul style="list-style-type: none"> • HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ration 	4.5 to 5.5		4.9	12	mA	
	IDDHALT(2)		<ul style="list-style-type: none"> • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ration 	3.0 to 3.6		2.6	6.3		

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

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Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Conditions	Specification							
				V _{DD} [V]	min	typ	max	unit			
HALT mode consumption current (Note 7-1)	IDDHALT(3)	V _{DD1} =V _{DD2} =V _{DD3}	<ul style="list-style-type: none"> • HALT mode • FmCF=16MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 16MHz side 	4.5 to 5.5		5.7	14	mA			
	IDDHALT(4)		<ul style="list-style-type: none"> • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ration 	3.0 to 3.6		3.1	7.6				
	IDDHALT(5)		<ul style="list-style-type: none"> • HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side 	4.5 to 5.5		8.9	23				
	IDDHALT(6)		<ul style="list-style-type: none"> • Internal PLL oscillation mode • Internal RC oscillation stopped • USB circuit active • 1/1 frequency division ration 	3.0 to 3.6		4.6	12				
	IDDHALT(7)		<ul style="list-style-type: none"> • HALT mode • FmCF=16MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 16MHz side 	4.5 to 5.5		9.7	24				
	IDDHALT(8)		<ul style="list-style-type: none"> • Internal PLL oscillation mode • Internal RC oscillation stopped • USB circuit active • 1/1 frequency division ration 	3.0 to 3.6		5.0	13				
	IDDHALT(9)		<ul style="list-style-type: none"> • HALT mode • FmCF=12MHz ceramic oscillation mode 	4.5 to 5.5		3.0	7.2				
	IDDHALT(10)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side 	3.0 to 3.6		1.6	3.8				
	IDDHALT(11)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/2 frequency division ration 	2.7 to 3.0		1.3	2.9				
	IDDHALT(12)		<ul style="list-style-type: none"> • HALT mode • FmCF=16MHz ceramic oscillation mode 	4.5 to 5.5		3.5	8.6				
	IDDHALT(13)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side 	3.0 to 3.6		1.9	4.6				
	IDDHALT(14)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/2 frequency division ration 	2.7 to 3.0		1.5	3.5				
	IDDHALT(15)		<ul style="list-style-type: none"> • HALT mode • FmCF=0MHz (oscillation stopped) 	4.5 to 5.5		0.41	2.0				
	IDDHALT(16)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation 	3.0 to 3.6		0.20	0.93				
	IDDHALT(17)		<ul style="list-style-type: none"> • 1/2 frequency division ration 	2.7 to 3.0		0.16	0.69				
	IDDHALT(18)		<ul style="list-style-type: none"> • HALT mode • FmCF=0MHz (oscillation stopped) 	4.5 to 5.5		32	134				
	IDDHALT(19)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side 	3.0 to 3.6		8.8	60				
	IDDHALT(20)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • 1/2 frequency division ration 	2.7 to 3.0		6.0	40				
	HOLD mode consumption current		IDDHOLD(1)	V _{DD1}	HOLD mode	4.5 to 5.5			0.08	30	μA
			IDDHOLD(2)		<ul style="list-style-type: none"> • CF1=V_{DD} or open (External clock mode) 	3.0 to 3.6			0.03	18	
IDDHOLD(3)			2.7 to 3.0			0.02	15				
IDDHOLD(4)		HOLD mode	4.5 to 5.5			2.9	38				
IDDHOLD(5)		<ul style="list-style-type: none"> • Internal counter watchdog timer operation mode (internal low-speed RC oscillation circuit operation) • CF1=V_{DD} or open (External clock mode) 	3.0 to 3.6			1.4	23				
IDDHOLD(6)			2.7 to 3.0			1.2	20				
Timer HOLD mode consumption current	IDDHOLD(7)	V _{DD1}	Timer HOLD mode	4.5 to 5.5		27	118				
	IDDHOLD(8)		<ul style="list-style-type: none"> • CF1=V_{DD} or open (External clock mode) 	3.0 to 3.6		6.1	51				
	IDDHOLD(9)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode 	2.7 to 3.0		3.8	34				

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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USB Characteristics and Timing at $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
High level output	$V_{OH(USB)}$	• $15\text{k}\Omega \pm 5\%$ to GND	2.8		3.6	V
Low level output	$V_{OL(USB)}$	• $1.5\text{k}\Omega \pm 5\%$ to 3.6 V	0.0		0.3	V
Output signal crossover voltage	V_{CRS}		1.3		2.0	V
Differential input sensitivity	V_{DI}	• $ (D+)-(D-) $	0.2			V
Differential input common mode range	V_{CM}		0.8		2.5	V
High level input	$V_{IH(USB)}$		2.0			V
Low level input	$V_{IL(USB)}$				0.8	V
USB data rise time	t_R	• $R_S=27$ to 33Ω , $CL=50\text{pF}$ • $V_{DD3}=3.0$ to 3.6V	4		20	ns
USB data fall time	t_F	• $R_S=27$ to 33Ω , $CL=50\text{pF}$ • $V_{DD3}=3.0$ to 3.6V	4		20	ns

F-ROM Programming Characteristics at $T_a = +10^\circ\text{C}$ to $+55^\circ\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pin	Conditions	$V_{DD}[\text{V}]$	Specification			
					min	typ	max	unit
Onboard programming current	$I_{DDFW(1)}$	V_{DD1}	• Excluding power dissipation in the microcontroller block	3.0 to 5.5		5	10	mA
Programming time	$t_{FW(1)}$		• Erase operation	3.0 to 5.5		20	30	ms
	$t_{FW(2)}$		• Write operation			40	60	μs

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Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator at Ta = 0°C to +70°C

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant			Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rd1 [Ω]		typ [ms]	max [ms]	
8MHz	MURATA	CSTCE8M00G15L**-R0	(33)	(33)	680	2.7 to 5.5	0.1	0.5	C1 and C2 integrated SMD type
12MHz	MURATA	CSTCE12M0G15L**-R0	(33)	(33)	470	3.0 to 5.5	0.1	0.5	
16MHz	MURATA	CSTCE16M0V13L**-R0	(15)	(15)	330	3.0 to 5.5	0.05	0.25	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 4):

- Till the oscillation gets stabilized after V_{DD} goes above the operating voltage lower limit.
- Till the oscillation gets stabilized after the instruction for starting the main clock oscillation circuit is executed
- Till the oscillation gets stabilized after the HOLD mode is reset.
- Till the oscillation gets stabilized after the X'tal HOLD mode is reset with CFSTOP (OCR register, bit 0) set to 0

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	OPEN	560k	2.7 to 5.0	1.1	3.0	Applicable CL value=12.5pF SMD type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 4):

- Till the oscillation gets stabilized after the instruction for starting the subclock oscillation circuit is executed
- Till the oscillation gets stabilized after the HOLD mode is reset with EXTOSC (OCR register, bit 6) set to 1

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

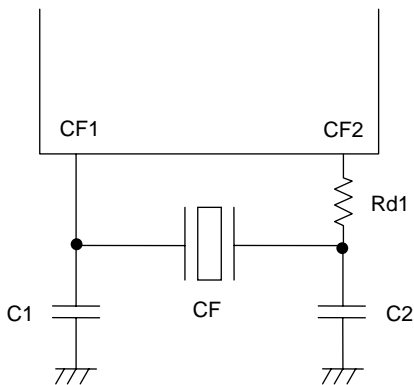


Figure 1 CF Oscillator Circuit

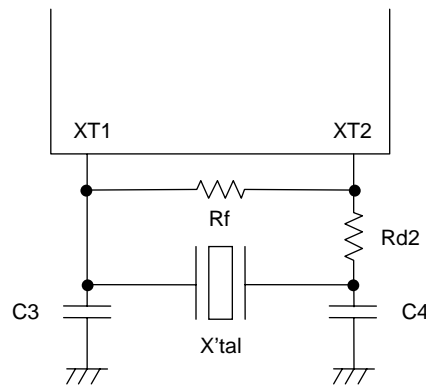


Figure 2 XT Oscillator Circuit

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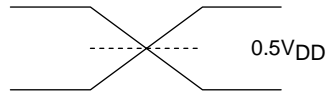
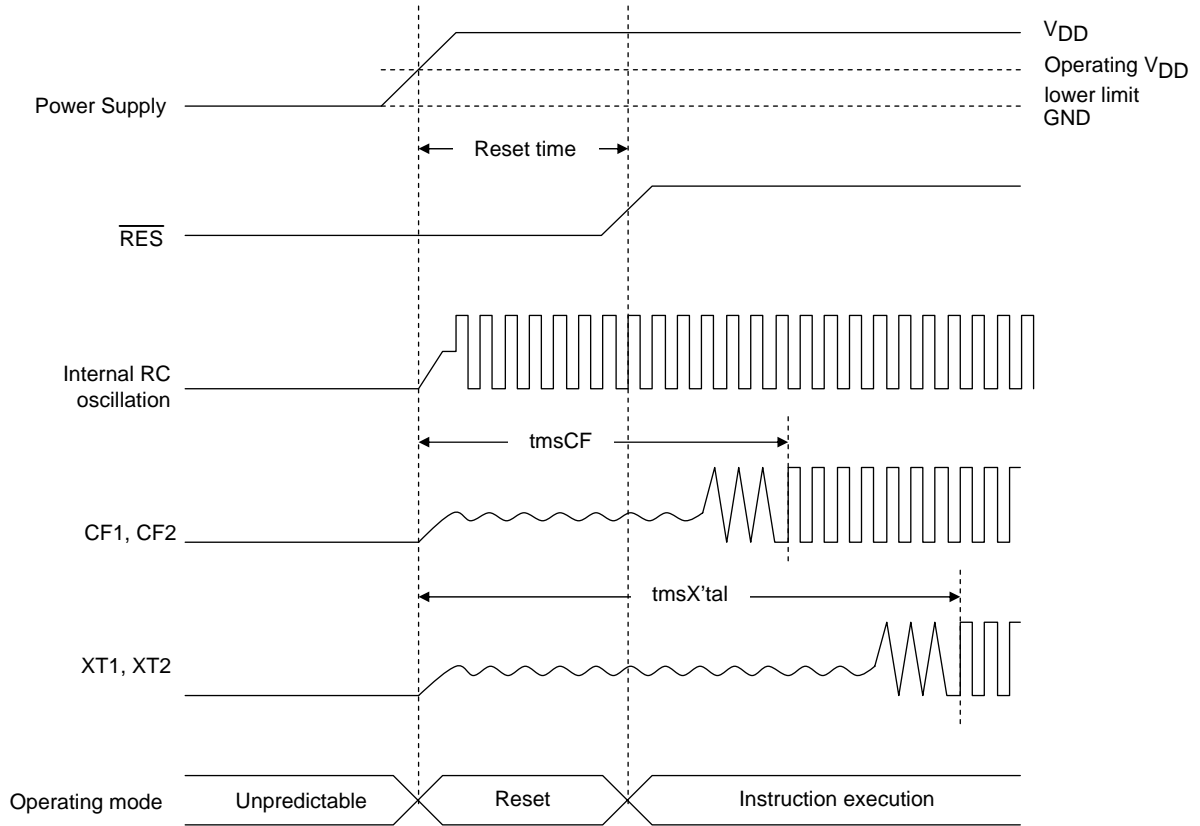
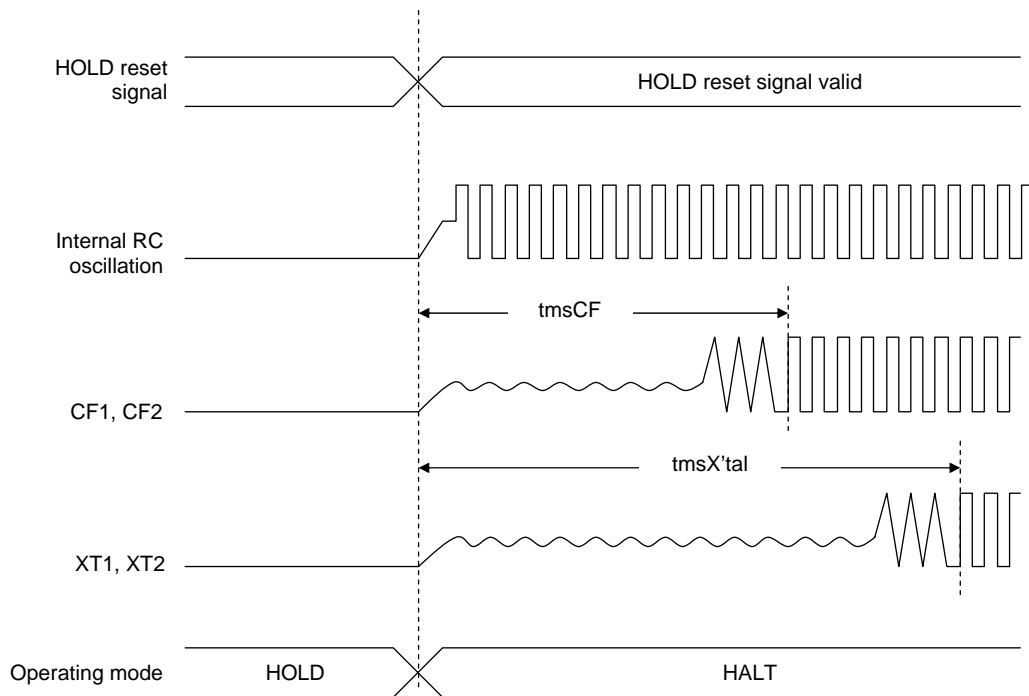


Figure 3 AC Timing Measurement Point

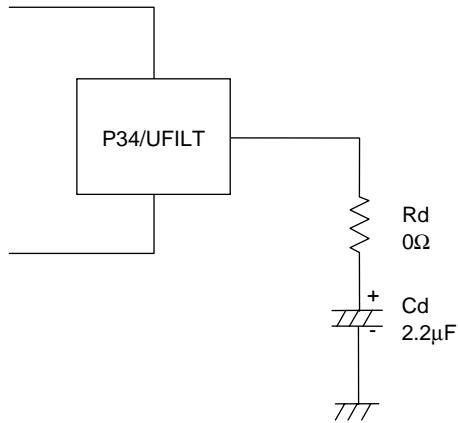


Reset Time and Oscillation Stabilization Time



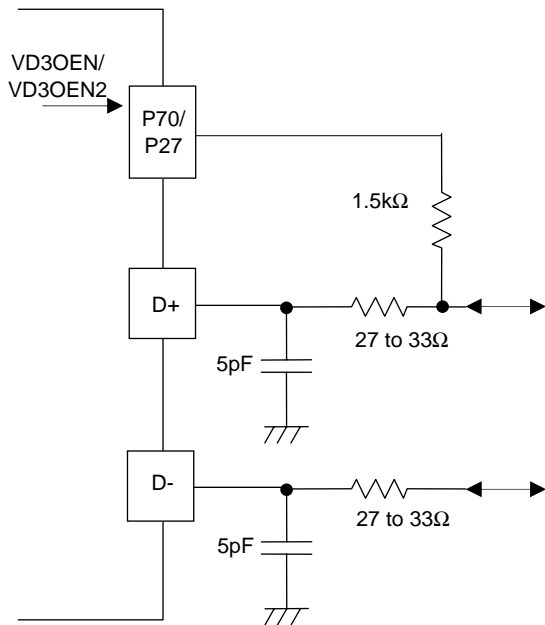
HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



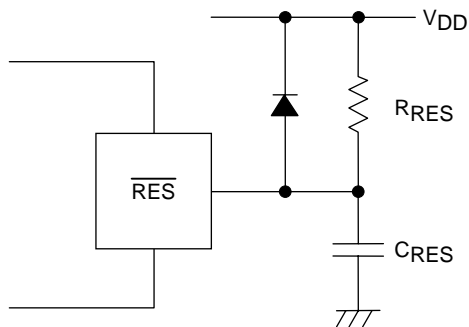
When using the internal PLL circuit to generate the 48MHz clock for USB , it is necessary to connect a filter circuit such as that shown to the left to the P34/UFILT pin.

Figure 5 External Filter Circuit for the Internal USB-dedicated PLL Circuit



Note:
It's necessary to adjust the Circuit Constant of the USB Port Peripheral Circuit each mounting board. Make the D+ Pull-up resistors available to control on/off according to the Vbus.

Figure 6 USB Port Peripheral Circuit



Note:
Determine the value of CRES and RRES so that the reset signal is present for a period of 200μs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 7 Reset Circuit

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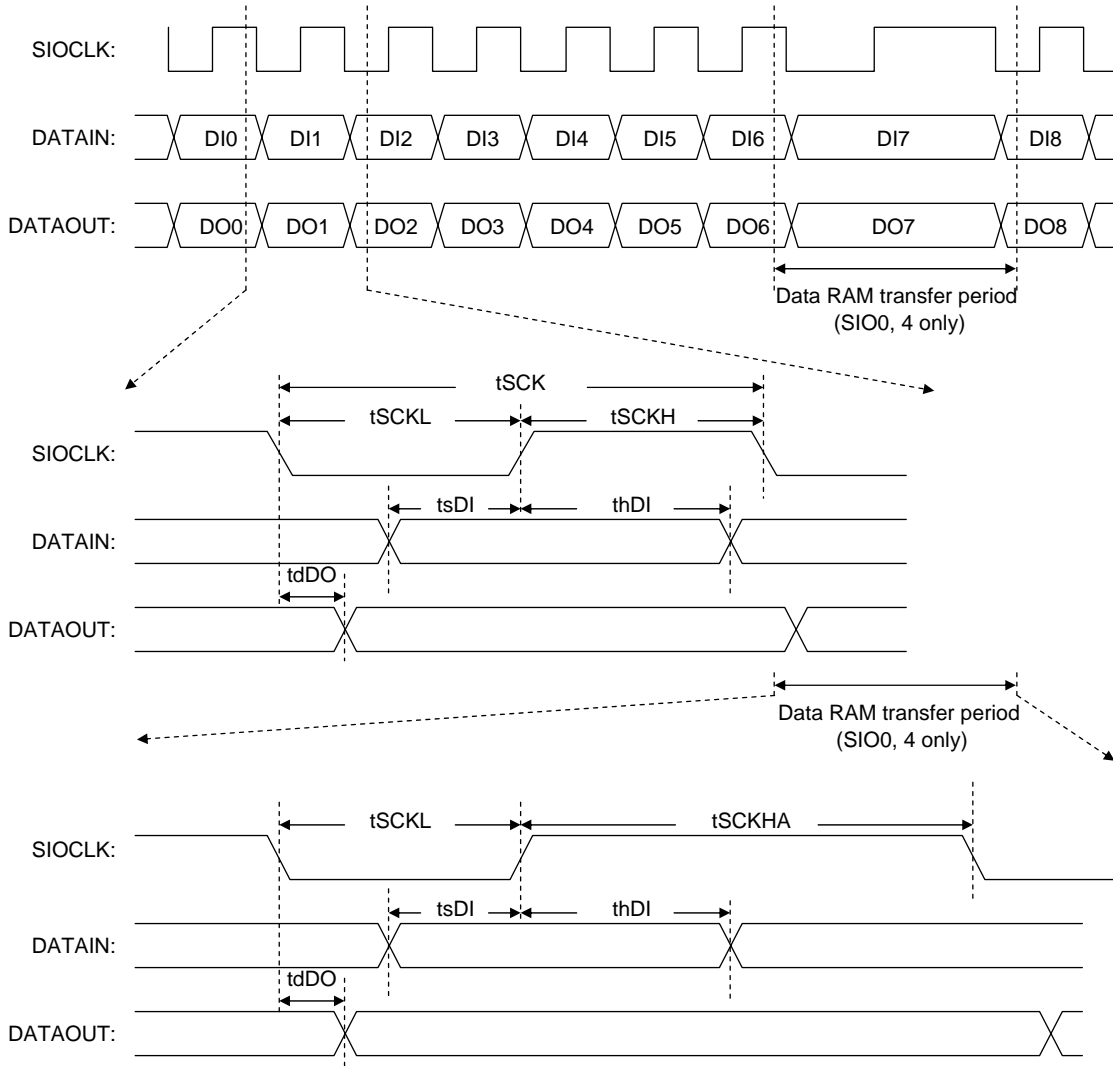


Figure 8 Serial I/O Waveforms

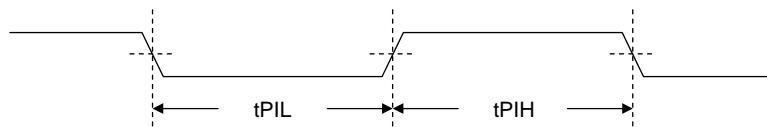


Figure 9 Pulse Input Timing Signal Waveform

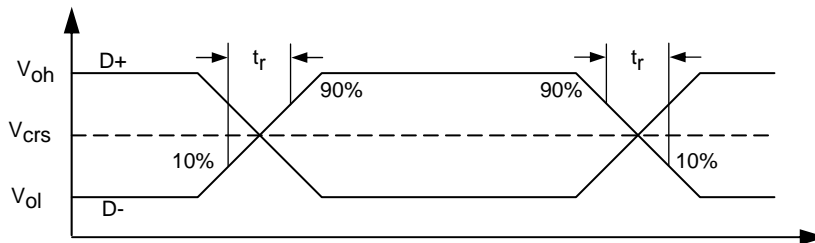


Figure 10 USB Data Signal Timing and Voltage Level

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