Ordering number : ENN7941

SANYO Semiconductors
DATA SHEET

LC87F5564A

CMOS IC
FROM 64K-byte, RAM 1K-byte on chip
8-bit 1-chip Microcontroller

Overview

The LC87F5564A is 8-bit single chip microcontroller with the following one-chip features :

- CPU : Operable at a minimum bus cycle time of 100ns
- On-chip Flash ROM Capacity : 64K-bytes (on-board rewritable)
- On-chip RAM Capacity : 1K-bytes
- Two high performance 16-bit timer/counters (can be divided into 8-bit timers)
- Four 8-bit timers with prescalers
- Timer for use as date/time clock
- One synchronous serial I/O port (with automatic block transmit/receive function)
- One asynchronous/synchronous serial I/O port
- 12-bit PWM × 2
- 12-channel × 8-bit AD converter
- High speed clock counter
- System clock divider
- 20-source 10-vectored interrupt system

Features

■Read Only Memory (Flash ROM)
- Single 5V power supply, on-board writeable
- Block erase in 128-byte units
- 65536 × 8-bits (LC87F5564A)

■Minimum Bus Cycle Time
- 100ns (10MHz)

  Note : Bus cycle time indicates the speed to read ROM.

■Minimum Instruction Cycle Time
- 300ns (10MHz)

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■Ports

- Input/output ports
  Input/output programmable for each bit individually 27 (P1n, P2n, P3n, P70 to P73)
  Data direction programmable in nibble units 8 (P0n)
- Input ports 2 (XT1, XT2)
- PWM output ports 2 (PWM0, PWM1)
- Oscillator pins 2 (CF1, CF2)
- Reset pin 1 ($\overline{\text{RES}}$)
- Power supply 6 (V_{SS}1 to 3, V_{DD}1 to 3)

■Timer

- Timer 0 : 16-bit timer/counter with capture register
  Mode 0 : Two 8-bit timers with programmable 8-bit prescaler and 8-bit capture register
  Mode 1 : 8-bit timer with 8-bit programmable prescaler and 8-bit capture register + 8-bit counter with 8-bit capture register
  Mode 2 : 16-bit timer with 8-bit programmable prescaler and 16-bit capture register
  Mode 3 : 16-bit counter with 16-bit capture register
- Timer 1 : PWM/16-bit timer/counter with toggle output
  Mode 0 : 8-bit timer (with toggle output) + 8-bit timer/counter (with toggle output)
  Mode 1 : Two 8-bit PWM
  Mode 2 : 16-bit timer/counter (with toggle output)
  Toggle output is also possible by using the lower order 8-bits.
  Mode 3 : 16-bit timer (with toggle output) The lower order 8-bits can be used as PWM output.
- Timer 4 : 8-bit timer with 6-bit prescaler
- Timer 5 : 8-bit timer with 6-bit prescaler
- Timer 6 : 8-bit timer with 6-bit prescaler
- Timer 7 : 8-bit timer with 6-bit prescaler
- Base timer
  1. Clock for the base timer is selectable from sub-clock (32.768kHz crystal oscillation), system clock or programmable prescaler output of timer 0.
  2. There can be five separate interrupt sources.

■High speed clock counter

1. Maximum of 20MHz possible (when using a 10MHz main clock)
2. Real-time output

■Serial interface

- SIO0 : 8-bit synchronous serial interface
  1. LSB first/MSB first-function available
  2. An internal 8-bit baud-rate generator (maximum transmit clock period 4/3 tCYC)
  3. Consecutive automatic data communication (1 to 256-bits)
- SIO1 : 8-bit asynchronous/synchronous serial interface
  Mode 0 : Synchronous 8-bit serial I_O (2-wire or 3-wire, transmit clock 2 to 512 tCYC)
  Mode 1 : Asynchronous serial I_O (half duplex, 8 data bits, 1 stop bit, baud-rate 8 to 2048 tCYC)
  Mode 2 : Bus mode 1 (start bit, 8 data bits, transmit clock 2 to 512 tCYC)
  Mode 3 : Bus mode 2 (start detection, 8 data bits, stop detection)

■AD converter

- 12-channel × 8-bit AD converter

■PWM

- 2-channel × synchronous variable 12-bit PWM

■Remote receiver circuit (share with P73/INT3/T0IN terminal)

- Noise rejection function (The filtering time of the noise rejection filter (1 tCYC/32 tCYC /128 tCYC) can be switched by program.)

■Watchdog timer
- External RC circuit is required.
- Interrupt or system reset is activated when the timer overflows.

■Interrupts
- 20-source and 10-vectored interrupt function :
  1. Three interrupt priorities, low (L), high (H) and highest (X) are supported with multi-level nesting possible. During interrupt handling, an equal or lower level interrupt request is refused.
  2. If interrupt requests for two or more vector addresses occur at once, the higher level interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt Signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/Base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

- Priority Level : X > H > L
- For equal priority levels, vector with lowest address takes precedence.

■Subroutine stack levels
- A maximum of 512 levels (set stack inside RAM)

■Multiplication and division
- 16-bits × 8-bits (5 instruction-cycle times)
- 24-bits × 16-bits (12 instruction-cycle times)
- 16-bits ÷ 8-bits (8 instruction-cycle times)
- 24-bits ÷ 16-bits (12 instruction-cycle times)

■Oscillation circuits
- Built-in RC oscillation circuit used for the system clock
- CF oscillation circuit used for the system clock
- Crystal oscillation circuit used for the system clock
- Built-in frequency variable RC oscillation circuit used for the system clock

■System clock divider
- Operable on the lowest power consumption
- Minimum instruction cycle time 300ns, 600ns, 1.2µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs can be switched by program (when using 10MHz main clock)

■Standby function
- HALT mode
  The HALT mode stops program execution while the peripheral circuits keep operating and minimizes power consumption. This operation mode can be released by a system reset or an interrupt request.

- HOLD mode
  The HOLD mode stops program execution and all oscillation circuits : CF, RC and Crystal oscillations.
  This mode can be released by the following conditions.
  1. Supply "L" level to the reset terminal ($\overline{RES}$)
  2. Supply the selected level to at lease one of INT0, INT1, INT2, INT4 INT5.
  3. Supply an interrupt condition to Port 0.

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- X'tal HOLD mode

  The X'tal HOLD mode stops program execution and all peripheral circuits except for the base timer.
  The crystal oscillator maintains its state at HOLD mode inception.
  This mode can be released by the following conditions.

  1. Supply "L" level to the reset terminal ($\overline{RES}$).
  2. Supply the selected level to at least one of INT0, INT1, INT2, INT4, INT5
  3. Supply an interrupt condition to Port 0.
  4. Supply an interrupt condition to the base timer circuit.

■Shipping form

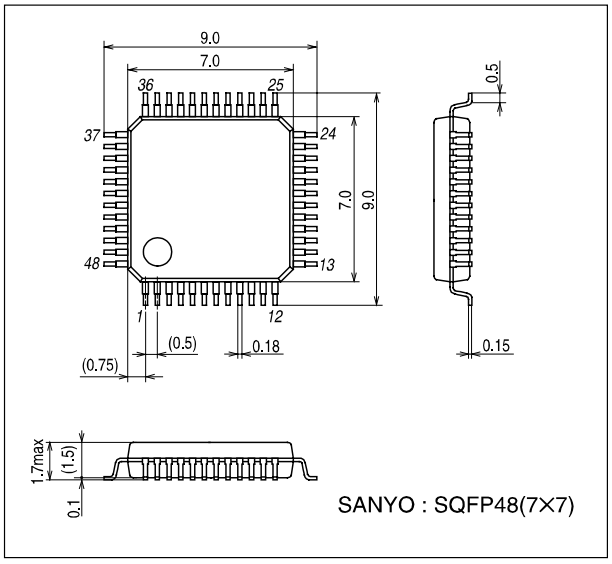
- QIP48E
- SQFP48

■Development tools

- Evaluation (EVA) chip : LC876093
- Emulator : EVA62S + ECB876600A + SUB875500 + POD48QFP
- Flash ROM writer adapter : W87F5564Q (QIP48E), W87F5564SQ (SQFP48)

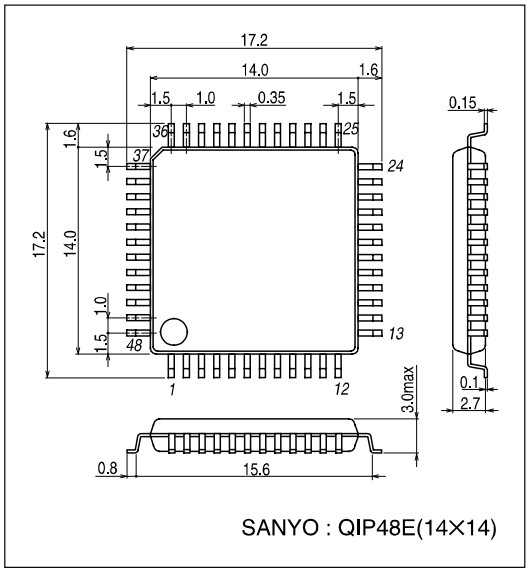
Package Dimensions

unit : mm
3163B

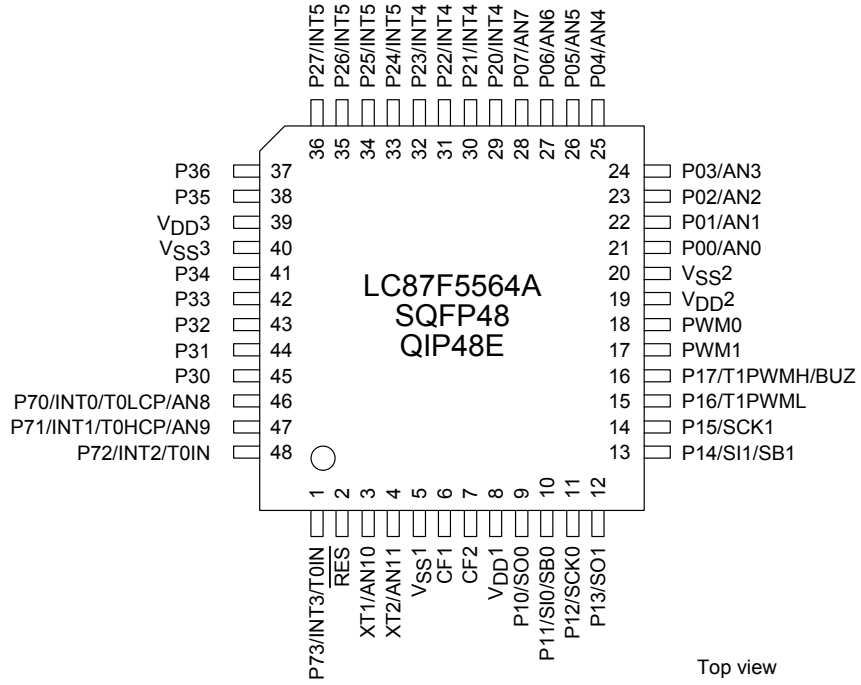


Package Dimensions

unit : mm
3156



Pin Assignment



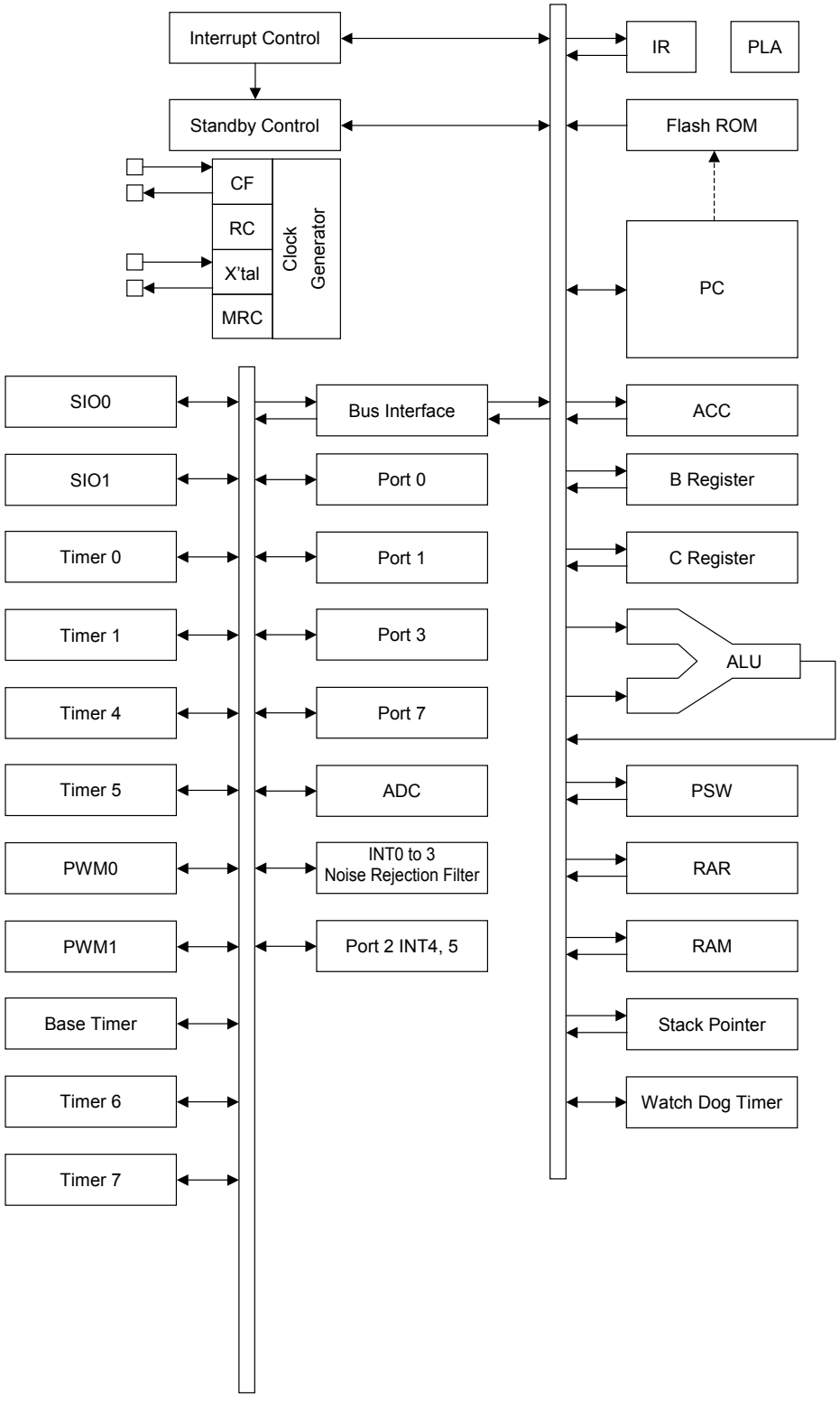
Top view

PAD Coordinate Values

SQFP/QIP	NAME
1	P73/INT3/T0IN
2	$\overline{\text{RES}}$
3	XT1/AN10
4	XT2/AN11
5	$V_{SS}1$
6	CF1
7	CF2
8	$V_{DD}1$
9	P10/SO0
10	P11/SI0/SB0
11	P12/SCK0
12	P13/SO1
13	P14/SI1/SB1
14	P15/SCK1
15	P16/T1PWML
16	P17/T1PWMH/BUZ
17	PWM1
18	PWM0
19	$V_{DD}2$
20	$V_{SS}2$
21	P00/AN0
22	P01/AN1
23	P02/AN2
24	P03/AN3

SQFP/QIP	NAME
25	P04/AN4
26	P05/AN5
27	P06/AN6
28	P07/AN7
29	P20/INT4
30	P21/INT4
31	P22/INT4
32	P23/INT4
33	P24/INT5
34	P25/INT5
35	P26/INT5
36	P27/INT5
37	P36
38	P35
39	$V_{DD}3$
40	$V_{SS}3$
41	P34
42	P33
43	P32
44	P31
45	P30
46	P70/INT0/T0LCP/AN8
47	P71/INT1/T0HCP/AN9
48	P72/INT2/T0IN

System Block Diagram



Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$, $V_{SS}3$</td><td>-</td><td>Power terminal (-)</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$, $V_{DD}3$</td><td>-</td><td>Power terminal (+)</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable in nibble units
• Pull-up resistor provided/not provided (specified in nibble units)
• HOLD release input
• Port 0 interrupt input
• AD converter input port : AN0 (P00) to AN7 (P07)</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P10 : SIO0 data output
P11 : SIO0 data input, bus input/output
P12 : SIO0 clock input/output
P13 : SIO1 data output
P14 : SIO1 data input, bus input/output
P15 : SIO1 clock input/output
P16 : Timer 1 PWML output
P17 : Timer 1 PWMH output/Buzzer output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P20 to P23 : INT4 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input
P24 to P27 : INT5 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input
• Interrupt detection style
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P36</td><td>I/O</td><td>• 7-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)</td><td>Yes</td></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P70 : INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer
P71 : INT1 input/HOLD release input/Timer 0H capture input
P72 : INT2 input/HOLD release input/Timer 0 event input/Timer 0L capture input
P73 : INT3 input with noise filter/Timer 0 event input/Timer 0H capture input
• Interrupt detection style
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>• AD converter input port : AN8 (P70), AN9 (P71)</td><td>No</td></tr>
<tr><td>PWM0</td><td>O</td><td>PWM0 output port</td><td>No</td></tr>
<tr><td>PWM1</td><td>O</td><td>PWM1 output port</td><td>No</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset terminal</td><td>No</td></tr>
</table>

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Pin name	I/O	Function	Option
XT1	I	• Input terminal for 32.768kHz X'tal oscillation • Other function AN10 : AD converter input port General input port When not in use, connect terminal to $V_{DD}1$.	No
XT2	I/O	• Output terminal for 32.768kHz X'tal oscillation • Other function AN11 : AD converter input port General input port When not in use, set as oscillation and leave terminal open	No
CF1	I	Input terminal for ceramic resonator	No
CF2	O	Output terminal for ceramic resonator	No

Port Output Configuration

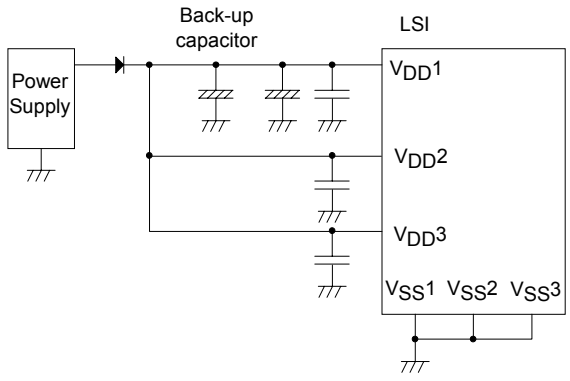
Output configuration and pull-up resistor options are shown in the following table.
Input is possible even when a port is in output mode.

Terminal	Option applies to :	Option	Output format	Pull-up resistor
P00 to P07	each bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	None
P10 to P17 P20 to P27 P30 to P36	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	None	Nch-open drain	Programmable
P71 to P73	-	None	CMOS	Programmable
PWM0, PWM1	-	None	CMOS	None
XT1	-	None	Input only	None
XT2	-	None	Output for 32.768kHz crystal oscillation	None

Note 1 : Programmable pull-up resistor of Port 0 is specified in nibble units (P00 to P03, P04 to P07).

Note : To reduce V_{DD} signal noise and to increase the duration of the backup battery supply, $V_{SS}1$, $V_{SS}2$ and $V_{SS}3$ should connect to each other and they should also be grounded.

Example 1 : During backup in hold mode, port output "H" level is supplied from the back-up capacitor.



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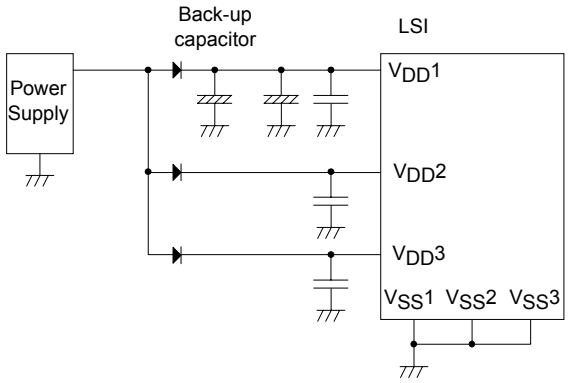
Example 2 : During backup in hold mode, output is not held high and its value in unsettled.



Absolute Maximum Ratings / Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pins	Conditions	Limits				
					V_{DD} [V]	min	typ	max	unit
Supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1 = V_{DD}2 = V_{DD}3$		-0.3		+6.5	V
Input voltage		V_I(1)	XT1, XT2, CF1			-0.3		V_{DD}+0.3	
Output voltage		V_O(1)	PWM0, PWM1			-0.3		V_{DD}+0.3	
Input/Output voltage		V_{IO}(1)	• Ports 0, 1, 2 • Ports 3, 7 • PWM0, PWM1			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	• Ports 0, 1, 2, 3 • PWM0, PWM1	• CMOS output • For each pin.		-10			mA
		IOPH(2)	P71 to P73	For each pin.		-5			
	Total output current	ΣIOAH(1)	P71 to P73	Total of all pins		-5			
		ΣIOAH(2)	• Port 1 • PWM0, PWM1	Total of all pins		-30			
		ΣIOAH(3)	Port 0	Total of all pins		-20			
		ΣIOAH(4)	Ports 2, 3	Total of all pins		-20			
Low level output current	Peak output current	IOPL(1)	• P02 to P07 • Ports 1, 2, 3 • PWM0, PWM1	For each pin.				20	
		IOPL(2)	P00, P01	For each pin.				30	
		IOPL(3)	Port 7	For each pin.				5	
	Total output current	ΣIOAL(1)	Port 7	Total of all pins				15	
		ΣIOAL(2)	• Port 1 • PWM0, PWM1	Total of all pins				50	
		ΣIOAL(3)	Port 0	Total of all pins				50	
		ΣIOAL(4)	Ports 2, 3	Total of all pins				40	
Maximum power consumption		Pd max	SQFP48	Ta = -20 to +70°C				199	mW
			QIP48E					338	
Operating temperature range		Topr				-20		70	°C
Storage temperature range		Tstg				-55		125	

Recommended Operating Range / Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
Operating supply voltage range	$V_{DD}(1)$	$V_{DD}1 = V_{DD}2 = V_{DD}3$	0.294µs ≤ tCYC ≤ 200µs		4.5		5.5	V
			0.588µs ≤ tCYC ≤ 200µs Except for on-board rewriting		2.5		5.5	
HOLD voltage	VHD	$V_{DD}1 = V_{DD}2 = V_{DD}3$	RAM and register data are kept in HOLD mode.		2.0		5.5	
Input high voltage	$V_{IH}(1)$	• Ports 1, 2, 3 • P71 to P73 • P70 port input/interrupt		2.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	• Port 0		2.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	Port 70 Watchdog timer		2.5 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 5.5	$0.75V_{DD}$		V_{DD}	
Input low voltage	$V_{IL}(1)$	• Ports 1, 2, 3 • P71 to P73 • P70 port input/interrupt		2.5 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
	$V_{IL}(2)$	• Port 0		2.5 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
	$V_{IL}(3)$	Port 70 Watchdog timer		2.5 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(4)$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 5.5	V_{SS}		$0.25V_{DD}$	
Operation cycle time	tCYC			4.5 to 5.5	0.294		200	µs
			Except for on-board rewriting	2.5 to 5.5	0.588		200	
External system clock frequency	FEXCF(1)	CF1	• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY = 50±5%	4.5 to 5.5	0.1		10	MHz
			• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY = 50±5%	2.5 to 5.5	0.1		5	
			• Leave CF2 pin open • System clock divider set to 1/2	4.5 to 5.5	0.2		20.4	
			• Leave CF2 pin open • System clock divider set to 1/2	2.5 to 5.5	0.1		10	
Oscillation frequency range	FmCF(1)	CF1, CF2	10MHz ceramic resonator oscillation Refer to figure 1	4.5 to 5.5		10		
	FmCF(2)	CF1, CF2	5MHz ceramic resonator oscillation Refer to figure 1	2.5 to 5.5		5		
	FmRC		RC oscillation	2.5 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.5 to 5.5		50		
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation Refer to figure 2	2.5 to 5.5		32.768		kHz

Note 1 : The oscillation parameters are shown on Tables 1 and 2.
Note 2 : $V_{DD} \geq 4.5V$ is required for on-board flash ROM rewriting.

Electrical Characteristics / Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
Input high current	$I_{IH}(1)$	• Ports 0, 1, 2 • Ports 3, 7 • $\overline{RES}$ • PWM0, PWM1	• Output disable • Pull-up resistor OFF • $V_{IN} = V_{DD}$ (Including the off-leak current of the output Tr.)	2.5 to 5.5			1	μA
	$I_{IH}(2)$	XT1, XT2	• Using as an input port • $V_{IN} = V_{DD}$	2.5 to 5.5			1	
	$I_{IH}(3)$	CF1	$V_{IN} = V_{DD}$	2.5 to 5.5			15	
Input low current	$I_{IL}(1)$	• Ports 0, 1, 2 • Ports 3, 7 • PWM0, PWM1	• Output disable • Pull-up resistor OFF • $V_{IN} = V_{SS}$ (Including the off-leak current of the output Tr.)	2.5 to 5.5	-1			
	$I_{IL}(2)$	XT1, XT2	• Using as an input port • $V_{IN} = V_{SS}$	2.5 to 5.5	-1			
	$I_{IL}(3)$	CF1	$V_{IN} = V_{SS}$	2.5 to 5.5	-15			
Output high voltage	$V_{OH}(1)$	• Ports 0, 1, 2, 3 • PWM0, PWM1	I_{OH} = -1.0mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH} = -0.1mA	2.5 to 5.5	V_{DD}-0.5			
	$V_{OH}(3)$	Ports 71, 72, 73	I_{OH} = -0.4mA	4.5 to 5.5	V_{DD}-1			
Output low voltage	$V_{OL}(1)$	• Ports 0, 1, 2, 3 • PWM0, PWM1	I_{OL} = 10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL} = 1.6mA	4.5 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL} = 1mA	2.5 to 5.5			0.4	
	$V_{OL}(4)$	P00, P01	I_{OL} = 30mA	4.5 to 5.5			1.5	
	$V_{OL}(5)$	Port 7	I_{OL} = 1mA	2.5 to 5.5			0.4	
	$V_{OL}(6)$							
Pull-up resistor	Rpu	• Ports 0, 1, 2, 3 • Port 7	$V_{OH} = 0.9V_{DD}$	2.5 to 5.5	15	40	70	kΩ
Hysteresis voltage	VHIS	• $\overline{RES}$ • Port 1 • Port 2 • Port 7		2.5 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	• All pins except the measured terminal : $V_{IN} = V_{SS}$ • f = 1MHz • Ta = 25°C	2.5 to 5.5		10		pF

Serial Input/Output Characteristics / Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter			Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
Serial clock	Input clock	Cycle	tSCK(1)	SCK0 (P12), SI2P2	Refer to figure 6	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
			tSCKLA(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)				3 (SIO0)			
		Cycle	tSCK(2)	SCK1 (P15)	Refer to figure 6	2.5 to 5.5	2			
		Low level pulse width	tSCKL(2)				1			
		High level pulse width	tSCKH(2)				1			
	Output clock	Cycle	tSCK(3)	SCK0 (P12), SI2P2 SI2P3	• CMOS output • Refer to figure 6	2.5 to 5.5	4/3			
		Low level pulse width	tSCKL(3)					1/2		tSCK
			tSCKLA(2)		SCK0 (P12) SIO0			3/4		
					SI2P2, SI2P3 SIO2			1		
		High level pulse width	tSCKH(3)					1/2		
			tSCKHA(2)		SCK0 (P12) SIO0			2		
		Cycle	tSCK(4)	SCK1 (P15)	• CMOS output • Refer to figure 6	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(4)					1/2		tSCK
		High level pulse width	tSCKH(4)					1/2		
Serial input	Data set-up time		tsDI	SB0 (P11), SB1 (P14), SI2P1 SI0, SI1	• Data set-up to SI0CLK • Data hold from SI0CLK • Refer to figure 6	2.5 to 5.5	0.03			µs
	Data hold time		thDI				0.03			
Serial output	Output delay time		tdD0	SO0 (P10), SO1 (P13), SB0 (O11), SB1 (P14), SI2P0 SI2P1	• Data hold from SI0CLK • Time delay from SI0CLK trailing edge to the SO data change in the open drain • Refer to figure 6	2.5 to 5.5			1/3tCYC +0.05	

Pulse Input Conditions / Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0 (P70), INT1 (P71), INT2 (P72) INT4 (P20 to P23) INT5 (P24 to P27)	• Interrupt acceptable • Timer 0 and 1 event input acceptable	2.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3 (P73) (The noise rejection clock is selected to 1/1.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3 (P73) (The noise rejection clock is selected to 1/32.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 5.5	64			
	tPIH(4) tPIL(4)	INT3 (P73) (The noise rejection clock is selected to 1/128.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 5.5	256			
	tPIL(5)	$\overline{RES}$	Reset acceptable	2.5 to 5.5	200			µs

AD Converter Characteristics / Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
Resolution	N	AN0 (P00) to AN7 (P07) AN8 (P70) AN9 (P71) AN10 (XT1) AN11 (XT2)		3.0 to 5.5		8		bit
Absolute precision	ET		(Note 2)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time = 32 × tCYC (ADCR2 = 0) (Note 3)	4.5 to 5.5	15.10 (tCYC = 0.588µs)		97.92 (tCYC = 3.06µs)	µs
				3.0 to 5.5	31.36 (tCYC = 0.980µs)		97.92 (tCYC = 3.06µs)	
			AD conversion time = 64 × tCYC (ADCR2 = 1) (Note 3)	4.5 to 5.5	18.82 (tCYC = 0.294µs)		97.92 (tCYC = 1.53µs)	
				3.0 to 5.5	62.72 (tCYC = 0.980µs)		97.92 (tCYC = 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN = V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN = V_{SS}	3.0 to 5.5	-1			

Note 2 : Absolute precision excludes the quantizing error (±1/2 LSB).

Note 3 : The conversion time is the time from executing the AD conversion instruction to setting the complete digital conversion value in the register.

Current Dissipation Characteristics / Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
Current drain during basic operation (Note 4)	IDDOP(1)	$V_{DD}1$ = $V_{DD}2$ = $V_{DD}3$	• FmCF = 10MHz by ceramic resonator • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF oscillation (10MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/1 divided	4.5 to 5.5		18	35	mA
	IDDOP(2)		• CF1 = 20MHz by external clock • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF1 oscillation (20MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		19	36	
	IDDOP(3)		• FmCF = 5MHz by ceramic resonator • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF oscillation (5MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/1divided	4.5 to 5.5		10	22	
	IDDOP(4)			2.5 to 4.5		5	15	
	IDDOP(5)		• FmCF = 0Hz (when oscillation stops) • FmX'tal = 32.768kHz by crystal oscillation • System clock : RC oscillation • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		2	8	
	IDDOP(6)			2.5 to 4.5		1	5	
	IDDOP(7)		• FmCF = 0Hz (when oscillation stops) • FmX'al = 32.768kHz by crystal oscillation • System clock : 1MHz with frequency variable RC oscilatin • Internal RC oscillation stops • 1/2 divided	4.5 to 5.5		2.5	13	
	IDDOP(8)			2.5 to 4.5		1.8	9	
	IDDOP(9)		• FmCF = 0Hz (when oscillation stops) • FmX'al = 32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		50	150	µA
	IDDOP(10)			2.5 to 4.5		30	120	
Current drain in HALT mode (Note 4)	IDDHALT(1)		• HALT mode • FmCF = 10MHz by ceramic resonator • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF oscillation (10MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/1 divided	4.5 to 5.5		4	10	mA
	IDDHALT(2)		• HALT mode • CF1 = 20MHz by external clock • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF1 oscillation (20MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		4.5	11	
	IDDHALT(3)		• HALT mode • FmCF = 5MHz by ceramic resonator • FmX'tal = 32.768kHz by crystal oscillation • System clock : CF oscillation (5MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/1divided	4.5 to 5.5		2	5	
	IDDHALT(4)			2.5 to 4.5		1	3.0	

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Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
Current drain in HALT mode (Note 4)	IDDHALT(5)	$V_{DD}1$ = $V_{DD}2$ = $V_{DD}3$	• HALT mode • FmCF = 0Hz (when oscillation stops) • FmX'tal = 32.768kHz by crystal oscillation • System clock : RC oscillation • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		0.5	1.5	mA
	IDDHALT(6)			2.5 to 4.5		0.3	1	
	IDDHALT(7)		• HALT mode • FmCF = 0Hz (when oscillation stops) • FmX'tal = 32.768kHz by crystal oscillation • System clock : 1MHz with frequency variable RC oscilatin • Internal RC oscillation stops • 1/2 divided	4.5 to 5.5		1.5	3.6	
	IDDHALT(8)			2.5 to 4.5		1.3	3.3	
	IDDHALT(9)		• HALT mode • FmCF = 0Hz (when oscillation stops) • FmX'tal = 32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		20	80	µA
	IDDHALT(10)			2.5 to 4.5		10	50	
Current drain during HOLD mode	IDDHOLD(1)	$V_{DD}1$	• HOLD mode • CF1 = V_{DD} or leave it open (when using external clock)	4.5 to 5.5		0.05	20	
	IDDHOLD(2)			2.5 to 4.5		0.01	15	
Current drain during time-base clock HOLD mode	IDDHOLD(3)	$V_{DD}1$	• Time-base clock HOLD mode • CF1 = V_{DD} or leave it open (when using external clock) • FmX'tal = 32.768kHz by crystal oscillation	4.5 to 5.5		15	70	
	IDDHOLD(4)			2.5 to 4.5		5	40	

Note 4 : The current of the output transistors and pull-up MOS transistors are excluded.

F-ROM Write Characteristics / Ta = +10°C to +55°C, $V_{SS}1$ = $V_{SS}2$ = $V_{SS}3$ = 0V

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
On-board writing current	IDDFW(1)	$V_{DD}1$	• 128-byte writing • Including erase time current	4.5 to 5.5		30	65	mA
Writing time	tFW(1)		• 128-byte writing • Including data erase time • Excluding time to fetch 128-byte data	4.5 to 5.5		5.0	10.0	mS

Main System Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions :

1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 1. Recommended circuit parameters for the main system clock using the ceramic resonator

Frequency	Manufacturer	Oscillator	Recommended circuit parameters			Operating supply voltage range	Oscillation stabilizing time		Note
			C1	C2	Rd1		typ	max	
10MHz	MURATA	CSLS10M0G53-B0	(15pF)	(15pF)	0Ω	4.5 to 5.5V	0.03ms	0.30ms	Internal C1, C2
		CSTCE10M0G52-R0	(10pF)	(10pF)	0Ω	4.5 to 5.5V	0.03ms	0.30ms	Internal C1, C2
5MHz	MURATA	CSTLS5M00G53-B0	(15pF)	(15pF)	0Ω	2.5 to 5.5V	0.03ms	0.30ms	Internal C1, C2
		CSTCR5M00G53-R0	(15pF)	(15pF)	0Ω	2.5 to 5.5V	0.03ms	0.30ms	Internal C1, C2

*The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (Refer to Figure 4)

Subsystem Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions :

1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 2. Recommended circuit parameters for the subsystem clock using the crystal oscillation

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Note
			C3	C4	Rf	Rd2		typ	max	
32.768kHz	SEIKO EPSON	MC-306	9pF	9pF	OPEN	820kΩ	2.5 to 5.5V	1.5s	3.0s	

*The oscillation stabilizing time is the period until the oscillation becomes stable, after executing the instruction which starts the sub-clock oscillator or after releasing a HOLD mode. (Refer to Figure 4)

Notes : Since the oscillation frequency precision is affected by the circuit pattern, place the oscillation related parts as close to the oscillation pins as possible, using the shortest possible pattern length.

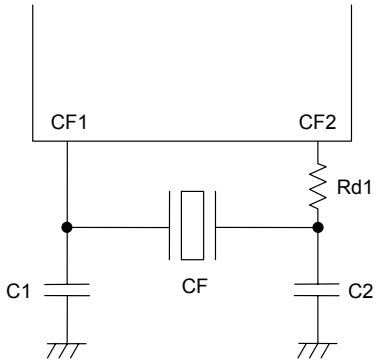


Figure 1 Ceramic oscillation circuit

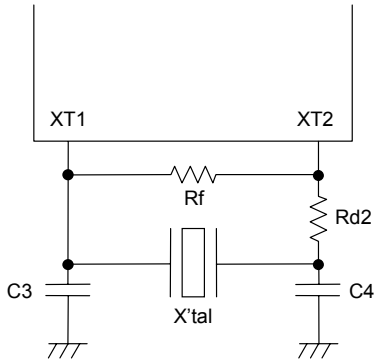


Figure 2 Crystal oscillation circuit

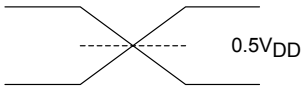
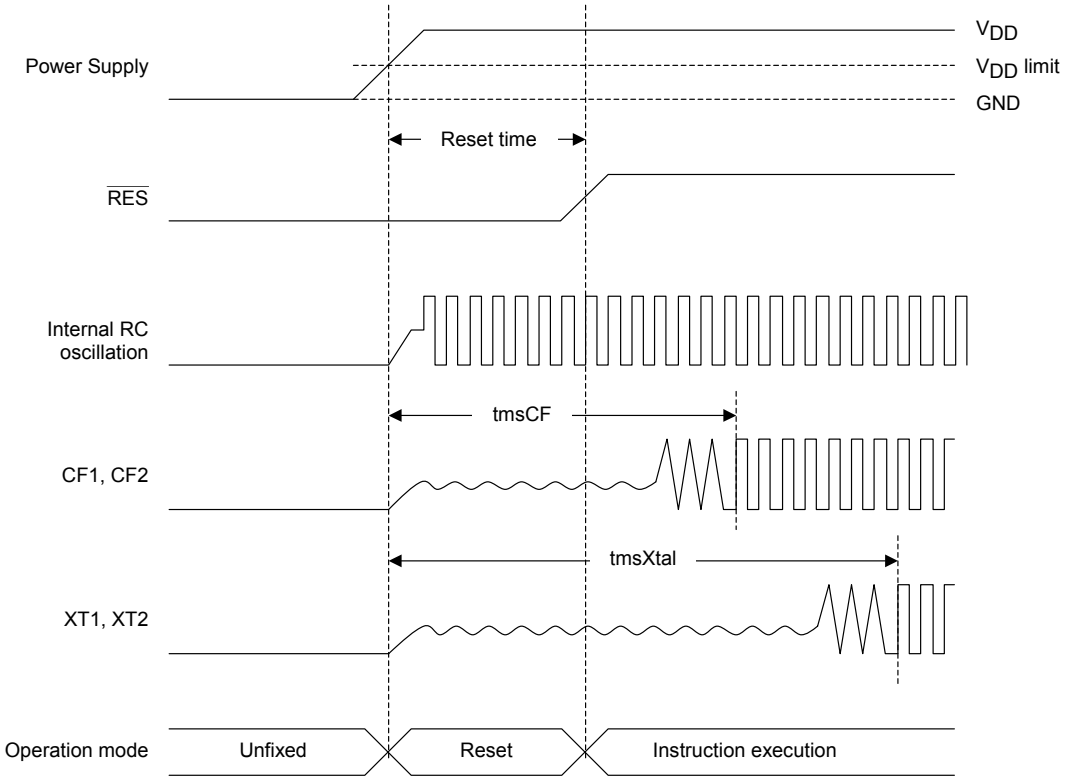
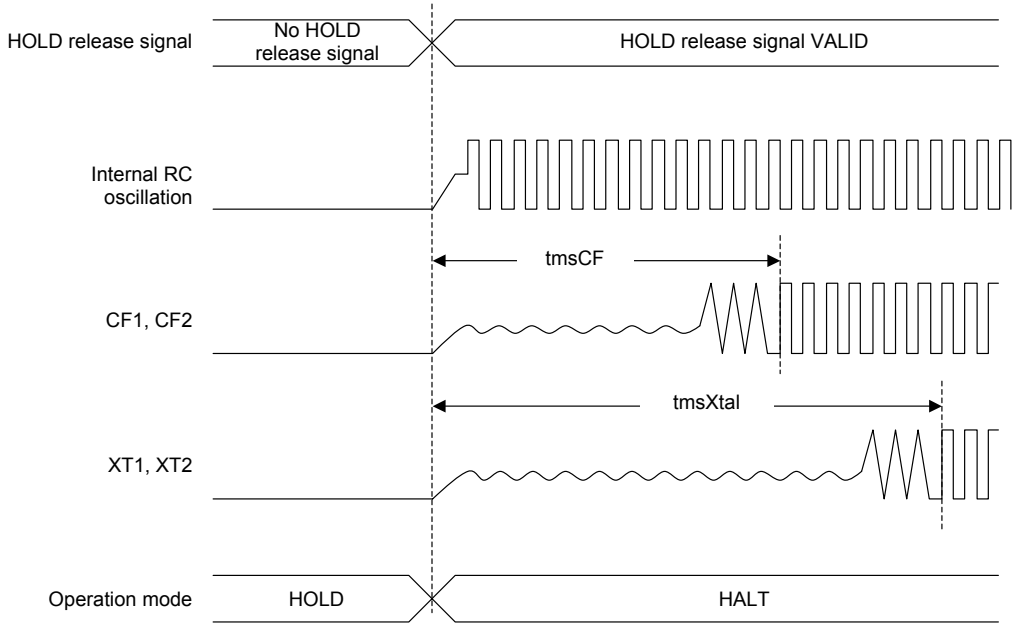


Figure 3 AC timing point

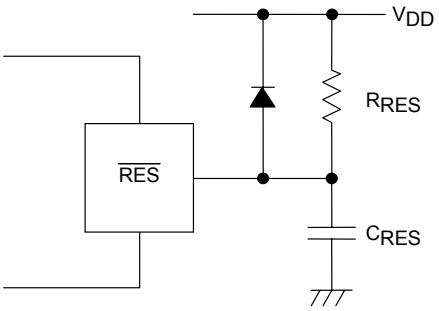


Reset time and oscillation stabilizing time



HOLD release signal and oscillation stabilizing time

Figure 4 Oscillation stabilizing time



(Note)
Select C_{RES} and R_{RES} value to assure that at least 200μs reset time is generated after the V_{DD} becomes higher than the minimum operating voltage.

Figure 5 Reset circuit

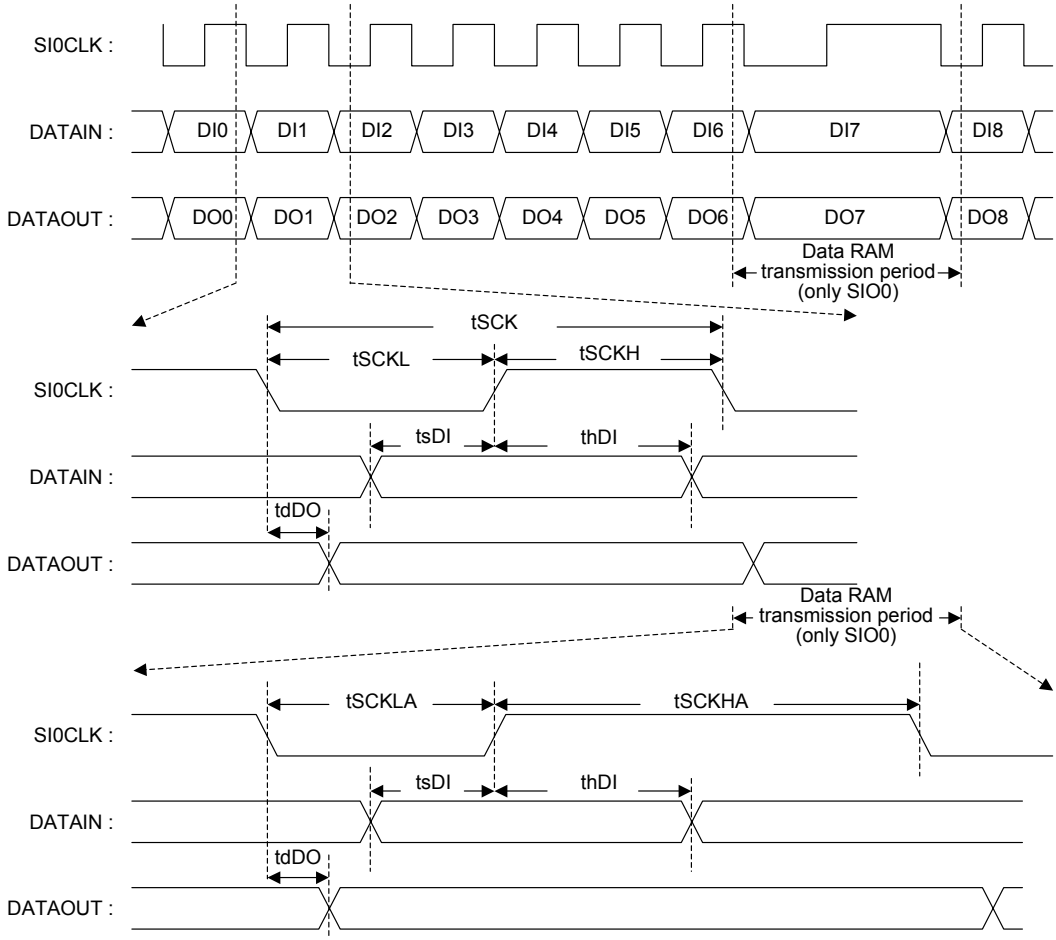


Figure 6 Serial input/output test condition

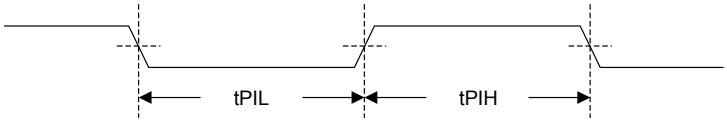


Figure 7 Pulse input timing condition