

SANYO Semiconductors DATA SHEET



CMOS IC FROM 98K byte, RAM 4096 byte on-chip 8-bit 1-chip Microcontroller

Overview

The SANYO LC87F5R96B is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 98K-byte flash ROM (onboard programmable), 4096-byte RAM, On-chip debugging function, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO port, two UART ports (full duplex), an 8-bit 11-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, and a 27-source 10-vector interrupt feature.

Features

■Flash ROM

- Capable of on-board-programing with wide range, 2.7 to 5.5V, of voltage source
- Block-erasable in 128 byte units
- 100352 × 8 bits (Address: 00000H to 17FFFH, 1F800H to 1FFFFH)

■RAM

• 4096 × 9 bits

■Minimum Bus Cycle Time

- 83.3ns (12MHz) V_{DD}=2.8 to 5.5V
- 125ns (8MHz) V_{DD}=2.5 to 5.5V
- 500ns (2MHz) V_{DD}=2.2 to 5.5V
- Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time (tCYC)

- 250ns (12MHz) V_{DD}=2.8 to 5.5V
- 375ns (8MHz) V_{DD}=2.5 to 5.5V
- 1.5µs (2MHz) V_{DD}=2.2 to 5.5V

■Ports

Normal withstand voltage I/O ports
 Ports whose I/O direction can be designated in 1-bit units
 46 (P1n, P2n, P3n, P70 to P73, P80 to P86, PCn, PWM2, PWM3, XT2)

 Ports whose I/O direction can be designated in 4-bit units
 Normal withstand voltage input port
 Dedicated oscillator ports
 Reset pins
 Power pins
 46 (P1n, P2n, P3n, P70 to P73, P80 to P86, PCn, PWM2, PWM3, XT2)
 CF1, CF2)
 RESET POWER PINS
 CF2, POWER PINS
 CF2, POWER PINS
 CF2, POWER PINS
 CF3, VDD1 to 3)

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SANYO Semiconductor Co., Ltd.

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■Timers

- Timer 0: 16-bit timer/counter with a capture register
 - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) ×2 channels
 - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)
 - + 8-bit counter (with an 8-bit capture register)
 - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
 - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)

Mode 1: 8-bit PWM with an 8-bit prescaler \times 2 channels

Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)

- (toggle outputs also possible from the lower-order 8-bits)
- Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
 - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
 - 2) Interrupts programmable in 5 different time schemes.

■High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 24MHz (at a main clock of 12MHz).
- 2) Can generate output real-time.

■SIO

- SIO0: 8-bit synchronous serial interface
 - 1) LSB first/MSB first mode selectable
 - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
 - 3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
 - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
 - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
 - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
 - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- ■UART: 2 channels
 - Full duplex
 - 7/8/9 bit data bits selectable
 - 1 stop bit (2 bit in continuous data transmission)
 - Built-in baudrate generator (with baudrates of 16/3 to 8192/3 tCYC)
- ■AD Converter: 8 bits × 11 channels
- ■PWM: Multifrequency 12-bit PWM × 2 channels

Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- 1) Noise filtering function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
- 2) The noise filtering function is available for the INT3, T0IN, or T0HCP signal at P73. When P73 is read with an instruction, the signal level at that pin is read regardless of the availability of the noise filtering function.
- ■Watchdog Timer
 - External RC watchdog timer
 - Interrupt and reset signals selectable

■Clock Output Function

- 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

■Interrupts

- 27 sources, 10 vector addresses
 - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INTO
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer0/base timer1
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/UART2 receive
8	0003BH	H or L	SIO/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 2048 levels (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions

- 16-bits \times 8-bits (5 tCYC execution time)
- 24-bits \times 16-bits (12 tCYC execution time)
- 16-bits ÷ 8-bits (8 tCYC execution time)
- 24-bits ÷ 16-bits (12 tCYC execution time)

■Oscillation Circuits

• CF oscillation circuit

- RC oscillation circuit (internal)
- : For system clock
- : For system clock, with internal Rf
- Crystal oscillation circuit
- : For low-speed system clock • Multifrequency RC oscillation circuit (internal) : For system clock

System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 250ns, 500ns, 1.0µs, 2.0µs, 4.0µs, 8.0µs, 16.0µs, 32.0µs, and 64.0µs (at a main clock rate of 12MHz).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC, and crystal oscillators automatically stop operation.
 - 2) There are three ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the lower level.
 - (2) Setting at least one of the INTO, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
 - 1) The CF and RC oscillators automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are four ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INTO, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established in the base timer circuit
- ■On-chip Debugger Function

• Permits software debugging with the test device installed on the target board.

- ■Package Form
 - QIP64E (14 × 14) : "Lead-free type"
- ■Development Tools
 - Evaluation (EVA) chip
 Emulator
 EVA62S + ECB876600D + SUB875M00 + POD64QFP

ICE-B877300 + SUB875M00 + POD64QFP

• On-chip-debugger : TCB87-TypeB + LC87F5R96B

■Programming Boards

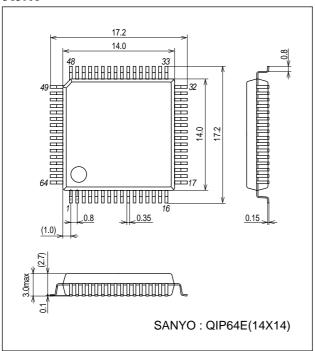
Package	Programming boards
QIP64E(14 × 14)	W87F50256Q

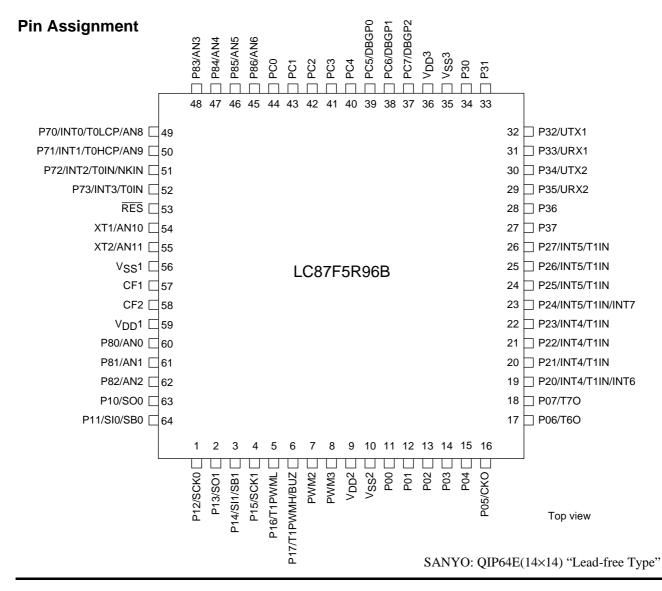
■Flash ROM Programmer

Maker	Model	Support version(Note)	Device
Flash Support Group, Inc.(Single)	AF9708/09/09B (including product of Ando Electric Co.,Ltd)	Revision : After Rev.02.73	LC87F76C8A
Flash Support	AF9723(Main body) (including product of Ando Electric Co.,Ltd)	Revision : After Rev.02.29	LC87F5NC8A
Group, Inc.(Gang)	AF9833(Unit) (including product of Ando Electric Co.,Ltd)	Revision : After Rev.01.88	LCOTFSINCOA
SANYO	SKK/SKK Type-B/SKK DBG Type-B (SANYO FWS)	Application Version: After 1.04 Chip Data Version: After2.11	LC87F5R96B

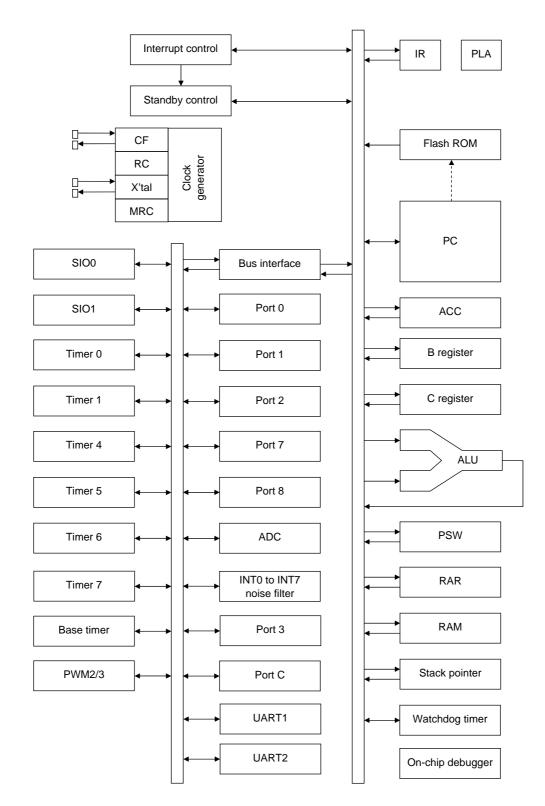
Package Dimensions

unit : mm (typ) 3159A





System Block Diagram



Pin Description

Pin Name	I/O			Des	scription			Op	otion
V _{SS} 1, V _{SS} 2 V _{SS} 3	-	- Power supply p	bin					1	No
V _{DD} 1, V _{DD} 2 V _{DD} 3	-	+ Power supply	pin					1	No
Port 0	I/O	8-bit I/O port						Y	/es
P00 to P07		 I/O specifiable 	in 4-bit units						
		 Pull-up resistor 	can be turned	on and off in 4-bi	it units				
		HOLD release	input						
		Port 0 interrupt	input						
	Shared Pins								
	P05: Clock output (system clock/can selected from sub clock)								
	P06: Timer 6 toggle output								
		P07: Timer 7 to	oggle output						
Port 1	I/O	8-bit I/O port						Y	res
P10 to P17		I/O specifiable							
		Pull-up resistor	can be turned	on and off in 1-bi	it units				
		Pin functions							
		P10: SIO0 data	•						
		P11: SIO0 data P12: SIO0 cloc	•						
		P12: SIOU Cloc P13: SIO1 data							
		P14: SIO1 data	-						
		P15: SIO1 cloc	•						
		P16: Timer 1 P							
			WMH output/be	eper output					
Port 2	I/O	8-bit I/O port						Y	/es
P20 to P27		 I/O specifiable 	in 1-bit units						
1 20 10 1 27		Pull-up resistor	can be turned	on and off in 1-bi	it units				
		Other functions	6						
		P20: INT4 inpu	t/HOLD reset ir	put/timer 1 even	t input/timer 0L o	capture input/			
		timer 0H	capture input/IN	IT6 input/timer 0I	L capture 1 input	t			
		P21 to P23: IN	T4 input/HOLD	reset input/timer	1 event input/tin	ner 0L capture ir	nput/		
		timer 0H	capture input						
		P24: INT5 inpu	t/HOLD reset ir	put/timer 1 even	t input/timer 0L o	capture input/			
		timer 0H	capture input/IN	IT7 input/timer 0	H capture 1 inpu	t			
		P25 to P27: IN	T5 input/HOLD	reset input/timer	1 event input/tin	ner 0L capture ir	nput/		
			capture input						
		 Interrupt acknowledge 	wledge type				1		
			Rising	Falling	Rising/ Falling	H level	L level		
		INT4	enable	enable	enable	disable	disable		
	1	INT5	enable	enable	enable	disable	disable		
		1110	onabio	01101010					
		INT6	enable	enable	enable	disable	disable		

Continued on next page.

I/O			Des	cription			Option	
I/O	• 4-bit I/O port						No	
	I/O specifiable in 1-bit units							
	Pull-up resistor can be turned on and off in 1-bit units							
	Shared Pins							
	P70: INT0 inpu	t/HOLD reset in	put/timer 0L capt	ure input/watchc	log timer output			
	P71: INT1 inpu	t/HOLD reset in	put/timer 0H cap	ure input				
	P72: INT2 inpu	t/HOLD reset in	put/timer 0 event	input/timer 0L c	apture input/			
	high spee	d clock counter	input					
	P73: INT3 inpu	t (with noise filte	er)/timer 0 event i	nput/timer 0H ca	apture input			
	AD converter in	put port: AN8 (F	P70), AN9 (P71)					
	 Interrupt ackno 	wledge type						
		Rising	Falling	Rising/ Falling	H level	L level		
	INT0	enable	enable	disable	enable	enable		
	INT1	enable	enable	disable	enable	enable		
	INT2	enable	enable	enable	disable	disable		
	INT3	enable	enable	enable	disable	disable		
I/O	• 7-bit I/O port						No	
	• I/O specifiable	in 1-bit units						
	Shared Pins							
	AD converter in	put port : AN0 (P80) to AN6 (P8	6)				
I/O	• PWM2 and PW	M3 output ports	5				No	
	General-purpos	se I/O available						
I/O	8-bit I/O port						Yes	
	 I/O specifiable 	in 1-bit units						
	Pull-up resistor can be turned on and off in 1-bit units							
	 Pin functions 							
	P32: UART1 transmit							
		ceive						
I/O							Yes	
		can be turned o	on and off in 1-bit	units				
			N. On chin Dohu					
lanut		P2(PC5 10 PC7): On-chip Debu	Jgei			No	
input							No	
	+ + 22 760kl la en/6	stal oscillator inp	out pin				No	
Input	-							
Input	Shared pins							
Input	Shared pins General-purpos							
Input	 Shared pins General-purpos AD converter in 	put port : AN10						
	Shared pins General-purpos AD converter in Must be conner	put port : AN10 cted to V _{DD} 1 if	not to be used.				No	
Input I/O	Shared pins General-purpos AD converter in Must be conner 32.768kHz crys	put port : AN10 cted to V _{DD} 1 if	not to be used.				No	
	Shared pins General-purpos AD converter in Must be conner 32.768kHz crys Shared pins	put port : AN10 cted to V _{DD} 1 if i stal oscillator inp	not to be used.				No	
	 Shared pins General-purpos AD converter in Must be connet 32.768kHz crys Shared pins General-purpos 	put port : AN10 <u>cted to V_{DD}1 if</u> stal oscillator inp se I/O port	not to be used.				No	
	Shared pins General-purpos AD converter in Must be conner 32.768kHz crys Shared pins General-purpos AD converter in	put port : AN10 cted to V _{DD} 1 if stal oscillator inp se I/O port sput port : AN11	not to be used. out pin) be used			No	
	Shared pins General-purpos AD converter in Must be conner 32.768kHz crys Shared pins General-purpos AD converter in	put port : AN10 cted to V _{DD} 1 if ttal oscillator inp se I/O port put port : AN11 oscillation and I	not to be used.	o be used.			No	
	I/O I/O	I/O 4-bit I/O port I/O specifiable i Pull-up resistor Shared Pins P70: INT0 input P71: INT1 input P72: INT2 input high spee P73: INT3 input AD converter in INT0 INT1 INT1 INT2 INT0 INT1 INT1 INT2 INT1 INT2 INT3 INT1 INT2 INT3 I/O • 7-bit I/O port I/O • 8-bit I/O port I/O • PWM2 and PW • General-purpos I/O I/O • 8-bit I/O port I/O • 8-bit I/O port	I/O • 4-bit I/O port I/O specifiable in 1-bit units • Pull-up resistor can be turned of • Shared Pins P70: INTO input/HOLD reset in P71: INT1 input/HOLD reset in P71: INT1 input/HOLD reset in P72: INT2 input/HOLD reset in P71: INT3 input (with noise filte AD converter input port: AN8 (f • Interrupt acknowledge type INT0 enable INT1 enable INT2 enable INT3 enable INT2 enable INT3 enable INT4 enable INT5 enable INT2 enable INT3 enable INT3 enable INT3 enable INT4 enable INT5 enable INT6 senable INT7 enable INT5 enable INT6 senable INT5 enable INT6 senable INT5 enable INT6 senable IN70 senaitI/O port	I/O • 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit • Shared Pins P70: INT0 input/HOLD reset input/timer 0L capt P71: INT1 input/HOLD reset input/timer 0 event high speed clock counter input P73: INT3 input (with noise filter)/timer 0 event i AD converter input port: AN8 (P70), AN9 (P71) • Interrupt acknowledge type INT0 enable INT1 enable INT2 enable INT2 enable INT2 enable INT3 enable INT2 enable INT3 enable INT2 enable INT3 enable INT3 enable INT2 enable INT3 enable INT4 enable INT5 enable INT2 enable INT3 enable INT4 enable INT5 Shared Pins AD converter input port : AN0 (P80) to AN6 (P80 I/O * Bit I/O port	I/O 4-bit I/O port I/O specifiable in 1-bit units Pull-up resistor can be turned on and off in 1-bit units Shared Pins P70: INT0 input/HOLD reset input/timer 0L capture input P71: INT1 input/HOLD reset input/timer 0 event input/timer 0L c high speed clock counter input P73: INT3 input (with noise filter)/timer 0 event input/timer 0H ca AD converter input port: AN8 (P70), AN9 (P71) Interrupt acknowledge type INT0 enable INT1 enable INT2 enable INT1 enable INT2 enable INT1 enable INT2 enable INT2 enable enable enable INT2 enable INT2 enable INT2 enable INT3 enable INT2 enable INT3 enable INT2 enable INT3 enable INT4 enable INT5 enable INT6 enable INT8	I/O • 4-bit I/O port I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Shared Pins P70: INT0 input/HOLD reset input/timer 0L capture input P71: INT1 input/HOLD reset input/timer 0H capture input P72: INT2 input/WolD reset input/timer 0 event input/timer 0L capture input P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input AD converter input port: AN8 (P70), AN9 (P71) • Interrupt acknowledge type INT0 enable INT1 enable INT2 enable INT3 enable INT4 enable INT5 enable INT4 enable INT5 enable INT4 enable INT5 enable INT6 <td< td=""><td>I/O • 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Shared Pins P70: INT0 input/HOLD reset input/timer 0L capture input/ P71: INT1 input/HOLD reset input/timer 0 event input/timer 0L capture input/ high speed clock counter input P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input AD converter input port: AN8 (P70), AN9 (P71) • Interrupt acknowledge type INT0 enable INT1 enable enable enable disable enable INT2 enable enable enable enable enable enable enable enable enable INT2 enable enable enable enable enable enable enable disable disable INT3 enable enable enable enable enable disable disable INT3 enable O specifiable in 1-bit u</td></td<>	I/O • 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Shared Pins P70: INT0 input/HOLD reset input/timer 0L capture input/ P71: INT1 input/HOLD reset input/timer 0 event input/timer 0L capture input/ high speed clock counter input P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input AD converter input port: AN8 (P70), AN9 (P71) • Interrupt acknowledge type INT0 enable INT1 enable enable enable disable enable INT2 enable enable enable enable enable enable enable enable enable INT2 enable enable enable enable enable enable enable disable disable INT3 enable enable enable enable enable disable disable INT3 enable O specifiable in 1-bit u	

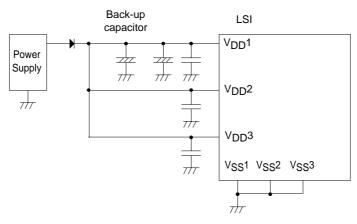
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

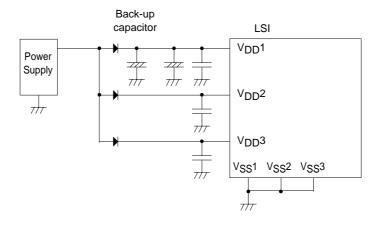
Port	Options Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P37	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P86	-	No	Nch-open drain	No
PWM2, PWM3	-	No	CMOS	No
PC0 to PC7	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
XT1	-	No	Input for 32.768kHz crystal oscillator (Input only)	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

⁽Example 1) When backup is active in the HOLD mode, the high level of the port outputs is supplied by the backup capacitors.



(Example 2) The high-level output at the ports is unstable when the HOLD mode backup is in effect.



^{*1:} Make the following connection to minimize the noise input to the V_{DD}1 pin and prolong the backup time. Be sure to electrically short the V_{SS}1, V_{SS}2, and V_{SS}3 pins.

Absolute Maximum Ratings at $Ta = 25^{\circ}C$, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

	Parameter	Symbol	Pins/Remarks	Conditions		ļ,	Spec	ification	
		V _{DD} [V] r		min	typ	max	un		
	ximum supply tage	V _{DD} max	V _{DD} 1, V _{DD} 2, V _{DD} 3	V _{DD} 1=V _{DD} 2=V _{DD} 3		-0.3		+6.5	
Input voltage		V _I (1)	XT1, CF1			-0.3		V _{DD} +0.3	
Inp	ut/Output voltage	V _{IO} (1) Ports 0, 1, 2 Ports 7, 8 Ports 3, C PWM0, PWM1, XT2				-0.3		V _{DD} +0.3	V
	Peak output current	IOPH(1)	Ports 0, 1, 2 Ports 3, C	CMOS output select Per 1 application pin		-10			
		IOPH(2)	PWM2, PWM3	Per 1 application pin.		-20			
		IOPH(3)	P71 to P73	Per 1 application pin.		-5			
t	Mean output current	IOMH(1)	Ports 0, 1, 2 Ports 3, C	CMOS output select Per 1 application pin		-7.5			
rrent	(Note1-1)	IOMH(2)	PWM2, PWM3	Per 1 application pin		-10			
ut cu		IOMH(3)	P71 to P73	Per 1 application pin		-3			
outpi	Total output	ΣIOAH(1)	P71 to P73	Total of all applicable pins		-10			
High level output current	current	ΣIOAH(2)	Port 1 PWM2, PWM3	Total of all applicable pins		-25			
High		ΣIOAH(3)	Ports 0, 2	Total of all applicable pins		-25			
		ΣIOAH(4)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins		-45			
		ΣIOAH(5)	Port 3	Total of all applicable pins		-25			
		ΣIOAH(6)	Port C	Total of all applicable pins		-25			
		ΣIOAH(7)	Ports 3, C	Total of all applicable pins		-45			
	Peak output	IOPL(1)	P02 to P07	Per 1 application pin.					
	current		Ports 1, 2 Ports 3, C PWM2, PWM3					20	m
		IOPL(2)	P00, P01	Per 1 application pin.				30	
		IOPL(3)	Ports 7, 8, XT2	Per 1 application pin.				10	
rrent	Mean output current (Note1-1)	IOML(1)	P02 to P07 Ports 1, 2 Ports 3, C PWM2, PWM3	Per 1 application pin.				15	
curr		IOML(2)	P00, P01	Per 1 application pin.				20	
tput		IOML(3)	Ports 7, 8, XT2	Per 1 application pin.				7.5	
Low level output cui	Total output current	ΣIOAL(1)	Port 7 P83 to P86, XT2	Total of all applicable pins				15	
-ow		ΣIOAL(2)	P80 to P82	Total of all applicable pins				15	
-		ΣIOAL(3)	Ports 7, 8, XT2	Total of all applicable pins				20	
		ΣIOAL(4)	Port 1 PWM2, PWM3	Total of all applicable pins				45	
		ΣIOAL(5)	Ports 0, 2	Total of all applicable pins				45	
		ΣIOAL(6)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins				80	
		ΣIOAL(7)	Port 3	Total of all applicable pins				45	
		ΣIOAL(8)	Port C	Total of all applicable pins				45	
		ΣIOAL(9)	Ports 3, C	Total of all applicable pins				80	
Po	wer dissipation	Pd max	QIP64E(14×14)	Ta=-40 to +85°C				300	m
•	erating ambient	Topr				-40		+85	° (
	orage ambient	Tstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Deremeter	Cumhal	Pins/Remarks	Conditions			Specif	ication		
Parameter	Symbol	Pins/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
Operating	V _{DD} (1)	V _{DD} 1=V _{DD} 2=V _{DD} 3	0.245µs≤ tCYC≤200µs		2.8		5.5		
supply voltage			0.367µs≤ tCYC≤200µs		2.5		5.5		
(Note2-1)			1.47μs≤ tCYC≤200μs		2.2		5.5		
Memory sustaining supply voltage	VHD	V _{DD} 1=V _{DD} 2=V _{DD} 3	RAM and register contents sustained in HOLD mode		2.0		5.5		
High level input voltage	V _{IH} (1)	Ports 1, 2 P71 to P73 P70 port input/ interrupt side		2.2 to 5.5	0.3V _{DD} +0.7		V _{DD}		
	V _{IH} (2)	Ports 0, 8, 3, C PWM2, PWM3		2.2 to 5.5	0.3V _{DD} +0.7		V _{DD}		
	V _{IH} (3)	Port P70 watchdog timer side		2.2 to 5.5	0.9V _{DD}		V _{DD}	V	
	V _{IH} (4)	XT1, XT2, CF1, RES		2.2 to 5.5	0.75V _{DD}		V _{DD}		
Low level input voltage	∨ _{IL} (1)	Ports 1, 2 P71 to P73		4.0 to 5.5	V _{SS}		0.1V _{DD} +0.4		
		P70 port input/ Interrupt side		2.2 to 4.0	V _{SS}		0.2V _{DD}		
	V _{IL} (2)	Ports 0, 8, 3, C PWM2, PWM3		4.0 to 5.5	V _{SS}		0.15V _{DD} +0.4		
				2.2 to 5.5	VSS		0.2V _{DD}		
	V _{IL} (3)	Port 70 watchdog timer side		2.2 to 5.5	V _{SS}		0.8V _{DD} -1.0		
	V _{IL} (4)	XT1, XT2, CF1, RES		2.2 to 5.5	VSS		0.25V _{DD}		
Instruction cycle	tCYC			2.8 to 5.5	0.245		200		
time					2.5 to 5.5	0.367		200	μs
(Note2-2)				2.2 to 5.5	1.47		200		
External system	FEXCF(1)	CF1	CF2 pin open	2.8 to 5.5	0.1		12		
clock frequency			System clock frequency	2.5 to 5.5	0.1		8		
			 division rate=1/1 External system clock duty=50±5% 	2.2 to 5.5	0.1		2	MHz	
			CF2 pin open	2.8 to 5.5	0.2		24.4		
			System clock frequency	2.5 to 5.5	0.1		16		
			division rate=1/2	2.2 to 5.5	0.1		4		
Oscillation frequency	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	2.8 to 5.5		12			
range (Note2-3)	FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		8			
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		4		MHz	
	FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0]	
	FmMRC		Frequency variable RC oscillation	2.5 to 5.5		16			
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.2 to 5.5		32.768		kHz	

Allowable Operating Conditions at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Note 2-1: V_{DD} must be held greater than or equal to 2.7V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Parameter	Symbol	Pins/Remarks	Conditions			Specific	ation	
Parameter	Symbol	Pins/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High level input current	I _{IH} (1)	Ports 0, 1, 2 Ports 7, 8 Ports 3, C RES PWM2, PWM3	Output disabled Pull-up resistor off VIN=VDD (Including output Tr's off leakage current))	2.2 to 5.5			1	
	I _{IH} (2)	XT1, XT2	For input port specification VIN=VDD	2.2 to 5.5			1	
	I _{IH} (3)	CF1	V _{IN} =V _{DD}	2.2 to 5.5			15	1.
Low level input current	I _{IL} (1)	Ports 0, 1, 2 Ports 7, 8 Ports 3, C RES PWM2, PWM3	Output disabled Pull-up resistor off VIN=VSS (Including output Tr's off leakage current))	2.2 to 5.5	-1			μΑ
	I _{IL} (2)	XT1, XT2	For input port specification VIN=VSS	2.2 to 5.5	-1			
	I _{IL} (3)	CF1	VIN=VSS	2.2 to 5.5	-15			
High level output	V _{OH} (1)	Ports 0, 1, 2	I _{OH} =-1mA	4.5 to 5.5	V _{DD} -1			
voltage	V _{OH} (2)	Ports 3, C	I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (3)		I _{OH} =-0.2mA	2.2 to 5.5	V _{DD} -0.4			
	V _{OH} (4)	Ports 71 to 73	I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (5)		I _{OH} =-0.2mA	2.2 to 5.5	V _{DD} -0.4			
	V _{OH} (6)	PWM2, PWM3	I _{OH} =-10mA	4.5 to 5.5	V _{DD} -1.5			
	V _{OH} (7)		I _{OH} =-1.6mA	3.0 to 5.5	V _{DD} -0.4			v
	V _{OH} (8)		I _{OH} =-1mA	2.2 to 5.5	V _{DD} -0.4			
Low level output	V _{OL} (1)	Ports 0, 1, 2	I _{OL} =10mA	4.5 to 5.5			1.5	
voltage	V _{OL} (2)	Ports 3, C	I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (3)	PWM2, PWM3,	I _{OL} =1mA	2.2 to 5.5			0.4	
	V _{OL} (4)	Ports 7, 8	I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (5)	XT2	I _{OL} =1mA	2.2 to 5.5			0.4	
	V _{OL} (6)	P00, P01	I _{OL} =30mA	4.5 to 5.5			1.5	
	V _{OL} (7)		I _{OL} =5mA	3.0 to 5.5			0.4	
	V _{OL} (8)		I _{OL} =2.5mA	2.2 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 7	V _{OH} =0.9V _{DD}	4.5 to 5.5	15	35	80	
	Rpu(2)	Ports 3, C		2.2 to 5.5	18	35	150	kΩ
Hysteresis voltage	VHYS	RES Ports 1, 2, 7		2.2to 5.5		0.1V _{DD}		v
Pin capacitance	СР	All pins	 For pins other than that under test: V_{IN}=V_{SS} f=1MHz Ta=25°C 	2.2 to 5.5		10		pF

Electrical Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Serial I/O Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$ 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter		Oursels al	Pins	Openditions		Specification			
Pa	arameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 6.		2			
×	Low level pulse width	tSCKL(1)				1			
put cloo	High level pulse width	tSCKH(1)			2.2 to 5.5	1			101/0
Ч		tSCKHA(1)		Continuous data transmission/reception mode See Fig. 6. (Note 4-1-2)		4			tCYC
	Frequency	tSCK(2)	SCK0(P12)	CMOS output selected See Fig. 6.		4/3			
ck	Low level pulse width	tSCKL(2)					1/2		10.01/
itput clo	High level pulse width	tSCKH(2)			2.2 to 5.5		1/2		tSCK
ŋ		tSCKHA(2)		Continuous data transmission/reception mode CMOS output selected See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Da	ta setup time	tsDI(1)	SB0(P11), SI0(P11)	 Must be specified with respect to rising edge of SIOCLK See fig. 6. 	2.2 to 5.5	0.03			
Da	ita hold time	thDI(1)			2.2 to 5.5	0.03			
clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11),	Continuous data transmission/reception mode (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.05	
Input		tdD0(2)		Synchronous 8-bit mode (Note 4-1-3)	2.2 to 5.5			1tCYC +0.05	μs
Output clock		tdD0(3)		• (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.15	
	Input clock	Low level pulse width High level pulse width High level pulse width Korr Korr High level pulse width Heigh level pulse width	Image: second	Image: section of the sectio	Image: Note of the section of the s	Image: continuence of the continue	Image: setup time Image: setup time	Image: set prime page page: page width light level pulse width pulse width pulse width pulse width pulse width pulse width pulse width pulse width pulse width image width 	Image Image <t< td=""></t<>

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIORUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

	р	arameter	Symbol	Pins/	Conditions		Specification				
	F	Remarks		Conditions	V _{DD} [V]	min	typ	max	unit		
	×	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 6.		2				
	Input clock	Low level pulse width	tSCKL(3)			2.2 to 5.5	1				
clock	lı	High level pulse width	tSCKH(3)				1			tCYC	
Serial clock	ock	Frequency	tSCK(4)	SCK1(P15)	CMOS output selected. See Fig. 6.		2				
	Output clock	Low level pulse width	tSCKL(4)			2.2 to 5.5	1/2			tSCK	
	õ	High level pulse width	tSCKH(4)					1/2		tSCK	
Serial input	Data setup time		tsDI(2)	SB1(P14) SI1(P14),	 Must be specified with respect to rising edge of SIOCLK See fig. 6. 		0.03				
Serial	Da	ta hold time	thDI(2)	-		2.2 to 5.5	0.03				
Serial output	Ou tim	itput delay ie	tdD0(4)	SO1(P13), SB1(P14)	 Must be specified with respect to falling edge of SIOCLK Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6. 	2.2 to 5.5			(1/3)tCYC +0.05	μs	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Parameter	Cumb al	Pins/Remarks	Conditions			Speci	fication	ication			
Parameter	Symbol	Pins/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit			
High/low level	tPIH(1)	INT0(P70),	 Interrupt source flag can be set. 								
pulse width	tPIL(1)	INT1(P71),	Event inputs for timer 0 or 1 are								
		INT2(P72)	enabled.		2 to 5.5 1						
		INT4(P20 to P23),		2.2 to 5.5							
		INT5(P24 to P27),									
		INT6(P20)									
		INT7(P24)						tCYC			
	tPIH(2)	INT3(P73) when noise filter	 Interrupt source flag can be set. 	2.2 to 5.5	2						
	tPIL(2)	time constant is 1/1.	• Event inputs for timer 0 are enabled.	2.2 10 5.5	2						
	tPIH(3)	INT3(P73) when noise filter	 Interrupt source flag can be set. 	2.2 to 5.5	64						
	tPIL(3)	time constant is 1/32	• Event inputs for timer 0 are enabled.	2.2 10 5.5	64						
	tPIH(4)	INT3(P73) when noise filter	 Interrupt source flag can be set. 	2.2 to 5.5	256						
	tPIL(4)	time constant is 1/128	• Event inputs for timer 0 are enabled.	2.2 to 5.5	256						
	tPIL(5)	RES	Resetting is enabled.	2.2 to 5.5	200			μs			

AD Converter Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

					~~			
	0	Pins/Remarks				Specifi	cation	
Parameter	Symbol	Pins/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to		3.0 to 5.5		8		bit
Absolute accuracy	ET	AN6(P86), AN8(P70),	(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD	AN9(P71), AN10(XT1), AN11(XT2),	AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	11.74 (tCYC= 0.367µs)		97.92 (tCYC= 3.06μs)	
				3.0 to 5.5	23.53 (tCYC= 0.735μs)		97.92 (tCYC= 3.06μs)	
			AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	15.68 (tCYC= 0.245μs)		97.92 (tCYC= 1.53μs)	μs
				3.0 to 5.5	23.49 (tCYC= 0.376μs)		97.92 (tCYC= 1.53μs)	
Analog input voltage range	VAIN	1		3.0 to 5.5	V _{SS}		V _{DD}	V
Analog port	IAINH]	VAIN=V _{DD}	3.0 to 5.5			1	
input current	IAINL		VAIN=V _{SS}	3.0 to 5.5	-1			μA

Note 6-1: The quantization error ($\pm 1/2$ LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

Consumption Current Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins/Remarks	Conditions			Specifi	ation				
Falametei	Symbol	FIIIS/ITEIIIdIKS	Conditions	V _{DD} [V]	min	typ	max	unit			
Normal mode consumption current	IDDOP(1)	V _{DD} 1 =V _{DD} 2 =V _{DD} 3	FmCF=12MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		9.1	18.5				
(Note 7-1)			 System clock set to 12MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. 	2.8 to 4.5		5.3	13.5				
	IDDOP(2)		FmCF=8MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		6.7	14				
	IDDOP(3)		 System clock set to 8MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. 	2.5 to 4.5		3.8	10				
	IDDOP(4)		FmCF=4MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode Crystem class costs 400 km side	4.5 to 5.5		2.7	6	mA			
	IDDOP(5)		 System clock set to 4MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. 	2.2 to 4.5		1.45	3.8				
	IDDOP(6)		FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		0.95	4.3				
	IDDOP(7)		 System clock set to internal RC oscillation frequency variable RC oscillation stopped 1/2 frequency division ratio. 	2.2 to 4.5		0.53	3.0				
	IDDOP(8)		FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode. Conservation state 444 by with foreseenergy.	4.5 to 5.5		1.25	5.2				
	IDDOP(9)		 System clock set to 1MHz with frequency variable RC oscillation Internal RC oscillation stopped 1/2 frequency division ratio. 	2.2 to 4.5		0.67	4.2				
	IDDOP(10)		FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode. Syndem cleak cet to 22.768kHz bids	4.5 to 5.5		38	112				
	IDDOP(11)		 System clock set to 32.768kHz side. Internal RC oscillation stopped frequency variable RC oscillation stopped 1/2 frequency division ratio. 	2.2 to 4.5		19	72	μA			
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V _{DD} 1 =V _{DD} 2 =V _{DD} 3	 HALT mode FmCF=12MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode 	4.5 to 5.5		3.2	7.5				
(Note 1-1)			 System clock set to 12MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. 	2.8 to 5.5		1.8	4				
	IDDHALT(2)		 HALT mode FmCF=8MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode 	4.5 to 5.5		2.4	5.3	mA			
	IDDHALT(3)		 System clock set to 8MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. 	2.5 to 4.5		12.5	2.8				

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

Continued on next page.

Parameter	Symbol	Pins/Remarks	Conditions			Specifi	ication	1
i didilletei	Gymbol	T III3/Itemarks	Conditions	V _{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(4)	V _{DD} 1 =V _{DD} 2 =V _{DD} 3	 HALT mode FmCF=4MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode 	4.5 to 5.5		1	2.3	
	IDDHALT(5)		 System clock set to 4MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. 	2.2 to 4.5		0.5	1.3	
	IDDHALT(6)		 HALT mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode 	4.5 to 5.5		0.33	0.9	mA
	IDDHALT(7)		 System clock set to internal RC oscillation frequency variable RC oscillation stopped 1/2 frequency division ratio. 	2.2 to 4.5		0.17	0.7	
	IDDHALT(8)		HALT mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode.	4.5 to 5.5		1	3.8	
	IDDHALT(9)	IDDHALT(9) • System clock set to 1MHz with frequency variable RC oscillation • Internal RC oscillation stopped • 1/2 frequency division ratio.		2.2 to 4.5		0.5	2.7	
	IDDHALT(10)		 HALT mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode. 	4.5 to 5.5		18	73	
	IDDHALT(11)		 System clock set to 32.768kHz side. Internal RC oscillation stopped frequency variable RC oscillation stopped 1/2 frequency division ratio. 	2.2 to 4.5		5	65	μА
HOLD mode	IDDHOLD(1)	V _{DD} 1	• HOLD mode	4.5 to 5.5		0.035	20	
consumption current	IDDHOLD(2)	1	 CF1=V_{DD} or open (External clock mode) 	2.2 to 4.5		0.015	16	
Timer HOLD mode	IDDHOLD(3)		Timer HOLD mode CF1=V _{DD} or open (External clock mode)	4.5 to 5.5		16	65	
consumption current						3.5	52	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

F-ROM Programming Characteristics at $Ta = +10^{\circ}C$ to $+55^{\circ}C$, VSS1 = VSS2 = VSS3 = 0V

Deremeter	Symbol	Pins/Remarks	Conditions		Specif	Specification			
Parameter	Parameter Symbol Pins/Remarks Conditions	V _{DD} [V]	min	typ	max	unit			
Onboard programming current	IDDFW(1)	V _{DD} 1	Without CPU current	2.70 to 5.5		5	10	mA	
Programming	tFW(1)		• Erasing	2.7 to 5.5		20	30	ms	
time	tFW(2)		programming	2.7 to 5.5		40	60	μs	

UART (Full Duplex) Operat	ng Conditions at $Ta = -40^{\circ}C$	$C \text{ to } +85^{\circ}\text{C}, \text{ V}_{\text{SS}}1 = \text{V}_{\text{SS}}2 = \text{V}_{\text{SS}}3 = 0^{\text{V}}$	V
----------------------------------	---	--	---

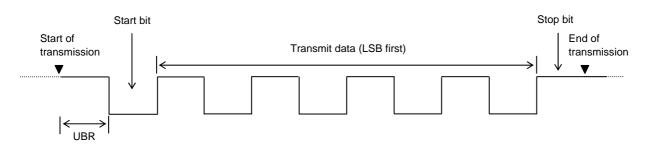
Parameter	Symbol	Pins/Pomarks	Conditions		Specification				
Parameter	Parameter Symbol Pins/Remarks Conditions		V _{DD} [V]	min	typ	max	unit		
Transfer rate	UBR	P32 (UTX1),			16/3				
		P33 (URX1),					8192/3	tCYC	
		P34 (UTX2),		2.5 to 5.5			0192/3	1010	
		P35 (URX2)							

Data length: 7/8/9 bits (LSB first)

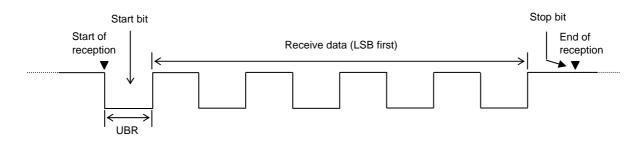
Stop bits : 1-bit (2-bit in continuous data transmission)

Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



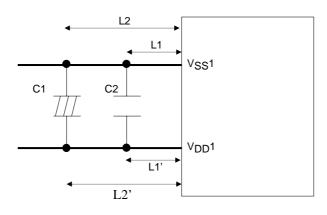
Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)



VDD1, VSS1 Terminal Condition

It is necessary to place capacitors between V_{DD1} and V_{SS1} as describe below.

- Place capacitors as close to $V_{DD}1$ and $V_{SS}1$ as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L1 = L1', L2 = L2').
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
- \bullet Capacitance of C2 must be more than 0.1 $\mu F.$
- Use thicker pattern for VDD1 and VSS1.



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Nominal Vendor		Circuit Constant			Operating Voltage	Oscillation Stabilization Time					
Frequency	Name	Oscillator Name	C1	C2	Rf1	Rd1	Range	typ	max	Remarks	
			[pF]	[pF]	[Ω]	[Ω]	[V]	[ms]	[ms]		
12MHz		CSTCE12M0G52-R0	(10)	(10)	Open	470	2.6 to 5.5	0.03	0.5	Internal C1,C2	
10MHz		CSTCE10M0G52-R0	(10)	(10)	Open	470	2.4 to 5.5	0.03	0.5	Internal C1,C2	
				CSTLS10M0G53-B0	(15)	(15)	Open	680	2.6 to 5.5	0.03	0.5
01411-	MURATA	CSTCE8M00G52-R0	(10)	(10)	Open	680	2.3 to 5.5	0.03	0.5	Internal C1,C2	
8MHz		CSTLS8M00G53-B0	(15)	(15)	Open	1k	2.5 to 5.5	0.03	0.5	Internal C1,C2	
		CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.03	0.5	Internal C1,C2	
4MHz		CSTLS4M00G53-B0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.03	0.5	Internal C1,C2	

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Fig. 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYOdesignated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

	ubie 2 Characteristics of a Sample Subsystem Clock Osemator Chedat what a Crystar Osemator										
Nominal	Vendor	Oscillator Name	Circuit Constant			Operating Voltage	Oscillation Stabilization Time		Remarks		
Frequency	Name	Oscillator Name	C3	C4	Rf2	Rd2	Range [V]	typ	max	Remarks	
			[pF]	[pF]	[Ω]	[Ω]	[v]	[s]	[s]		
32.768kHz	SEIKO TOYOCOM	MC-306	18	18	Open	560k	2.2 to 5.5	1.2	3.0	Applicable CL value=12.5pF	

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure. 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

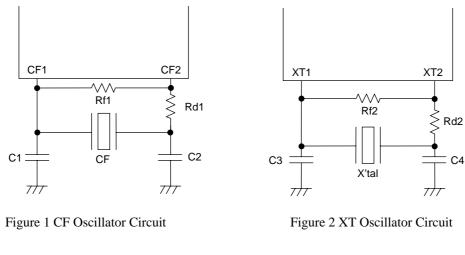
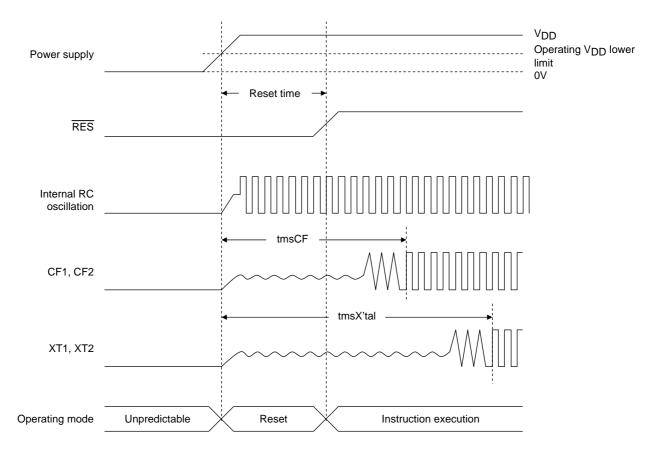
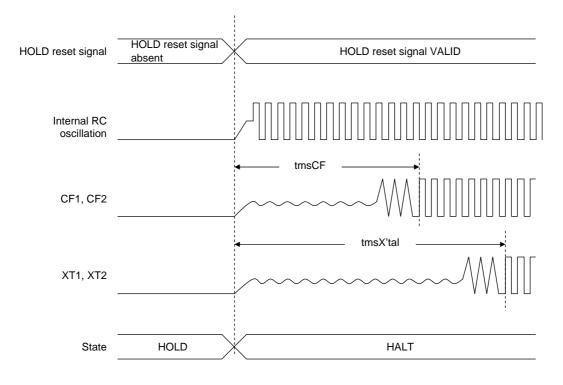




Figure 3 AC Timing Measurement Point

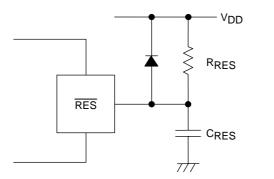


Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note:

Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage.



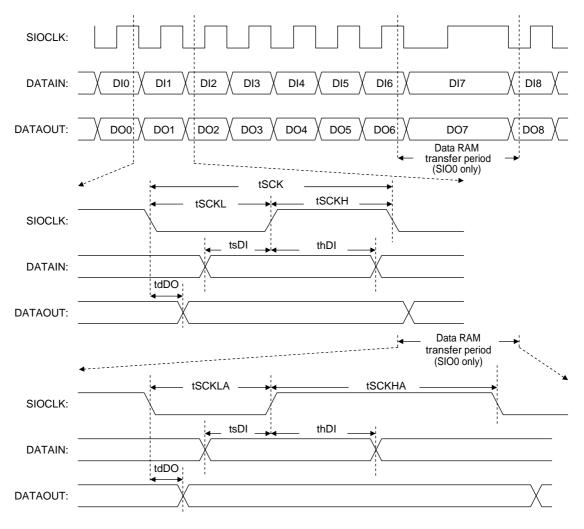


Figure 6 Serial I/O Waveforms

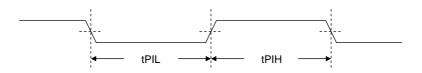


Figure 7 Pulse Input Timing Signal Waveform

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