Ordering number : ENA0147

SANYO Semiconductors
DATA SHEET

LC87F7CC8A — CMOS IC FROM 128K byte, RAM 4096 byte on-chip 8-bit 1-chip Microcontroller

Overview

The LC877C00 series are an 8-bit single chip microcontroller with the following on-chip functional blocks. :

- CPU: operable at a minimum bus cycle time of 83.3ns
- 128K bytes Flash ROM (single 5V power supply, re-writeable on board)
- On-chip RAM: 4096 bytes
- LCD controller / driver
- 16-bit timer/counters (can be divided into 8-bit units)
- 16-bit timer / PWM (can be divided into two 8-bit timers)
- Four 8-bit timer with prescalers
- Timer for use as date/time clock
- Synchronous serial I/O port (with automatic block transmit / receive function)
- Asynchronous / synchronous serial I/O port
- 2 channel 12-bit PWM
- 12-channel × 8-bit AD converter
- High-speed clock counter
- System clock divider
- Small signal detector
- 20 source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

■Flash ROM

- Single 5V power supply, writeable on-board.
- Block erase in 128-byte units
- 131072 × 8 bits (LC87F7CC8A)

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■RAM
- 4096 × 9-bits (LC87F7CC8A)

■Minimum Bus Cycle Time
- 83.3ns (12MHz) V_{DD}=4.5 to 5.5V
- 100ns (10MHz) V_{DD}=2.8 to 5.5V
- 250ns (4MHz) V_{DD}=2.2 to 5.5V

Note: The bus cycle time indicates ROM read time.

■Minimum Instruction Cycle Time (tCYC)
- 250 ns (12MHz) V_{DD}=4.5 to 5.5V
- 300 ns (10MHz) V_{DD}=2.8 to 5.5V
- 750 ns (4MHz) V_{DD}=2.2 to 5.5V

■Ports
- Input/output ports
  Data direction programmable for each bit individually: 20 (P1n, P70 to P73, P8n)
  Data direction programmable in nibble units: 8 (P0n)
  (When N-channel open drain output is selected, data can be input in bit units.)
- Input ports: 2 (XT1, XT2)
- Output ports: 2 (PWM2, PWM3)
- LCD ports
  Segment output: 32 (S00 to S15, S24 to S39)
  Common output: 4 (COM0 to COM3)
  Bias terminals for LCD driver: 3 (V1 to V3)
  Other functions
  Input/output ports: 32 (PAn, PBn, PDn, PEn)
  Input ports: 7 (PLn)
- Oscillator pins: 2 (CF1, CF2)
- Reset pin: 1 ($\overline{RES}$)
- Power supply: 6 (V_{SS}1 to 3, V_{DD}1 to 3)

■LCD Controller
- Seven display modes are available (static, 1/2, 1/3, 1/4 duty × 1/2, 1/3 bias)
- Segment output and common output can be switched to general purpose input/output ports.

■Small Signal Detection (MIC signals etc)
- Counts pulses with the level which is greater than a preset value
- 2 bit counter

■Timers
- Timer 0: 16-bit timer / counter with capture register
  Mode 0: 2 channel 8-bit timer with programmable 8-bit prescaler and 8-bit capture register
  Mode 1: 8-bit timer with 8-bit programmable prescaler and 8-bit capture register
  +8-bit counter with 8-bit capture register
  Mode 2: 16-bit timer with 8-bit programmable prescaler and 16-bit capture register
  Mode 3: 16-bit counter with 16-bit capture register
- Timer 1: PWM / 16-bit timer/counter with toggle output function
  Mode 0: 8-bit timer with 8-bit prescaler (and toggle output) +8-bit timer / counter with 8-bit prescaler (and toggle output)
  Mode 1: 2 channel 8-bit PWM with 8-bit prescaler
  Mode 2: 16-bit timer/counter with 8-bit prescaler (and toggle output)
  (Toggle output also possible using the lower order 8-bits)
  Mode 3: 16-bit timer with 8-bit prescaler (and toggle output)
  (The lower order 8 bits can be used as PWM output)

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- Timer 4: 8-bit timer with 6-bit prescaler
- Timer 5: 8-bit timer with 6-bit prescaler
- Timer 6: 8-bit timer with 6-bit prescaler (and toggle output)
- Timer 7: 8-bit timer with 6-bit prescaler (and toggle output)
- Base Timer
  1) The clock signal can be selected from any of the following :
     Sub-clock (32.768kHz crystal oscillator), system clock, and prescaler output from timer 0
  2) Interrupts of five different time intervals are possible.

■High-speed Clock Counter
- Countable up to 20MHz clock (when using 10MHz main clock)
- Real time output

■SIO
- SIO 0: 8-bit synchronous serial interface
  1) LSB first/MSB first is selectable
  2) Internal 8-bit baud-rate generator (fastest clock period 4/3 tCYC)
  3) Consecutive automatic data communication (1 to 256 bits)
- SIO 1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8 bit serial I/O (2-wire or 3-wire, transmit clock 2 to 512 tCYC)
  Mode 1: Asynchronous serial I/O (half duplex, 8 data bits, 1 stop bit, baud rate 8 to 2048 tCYC)
  Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2 to 512 tCYC)
  Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

■AD Converter: 8-bits × 12 channels

■PWM: 2 Channels Multi-frequency 12-bit PWM

■Remote Control Receiver Circuit (connected to P73/INT3/T0IN terminal)
- Noise rejection function (noise rejection filter's time constant can be selected from 1/32/128 tCYC)

■Watchdog Timer
- The watching time period is determined by an external RC.
- Watchdog timer can produce interrupt or system reset

■Interrupts: 20 sources, 10 vectors
1) Three priority (low, high, and highest) multiple interrupts are supported. During interrupt handling, an equal or lower priority interrupt request is postponed.
2) If interrupt requests to two or more vector addresses occur at once, the higher priority interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L
4	0001BH	H or L	INT3/Base timer0 /Base timer1
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC/MIC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3

- Priority level: X > H > L
- For equal priority levels, vector with lowest address takes precedence.

■Subroutine Stack Levels: 2048 levels max
Stack is located in RAM.

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits
- On-chip RC oscillation for system clock use.
- CF oscillation for system clock use. (Rf built in, Rd external)
- Crystal oscillation low speed system clock use. (Rf built in, Rd external)
- On-chip frequency variable RC oscillation circuit for system clock use.

■System Clock Divider Function
- Low power consumption operation is available
- Minimum instruction cycle time (300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs can be switched by program (when using 10MHz main clock)

■Standby Function
- HALT mode
  HALT mode is used to reduce power consumption. During the HALT mode, program execution is stopped but peripheral circuits keep operating (some parts of serial transfer operation stop).
  1) Oscillation circuits are not stopped automatically.
  2) Released by the system reset or interrupts.
- HOLD mode
  HOLD mode is used to reduce power consumption. Program execution and peripheral circuits are stopped.
  1) CF, RC, X'tal and multi-frequency RC oscillation circuits stop automatically.
  2) Released by any of the following conditions.
    (1) Low level input to the reset pin
    (2) Specified level input to one of INT0, INT1, and INT2
    (3) Port 0 interrupt
- X'tal HOLD made
  X'tal HOLD mode is used to reduce power consumption. Program execution is stopped.
  All peripheral circuits except the base timer are stopped.
  1) CF, RC and multi-frequency RC oscillation circuits stop automatically.
  2) Crystal oscillator operation is kept in its state at HOLD mode inception.
  3) Released by any of the following conditions
    (1) Low level input to the reset pin
    (2) Specified level input to one of INT0, INT1, and INT2
    (3) Port 0 interrupt
    (4) Base-timer interrupt

■Package Form
- QFP80 (14 × 14): Lead-free type
- TQFP80J (12 × 12): Lead-free type

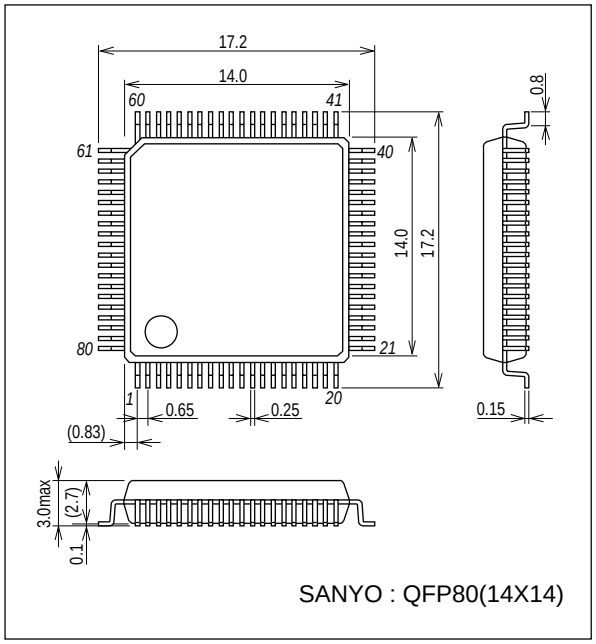
■Development Tools
- Evaluation chip: LC87EV690
- Emulator: EVA62S + ECB876600D + SUB877100 + POD80QFP(14 × 14) or POD80SQFP
  ICE-B877300 + SUB877100 + POD80QFP(14 × 14) or POD80SQFP
- Flash ROM write adapter: W87F71256QF or W87F71256SQ

■Same Package and Pin Assignment as Mask ROM Version.
1) LC877C00 series options can be set by using flash ROM data. Thus the board used for mass production can be used for debugging and evaluation without modifications.
2) If the program for the mask ROM version is used, the usable ROM/RAM capacity is the same as the mask ROM version.

Package Dimensions

unit : mm (typ)

3255

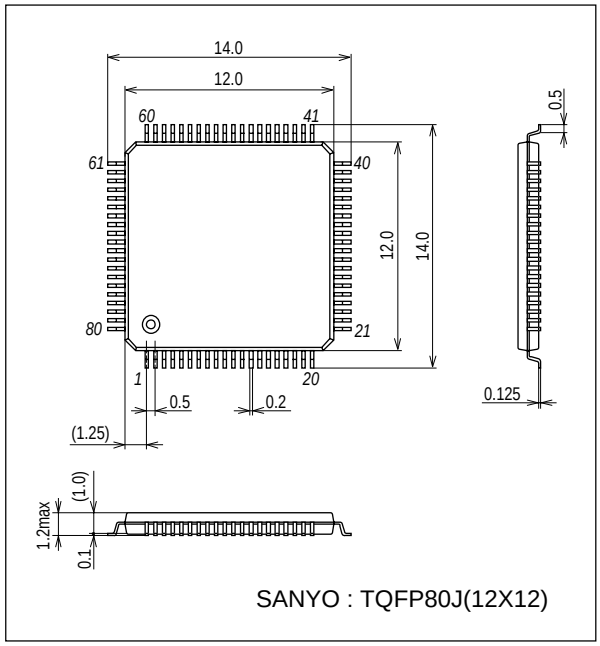


SANYO : QFP80(14X14)

Package Dimensions

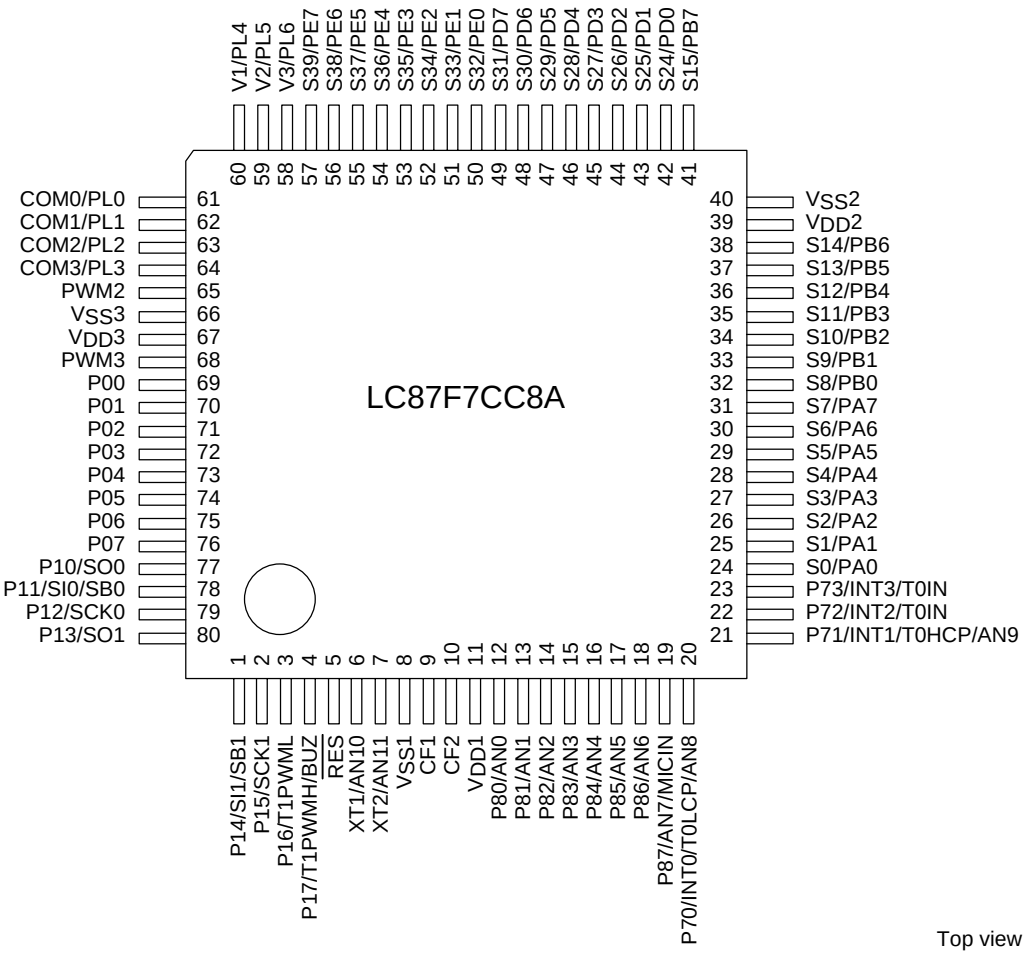
unit : mm (typ)

3290



SANYO : TQFP80J(12X12)

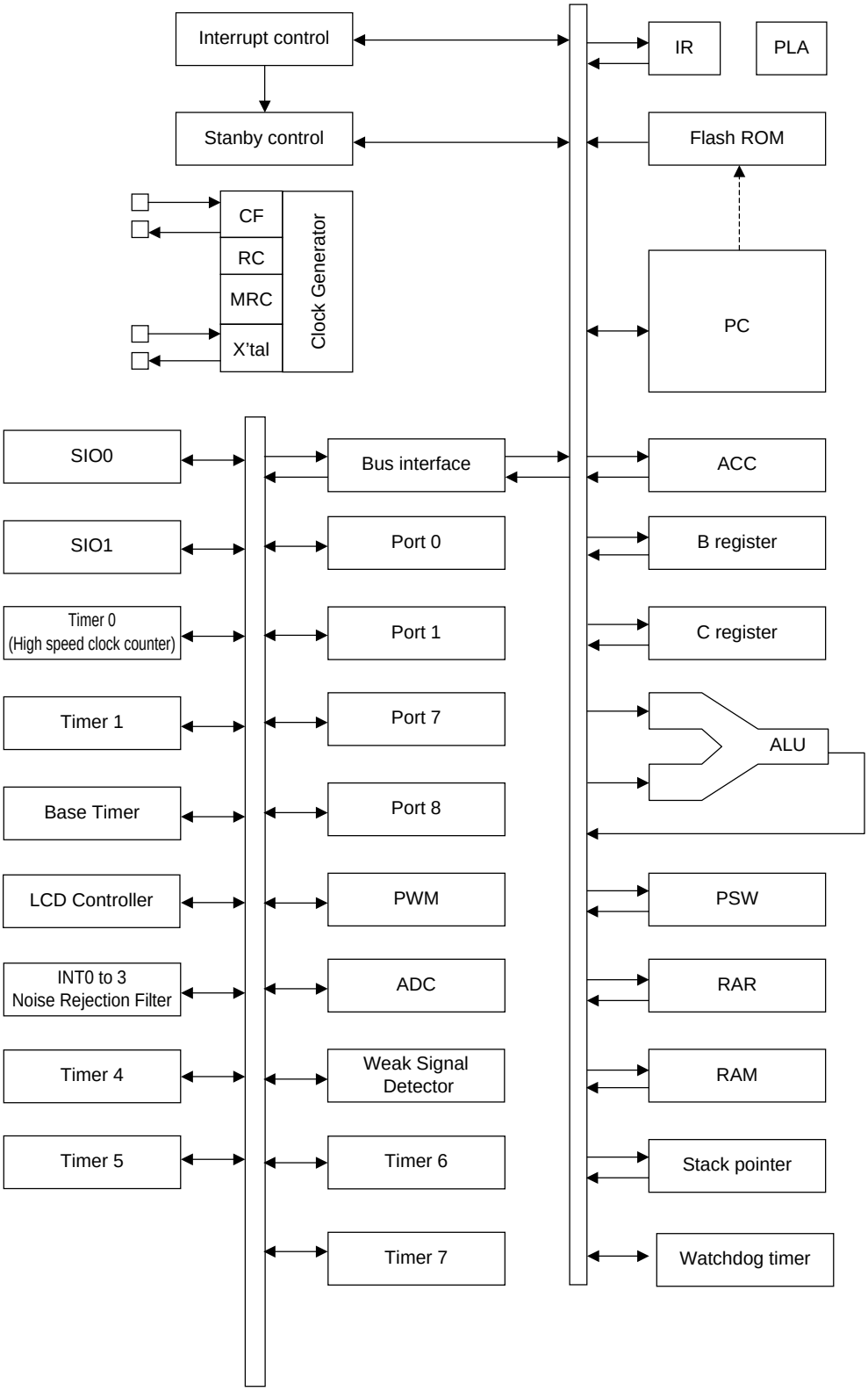
Pin Assignment



Top view

SANYO : QFP80 (14 × 14) “Lead-free Type”
SANYO : TQFP80J (12 × 12) “Lead-free Type”

System Block Diagram



Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$,
$V_{SS}3$</td><td>-</td><td>• Power supply (-)</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$
$V_{DD}3$</td><td>-</td><td>• Power supply (+)</td><td>No</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable in nibble units
• Use of pull-up resistor can be specified in nibble units
• Input for HOLD release
• Input for port 0 interrupt
• Other functions
P05: clock output (system clock/can selected from sub clock)
P06: timer 6 toggle output
P07: timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit
• Use of pull-up resistor can be specified for each bit individually
• Other pin functions
P10 SIO0 data output
P11 SIO0 data input or bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input or bus input/output
P15 SIO1 clock input/output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/buzzer output</td><td>Yes</td></tr>
<tr><td>PORT7
P70 to P73</td><td>I/O</td><td>• 4-bit Input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit individually
• Other functions
P70: INT0 input/HOLD release input/timer0L capture input/output for watchdog timer
P71: INT1 input/HOLD release input/timer0H capture input
P72: INT2 input/HOLD release input/timer 0 event input/timer0L capture input
P73: INT3 input(noise rejection filter attached)/timer 0 event input/timer0H capture input
AD input port: AN8(P70), AN9(P71)
• Interrupt detection selection
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising and falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
</td><td>No</td></tr>
</table>

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Pin name	I/O	Description	Option
PORT8 P80 to P87	I/O	• 8-bit Input/output port • Input/output can be specified for each bit individually • Other functions: AD input port: AN0 to AN7 Small signal detector input port: MICIN(P87)	No
S0/PA0 to S7/PA7	I/O	• Segment output for LCD • Can be used as general-purpose input/output port (PA)	No
S8/PB0 to S15/PB7	I/O	• Segment output for LCD • Can be used as general-purpose input/output port (PB)	No
S24 /PD0 to S31/PD7	I/O	• Segment output for LCD • Can be used as general-purpose input/output port (PD)	No
S32/PE0 to S39/PE7	I/O	• Segment output for LCD • Can be used as general-purpose input/output port (PE)	No
COM0/PL0 to COM3/PL3	I/O	• Common output for LCD • Can be used as general-purpose input port (PL)	No
V1/PL4 to V3/PL6	I/O	• LCD output bias power supply • Can be used as general-purpose input port (PL)	No
PWM2	O	PWM2 output port	No
PWM3	O	PWM3 output port	No
$\overline{\text{RES}}$	I	Reset terminal	No
XT1	I	• Input for 32.768kHz crystal oscillation • Other functions: General-purpose input port AD input port: AN10 • When not in use, connect to $V_{DD}1$	No
XT2	I/O	• Output for 32.768kHz crystal oscillation • Other functions: General-purpose input port AD input port: AN11 • When not in use, set to oscillation mode and leave open	No
CF1	I	Input terminal for ceramic oscillator	No
CF2	O	Output terminal for ceramic oscillator	No

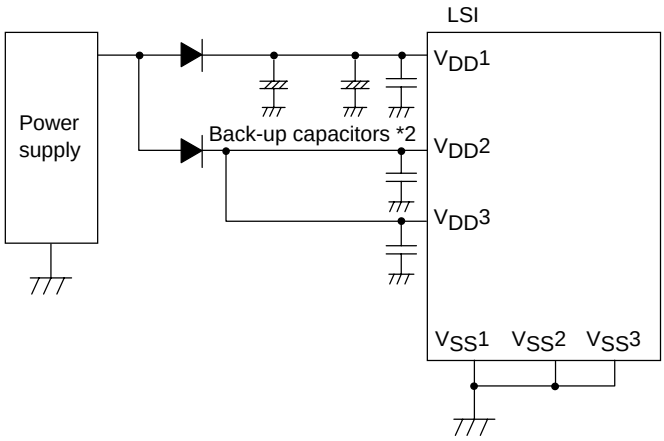
Port Output Types

Port form and pull-up resistor options are shown in the following table.
Port status can be read even when port is set to output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	each bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	None
P10 to P17	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	None	Nch-open drain	Programmable
P71 to P73	-	None	CMOS	Programmable
P80 to P87	-	None	Nch-open drain	None
S0/PA0 to S15/PB7 S24/PD7 to S39/PE7	-	None	CMOS	Programmable
COM0/PL0 to COM3/PL3	-	None	Input only	None
V1/PL4 to V3/PL6	-	None	Input only	None
PWM2, PWM3	-	None	CMOS	None
XT1	-	None	Input only	None
XT2	-	None	Output for 32.768kHz crystal oscillation	None

Note 1: Attachment of Port0 programmable pull-up resistors is controllable in nibble units (P00 to 03, P04 to 07).

*1: Connect as follows to reduce noise on V_{DD}.
$V_{SS}1$, $V_{SS}2$, and $V_{SS}3$ must be connected together and grounded.



*2: The power supply for the internal memory is $V_{DD}1$ but it uses the $V_{DD}2$ as the power supply for ports.
When the $V_{DD}2$ is not backed up, the port level does not become “H” even if the port latch is in the “H” level. Therefore, when the $V_{DD}2$ is not backed up and the port latch is “H” level, the port level is unstable in the HOLD mode, and the back up time becomes shorter because the through current runs from V_{DD} to GND in the input buffer. If $V_{DD}2$ is not backed up, output “L” by the program or pull the port to “L” by the external circuit in the HOLD mode so that the port level becomes “L” level and unnecessary current consumption is prevented.

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions		Specification			
					V_{DD} [V]	min	typ	max	unit
Supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		+6.5	V
Supply voltage for LCD		VLCD	V1/PL4, V2/PL5, V3/PL6	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		V_{DD}	
Input voltage		V_I	Port L XT1, XT2, CF1, $\overline{RES}$			-0.3		V_{DD}+0.3	
Input/Output voltage		V_{IO}(1)	• Ports 0, 1, 7, 8 • Ports A, B, D, E • PWM2, PWM3			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0,1	• CMOS output selected • Current at each pin		-10			mA
		IOPH(2)	Ports 71,72,73	Current at each pin		-5			
		IOPH(3)	• Ports A, B, D, E • PWM2, PWM3	Current at each pin		-5			
	Average output current (Note 1-1)	IOMH(1)	Ports 0,1	• CMOS output selected • Current at each pin		-7.5			
		IOMH(2)	Ports 71, 72, 73	Current at each pin		-3			
		IOMH(3)	• Ports A, B, D, E • PWM2, PWM3	Current at each pin		-3			
	Total output current	∑IOAH(1)	• Ports 0, 1 • PWM2, PWM3	Total of all pins		-25			
		∑IOAH(2)	Port 7	Total of all pins		-10			
		∑IOAH(3)	Ports A, B,	Total of all pins		-25			
		∑IOAH(4)	Ports D, E	Total of all pins		-25			
		∑IOAH(5)	Ports A, B, D, E	Total of all pins		-45			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1	Current at each pin				20	
		IOPL(2)	Ports 7,8	Current at each pin				10	
		IOPL(3)	• Ports A, B, D, E • PWM2, PWM3	Current at each pin				10	
	Average output current (Note 1-1)	IOML(1)	Ports 0, 1	Current at each pin				15	
		IOML(2)	Ports 7, 8	Current at each pin				7.5	
		IOML(3)	• Ports A, B, D, E • PWM2, PWM3	Current at each pin				7.5	
	Total output current	∑IOAL(1)	• Ports 0, 1 • PWM2, PWM3	Total of all pins				45	
		∑IOAL(2)	Ports 7, 8	Total of all pins				15	
		∑IOAL(3)	Ports A, B	Total of all pins				45	
		∑IOAL(4)	Ports D, E	Total of all pins				45	
		∑IOAL(5)	Ports A, B, D, E	Total of all pins				80	
Maximum power consumption		Pd max	QFP80(14×14)	Ta = -20 to +70°C				381	mW
			TQFP80J(12×12)					325	
Operating temperature range		Topr				-20		+70	°C
Storage temperature range		Tstg				-55		+125	

Note 1-1: Average output current indicates average value for 100ms term.

Allowable Operating Range at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Operating supply voltage range (Note2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3$	0.245μs≤ tCYC≤ 200μs		4.5		5.5	V
	$V_{DD}(2)$		0.294μs≤ tCYC≤ 200μs		2.8		5.5	
	$V_{DD}(3)$		0.735μs≤ tCYC≤ 200μs		2.2		5.5	
Supply voltage range in Hold mode	VHD	$V_{DD}1$	Keep RAM and register data in HOLD mode.		2.0		5.5	
Input high voltage	$V_{IH}(1)$	• Ports 0, 8 • Ports A, B, D, E, L	Output disable	2.2 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	• Port 1 • Ports 71, 72, 73 • P70 port input/interrupt	Output disable	2.2 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	P87 small signal input	Output disable	2.2 to 5.5	$0.75V_{DD}$		V_{DD}	
	$V_{IH}(4)$	Port 70 Watchdog timer	Output disable	2.2 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(5)$	XT1, XT2, CF1, $\overline{RES}$		2.2 to 5.5	$0.75V_{DD}$		V_{DD}	
Input low voltage	$V_{IL}(1)$	• Ports 0, 8 • Ports A, B, D, E, L	Output disable	4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
	$V_{IL}(2)$			2.2 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	• Port 1 • Ports 71, 72, 73 • P70 port input/interrupt	Output disable	4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
	$V_{IL}(4)$			2.2 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(5)$	Port 87 small signal Input	Output disable	2.2 to 5.5	V_{SS}		$0.25V_{DD}$	
	$V_{IL}(6)$	Port 70 Watchdog timer	Output disable	2.2 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(7)$	XT1, XT2, CF1, $\overline{RES}$		2.8 to 5.5	V_{SS}		$0.25V_{DD}$	
Operation cycle time (Note 2-2)	tCYC			4.5 to 5.5	0.245		200	μs
				2.8 to 5.5	0.294		200	
				2.2 to 5.5	0.735		200	
External system clock frequency	FEXCF(1)	CF1	• CF2 open • system clock divider :1/1 • external clock DUTY = 50 ± 5%	4.5 to 5.5	0.1		12	MHz
				2.8 to 5.5	0.1		10	
				2.2 to 5.5	0.1		4	
			• CF2 open • system clock divider :1/2	4.5 to 5.5	0.2		24.4	
				2.8 to 5.5	0.2		20	
				2.2 to 5.5	0.2		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	12MHz ceramic resonator oscillation See Fig. 1.	4.5 to 5.5		12		MHz
	FmCF(2)		10MHz ceramic resonator oscillation See Fig. 1.	2.8 to 5.5		10		
	FmCF(3)		4MHz ceramic resonator oscillation See Fig. 1.	2.2 to 5.5		4		
	FmRC		RC oscillation	2.2 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.2 to 5.5		16		
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation See Fig. 2.	2.2 to 5.5		32.768		kHz

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.
Note 2-2: Oscillation frequency and Operation cycle time (tCYC) rerationship: 1/1divide-3/FmCF, 1/2divide-6/FmCF
Note 2-3: The parts value of oscillation circuit is shown in Table 1 and Table 2.

Electrical Characteristics at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
High level input current	$I_{IH}(1)$	• Ports 0, 1, 7, 8 • Ports A, B, D, E, L • PWM2, PWM3	• Output disabled • Pull-up resister OFF. • $V_{IN}=V_{DD}$ (including OFF state leak current of the output Tr.)	2.2 to 5.5			1	µA
	$I_{IH}(2)$	$\overline{RES}$	$V_{IN}=V_{DD}$	2.2 to 5.5			1	
	$I_{IH}(3)$	XT1, XT2	When configured as an input port. $V_{IN}=V_{DD}$	2.2 to 5.5			1	
	$I_{IH}(4)$	CF1	$V_{IN}=V_{DD}$	2.2 to 5.5			15	
	$I_{IH}(5)$	P87/AN7/MICIN small signal input	$V_{IN}=V_{BIS}+0.5V$ (V_{BIS}: Bias voltage)	4.5 to 5.5	5	10	20	
Low level input current	$I_{IL}(1)$	• Ports 0, 1, 7, 8 • Ports A, B, D, E, L • PWM2, PWM3	• Output disabled • Pull-up resister OFF. • $V_{IN}=V_{SS}$ (including OFF state leak current of the output Tr.)	2.2 to 5.5	-1			
	$I_{IL}(2)$	$\overline{RES}$	$V_{IN}=V_{SS}$	2.2 to 5.5	-1			
	$I_{IL}(3)$	XT1,XT2	When configured as an input port. $V_{IN}=V_{SS}$	2.2 to 5.5	-1			
	$I_{IL}(4)$	CF1	$V_{IN}=V_{SS}$	2.2 to 5.5	-15			
	$I_{IL}(5)$	P87/AN7/MICIN small signal input	$V_{IN}=V_{BIS}-0.5V$ (V_{BIS}: Bias voltage)	4.5 to 5.5	-20	-10	-5	
High level output voltage	$V_{OH}(1)$	Ports 0, 1: CMOS output option	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
	$V_{OH}(4)$	Port 7	I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(5)$		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
	$V_{OH}(6)$	• Ports A, B, D, E, • PWM2, PWM3	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			
	$V_{OH}(7)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(8)$		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL}=1.0mA	2.2 to 5.5			0.4	
	$V_{OL}(4)$	Ports 7, 8	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(5)$		I_{OL}=1.0mA	2.2 to 5.5			0.4	
	$V_{OL}(6)$	• Ports A, B, D, E, • PWM2, PWM3	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(7)$		I_{OL}=1.0mA	2.2 to 5.5			0.4	
LCD output voltage regulation	VODLS	S0 to S15, S24 to S39	I_O=0mA VLCD, 2/3VLCD, 1/3VLCD level output See Fig. 8.	2.2 to 5.5	0		±0.2	
	VODLC	COM0 to COM3	I_O=0mA VLCD, 2/3VLCD, 1/2VLCD 1/3VLCD level output See Fig. 8.	2.2 to 5.5	0		±0.2	
LCD bias resistor	RLCD(1)	Resistance per one bias resistor	See Fig. 8.	2.2 to 5.5		60		kΩ
	RLCD(2)	• Resistance per one bias resistor • 1/2R mode	See Fig. 8.	2.2 to 5.5		30		

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Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Resistance of pull-up MOS Tr.	Rpu	• Ports 0, 1, 7 • Ports A, B, D, E	V_{OH}=0.9V_{DD}	4.5 to 5.5	15	35	80	kΩ
				2.2 to 4.5	18	50	150	
Hysterisis voltage	VHYS(1)	• Ports 1, 7 • $\overline{RES}$		2.2 to 5.5		0.1V_{DD}		V
	VHYS(2)	Port 87 small signal input		2.2 to 5.5		0.1V_{DD}		
Pin capacitance	CP	All pins	• All Other Terminals Connected To V_{SS}. • f=1MHz • Ta=25°C	2.2 to 5.5		10		pF
Input sensitivity	Vsen	Port 87 small signal input		2.2 to 5.5	0.12V_{DD}			Vp-p

Serial I/O Characteristics at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	Specification				
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 6. • (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.		4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.2 to 5.5	0.03			µs
	Data hold time		thDI(1)			2.2 to 5.5	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.2 to 5.5			1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.15	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.2 to 5.5	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.2 to 5.5	0.03			µs
	Data hold time		thDI(2)			2.2 to 5.5	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.2 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72) INT4(P30 to P33) INT5(P34 to P35)	• Condition that interrupt is accepted • Condition that event input to timer 0 is accepted	2.2 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (Noise rejection ratio is 1/1.)	• Condition that interrupt is accepted • Condition that event input to timer 0 is accepted	2.2 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (Noise rejection ratio is 1/32.)	• Condition that interrupt is accepted • Condition that event input to timer 0 is accepted	2.2 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (Noise rejection ratio is 1/128.)	• Condition that interrupt is accepted • Condition that event input to timer 0 is accepted	2.2 to 5.5	256			
	tPIL(5) tPIL(5)	MICIN(P87)	• Condition that signal is accepted to small signal detection counter.	2.2 to 5.5	1			
	tPIL(6)	$\overline{RES}$	• Condition that reset is accepted	2.2 to 5.5	200			µs

AD Converter Characteristics at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		3.0 to 5.5		8		bit
Absolute precision	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32 × tCYC (ADCR2=0) (Note 6-2)	4.5 to 5.5	15.62 (tCYC= 0.488µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 5.5	23.52 (tCYC= 0.735µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time=64 × tCYC (ADCR2=1) (Note 6-2)	4.5 to 5.5	18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
				3.0 to 5.5	47.04 (tCYC= 0.735µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 6-1: Absolute precision does not include quantizing error (±1/2 LSB).

Note 6-2: Conversion time means time from executing AD conversion instruction to loading complete digital value to register.

Consumption Current Characteristics at Ta = -20°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Current consumption during normal operation (Note 7-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• FmCF=12MHz ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • System clock: CF 12MHz oscillation • Frequency variable RC oscillation stopped • Internal RC oscillation stopped. • Divider: 1/1	4.5 to 5.5		7.2	20	mA
	IDDOP(2)		• FmCF=10MHz ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • System clock: CF 10MHz oscillation • Frequency variable RC oscillation stopped • Internal RC oscillation stopped. • Divider: 1/1	4.5 to 5.5		6.6	16.5	
	IDDOP(3)			3.0 to 3.6		3.8	9.6	
	IDDOP(4)			2.8 to 3.0		2.5	7.4	
	IDDOP(5)		• FmCF=4MHz ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • System clock: CF 4MHz oscillation • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped • Divider:1/1	4.5 to 5.5		2.5	6.3	
	IDDOP(6)			3.0 to 3.6		1.4	3.5	
	IDDOP(7)			2.2 to 3.0		0.9	2.7	
	IDDOP(8)		• FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • Frequency variable RC oscillation stopped • System clock: RC oscillation • Divider:1/2	4.5 to 5.5		0.75	3.1	
	IDDOP(9)			3.0 to 3.6		0.4	1.7	
	IDDOP(10)			2.2 to 3.0		0.28	1.35	
	IDDOP(11)		•FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz crystal oscillation •Internal RC oscillation stopped. •System clock: 1MHz with frequency variable RC oscillation •Divider:1/2	4.5 to 5.5		1.3	5.4	
	IDDOP(12)			3.0 to 3.6		0.7	3.1	
	IDDOP(13)			2.2 to 3.0		0.5	2.4	
	IDDOP(14)		• FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • System clock: 32.768kHz • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped • Divider:1/2	4.5 to 5.5		35	115	µA
	IDDOP(15)			3.0 to 3.6		18	65	
	IDDOP(16)			2.2 to 3.0		12	46	
Current consumption during HALT mode (Note 7-1)	IDDHALT(1)		HALT mode • FmCF=12MHz ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • System clock: CF 12MHz oscillation • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped • Divider: 1/1	4.5 to 5.5		3	7.8	mA
	IDDHALT(2)		HALT mode • FmCF=10MHz ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • System clock: CF 10MHz oscillation • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped • Divider: 1/1	4.5 to 5.5		2.6	5.9	
	IDDHALT(3)			3.0 to 3.6		1.4	3.3	
	IDDHALT(4)			2.8 to 3.0		1	2.5	
	IDDHALT(5)		HALT mode • FmCF=4MHz ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • System clock: CF 4MHz oscillation • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped • Divider: 1/1	4.5 to 5.5		1.15	2.65	
	IDDHALT(6)			3.0 to 3.6		0.6	1.5	
	IDDHALT(7)			2.2 to 3.0		0.4	1.1	

Note 7-1: The currents through the output transistors and the pull-up MOS transistors are ignored.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Current consumption during HALT mode (Note 7-1)	IDDHALT(8)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	HALT mode • FmCF=0Hz (Oscillation stop) • FsX'tal=32.768kHz crystal oscillation • System clock: RC oscillation • Frequency variable RC oscillation stopped • Divider: 1/2	4.5 to 5.5		0.37	1.3	mA
	IDDHALT(9)			3.0 to 3.6		0.2	0.75	
	IDDHALT(10)			2.2 to 3.0		0.13	0.54	
	IDDHALT(11)		HALT mode • FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • Internal RC oscillation stopped. • System clock: 1MHz with frequency variable RC oscillation • Divider :1/2	4.5 to 5.5		1	3.5	
	IDDHALT(12)			3.0 to 3.6		0.55	2	
	IDDHALT(13)			2.2 to 3.0		0.37	1.5	
	IDDHALT(14)		HALT mode • FmCF=0Hz (Oscillation stop) • FsX'tal=32.768kHz crystal oscillation • System clock: 32.768kHz • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped • Divider: 1/2	4.5 to 5.5		18.5	68	µA
	IDDHALT(15)			3.0 to 3.6		10	38	
	IDDHALT(16)			2.2 to 3.0		6.5	26	
Current consumption during HOLD mode	IDDHOLD(1)	$V_{DD}1$	HOLD mode • CF1=V_{DD} or open (when using external clock)	4.5 to 5.5		0.05	20	
	IDDHOLD(2)			3.0 to 3.6		0.03	12	
	IDDHOLD(3)			2.2 to 3.0		0.02	8	
Current consumption during Date/time clock HOLD mode	IDDHOLD(4)		Date/time clock HOLD mode • CF1=V_{DD} or open (when using external clock) • FmX'tal=32.768kHz crystal oscillation	4.5 to 5.5		16	58	
	IDDHOLD(5)			3.0 to 3.6		8.5	32	
	IDDHOLD(6)			2.2 to 3.0		5	20	

Note 7-1: The currents through the output transistors and the pull-up MOS transistors are ignored.

F-ROM Write Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
On-board writing current	IDDFW(1)	$V_{DD}1$	• 128-byte writing • Including erase time current	3.0 to 5.5		25	40	mA
Writing time	tFW(1)		• 128-byte writing • Including data erase time • Excluding time to fetch 128 byte data	3.0 to 5.5		22.5	45	ms

Characteristics of a Sample Main System Clock Oscillation Circuit

The characteristics in the table bellow is based on the following conditions:
(1) Use the standard evaluation board SANYO has provided.
(2) Use the peripheral parts with indicated value externally.
(3) The peripheral parts value is a recommended value of oscillator manufacturer

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	Open	470	4.5 to 5.5	0.05	0.15	Internal C1, C2
10MHz	MURATA	CSTCE10M0G52-R0	(10)	(10)	Open	1.0k	2.8 to 5.5	0.05	0.15	Internal C1, C2
		CSTLS10M0G53-B0	(15)	(15)	Open	680	2.8 to 5.5	0.05	0.15	
4MHz	MURATA	CSTCR4M00G53-R0	(15)	(15)	Open	3.3k	2.2 to 5.5	0.05	0.15	Internal C1, C2
		CSTLS4M00G53-B0	(15)	(15)	Open	3.3k	2.2 to 5.5	0.05	0.15	

The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage (See Fig. 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

The characteristics in the table bellow is based on the following conditions:
(1) Use the standard evaluation board SANYO has provided.
(2) Use the peripheral parts with indicated value externally.
(3) The peripheral parts value is a recommended value of oscillator manufacturer

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	SEIKO EPSON	MC-306	18	18	Open	560k	2.2 to 5.5	1.3	3.0	Applicable CL value =12.5pF

The oscillation stabilizing time is a period until the oscillation becomes stable after executing the instruction which starts the sub-clock oscillation or after releasing the HOLD mode (See Fig. 4).

Note : Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

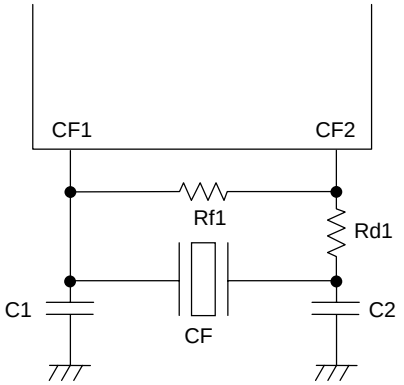


Figure 1 Ceramic Oscillator Circuit

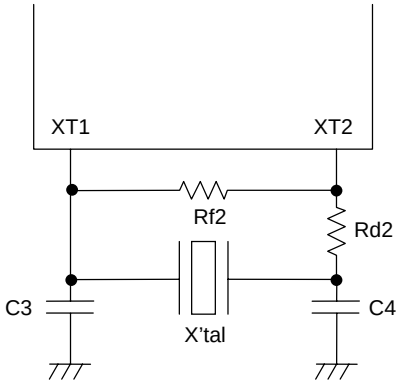


Figure 2 Crystal Oscillator Circuit

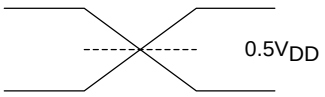
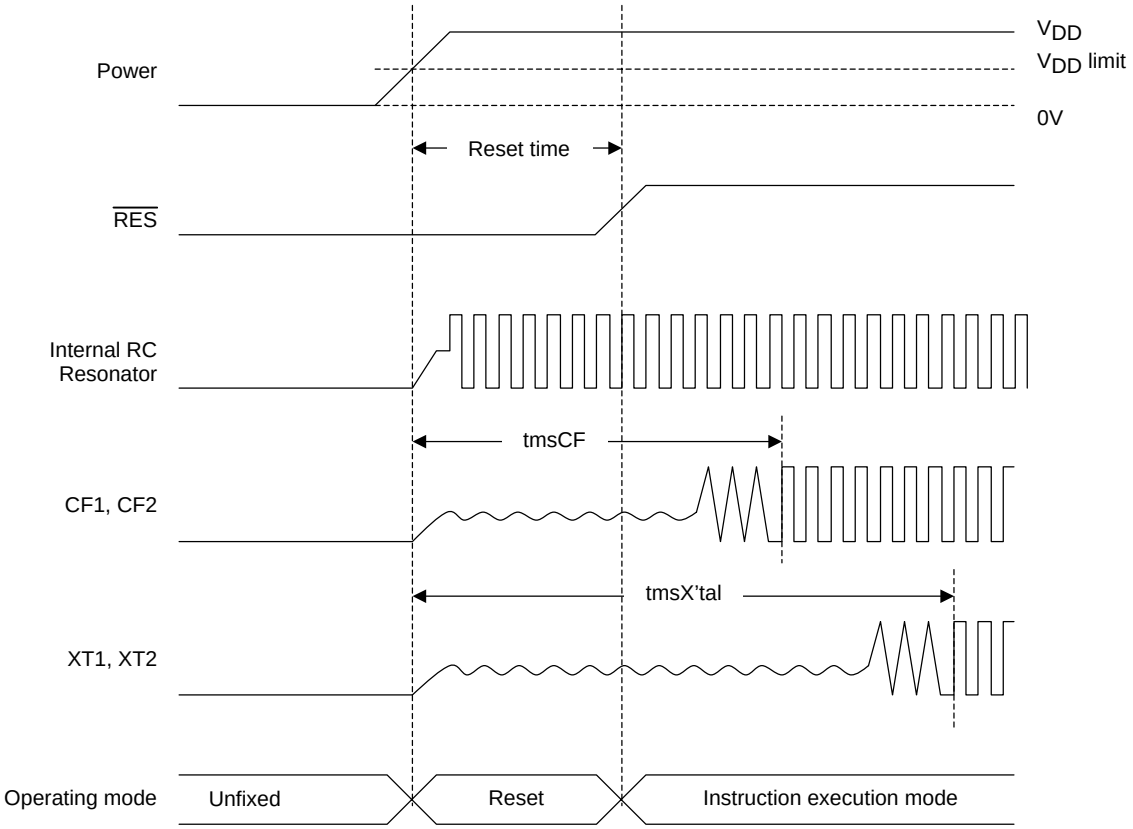
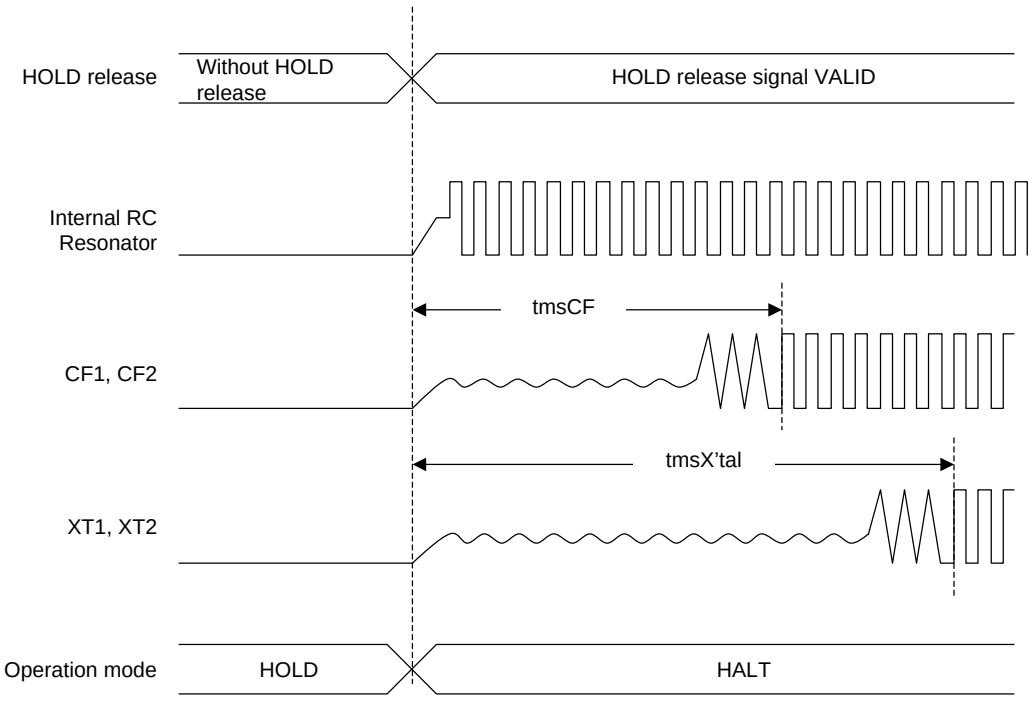


Figure 3 AC Timing Measurement Point

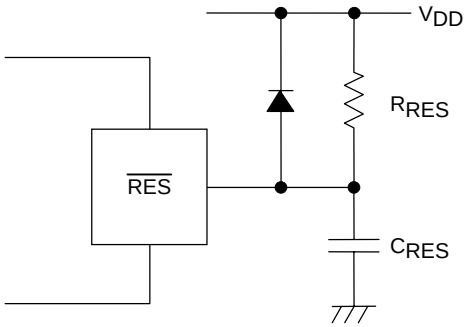


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note :
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

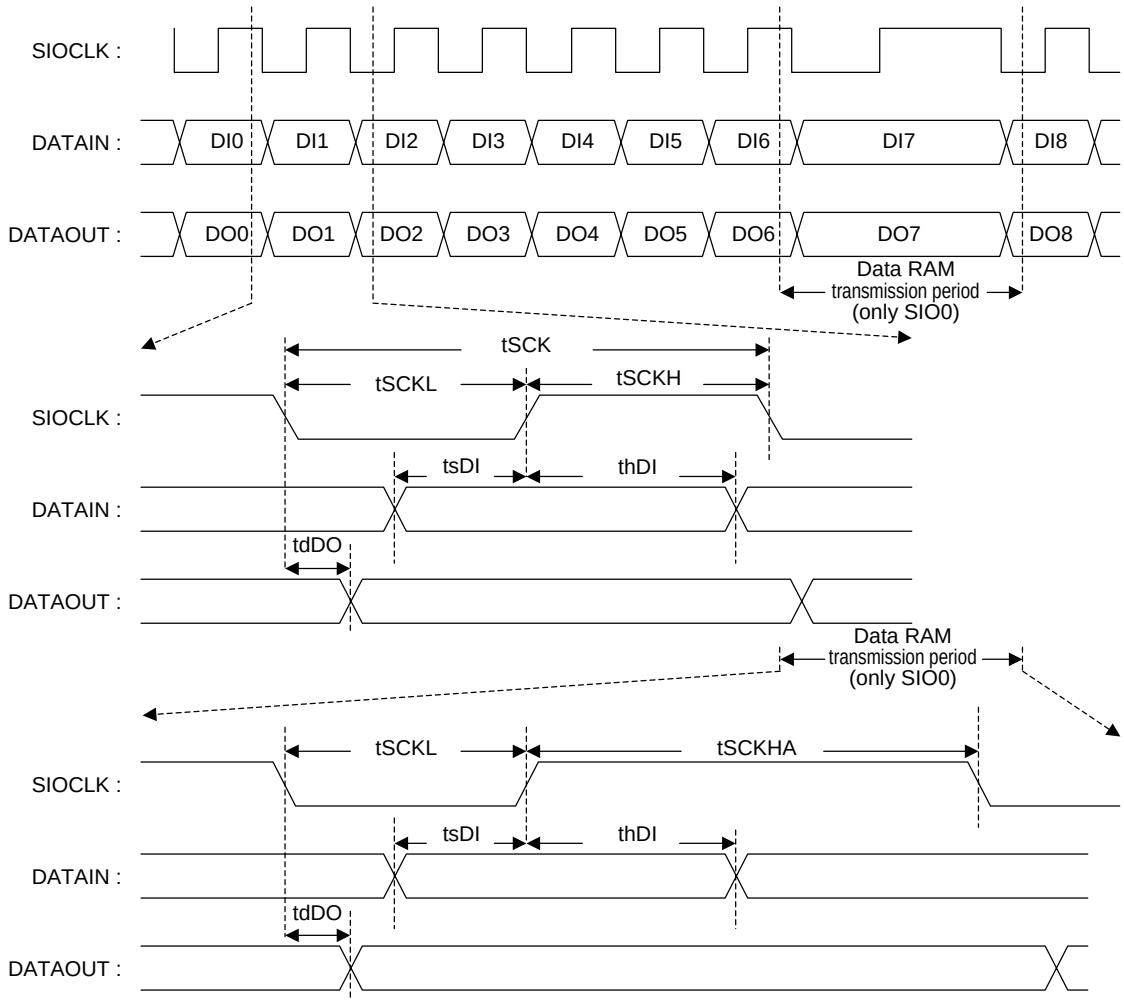


Figure 6 Serial I/O Wave form

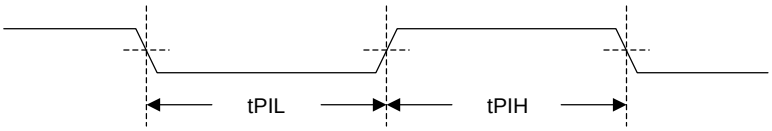


Figure 7 Pulse Input Timing Signal Waveform

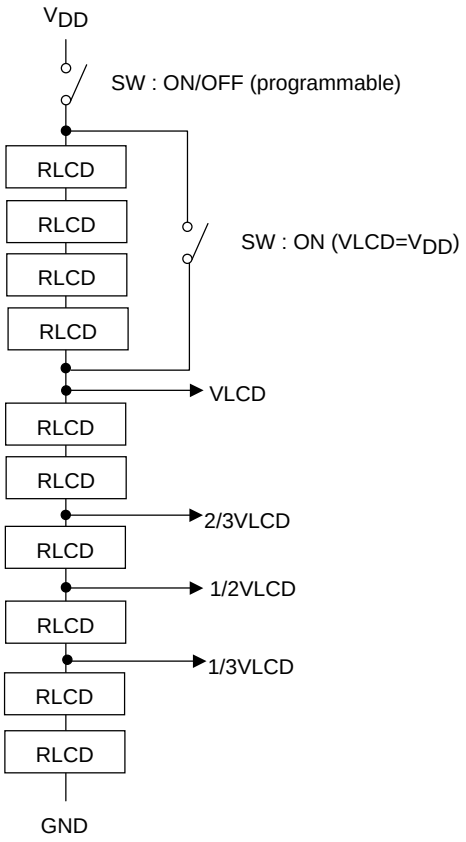


Figure 8 LCD bias resistor