Ordering number : EN*5014B

CMOS LSI

LC8904Q

Digital Audio Interface Receiver

Preliminary

Overview

The LC8904Q demodulates data transmitted between digital audio equipment in the EIAJ format (CP-1201) to a normal format signal synchronized with the receiving side input signal.

Features

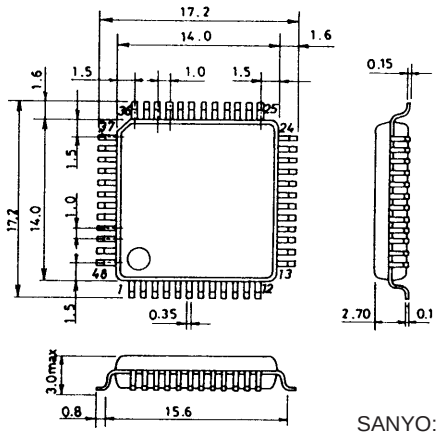
- Synchronizes with the transmitted EIAJ format signal using a built-in PLL circuit.
- Modes are set up and codes are output according to commands sent over a microprocessor interface.
  - — Input pin and output data format setup
  - — Selection of digital source mode or analog source mode
  - — 32-bit channel status output (consumer product mode 0)
  - — 80-bit subcode Q data output (CRC check included)
- Either a 384fs or a 512fs clock can be selected as the system clock.
- Provides 256fs, 128fs, BCLK, and LRCK clock outputs.
- Implements a CD subcode interface (CP-2401) using user bits.
- Fabricated in a CMOS single-voltage power supply process
- Package: QFP-48E

Package Dimensions

unit: mm

3156-QFP48E

[LC8904Q]



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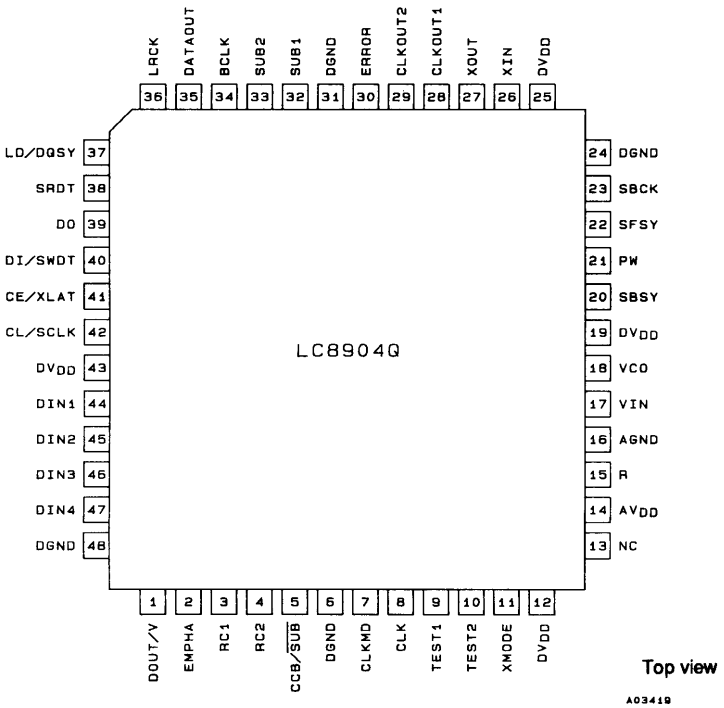
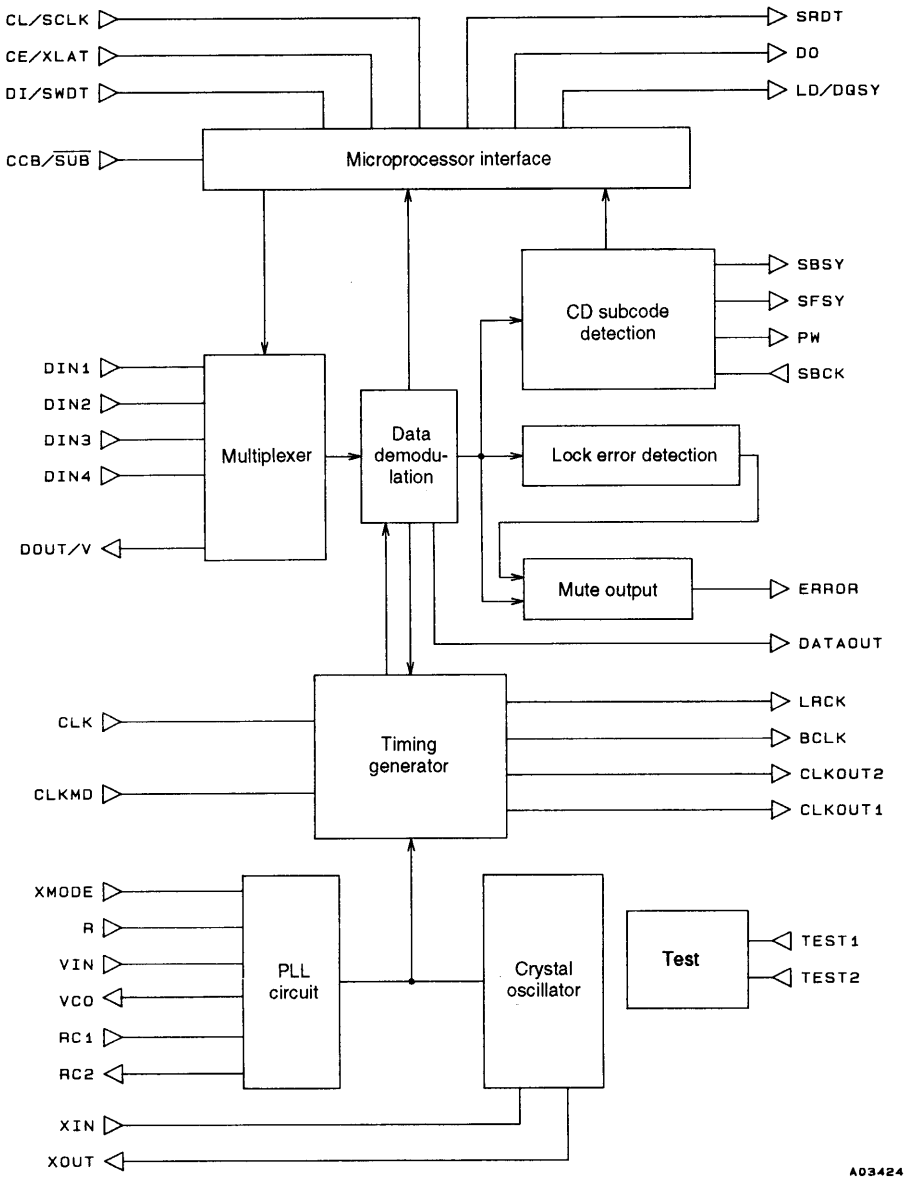
Pin Assignment



Block Diagram



Pin Functions

No.	Symbol	I/O	Function
1	DOUT/V	O	EIAJ data and validity flag output
2	EMPHA	O	Emphasis monitor output (High: emphasis applied)
3	RC1	I	CR oscillator input
4	RC2	O	CR oscillator output
5	CCB/$\overline{\text{SUB}}$	I	Microprocessor interface selection input (High: CCB, low: SUB)
6	DGND		Digital system ground
7	CLKMD	I	Clock output switching (High: 256fs, low: 128fs)
8	CLK	I	Clock switching input (High: 512fs, low: 384fs)
9	TEST1	I	Test pin (Must be tied low during normal operation.)
10	TEST2	I	Test pin (Must be tied low during normal operation.)
11	XMODE	I	Reset input
12	DV_{DD}		Digital system power supply
13	NC		No connection
14	AV_{DD}		Analog system power supply
15	R	I	VCO oscillator band adjustment input
16	AGND		Analog system ground
17	VIN	I	VCO free-running frequency setting input
18	VCO	O	PLL low-pass filter connection
19	DV_{DD}		Digital system power supply
20	SBSY	O	CD subcode interface: block sync output
21	PW	O	CD subcode interface: data output
22	SFSY	O	CD subcode interface: frame sync output
23	SBCK	I	CD subcode interface: data read shift clock input
24	DGND		Digital system ground
25	DV_{DD}		Digital system power supply
26	XIN	I	Crystal oscillator input
27	XOUT	O	Crystal oscillator output
28	CLKOUT1	O	VCO and crystal oscillator clock output
29	CLKOUT2	O	256fs or 128fs clock output (selected by CLKMD)
30	ERROR	O	Error mute output
31	DGND		Digital system ground
32	SUB1	O	Sampling frequency monitor output
33	SUB2	O	Sampling frequency monitor output
34	BCLK	O	Bit clock output
35	DATAOUT	O	Audio data output
36	LRCK	O	L/R clock output (High: left channel, low: right channel)
37	LD/DQSY	O	Microprocessor interface: subcode Q data sync output
38	SRDT	O	Microprocessor interface: data output when CCB/$\overline{\text{SUB}}$ is low (3-state output)
39	DO	O	Microprocessor interface: data output when CCB/$\overline{\text{SUB}}$ is high (High-level open drain output)
40	DI/SWDT	I	Microprocessor interface: data input
41	CE/XLAT	I	Microprocessor interface: chip enable/latch input
42	CL/SCLK	I	Microprocessor interface: clock input
43	DV_{DD}		Digital system power supply
44	DIN1	I	Data input with built-in amplifier
45	DIN2	I	Data input with built-in amplifier
46	DIN3	I	Data input with built-in amplifier
47	DIN4	I	Data input with built-in amplifier
48	DGND		Digital system ground

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input and output voltage	V_I · V_O		–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V

Electrical Characteristics

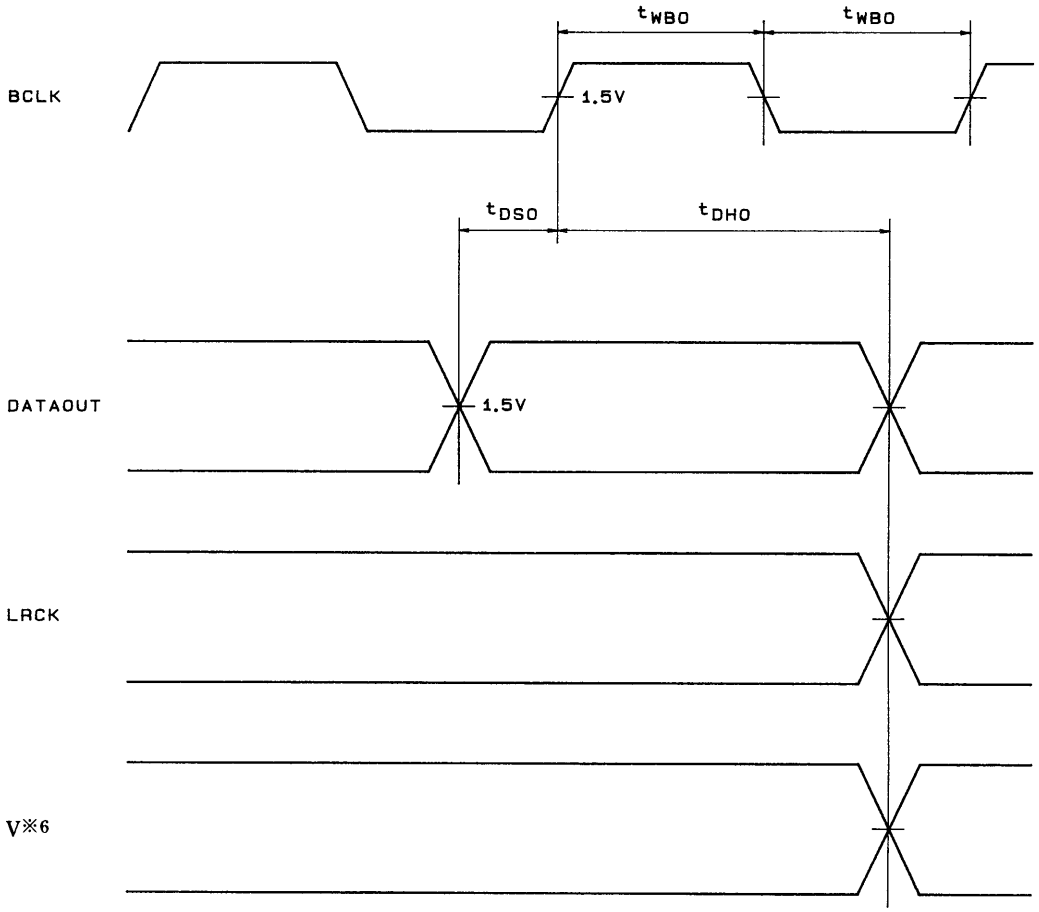
DC Characteristics at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level voltage	$V_{IH}1$	*1	2.2		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}1$	*1	–0.3		+0.8	V
Input high-level voltage	$V_{IH}2$	*2	0.7 V_{DD}		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}2$	*2	–0.3		0.3 V_{DD}	V
Input high-level voltage	$V_{IH}3$	*3	0.8 V_{DD}		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}3$	*3	–0.3		0.2 V_{DD}	V
Output high-level voltage	V_{OH}	I_{OH} = –1 µA	V_{DD} – 0.05			V
Output low-level voltage	V_{OL}	I_{OL} = 1 µA			V_{SS} + 0.05	V
Current drain	I_{DD}	*4		30	45	mA
Input amplitude	V_{PP}	*5	0.4		V_{DD} + 0.3	V

Note: 1. Input pins other than DIN1, DIN2, DIN3, DIN4, RC1, and XMODE. TTL compatible.
2. The XIN pin. CMOS compatible.
3. The XMODE and RC1 pins. CMOS Schmitt compatible.
4. V_{DD} = 5.0 V, Ta = 25°C, and input data with an fs of 48 kHz.
5. Conditions prior to the capacitances of the DIN1, DIN2, DIN3, and DIN4 pins.

AC Characteristics at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Output pulse width	t_{WBO}	fs = 48 kHz, load = 30 pF	160			ns
Output data setup time	t_{DSO}	fs = 48 kHz, load = 30 pF	80			ns
Output data hold time	t_{DHO}	fs = 48 kHz, load = 30 pF	80			ns

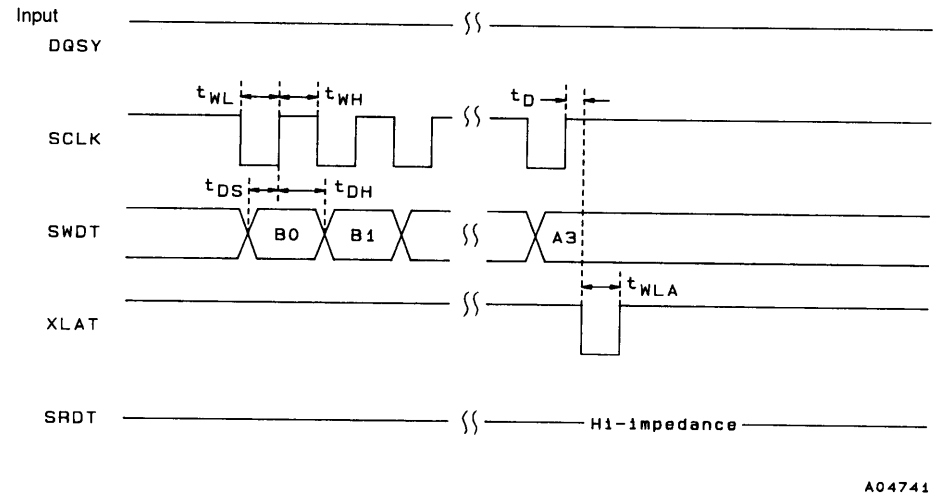


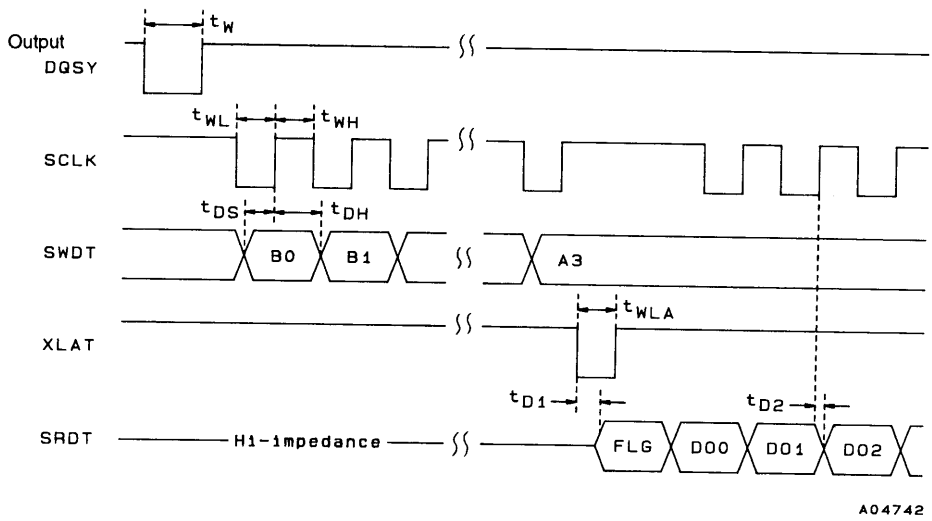
Note: When the validity fag is output from the DOUT/V pin.

Microprocessor Interface AC Characteristics (when CCB/$\overline{\text{SUB}}$ is low)

at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
SCLK low-level pulse width	t_{WL}		100			ns
SCLK high-level pulse width	t_{WH}		100			ns
Setup time	t_{DS}		50			ns
Hold time	t_{DH}		50			ns
Delay time	t_D		100			ns
Latch pulse time	t_{WLA}		100			ns
DQSY pulse time	t_W	fs = 44.1 kHz		136		µs
Data delay time	t_{D1}	C_L = 30 pF			75	ns
Data delay time	t_{D2}	C_L = 30 pF			75	ns

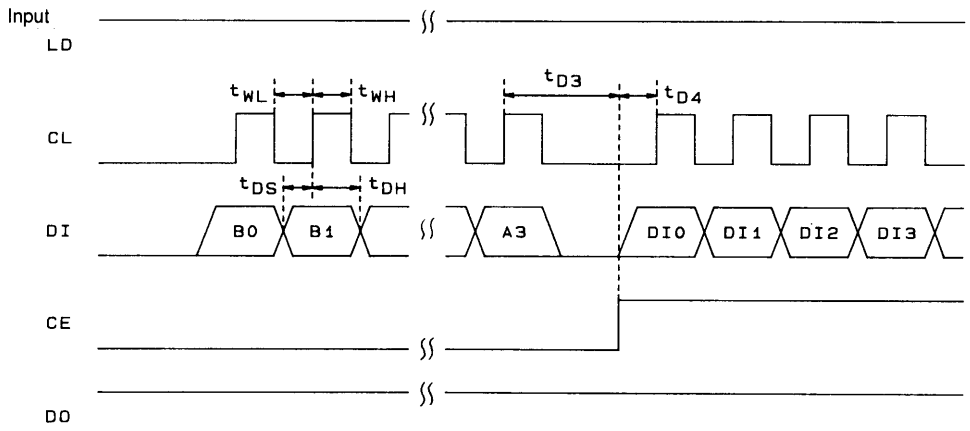


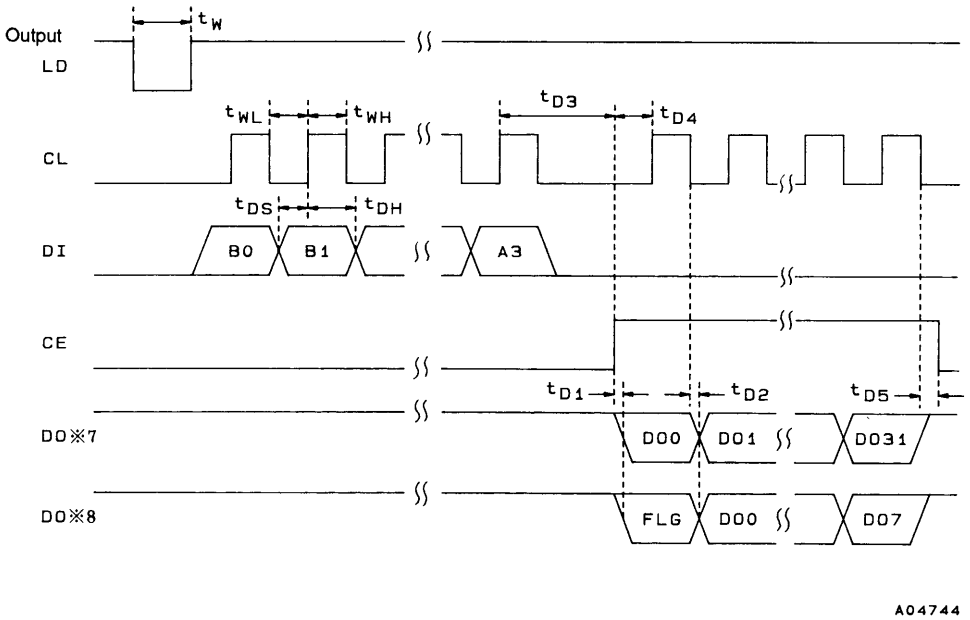


Microprocessor Interface AC Characteristics (when CCB/$\overline{\text{SUB}}$ is high)

at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
CL low-level pulse width	t_{WL}		100			ns
CL high-level pulse width	t_{WH}		100			ns
Data setup time	t_{DS}		50			ns
Data hold time	t_{DH}		50			ns
CE delay time	t_{D3}		1.0			µs
CL delay time	t_{D4}		50			ns
CE delay time	t_{D5}				100	ns
LD pulse time	t_W	fs = 44.1 kHz		136		µs
Data delay time	t_{D1}	C_L = 30 pF			75	ns
Data delay time	t_{D2}	C_L = 30 pF			75	ns

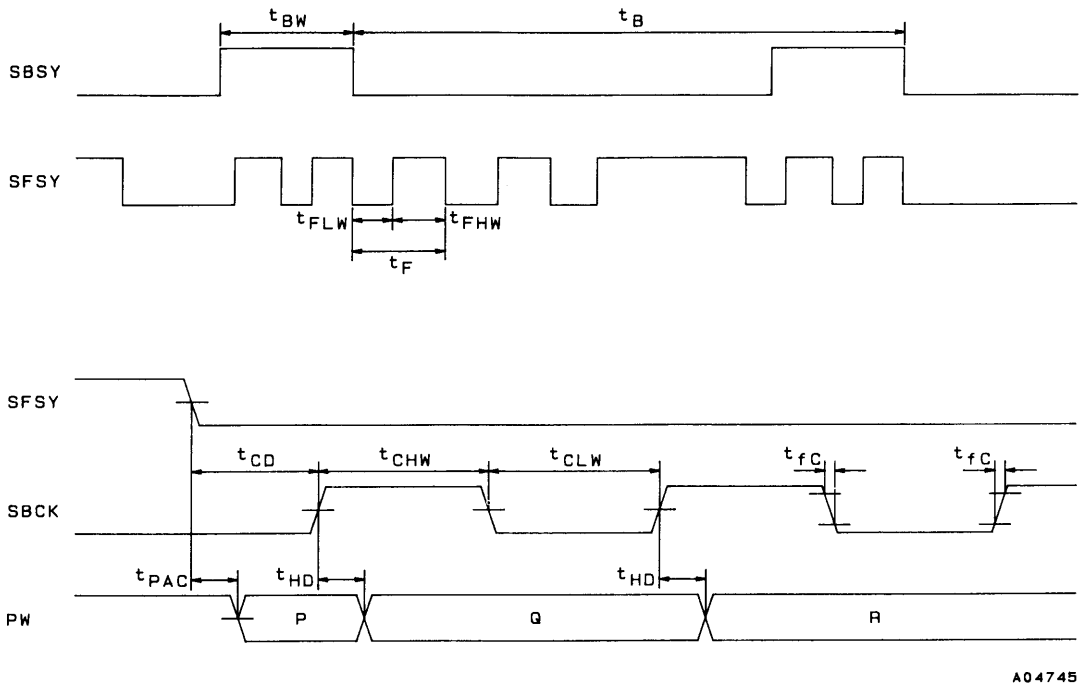




Note 1. C bit output
2. Subcode Q output

CD Subcode Interface AC Characteristics at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
SBSY block period	t_B		12.0	13.3	14.7	ms
SBSY pulse width	t_{BW}	*1	110			µs
SFSY frame period	t_F	*2	90	136	165	µs
SFSY high-level pulse width	t_{FHW}		4			µs
SFSY low-level pulse width	t_{FLW}		1.5			µs
SBCK high-level pulse width	t_{CHW}	*3	2.0	4.0	5.0	µs
SBCK low-level pulse width	t_{CLW}	*3	2.0	4.0	5.0	µs
SBCK rise time	t_{rC}				30	ns
SBCK fall time	t_{fC}				30	ns
SBCK delay time	t_{CD}	*3	10	20	30	µs
P data access time	t_{PAC}			3	10	µs
Data hold time	t_{HD}		0			µs



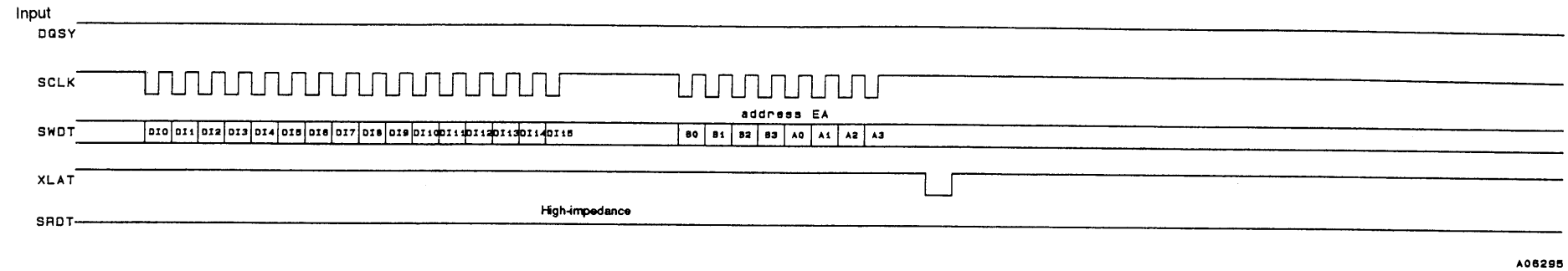
The LC8904Q subcode interface uses the user bit subcode sync word and start bit for system timing extraction. Therefore, since SBSY and SFSY will change with that timing, user bit transmission must follow the table shown below when using the values of t_{BW}, t_F, t_{CHW}, t_{CLW}, and t_{CD} with the specifications listed in the preceding tables.

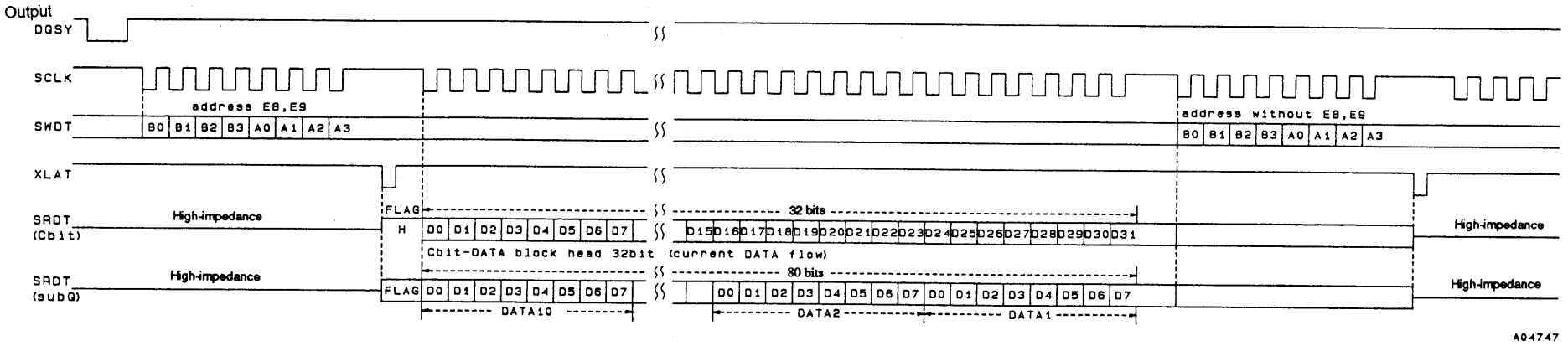
	1	2	3	4	5	6	7	8	9	10	11	12	
S0	0	0	0	0	0	0	0	0	0	0	0	0	Subcode sync word*1, 2
S1	0	0	0	0	0	0	0	0	0	0	0	0	
S2	1	Q2	R2	S2	T2	U2	V2	W2	0	0	0	0	
S3	1	Q3	R3	S3	T3	U3	V3	W3	0	0	0	0	
:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	
S97	1	Q97	R97	S97	T97	U97	V97	W97	0	0	0	0	
S0	0	0	0	0	0	0	0	0	0	0	0	0	Subcode sync word*1, 2
S1	0	0	0	0	0	0	0	0	0	0	0	0	
S2	1	Q2	R2	S2	T2	U2	V2	W2	0	0	0	0	Word length*2, 3
:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	

Note: 1. The subcode sync word is defined as the block sync section (block start) when 0-valued data has been received consecutively for at least 22 bits.
2. The period of the frame sync signal S0 is 90.7 µs. The S1 period also has a minimum length of 90.7 µs (when 0-valued data is received consecutively for 22 bits), depending on the subcode sync word period. Not that the shortest word is 10 bits.
3. The SBCK signal input delay (t_{HD}) and pulse widths (t_{CHW} and t_{CLW}) must be set to values less than or equal to the typical values when the shortest user data word length is used.

Microprocessor Interface

1. When CCB/$\overline{\text{SUB}}$ is low

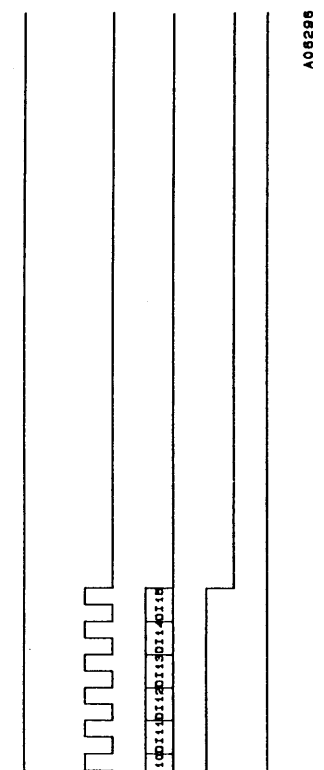




	CPU. IF address	DATA bit	FLAG	DATA flow									
C bit	E9	32 bits	H const	bit0 to bit31									
Sub Q	E8	80 bits	CRC ERROR L	DATA10	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1
				ADRS CTL	TNO	INDEX (POINT)	MIN	SEC	FRAME	ZERO	AMIN (PMIN)	ASEC (PSEC)	AFRAME (PFRAME)

sub Q I/F to CPU: LSB first 8 bits form output

2. When CCB/$\overline{\text{SUB}}$ is high



				DATA flow									
	CPU. IF address	DATA bit	FLAG	bit0 to bit31									
C bits	F8	32 bits	—	DATA10	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1
Sub Q	F9	80 bits	CRC ERROR L	ADRS/CTL	TNO	INDEX (POINT)	MIN	SEC	FRAME	ZERO	AMIN (PMIN)	ASEC (PSEC)	AFRAME (PFRAME)

sub Q I/F to CPU: LSB first 8 bits form output

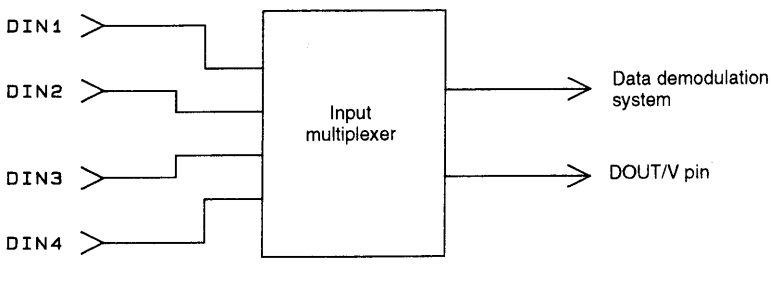
The microprocessor interface controls the following settings and outputs.

1. System stop
2. Data input pin settings
3. Validity flag (V flag) output selection
4. Analog source mode setting
5. Output data format setting
6. Channel status (32 bits) output
7. Output of the 80-bit subcode Q data with CRC flags.

- CCB/$\overline{\text{SUB}}$ pin
  The CCB/$\overline{\text{SUB}}$ pin selects one of two formats. The clocks and codes must be set up appropriately for each of these formats. SRDT is the output pin when CCB/$\overline{\text{SUB}}$ is low. SRDT goes to the high-impedance state when the CCB/$\overline{\text{SUB}}$ pin is high, during writes, and when an address for a different output is latched. In contrast with the SRT pin, the DO pin is a high-level open drain output that functions as the output pin when CCB/$\overline{\text{SUB}}$ is high.
- Data I/O address
  Address are allocated according to the differing formats as listed below.

Format / I/O	CCB/$\overline{\text{SUB}}$ = low									CCB/$\overline{\text{SUB}}$ = high								
		B0	B1	B2	B3	A0	A1	A2	A3		B0	B1	B2	B3	A0	A1	A2	A3
Data input	EA	0	1	0	1	0	1	1	1	F7	1	1	1	0	1	1	1	1
Data output (C bits)	E9	1	0	0	1	0	1	1	1	F8	0	0	0	1	1	1	1	1
Data output (subcode Q)	E8	0	0	0	1	0	1	1	1	F9	1	0	0	1	1	1	1	1

- Input
  The DIN1 to DIN4 data input pins have built-in amplifiers, and can accept signals with amplitudes of about 400 Vp-p. Note that the DOUT pin can be set up to output the EIAJ format data by microprocessor interface commands. (It can also be used to output the V flag.)



- Input code settings
  System stop by stopping both the VCO and crystal oscillators (DI4)

DI4	L	H
System	Run	Stop

Selection of data to demodulate (DI5, DI6)

DI5	L	H	L	H
DI6	L	L	H	H
Demodulation data input	DIN1	DIN2	DIN3	DIN4

Input data (EIAJ format) output selection

DI7	L	H	L	H
DI8	L	L	H	H
DOUT/V pin	DIN1	DIN2	DIN3	DIN4

V flag output selection (DI9)

DI9	L	H
DOUT/V pin	Data selected by DI7 and DI8	V flag

Source selection (DI10)

DI10	L	H
Mode	Digital source	Analog source

Audio data output format setting (DI11, DI12, DI13)

DI11	L	L	H	H	H	H
DI12	L	L	L	H	L	H
DI13	L	H	L	L	H	H
DATAOUT	16 bits MSB first Rear packed	16 bits MSB first Front packed	20 bits MSB first Rear packed	20 bits LSB first Rear packed	20 bits MSB first Front packed	20 bits LSB first Front packed

DI4 to DI13 are set to an initial value of low, immediately after the XMODE pin goes from low to high. Since DI0 to DI3 and DI14 to DI15 are unused they can be set to either low or high.

- Output

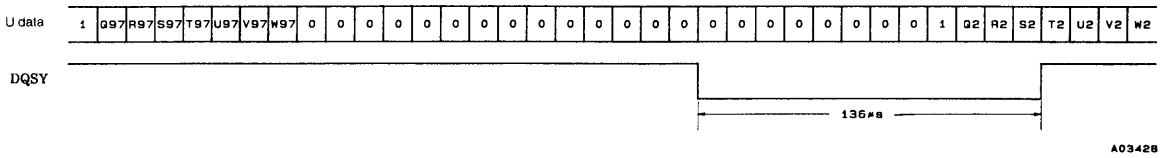
C bits

— This product only supports 32 bits, since it is designed for mode 0 consumer applications.
— In readout when CCB/$\overline{\text{SUB}}$ is low, after the output address is loaded into SWDT, the flag (fixed at the high level) is output on the fall of XLAT, and then 32 bits of data is output according to SCLK.
— In readout when CCB/$\overline{\text{SUB}}$ is high, after the output address is loaded into DI, the 32 bits of data are output from DO according to CL while CE is high.
— Since the C bits are not checked for errors, processing is performed after the PLL lock state is detected. Therefore, data must be read out only after the ERROR pin goes low.
— If a lock error occurs during readout (ERROR = high), the shift register will be reset and all data will become 0 (low). However, while the ERROR pin will also go high on a parity error, this error processing will not be performed.
— An interval of at least 6 ms or longer must be provided between readout operations.

Subcode Q

— The LC8904Q provides the following two functions for subcode readout:
  1. CD subcode interface (CP-2401) is possible
  2. Output of subcode Q data with CRC flags included, which corresponds to the CD and MD formats
  The microprocessor interface uses the readout function of item 2.
— The subcode Q data, which is reproduced at 1 bit per frame, is input to an 80-bit register and a CRC checking circuit. After the 96 bits of data have been input, it is loaded into a shift register on the falling edge of LD/DQSY. The data must be read out after this load operation.
— In readout when CCB/$\overline{\text{SUB}}$ is low, after the output address has been loaded into SWDT, the CRC flags are output on the falling edge of XLAT. If the CRC flags indicate that the check was OK, a high level is output. Next, 80 bits of data is output from SRDT according to SCLK. Note that the subcode Q data is updated on every falling edge of the DQSY signal.
— Readout when CCB/$\overline{\text{SUB}}$ is high is identical to that described in item 3. (See the timing charts for details.)
— The data output from SRDT (DO) has the same order on a per-byte basis, but the bit order within each byte is LSB first.
— If a lock error occurs between the fall of DQSY and the fall of XLAT, the CRC flags will go low. However, if a lock error after the fall of XLAT, the CRC flags will not go low, since correct data will be output.

— When the 96 bits of the subcode Q data have been read in with the PLL circuit in the locked state, a sync signal that has a low period with a pulse width of 136 µs is output by outputting at least 22 bits of continuous 0-valued data after the 96 bits of W data (W97) from DQSY. Note that this sync signal low-level pulse will not be output unless 96 bits of subcode Q data including the CRC flags are input.

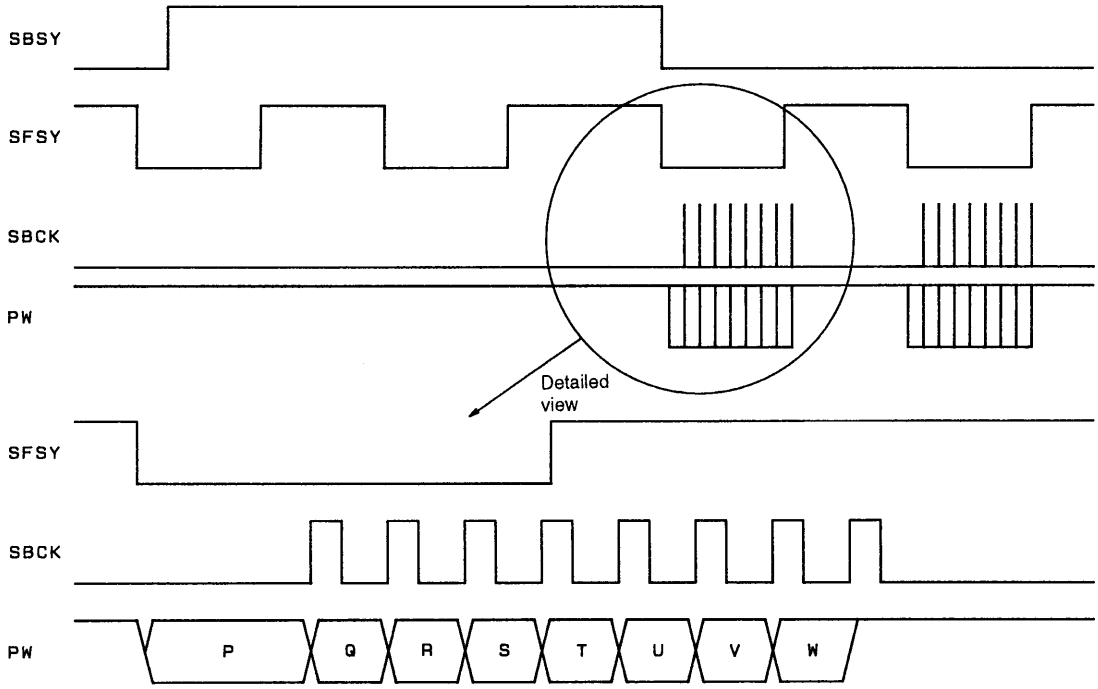


When not Using the Microprocessor Interface

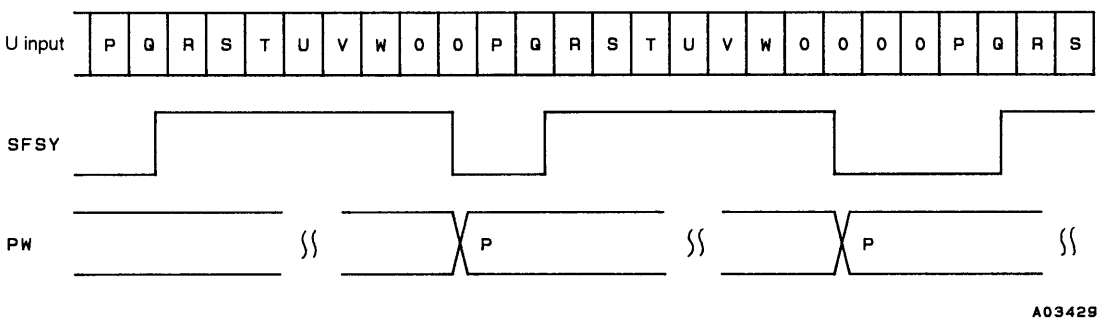
If the LC8904Q is used without using the microprocessor interface, the microprocessor interface pins must be tied to fixed levels and data only input to pin DIN1. This configuration can be useful as a simplified circuit evaluation method.

CD Subcode Interface

The LC8904Q outputs CD subcode data from the SFSY, SBCK, PW, and SBSY pins. These pins output user bits that were transmitted according to the CP-1201 standard and that were converted to the CP-2401 standard.



The timing of the rise and fall of the SFSY signal is converted into that shown in the figure below according to the timing of the start bit in the user bits in the input data.



The CLK, CLKMD, CLKOUT1, and CLKOUT2 Pins

The output clocks for the CLKOUT1 and CLKOUT2 clock output pins is selected by the CLK and CLKMD pins.

CLK	CLKOUT*1
L	Outputs a 384fs clock
H	Outputs a 512fs clock

CLKMD	CLKOUT2
L	Outputs a 256fs clock*2
H	Outputs a 128fs clock

Note: 1. The crystal oscillator clock is output in analog source mode.
2. The 256fs clock has a H:L duty ratio of 2:1 when the CLK pin is low.

The SUB1 and SUB2 Pins

These pins indicate the sampling frequency of the input data.

Pin	32 kHz	44.1 kHz	48 kHz	#1
SUB1	H	L	L	H
SUB2	H	L	H	L

The state “#1” is indicated on a PLL lock error and in analog source mode.
Also note that the DATAOUT and EMPHA pins will output low levels in this state.

The EMPHA Pin

Pin	Emphasis applied	Emphasis not applied	Analog source mode
EMPHA	H	L	L

The ERROR pin and Error Processing

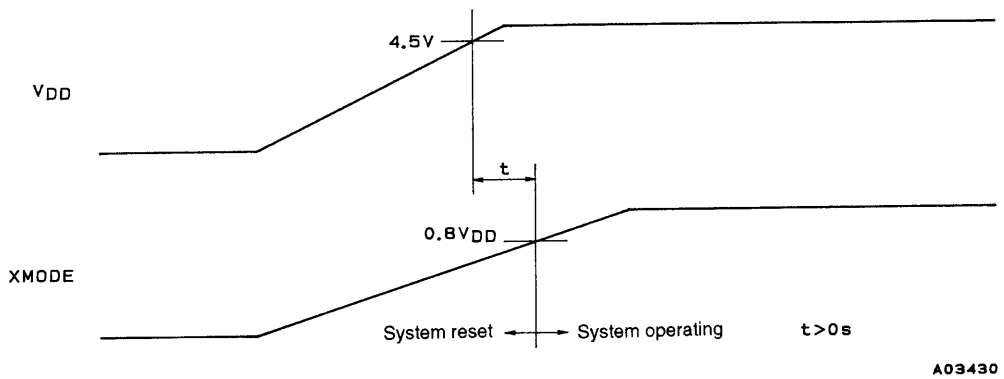
ERROR pin: When an error exists in the input data or when the PLL circuit is in the unlocked state, this pin goes high and holds that high level for about 200 to 300 ms after data demodulation returns to normal. The table below lists the data processing applied when an error occurs.

Type of error	DATAOUT	SUB1, SUB2	C bit	Sub Q*
Up to eight consecutive parity errors	Previous data	Output	Output	Output
Eight or more consecutive parity errors	L	Output	Output	Output
PLL lock error	L	#1	L	L

Note: * The CRC flags go low when a PLL lock error occurs.
Note: PLL lock error determination is performed starting from preamble detection.

The XMODE Pin

This pin is used for system reset. The system will start to operate normally if this pin is set high after the power supply has risen to at least 4.5 V. If XMODE is set low, the VCO free-running clock will be output from the CLKOUT1 pin.



After application of power, the system will be reset if the XMODE pin is set low again.

Analog Source Mode

The LC8904Q enters analog source mode in the following two cases:

1. Analog source mode is selected from the microprocessor interface.
2. If the input pin specified for data demodulation goes to the no signal state.

In this mode, the clock that operates the whole system is taken from the crystal oscillator clock, and the PLL and data demodulation circuits are stopped. The BCLK, LRCK, CLKOUT1, and CLKOUT2 clocks are output.

The output pins have the following functions in analog source mode:

1. DOUT/V
   Data output as specified by the microprocessor interface
2. ERROR
   Outputs the error state, i.e. a high level.
3. SUB1 and SUB2
   These pins output the “#1” lock error state.
4. DATAOUT
   Outputs the lock error state, i.e., a low level.
5. EMPHA
   Outputs the lock error state, i.e., a low level.
6. Microprocessor interface codes
   Input codes: The codes loaded from the microprocessor interface are retained.
   Output codes: The same codes as output for a PLL lock error.

Crystal Oscillator

1. A built-in detector circuit determines whether or not a data input signal is present. This circuit operates from either the VCO or the crystal oscillator clock. When the power supply is coming up, this clock is supplied from the VCO, and if a no-data state is detected, the system switches to the crystal oscillator clock. Here, if the clock is not supplied from the crystal oscillator after a no-data state is detected, the whole system goes to the stopped state, and, since the detector circuit does not operate even if data is supplied, the system will remain in the stopped state.
2. The XIN and XOUT pins include a built-in oscillator amplifier circuit, and operate as follows when a crystal oscillator element is attached.

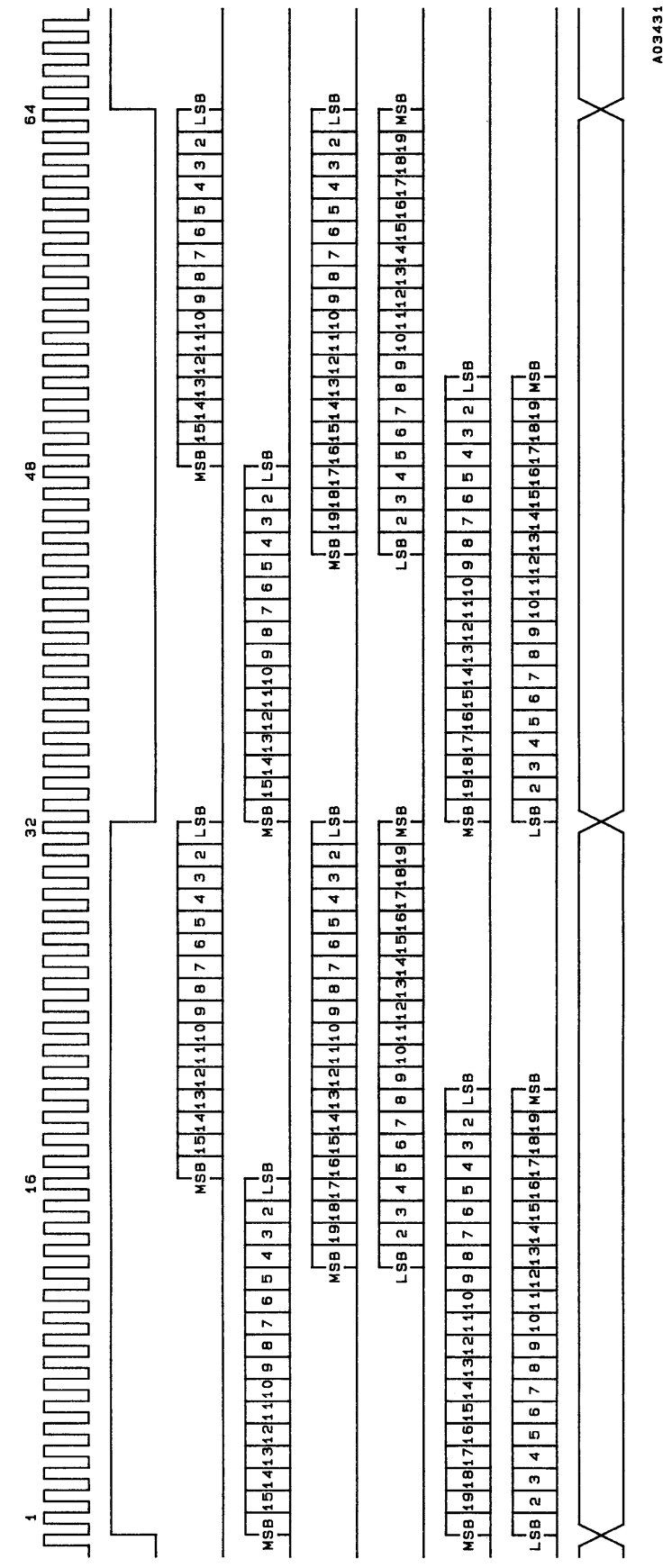
Pin	Data present*	No data
XIN	H	Crystal oscillator input accepted
XOUT	L	Outputs the inverse of the XIN pin state.

Note: * When data is present, the XIN pin is pulled up internally.

Data Output Timing

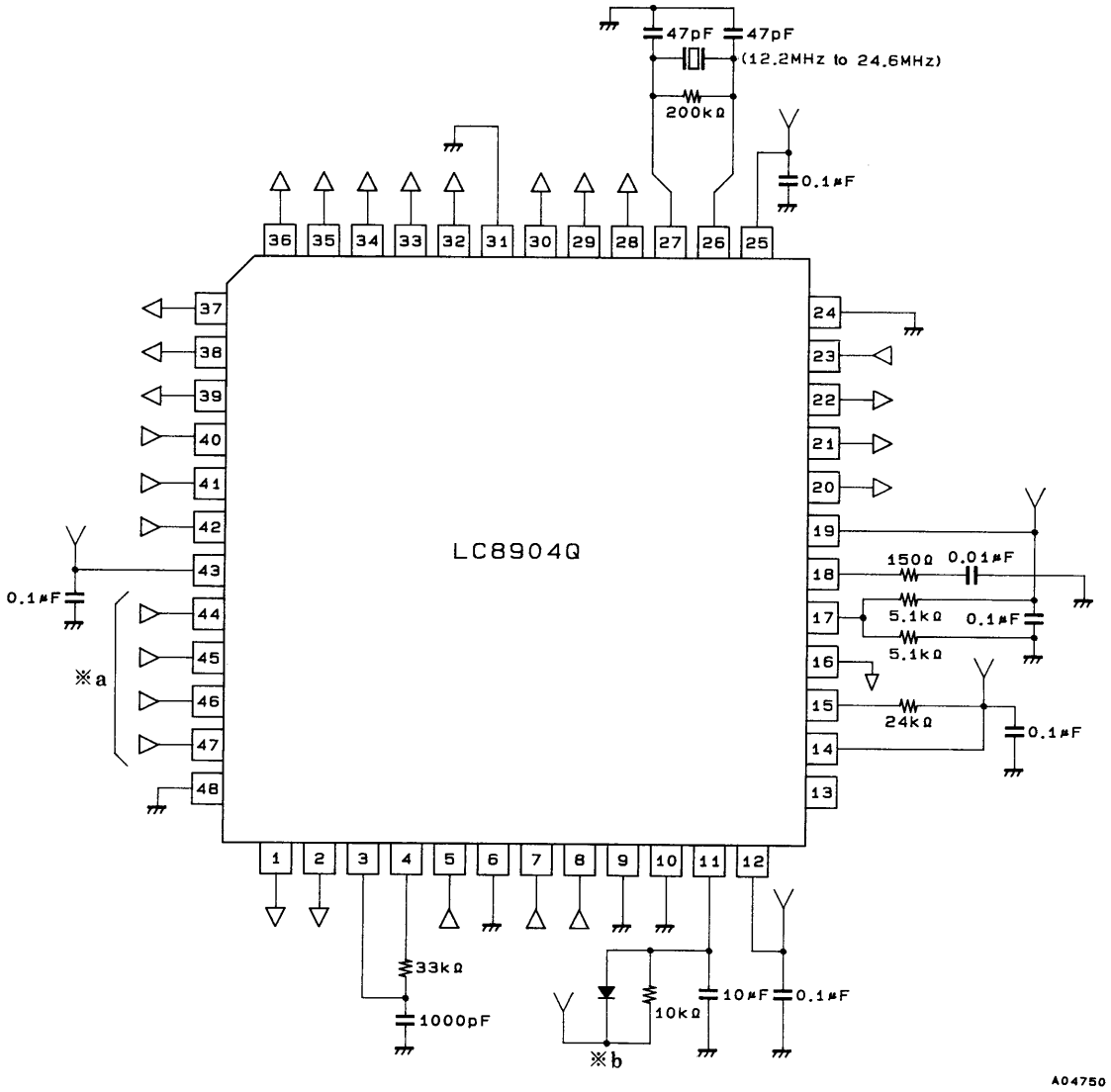
1. Data is output in synchronization with the falling edge of the BCLK signal.
2. Data, BCLK, and LRCK are output in synchronization with the rising edge of the 256fs clock.
3. The figure on the following page shows the data output timing.

Data Output Timing

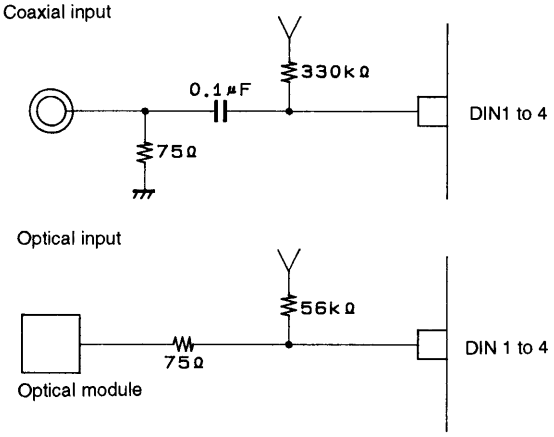


(1) 16-bit MSB-first rear-justified data output
(2) 16-bit MSB-first front-justified data output
(3) 20-bit MSB-first rear-justified data output
(4) 20-bit LSB-first rear-justified data output
(5) 20-bit MSB-first front-justified data output
(6) 20-bit LSB-first front-justified data output

Application Circuit Example



※a Coaxial input



※b
Shows the case for power on reset.