Ordering number : EN* 5192B

CMOS LSI

LC895195

ATA-PI (IDE) CD-ROM Decoder LSI

Preliminary

Overview

The LC895195 is a CD-ROM decoder LSI that includes both an on-chip IDE interface that was developed jointly with Western Digital and an on-chip subcode ECC function.

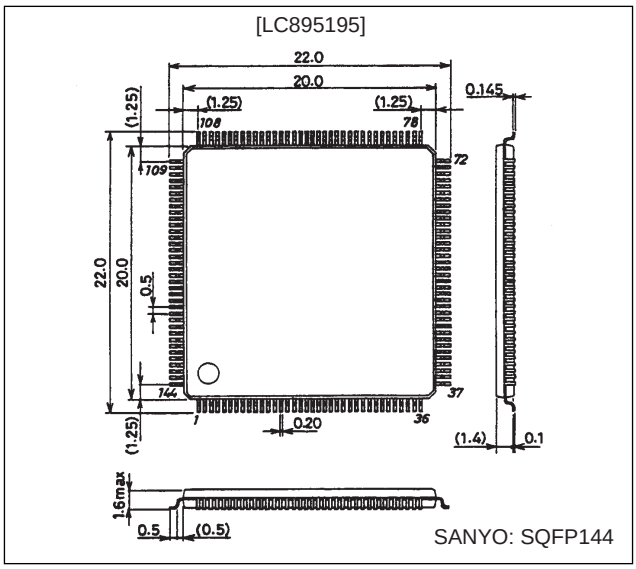
Features

- ATA-PI (IDE) interface
- Supports 16× playback (with IORDY) - Using ×16 70 ns DRAMs
- 16.6 MB/s transfer rate: Using ×16 70 ns DRAMs
- 8.33 MB/s transfer rate: Using ×8 70 ns DRAMs
- Supports the use of from 1 M to 32 M of buffer RAM. (DRAM)
- Allows the user to arbitrarily set the CD main channel, C2 flag and subcode areas in buffer RAM.
- Batch transfer function (function for transferring the CD main channel, C2 flag and subcode data in one operation)
- Multi-transfer function (function for sending multiple blocks in one operation)

Package Dimensions

unit: mm

3214-SQFP144



Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
I/O voltages	V_I, V_O max	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	550	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering heat resistances (pins only)		10 seconds	235	°C
I/O current	I_I, I_O max		±20*	mA

Note: * Per cell for basic I/O cells

Allowable Operating Ranges at Ta = –30 to +75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

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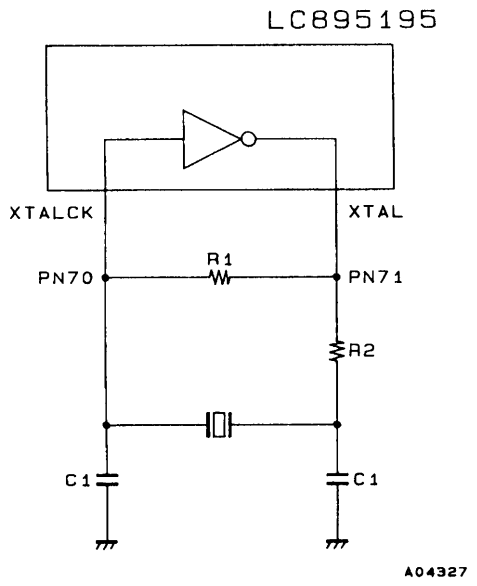
DC Characteristics at V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = –30 to +75°C

Parameter	Symbol	Applicable Pins* (See below)		min	typ	max	Unit
Input high level voltage	$V_{IH}1$	TTL compatible: (1)		2.2			V
Input low level voltage	$V_{IL}1$					0.8	V
Input high level voltage	$V_{IH}2$	TTL compatible, with pull-up resistor: (9)		2.2			V
Input low level voltage	$V_{IL}2$					0.8	V
Input high level voltage	$V_{IH}3$	TTL compatible, Schmitt: (2), and (10)		2.2			V
Input low level voltage	$V_{IL}3$					0.8	V
Output high level voltage	$V_{OH}1$	I_{OH} = –2 mA	(5), (7), and (9)	V_{DD} – 2.1			V
Output low level voltage	$V_{OL}1$	I_{OL} = 2 mA				0.4	V
Output high level voltage	$V_{OH}2$	I_{OH} = –8 mA	(3)	V_{DD} – 2.1			V
Output low level voltage	$V_{OL}2$	I_{OL} = 8 mA				0.4	V
Output high level voltage	$V_{OH}3$	I_{OH} = –4 mA	(6), and (10)	V_{DD} – 2.1			V
Output low level voltage	$V_{OL}3$	I_{OL} = 24 mA				0.4	V
Output high level voltage	$V_{OL}5$	I_{OL} = 24 mA: (8)				0.4	V
Output high level voltage	$V_{OL}4$	I_{OL} = 2 mA: (4)				0.4	V
Input leakage current	I_{IL}	V_I = V_{SS}, V_{DD}: (1), (2),and (10)		–10		+10	µA
Output leakage current	I_{OZ}	For high-impedance outputs: (6), and (10)		–10		+10	µA
Pull-up resistance	R_{UP}	(9)		40	80	160	kΩ

Note: * The entries in the “Applicable Pins” column specify the following pin sets.
[Input]
1: CSCTRL, SUA0 to SUA6, TEST0 to TEST4
2: SBSO, SCOR, WFCK, ZCS, ZDIOR, ZDIOW, ZDMACK, ZHRST, ZRESET, ZRD, ZWR, BCK, C2PO, LRCK, SDATA, DA0 to DA2, ZCS1FX, ZCS3FX
[Output]
3: MCK, MCK2
4: ZRSTCPU, ZRSTIC, ZINT1
5: ZINT, ZSWAIT
6: DMARQ, HINTRQ
7: RA0 to RA9, ZCAS0, ZCAS1, ZLWE, ZOE, ZRAS0, ZRAS1, ZUWE, EXCK
8: IORDY, ZIOCS16
[I/O]
9: D0 to D7, IO0 to IO15
10: DD0 to DD15, ZDASP, ZPDIAG

Note: XTAL, XTALCK
The above pins are not included in the DC characteristics.

Sample Recommended Oscillator Circuit



R1 = 120 kΩ
R2 = 47 kΩ
C1 = 30 pF
For a crystal oscillator frequency of 16.9344 MHz.
Alternatively:
R1 = 3.3 kΩ
R2 = None
C1 = 5 pF
For a crystal oscillator frequency of 33.8688 MHz.
For an oscillator frequency of 33.8688, the third harmonic is used. This means that precise component values will be influenced by the printed circuit board. Consult the manufacturer of the crystal to determine the circuit constants for this frequency.

Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
1	V_{SS0}	P	
2	ZRAS0	O	Buffer DRAM RAS signal output 0 (This pin is used normally.)
3	ZRAS1	O	Buffer DRAM RAS signal output 1
4	V_{SS0}	P	
5	ZCAS0	O	Buffer DRAM CAS signal output 0 (This pin is used normally.)
6	ZCAS1	O	Buffer DRAM CAS signal output 1
7	V_{SS0}	P	
8	ZOE	O	Buffer RAM output enable
9	ZUWE	O	Buffer RAM upper write enable
10	ZLWE	O	Buffer RAM lower write enable
11	RA0	O	RA0 to RA6 are the data buffer DRAM address signal output.
12	RA1	O	
13	RA2	O	
14	RA3	O	
15	RA4	O	
16	RA5	O	
17	RA6	O	
18	V_{DD}	P	
19	V_{SS0}	P	
20	RA7	O	RA7 to RA9 are the data buffer DRAM address signal output.
21	RA8	O	
22	RA9	O	
23	V_{SS0}	P	
24	TEST0	NC	
25		NC	
26	TEST1	NC	
27	TEST2	NC	
28	TEST3	NC	
29		NC	
30	IO0	B	Data buffer DRAM data I/O These pins have built-in pull-up resistors.
31	IO1	B	
32	IO2	B	
33	IO3	B	
34	IO4	B	
35	IO5	B	
36	V_{SS0}	P	
37	V_{DD}	P	
38	IO6	B	Data buffer DRAM data I/O These pins have built-in pull-up resistors.
39	IO7	B	
40	IO8	B	
41	IO9	B	
42	IO10	B	
43	IO11	B	
44	IO12	B	
45	IO13	B	
46	IO14	B	
47	IO15	B	
48	EXCK	O	SUB-CODE I/O
49	WFCK	I	
50	SBSO	I	

Note: 1. NC (no connection) pins must be left open.
2. Pin names (signal names) that begin with a Z have negative (inverted) logic.
3. V_{SS0} is the logic system ground and V_{SS1} is the IDE interface driver ground.

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
51	SCOR	I	SUB-CODE input pin
52	V_{SS0}	P	
53	V_{SS0}	P	
54	TEST4	I	Test input. This must be tied low.
55	V_{SS0}	P	
56	V_{SS0}	P	
57	ZINT1	O	Interrupt request signal output to the microcontroller from the IDE block.
58	V_{SS0}	P	
59	V_{SS0}	P	
60	V_{SS0}	P	
61		NC	
62		NC	
63	V_{SS0}	P	
64	SDATA	I	CD-DSP interface
65	BCK	I	
66	LRCK	I	
67	C2PO	I	
68	MCK2	O	XTALCK 1/1, 1/2, 1/512, and stop output
69	V_{SS0}	P	
70	XTALCK	I	Xtal oscillator input
71	XTAL	O	Xtal oscillator output
72	V_{SS0}	P	
73	V_{DD}	P	
74	MCK	O	XTALCK 1/1, 1/2, and stop output
75	V_{SS0}	P	
76	ZRSTIC	I	Reset signal to drive reset IC
77	CSCTRL	I	Selects active high or active low for the microcontroller CS line.
78	ZRESET	I	LSI reset
79	ZRD	I	Microcontroller data read signal input
80	ZWR	I	Microcontroller data write signal input
81	ZCS	I	Input for the register chip select signal from the microcontroller
82	V_{SS0}	P	
83	SUA0	I	Microcontroller register select signals
84	SUA1	I	
85	SUA2	I	
86	SUA3	I	
87	SUA4	I	
88	SUA5	I	
89	SUA6	I	
90	V_{DD}	P	
91	V_{SS0}	P	
92	D0	B	Microcontroller data signals These pins have built-in pull-up resistors.
93	D1	B	
94	D2	B	
95	D3	B	
96	D4	B	
97	D5	B	
98	D6	B	
99	D7	B	
100	ZINT	O	Interrupt request signal output to the microcontroller

Note: 1. NC (no connection) pins must be left open.
2. Pin names (signal names) that begin with a Z have negative (inverted) logic.
3. V_{SS0} is the logic system ground and V_{SS1} is the IDE interface driver ground.

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
101	ZRSTCPU	O	
102	ZWAIT	O	
103	ZHRST	I	ATAPI control signals
104	ZDASP	B	
105	ZCS3FX	I	
106	ZCS1FX	I	
107	DA2	I	
108	V_{SS0}	P	
109	V_{DD}	P	
110	DA0	I	ATAPI control signals
111	ZPDIAG	B	
112	DA1	I	
113	ZIOCS16	O	
114	HINTRQ	O	
115	ZDMACK	I	
116	V_{SS1}	P	
117	IORDY	O	ATAPI control signals
118	ZDIOR	I	
119	ZDIOW	I	
120	DMARQ	O	
121	DD15	B	ATAPI data bus
122	V_{SS1}	P	
123	DD0	B	
124	DD14	B	ATAPI data bus
125	DD1	B	
126	DD13	B	
127	V_{SS1}	P	
128	V_{DD}	P	
129	DD2	B	ATAPI data bus
130	DD12	B	
131	DD3	B	
132	V_{SS1}	P	
133	DD11	B	ATAPI data bus
134	DD4	B	
135	DD10	B	
136	V_{SS1}	P	
137	V_{DD}	P	
138	DD5	B	ATAPI data bus
139	DD9	B	
140	DD6	B	
141	V_{SS1}	P	
142	DD8	B	ATAPI data bus
143	DD7	B	
144	V_{DD}	P	

Note: 1. NC (no connection) pins must be left open.
2. Pin names (signal names) that begin with a Z have negative (inverted) logic.
3. V_{SS0} is the logic system ground and V_{SS1} is the IDE interface driver ground.

Pin Functions

1. ATA-PI Pins
   - ZCS1FX (input)
     Chip select signal for selecting the command block register.
   - ZCS3FX (input)
     Chip select signal for selecting the control block register.
   - DA0 to DA2 (input)
     Address for accessing the ATAPI registers.
   - ZDASP (I/O)
     Drive 1 is output and drive 0 is input.
     Signal used to indicate to drive 0 that drive 1 exists.
     An external pull-up resistor must be connected to this pin.
   - DD0 to DD15 (I/O)
     16-bit data bus. Can be used for either 8-bit or 16-bit data transfers.
   - ZDIOR (input)
     Read strobe signal from the host.
   - ZDIOW (input)
     Write strobe signal from the host.
   - ZDMACK (input)
     Acknowledge signal from the host in response to the drive DMARQ request signal during DMA transfers.
     The pin circuit does not include a pull-up resistor.
   - DMARQ (output)
     Drive request signal during DMA transfers
   - HINTRQ (output)
     Drive interrupt signal to the host
   - ZIOCS16 (output)
     Signal asserted by the drive when the drive supports 16-bit transfers.
     This signal is not asserted during DMA transfers.
   - IORDY (output)
     Signal that indicates that the drive has completed response preparations during data transfers.
     This signal is low when the drive is not ready.
   - ZPDIAG (I/O)
     Signal asserted by drive 1 to inform drive 0 that diagnostics have completed.
     An external pull-up resistor must be connected to this pin.
   - ZHRST (input)
     Reset signal from the host.
     The pin circuit does not include a pull-up resistor.

2. MC (microcontroller) Interface Pins
   - ZCS (input)
     Microcontroller chip select signal
   - CSCTRL (input)
     Microcontroller chip select logic selection signal
     High - ZCS functions as an active low signal.
     Low - ZCS functions as an active high signal.
   - ZRD, ZWR, SUA0 to SUA6 (input)
     Microcontroller interface control signals.
     The SUA0 to SUA6 pins are address lines.

- ZSWAIT (output)
  When the microcontroller is accessing RAM, the sub-CPU must wait if this pin is low.
- D7 to D0 (I/O)
  Microcontroller data bus. Pull-up resistors are built in.
- ZINT (output)
  Interrupt request signal output to the microcontroller. A pull-up resistor is built in.
- ZINT1 (output)
  Interrupt request signal output from the IDE block to the microcontroller. An external pull-up resistor must be connected to this pin.

3. Buffer RAM Pins
   - IO0 to IO15 (I/O)
     Buffer DRAM data bus. A pull-up resistor is built in.
   - RA0 to RA9 (output)
     Buffer RAM address lines.
   - ZRAS0, ZRAS1 (output)
     Buffer DRAM RAS outputs. Normally, ZRAS0 is used, but if two 1-Mb (64k × 16 bits) chips are used, then both ZRAS0 and ZRAS1 are used, one for each of the chips.
   - ZCAS0, ZCAS1 (output)
     Buffer DRAM CAS outputs. Normally, ZCAS0 is used, but if two 1-Mb (64k × 16 bits) chips are used, then both ZCAS0 and ZCAS1 are used, one for each of the chips. When using a two-CAS type DRAM, connect ZCAS0 to UCAS, and ZCAS1 to LCAS.
   - ZOE (output)
     Buffer DRAM read output signal.
   - ZUWE, ZLWE (output)
     Buffer DRAM write output signals. Connected the corresponding DRAM pins.

4. Subcode Interface Pins
   - EXCK, WFCK, SBSO, SCOR (input or output)
     These are the subcode interface connections. The LC895195 acquires subcode data by connection with the CD-DSP and sends that data to the host.

5. CD-DSP Data Pins
   - BCK, SDATA, LRCK, C2PO (input)
     The LC895195 reads in the CD-ROM data by connecting to the CD-DSP.
     The C2PO pin is used for the C2 flags.

6. Other Pins
   - ZRESET (input)
     This is the LC895195 reset pin. The LC895195 is reset by a low level on this pin.
     This pin must be held low for at least 1 μs when power is first applied.
   - XTALCK, XTAL
     These pins can drive a 16.9344-MHz or 33.8688-MHz oscillator.
     Alternatively, an external clock can be input to the XTALCK pin.
   - MCK (output)
     This pin outputs either the XTALCK frequency or that frequency divided by 2. This output can be turned off.
   - MCK2 (output)
     This pin outputs either the XTALCK frequency or that frequency divided by 512. This output can be turned off.
   - ZRSTIC (output)
     This pin can be set to output a low level either by writing to the microcontroller write register R46 bit 7 (ZSYSRTS) or by setting the ZHRST pin (pin 103) low. This pin goes to the high-impedance state when both ZSYSRST and ZHRST are high.
     Since this pin has an open-drain circuit, an external pull-up resistor must be used.

- ZRSTCPU (output)
  When an ATAPI soft reset command (08h) has been received, this pin generates a low-going pulse with a duration of about 1 ms (when the XTALCK frequency is 34 MHz). (This pulse will have a duration of about 2 ms when the XTALCK frequency is 16 MHz.)
  At this time a microcontroller interrupt will be generated. When the ZRESET pin (pin 78) becomes active (low), the ZRESET signal will be output without change to the ZRSTCPU pin.
  Since this pin has an open-drain circuit, an external pull-up resistor must be used.