



## 40× Playback/12× Write CD-R/RW Encoder/Decoder IC with Built-in ATAPI Interface

# LC898093

Preliminary

**BURN-Proof™**

### Functions

- CD-ROM decoder/encoder functions
- CD decoder/encoder functions
- Pit and wobble CLV servo
- CAV audio functions
- ATAPI interface (include the register block)
- Subcode encoder/decoder functions
- ATIP demodulator/ATIP decoder
- Write strategy function (CD-R/RW)

### Features

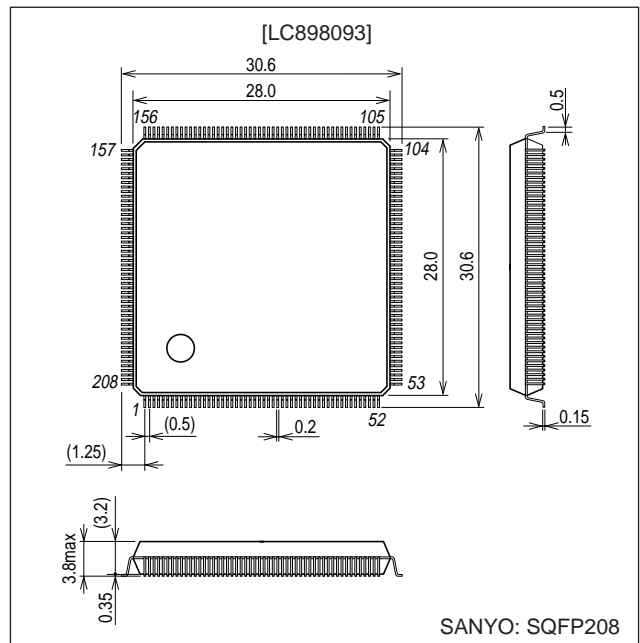
- ECC and EDC correction/addition (decoding/encoding) for CD-ROM data.
- ECC error correction/addition (decoding/encoding) for subcode data
- Servo control implemented in a digital servo system (decoding/encoding)
- CLV servo control using ATIP data (encoding)
- ATIP decoding function and CRC check function (decoding/encoding)
- CIRC code generation and addition and EFM modulation (encoding)
- CAV audio functions
- Provides high-precision CD-R/RW write strategy signal output
- Built-in ATAPI interface (with Ultra DMA 33 support)
- Supports 40× decoding and 12× encoding.  
Clock frequency: 33.8688 MHz
- Transfer rates: Up to 16.6 MB/s (when 32× IORDY used), up to 33 MB/s when Ultra DMA used. These values apply when 16-bit 45 ns EDO DRAM is used.

- From 1 to 64 Mbits of buffer RAM can be used. (16-bit data bus EDO DRAM)
- The user can freely set up the CD main channel, C2 flag, and subcode areas in buffer RAM.
- Batch transfer function (Function for transferring the CD main channel, C2 flag, subcode, and other data in a single operation)
- Multi-transfer function (Function for automatically transferring multiple block to the host in a single operation)
- CAV audio functions
- Supports Ultra DMA modes 0, 1, and 2.

### Package Dimensions

unit: mm

#### 3210-SQFP208



“BURN-Proof” stands for Proof against Buffer Under Run error, not for proof against burning.  
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## LC898093

## Specifications

Absolute Maximum Ratings at  $V_{SS} = 0\text{ V}$ 

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD5\text{ max}}$	$T_a \leq 25^\circ\text{C}$	-0.3 to +6.0	V
	$V_{DD3\text{ max}}$	$T_a \leq 25^\circ\text{C}$	-0.3 to +4.6	V
I/O voltages	$V_{I5}, V_{O5}$	$T_a \leq 25^\circ\text{C}$	-0.3 to $V_{DD5} + 0.3$	V
	$V_{I3}, V_{O3}$	$T_a \leq 25^\circ\text{C}$	-0.3 to $V_{DD3} + 0.3$	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 70^\circ\text{C}$	750	mW
Operating temperature	$T_{opr}$		-30 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$
Soldering conditions (pins only)		10 seconds	260	$^\circ\text{C}$

Allowable Operating Ranges at  $T_a = -30\text{ to }+70^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ 

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[I/O cells, 5.0 V power supply]						
Supply voltage	$V_{DD5}$		4.5	5.0	5.5	V
Input voltage range	$V_{IN}$		0		$V_{DD5}$	V
[Internal cells, 3.3 V power supply]						
Supply voltage	$V_{DD3}$		3.0	3.3	3.6	V
Input voltage range	$V_{IN}$		0		$V_{DD3}$	V

Electrical Characteristics at  $T_a = -30\text{ to }+70^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 4.5\text{ to }5.5\text{ V}$ 

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input voltage	$V_{IH}$	TTL level inputs: (1)	2.2			V
Low-level input voltage	$V_{IL}$				0.8	V
High-level input voltage	$V_{IH}$	TTL level inputs with built-in pull-up resistors: (4)	2.2			V
Low-level input voltage	$V_{IL}$				0.8	V
High-level input voltage	$V_{IH}$	TTL level Schmitt trigger inputs: (0), (7)	2.4			V
Low-level input voltage	$V_{IL}$				0.8	V
High-level input voltage	$V_{IH}$	TTL level Schmitt trigger inputs Built-in pull-up resistors: (9), (14)	2.4			V
Low-level input voltage	$V_{IL}$				0.8	V
High-level input voltage	$V_{IH}$	CMOS level inputs with built-in pull-up resistors: (10)	0.7 $V_{DD}$			V
Low-level input voltage	$V_{IL}$				0.3 $V_{DD}$	V
Analog input voltage	$V_{ANI}$	(11)	1/4 $V_{DD}$		3/4 $V_{DD}$	V
High-level output voltage	$V_{OH}$	$I_{OH} = -8\text{ mA}$ : (3), (8)	$V_{DD} - 2.1$			V
Low-level output voltage	$V_{OL}$	$I_{OL} = 8\text{ mA}$ : (3), (8)			0.4	V
High-level output voltage	$V_{OH}$	$I_{OH} = -2\text{ mA}$ : (2), (4), (6)	$V_{DD} - 2.1$			V
Low-level output voltage	$V_{OL}$	$I_{OL} = 2\text{ mA}$ : (2), (4), (6)			0.4	V
Low-level output voltage	$V_{OL}$	$I_{OL} = 2\text{ mA}$ : (5)			0.4	V
High-level output voltage	$V_{OH}$	$I_{OH} = -8\text{ mA}$ : (7), (12), (14), (15)	$V_{DD} - 2.1$			V
Low-level output voltage	$V_{OL}$	$I_{OL} = 24\text{ mA}$ : (7), (12), (14), (15)			0.4	V
Input leakage current	$I_{IL}$	$V_I = V_{SS}, V_{DD}$ : (0), (1), (7), (9)	-10		+10	$\mu\text{A}$
Output leakage current	$I_{OZ}$	In the high-impedance output state: (2), (7), (8), (12), (13), (14), (15)	-10		+10	$\mu\text{A}$
Pull-up resistance	$R_{UP}$	(10)	50	100	200	$\text{k}\Omega$
Pull-up resistance	$R_{UP}$	(4), (5)	40	80	160	$\text{k}\Omega$
Pull-up resistance	$R_{UP}$	(9), (13), (14)	7	10	13	$\text{k}\Omega$
Pull-up resistance	$R_{UP}$	(15)	7	10	13	$\text{k}\Omega$

The applicable pin groups are listed on the following page.

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**Applicable Pins****[INPUT]**

- (0) . . . . .  $\overline{CS}$ ,  $\overline{RD}$ ,  $\overline{WR}$ , WRITE, SUA0 to SUA7,  $\overline{RESET}$ , WOBBLE,  $\overline{CS1FX}$ ,  $\overline{CS3FX}$ ,  $\overline{DIOR}$ ,  $\overline{DIOW}$ ,  $\overline{HRST}$
- (9) . . . . .  $\overline{DMACK}$
- (1) . . . . . TEST0 to TEST4
- (10) . . . . . FG
- (11) . . . . . AD0, AD1, RREC, FE, TE, VREF, AD2, TES

**[OUTPUT]**

- (2) . . . . . PDS1 to PDS3, DSLB
- (3) . . . . . RA0 to RA9,  $\overline{CAS0}$  and  $\overline{CAS1}$ ,  $\overline{RAS0}$  to  $\overline{RAS2}$ ,  $\overline{LWE}$ ,  $\overline{UWE}$ ,  $\overline{OE}$ , SSP2/1, RAPC, WAPC, H11T0, LDH, ATEST3/1, WDAT, NWDAT, EFMG, SHOCK, LOCK, EFMO, ATIPSYNC, ACRCNG, PCK2
- (6) . . . . . LDON
- (12) . . . . . INTRQ,  $\overline{IOCS16}$
- (13) . . . . . IORDY
- (15) . . . . . DMARQ

**[INOUT]**

- (4) . . . . . D0 to D7, IO0 to IO15
- (5) . . . . .  $\overline{INT0}$  and  $\overline{INT1}$ ,  $\overline{SWAIT}$
- (7) . . . . . DD0 to DD15
- (8) . . . . . BIDATA, BICLK
- (14) . . . . . DASP,  $\overline{PDIAG}$

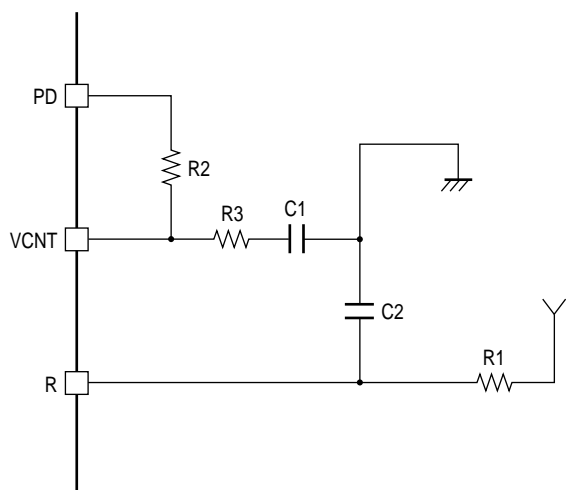
Note: The XTAL0 pin is not specified in the DC characteristics.

The pull-up and pull-down resistors on pins (9), (13), (14), and (15) are disabled after a reset.

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## External Circuit for the PLL Circuit

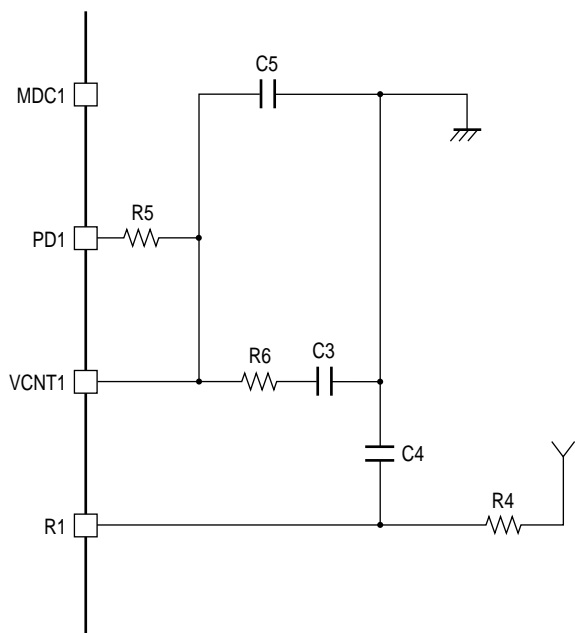
## 1. Internal Reference Clock Oscillator Block



Symbol	Value (typ)	Unit
R1	5.6 k	$\Omega$
R2	10 k	$\Omega$
R3	200	$\Omega$
C1	0.1 $\mu$	F
C2	0.1 $\mu$	F

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## 2. Write Strategy Block



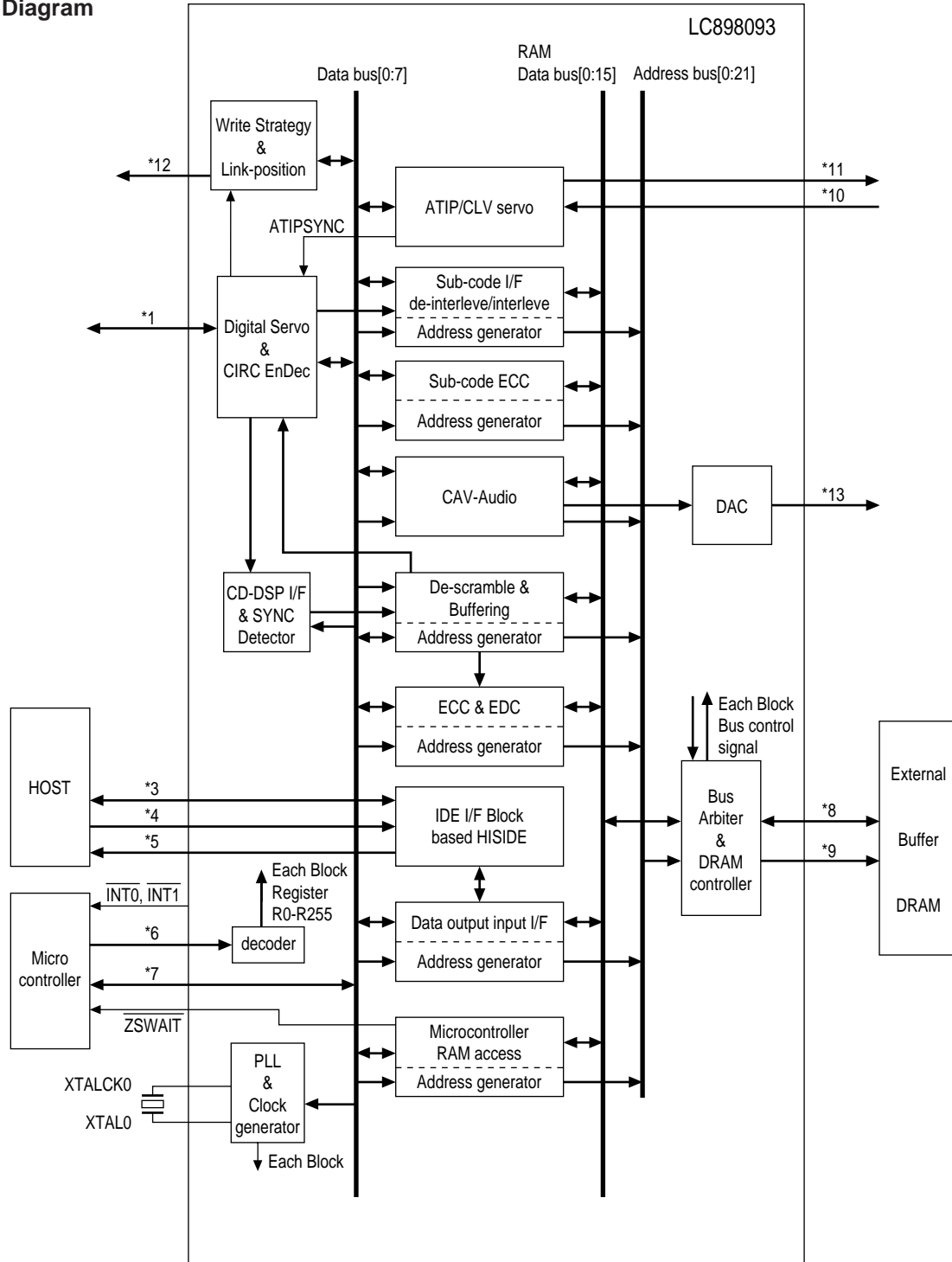
Symbol	Value (typ)	Unit
R4	5.6 k	$\Omega$
R5	15 k	$\Omega$
R6	220	$\Omega$
C3	0.1 $\mu$	F
C4	0.1 $\mu$	F
C5	0.1 $\mu$	F

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The analog  $V_{DD}$  and  $V_{SS}$  pins (pins 52, 53, 90, and 91) must be completely isolated from the logic system power supply and must not be influenced by fluctuations in the logic system power supply.

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Block Diagram



\*1 DSLB (pin96) to SUBSYNC (pin145), SHOCK (pin147) to PCK2 (pin155)

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\*3 DD0 to DD15,  $\overline{\text{DASP}}$ ,  $\overline{\text{PDIAG}}$

\*4  $\overline{\text{CS1FX}}$ ,  $\overline{\text{CS3FX}}$ , DA0 to DA2,  $\overline{\text{DIOR}}$ ,  $\overline{\text{DIOW}}$ ,  $\overline{\text{DMACK}}$

\*5  $\overline{\text{DMARQ}}$ ,  $\overline{\text{HINTRQ}}$ ,  $\overline{\text{IOCS16}}$ ,  $\overline{\text{IORDY}}$

\*6  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ , SUA0 to SUA7,  $\overline{\text{CS}}$

\*7 D0 to D7

\*8 IO0 to IO15

\*9 RA0 to RA9,  $\overline{\text{RAS0}}$ ,  $\overline{\text{RAS1}}$ ,  $\overline{\text{RAS2}}$ ,  $\overline{\text{CAS0}}$ ,  $\overline{\text{CAS1}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{UWE}}$ ,  $\overline{\text{LWE}}$

\*10 WOBBLE

\*11 ATIPSYNC, BIDATA, BICLK

\*12 WRITE, SSP2/1, RAPC, WAPC, H11T0, LDH, ATEST3, ATEST1, WDAT, NWDAT, EFMG

\*13 LOUT, ROUT

\*\*1 HISIDE (WD25C32) is made by WESTERN DIGITAL.

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## Pin Functions

Pin type					
I	Input	B	Bidirectional pin	NC	Not connected
O	Output	P	Power supply	A	Analog pin

Pin No.	Pin name	Type	Pin function
1	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
2	RA4	O	CD-ROM encoder/decoder DRAM address lines
3	RA5	O	
4	RA6	O	
5	RA7	O	
6	RA8	O	
7	RA9	O	
8	V <sub>DD</sub>	P	Digital system power supply (5 V)
9	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
10	IO0	B	CD-ROM encoder/decoder buffer RAM data lines These pins have built-in pull-up resistors.
11	IO1	B	
12	IO2	B	
13	IO3	B	
14	IO4	B	
15	IO5	B	
16	V <sub>DD</sub>	P	Digital system power supply (3.3 V)
17	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
18	IO6	B	CD-ROM encoder/decoder buffer RAM data lines These pins have built-in pull-up resistors.
19	IO7	B	
20	IO8	B	
21	IO9	B	
22	IO10	B	
23	V <sub>SS</sub>	P	
24	V <sub>DD</sub>	P	Digital system power supply (5 V)
25	IO11	B	CD-ROM encoder/decoder buffer RAM data lines These pins have built-in pull-up resistors.
26	IO12	B	
27	IO13	B	
28	IO14	B	
29	IO15	B	
30	ATIPSYNC	O	ATIP SYNC detection signal
31	BIDATA	B	ATIP demodulator signals
32	BICLK	B	
33	WOBBLE	I	
34	V <sub>DD</sub>	P	Digital system power supply (5 V)
35	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
36	ACRCNG	O	ATIP CRC result output signal
37	WRITE	I	Write strategy signal control input
38	SSP2	O	Servo sampling pulse output
39	SSP1	O	Servo sampling pulse output
40	RAPC	O	Laser control sampling pulse output
41	WAPC	O	Laser control sampling pulse output
42	H11T0	O	Running OPC sampling pulse

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Pin No.	Pin name	Type	Pin function
43	LDH	O	Recording laser diode control signal output
44	V <sub>DD</sub>	P	Analog system power supply (3.3 V)
45	V <sub>SS</sub>	P	Analog system ground (V <sub>SS</sub> )
46	ATEST3	O	RW output
47	ATEST1	O	Internal monitor test output
48	WDAT	O	Recording laser diode control signal output
49	NWDAT	O	Recording laser diode control signal output (WDAT inverted)
50	V <sub>DD</sub>	P	Analog system power supply (3.3 V)
51	V <sub>SS</sub>	P	Analog system ground (V <sub>SS</sub> )
52	V <sub>DD</sub>	P	Digital system power supply (5 V)
53	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
54	R1	I	Write strategy analog signals
55	VCNT1	I	
56	MDC1	O	
57	PD1	O	
58	$\overline{\text{SWAIT}}$	O	Wait signal to the microcontroller
59	$\overline{\text{INT0}}$	O	Interrupt request signal outputs to the microcontroller
60	$\overline{\text{INT1}}$	O	These are open-drain outputs with built-in pull-up resistors.
61	D0	B	Microcontroller data signal lines These pins have built-in pull-up resistors.
62	D1	B	
63	D2	B	
64	D3	B	
65	D4	B	
66	D5	B	
67	D6	B	
68	V <sub>DD</sub>	P	Digital system power supply (5 V)
69	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
70	D7	B	Microcontroller data signal line
71	SUA0	I	Command register selection address
72	SUA1	I	
73	SUA2	I	
74	SUA3	I	
75	SUA4	I	
76	SUA5	I	
77	SUA6	I	
78	SUA7	I	
79	$\overline{\text{CS}}$	I	Chip select signal input from the microcontroller
80	$\overline{\text{RD}}$	I	Data read signal input from the microcontroller
81	$\overline{\text{WR}}$	I	Data write signal input from the microcontroller
82	TEST0	I	Test pin. This pin must be tied to V <sub>SS</sub> .
83	VCNT	I	VCO control voltage
84	R	I	VCO bias resistor connection
85	PD	O	Charge pump output
86	V <sub>DD</sub>	P	Analog system power supply (3.3 V)
87	V <sub>SS</sub>	P	Analog system ground (V <sub>SS</sub> )
88	TEST1	I	Test pin. This pin must be tied to V <sub>SS</sub> .
89	$\overline{\text{RESET}}$	I	Reset input
90	XTALCK0	I	Crystal oscillator circuit input (33.8688 MHz)

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Pin No.	Pin name	Type	Pin function
91	XTAL0	O	Crystal oscillator circuit output
92	ROUT	O	D/A converter output
93	V <sub>SS</sub>	P	Analog system ground (V <sub>SS</sub> )
94	V <sub>DD</sub>	P	Analog system power supply (5 V)
95	LOUT	O	D/A converter output
96	DSL <sub>B</sub>	O	SLC PWM output
97	SLCIST1	I	EFM slice level setting input
98	SLCIST2	I	
99	V <sub>SS</sub>	P	Analog system ground (V <sub>SS</sub> )
100	V <sub>DD</sub>	P	Analog system power supply (3.3 V)
101	SLCO0	O	EFM slice level output
102	SLCO1	O	
103	SLCO2	O	
104	V <sub>DD</sub>	P	Digital system power supply (5 V)
105	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
106	SLCO3	O	EFM slice level output
107	EFMIN	I	EFM input
108	EFMIN2	I	
109	JITIN	I	Jitter discrimination input
110	JITC	O	Jitter output
111	RPO	O	P/N balance adjustment
112	OPP	I	
113	PCKISTF	I	Frequency comparator charge pump
114	PCKISTP	I	Phase comparator charge pump
115	V <sub>SS</sub>	P	Analog system ground (V <sub>SS</sub> )
116	V <sub>DD</sub>	P	Analog system power supply (3.3 V)
117	PDO	O	Charge pump filter
118	PDS1	O	Charge pump selection
119	PDS2	O	
120	V <sub>DD</sub>	P	Digital system power supply (3.3 V)
121	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
122	PDS3	O	Charge pump selection
123	FR	I	VCO frequency setting
124	TEST2	I	Test pin. This pin must be tied to V <sub>SS</sub> .
125	TEST3	I	Test pin. This pin must be tied to V <sub>SS</sub> .
126	TEST4	I	Test pin. This pin must be tied to V <sub>SS</sub> .
127	AD0	I	AD input
128	RREC	I	Optical signal discrimination input
129	FE	I	FE input
130	TE	I	TE input
131	VREF	I	VREF input
132	AD1	I	AD input
133	V <sub>SS</sub>	P	Analog system ground (V <sub>SS</sub> )
134	DA0	O	DA output
135	DA1	O	DA output
136	DA2	O	DA output
137	TDO	O	Tracking output

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Pin No.	Pin name	Type	Pin function
138	V <sub>DD</sub>	P	Analog system power supply (5 V)
139	V <sub>SS</sub>	P	Analog system ground (V <sub>SS</sub> )
140	FDO	O	Focus output
141	SLDO	O	Sled output
142	SPDO	O	Spindle output
143	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
144	V <sub>DD</sub>	P	Digital system power supply (3.3 V)
145	SUBSYNC	O	Subcode SYNC signal
146	EFMG	O	Write gate signal
147	SHOCK	O	Shock detection signal
148	LOCK	O	PLL lock state output
149	DEF	I	Defect detection signal input
150	HFL	I	Mirror detection signal input
151	TES	I	Tracking zero cross signal input
152	EFMO	O	Post-binarization EFM signal output
153	LDON	O	Laser control
154	FG	I	FG input
155	PCK2	O	PCK output
156	V <sub>DD</sub>	P	Digital system power supply (5 V)
157	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
158	HRST	I	IDE interface signals
159	DASP	B	
160	CS3FX	I	
161	CS1FX	I	
162	DA2	I	
163	DA0	I	
164	PDIAG	B	
165	DAI	I	
166	IOCS16	O	
167	INTRQ	O	
168	DMACK	I	
169	IORDY	O	
170	DIOR	I	
171	DIOW	I	
172	V <sub>DD</sub>	P	Digital system power supply (5 V)
173	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
174	DMARQ	O	IDE interface signals
175	DD15	B	
176	DD0	B	
177	DD14	B	
178	DD1	B	
179	DD13	B	
180	DD2	B	
181	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
182	DD12	B	IDE interface signals
183	DD3	B	
184	DD11	B	

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Pin No.	Pin name	Type	Pin function
185	DD4	B	IDE interface signals
186	DD10	B	
187	DD5	B	
188	DD9	B	
189	DD6	B	
190	V <sub>DD</sub>	P	Digital system power supply (3.3 V)
191	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
192	DD8	B	IDE interface signals
193	DD7	B	
194	RAS <sub>0</sub>	O	DRAM RAS signal outputs
195	RAS <sub>1</sub>	O	
196	RAS <sub>2</sub>	O	
197	LWE	O	DRAM lower write enable
198	V <sub>DD</sub>	P	Digital system power supply (5 V)
199	V <sub>SS</sub>	P	Digital system ground (V <sub>SS</sub> )
200	UWE	O	DRAM upper write enable
201	CAS <sub>0</sub>	O	DRAM CAS signal output
202	CAS <sub>1</sub>	O	
203	OE	O	DRAM output enable
204	RA0	O	CD-ROM encoder/decoder DRAM address lines
205	RA1	O	
206	RA2	O	
207	RA3	O	
208	V <sub>DD</sub>	P	Digital system power supply (5 V)

**Pin Functions**

&lt;ATAPI Pins&gt;

**CS1FX** (input)

Chip select signal that selects the command block register.

**CS3FX** (input)

Chip select signal that selects the control block register.

**DA0 to DA2** (input)

Address for accessing the ATAPI interface registers.

**DASP** (input/output)

Drive 1 is output and drive 0 is input.

Signal used to indicate to drive 0 that drive 1 exists.

**DD0 to DD15** (input/output)

16-bit data bus. This interface supports both 8-bit and 16-bit transfers.

**DIOR** (input)

Read strobe from the host.

**DIOW** (input)

Write strobe from the host.

**DMACK** (input)

Acknowledge signal from the host used during DMA transfers. Corresponds to the DMARQ request signal from the drive.

**DMARQ** (input)

Drive request signal used during DMA transfers.

**HINTRQ** (output)

Drive interrupt request signal to the host.

**IOCS16** (output)

Signal asserted by the drive when the drive supports 16-bit transfers.

This signal is not asserted during DMA transfers.

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**IRDY** (output)

Indicates that the drive is ready to respond. Used during data transfers.

This signal will be low when the drive is not ready.

**PDIAG** (input/output)

Signal asserted by drive 1 to indicate to drive 0 that diagnostics have completed.

**HRST** (input)

Reset signal from the host. The IDE interface is reset by a low-level input to this pin.

## &lt;Microcontroller Interface Pins&gt;

**CS** (input)

Chip select signal from the microcontroller. The microcontroller interface is active when this pin is low.

**RD, WR** (input)

Connect the microcontroller read and write lines to these inputs.

**SWAIT** (input)

Wait signal output to the microcontroller. When accessing buffer RAM, the microcontroller must wait if this pin is low.

**SUA0 to SUA7** (input)

Internal register address lines

**D0 to D7** (input/output)

Microcontroller data bus. These pins have built-in pull-up resistors.

**INT0, INT1** (output)

Interrupt request signals output to the microcontroller.  $\overline{\text{INT1}}$  can be set to output the ATAPI interrupt by setting INT1EN (Conf-R11 bit 7)

These are open drain outputs with built-in 80 k $\Omega$  (at room temperature, 5 V) pull-up resistors.

## &lt;Buffer RAM Pins&gt;

**I/O0 to I/O15** (input/output)

Buffer RAM data bus. These pins have built-in pull-up resistors.

**RA0 to RA9** (output)

Buffer RAM address lines.

**RAS0, RAS1, RAS2** (output)

Buffer DRAM RAS outputs. Normally,  $\overline{\text{RAS0}}$  is used. However, if two 16-Mbit DRAMs are used, connect the  $\overline{\text{RAS0}}$  and  $\overline{\text{RAS1}}$  lines to the RAS pins on the DRAMs. If four 16-Mbit DRAMs are used, connect the  $\overline{\text{RAS0}}$ ,  $\overline{\text{RAS1}}$ ,  $\overline{\text{RAS2}}$ , and  $\overline{\text{LWE}}$  lines to the RAS pins on the DRAMs.

**CAS0, CAS1** (output)

Buffer DRAM CAS outputs. Normally,  $\overline{\text{CAS0}}$  is used. However, if two 16-Mbit DRAMs are used, connect the  $\overline{\text{CAS0}}$  output to the CAS pins on the DRAMs. If 2-CAS type DRAMs are used, connect  $\overline{\text{CAS0}}$  to UCAS and  $\overline{\text{CAS1}}$  to LCAS.

**OE** (output)

Buffer RAM read output.

**UWE, LWE** (output)

Buffer RAM write outputs. Connect these to the corresponding pins. If 2-CAS type DRAMs are used, UWE must be connected. (Leave LWE open.)

## 1. Analog Interface Pins

**RREC** (input)

Optical discrimination input.

**FE** (input)

Focus error signal input.

**TE** (input)

Tracking error signal input.

**VREF** (input)

Input for the servo system reference voltage.

**AD0, AD1** (input)

A/D converter auxiliary inputs.

**DA0, DA1, DA2** (input)

D/A converter auxiliary inputs.

**TES** (input)

TES comparator input.

**TDO** (output)

Tracking control signal output.

**FDO** (output)

Focus control signal output.

**SLDO** (output)

Sled control signal output.

**SPDO** (output)

Spindle control signal output.

## 2. EFM Input Block Pins

**EFMIN** (input)

EFM signal input.

The high-frequency components of the RF signal acquired from the RF amplifier are cut with a capacitor, and this pin inputs that signal biased by the value of the SLCO0 to SLCO3 outputs passed through a low-pass filter.

**EFMIN2** (input)

Used to change the time constant of the low-pass filter.

**SLCIST1, SLCIST2** (input)

Slice level controller charge pump bias resistor connection.

**SLCO0, SLCO1, SLCO2, SLCO3** (output)

Slice level controller charge pump outputs.

These levels bias the RF signal input to the EFMIN pin after being passed through a low-pass filter.

**DSL B** (output)

Slice level control PWM output.

**EFMO** (output)

Post-binarization EFM signal output. (For monitoring)

## 3. EFM Clock Generation Block Pins

**FR** (input)

EFM reproduction PLL VCO bias resistor connection.

**PDO, PDS1, PDS2, PDS3** (output)

EFM reproduction PLL lag-lead filter connection.

**PCKISTF** (input)

EFM reproduction PLL frequency comparator charge pump bias resistor connection.

**PCKISTP** (input)

EFM reproduction PLL phase comparator charge pump bias resistor connection.

**RPO** (output)

P/N balance adjustment.

**OPP** (input)

P/N balance adjustment.

**PCK2** (output)

EFM reproduction bit clock output.

## 4. Jitter Discrimination Pins

**JITIN** (input)

Jitter discrimination input.

**JITC** (output)

Jitter output.

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**LC898093**


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## 5. Spindle Speed Detection Pins

**FG** (input)

Input for the speed monitor signal from the spindle driver.

## 6. Audio Interface Pins

**LOUT, ROUT** (output)

Left and right channel audio signal outputs.

## 7. RF Amplifier Interface Pins

**LDON** (output)

RF amplifier interface.

## 8. Write Strategy Pins

**WRITE, SSP2/1, RAPC, WAPC, H11T0, LDH, ATEST3, 1, WDAT, NWDAT** (I/O)

Write strategy signal connections.

## 9. ATIP Decoder Related Pins

**ATIPSYNC** (output)

ATIP synchronization detection signal. (For monitoring)

**BIDATA, BICLK** (I/O)

Input mode: Input for the biphase data and biphase clock when an external ATIP demodulator is used.

Output mode: Output of the biphase data and biphase clock when the internal ATIP demodulator is used. (For monitoring)

**WOBBLE** (input)

Wobble signal input when the internal ATIP demodulator is used.

**ACRCNG** (output)

Outputs the result of the ATIP decoder CRC check. (For monitoring)

## &lt;Other Pins&gt;

**RESET** (input)

The LC898093 reset input. A low level input resets the LC898093.

This pin must be held low for at least 1  $\mu$ s when power is first applied.

**TEST4 to TEST0** (input)

Test inputs. These pins must be connected to ground.

**XTALCKO** (input), **XTALO** (output)

Drive these pins at 33.8688 MHz. This signal is used, without modification, as main clock for the CD-ROM encoder and decoder blocks, including the DRAM interface.

Consult the manufacturer of the oscillator element concerning the design of the oscillator circuit.

**R, VCNT, PDO, R1, VCNT1, PD1, MDC1** (I/O)

Clock reproduction PLL circuit pins.

**SUBSYNC** (output)

Subcode SYNC output signal from the CIRC encoder during encoding. (For monitoring)

**EFMG** (output)

Outputs a high-level signal (5 V) during write operations.

**SHOCK** (output)

Outputs a high level (5 V) when a mechanical shock is detected during decoding.

**LOCK** (output)

Outputs a high level (5 V) when the PLL circuit is locked.

**DEF** (input)

Inputs the defect detection signal.

**HFL** (input)

Inputs the mirror detection signal.

This datasheet has been download from:

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

Datasheets for electronics components.