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LC898212XA

CMOS LSI

AF Control LSI

Overview

The AF control device, LC898212XA (LC898212XA-MH), provides an ideal way to implement the reduced power consumption and the improved autofocus precision and speed (reduced convergence time) required in high-pixel-count camera modules for use in smartphones.

The LC898212XA integrates on a single chip an equalizer circuit employing digital calculation, and it can be combined with position sensors to build a closed-loop actuator control system. Since closed-loop control provides better ability to maintain the control object than conventional open-loop systems and is not affected by position differences, the LC898212XA is ideal for use in AF systems used in a wide variety of cameras. A closed-loop system uses position sensors for position control, and power consumption is lower than with conventional open-loop control, which uses current values for position control.

In addition, a new PWM drive system employed suppresses noise that could affect image quality while achieving reduced power consumption, making this IC ideal for use in mobile devices such as smartphones. The filter coefficients of the equalizer circuit can be adjusted to any values desired by making register settings via I²C communication. This makes it possible to build a control circuit optimized to the various types of actuators and thereby achieve faster autofocus (reduced convergence time) performance.

The integrated ADC provides up to 10-bit precision for highly accurate AF position control. Also integrated on-chip are a constant current supply DAC for drive and an op-amp with adjustable gain for use with the position sensors indispensable for building a closed-loop control system.

* I²C Bus is a trademark of Philips Corporation.

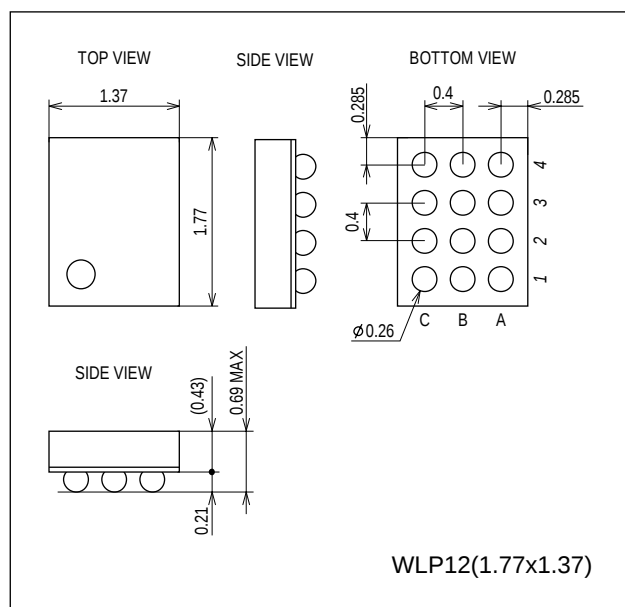
Features

- Built-in equalizer circuit using digital operation
 - AF control equalize circuit
 - Any coefficient can be specified by I²C I/F
- I²C Interface
- Built-in A/D converter
 - Maximum 10-bit
 - Input 2 channel
- Built-in D/A converter
 - 8-bit
 - Output 2-channel (Hall offset, Constant current Bias)
- Built-in OP Amp
 - 1 channel
 - Hall Amp
- Built-in OSC
 - 48MHz (Frequency adjustment function)
- Built-in PWM pulse generator circuit
 - PWM circuit for AF control
- 1-chip motor driver
 - Saturation drive H bridge 1 channel
- Package
 - WL-CSP 12-pin
 - Lead-free, halogen-free
- Supply voltage
 - Logic unit: Internal core typ 1.2V (1.08V to 1.32V), AV_{DD} (2.6V to 3.6V)
 - Driver unit: VM (2.6V to 3.6V)

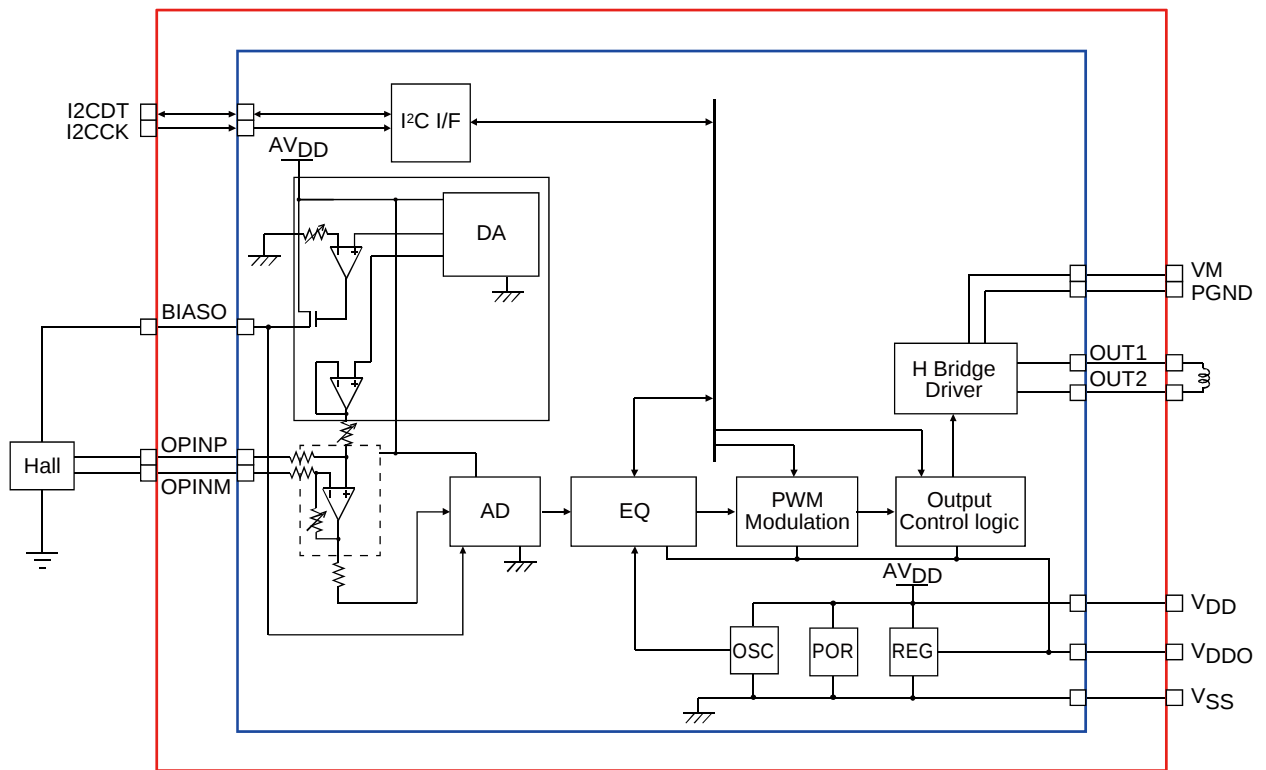
Package Dimensions

unit : mm (typ)

3440



Block Diagram



LC898212XA

Pin Description

TYPE					
I	INPUT	P	Power supply, GND	NC	NOT CONNECT
O	OUTPUT				
B	BIDIRECTION				

I²C interface

I2CCK	B	I ² C Clock pin
I2CDT	B	I ² C Data pin

D/A interface

BIASO	O	D/A output (Hall bias input)
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Op-Amp interface

OPINP	I	Op-Amp input
OPINM	I	Op-Amp input

Driver interface

OUT1	O	Actuator output pin
OUT2	O	Actuator output pin

Power supply pin

V _{DD}	P	Digital power supply
V _{SS}	P	Digital GND
V _{DDO}	P	LDO power supply out
VM	P	Motor power supply
PGND	P	Power GND

PIN TYPE “O” – Ensure that it is set to OPEN.

PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the V_{DD} or V_{SS} even when it is unused.

(Please contact Our company for more information about selection of V_{DD} or V_{SS}.)

PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

If you have any question, please feel free to contact us.

Pin Layout

Circuit Name	Number of Pins	Circuit Name	Number of Pins
Analog	4	Driver	4
Logic	4		

Backside pin layout diagram (Top View from the mold side)

4	V _{DDO}	VM	PGND
3	AV _{DD}	I2CDT	OUT1
2	OPINP	I2CCK	OUT2
1	V _{SS}	OPINM	BIASO
	A	B	C

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