

# LC898214XD

CMOS LSI

## AF Controller



**ON Semiconductor®**

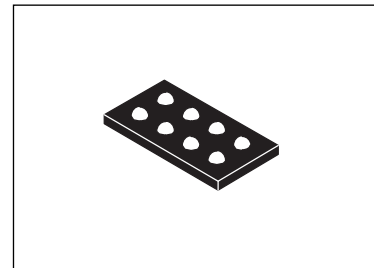
[www.onsemi.com](http://www.onsemi.com)

### Overview

This LSI is AF control LSI. It consists of 1 system of feedback circuit for AF control.

### Features

- Built-in equalizer circuit using digital operation
  - AF control equalize circuit
  - Any coefficient can be specified by I<sup>2</sup>C I/F
- I<sup>2</sup>C Interface
- Built-in A/D converter
  - Maximum 10-bit
  - Input 2 channel
- Built-in D/A converter
  - 8-bit
  - Output 2-channel (Hall offset, Constant current Bias)
- Built-in Hall Sensor
  - Si Hall sensor
- Built-in EEPROM
  - 128 byte (8 byte/page)
- Built-in VGA
  - Hall Amp
- Built-in OSC
  - 48MHz
- Built-in Constant Current Driver
- Package
  - WL-CSP 8-pin
  - Pb-Free, Halogen Free
- Supply voltage
  - V<sub>DD</sub> (2.6V to 3.6V)



WLCSP8, 1.15x2.37, 0.5P

\* I<sup>2</sup>C Bus is a trademark of Philips Corporation.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

## Pin Description

| TYPE |             |   |                      |    |             |
|------|-------------|---|----------------------|----|-------------|
| I    | INPUT       | P | Power supply,<br>GND | NC | NOT CONNECT |
| O    | OUTPUT      |   |                      |    |             |
| B    | BIDIRECTION |   |                      |    |             |

### ■ I<sup>2</sup>C interface

|       |   |                            |
|-------|---|----------------------------|
| I2CCK | B | I <sup>2</sup> C Clock pin |
| I2CDT | B | I <sup>2</sup> C Data pin  |

### ■ Hall interface

|      |   |                 |
|------|---|-----------------|
| HALL | O | Hall amp output |
|------|---|-----------------|

### ■ Driver interface

|      |   |                     |
|------|---|---------------------|
| OUT1 | O | Actuator output pin |
| OUT2 | O | Actuator output pin |

### ■ Power supply pin

|     |   |              |
|-----|---|--------------|
| VDD | P | Power supply |
| VSS | P | GND          |

### ■ Test pin

|      |   |          |
|------|---|----------|
| TEST | O | Test pin |
|------|---|----------|

### \*Process when pins are not used

PIN TYPE “O” – Ensure that it is set to OPEN.

PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the VDD or VSS even when it is unused.

(Please contact ON Semiconductor for more information about selection of VDD or VSS.)

PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

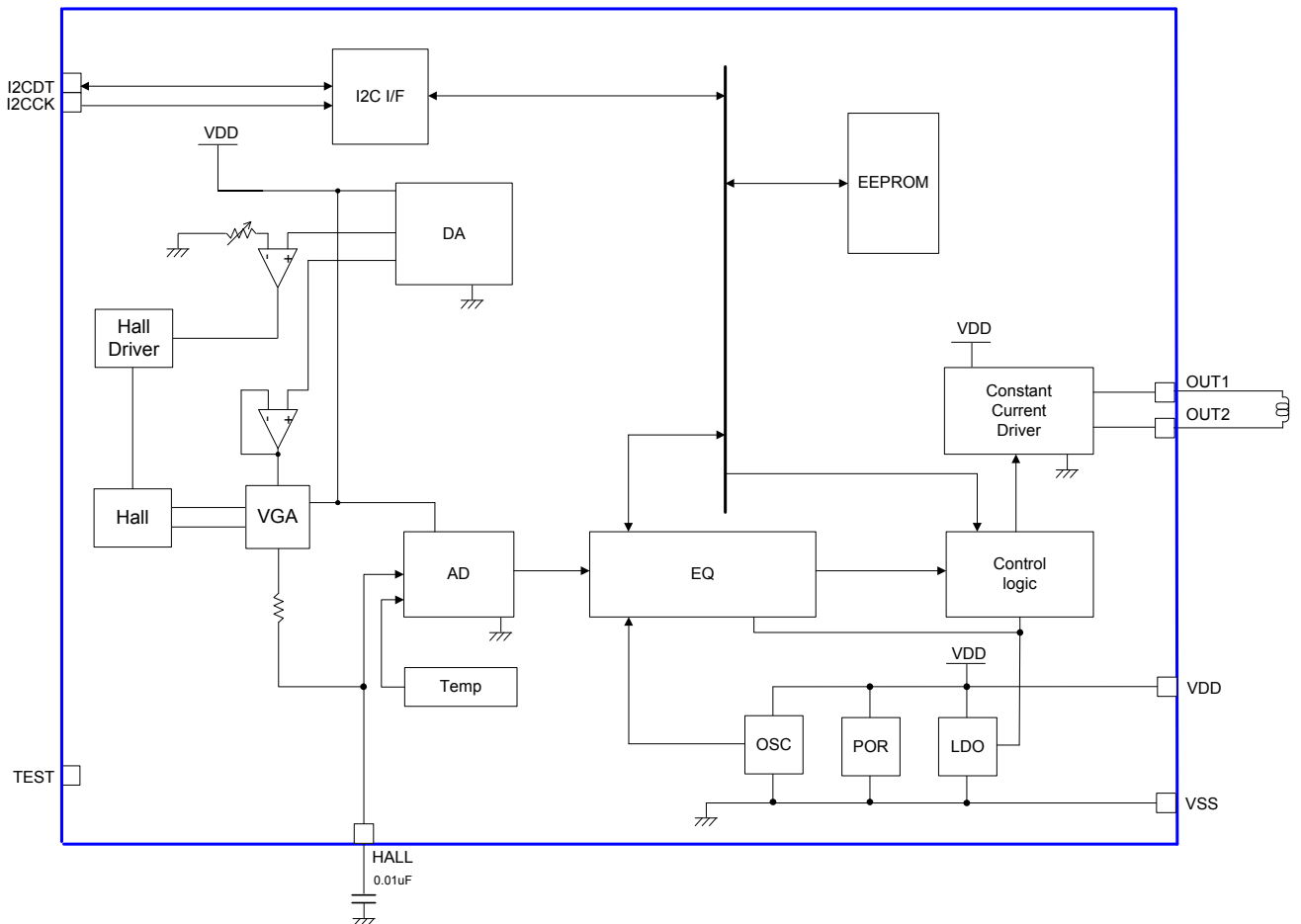
## Pin Layout

| Circuit Name | Number of Pins | Circuit Name | Number of Pins |
|--------------|----------------|--------------|----------------|
| Analog       | 4              | Driver       | 2              |
| Logic        | 2              |              |                |

Backside pin layout diagram (Top View from the mold side)

|   |       |       |
|---|-------|-------|
| 4 | TEST  | HALL  |
| 3 | I2CDT | I2CCK |
| 2 | VSS   | VDD   |
| 1 | OUT2  | OUT1  |
|   | A     | B     |

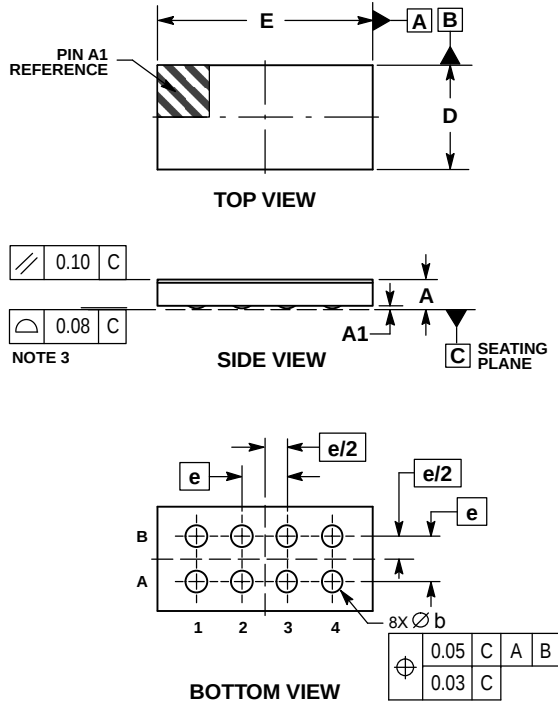
## Block Diagram



## Package Dimensions

unit : mm

**WLCSP8, 1.15x2.37, 0.5P**  
**CASE 567KL**  
**ISSUE A**

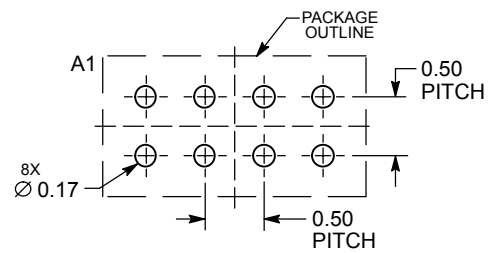


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF SOLDER BALLS.

| MILLIMETERS |          |      |
|-------------|----------|------|
| DIM         | MIN      | MAX  |
| A           | 0.27     | 0.33 |
| A1          | 0.04 REF |      |
| b           | 0.12     | 0.22 |
| D           | 1.12     | 1.18 |
| E           | 2.34     | 2.40 |
| e           | 0.50 BSC |      |

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## Electrical Characteristics

### 1) Absolute maximum rating at $V_{SS} = 0V$

| Item                          | Symbol             | Condition             | Rating                 | Unit       |
|-------------------------------|--------------------|-----------------------|------------------------|------------|
| Supply voltage                | $V_{DD33\max}$     | $T_a \leq 25^\circ C$ | -0.3 to 4.6            | V          |
| Input/output voltage          | $V_{I33}, V_{O33}$ | $T_a \leq 25^\circ C$ | -0.3 to $V_{DD33}+0.3$ | V          |
| Storage ambient temperature   | $T_{stg}$          |                       | -55 to 125             | $^\circ C$ |
| Operating ambient temperature | $T_{opr}$          |                       | -30 to 70              | $^\circ C$ |
| Continuous output current     | $I_{omax}$         | OUT1, OUT2            | 150                    | mA         |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### 2) Acceptable operation range at $T_a = -30$ to $70^\circ C$ , $V_{SS} = 0V$

3V power supply ( $V_{DD}$ )

| Item                | Symbol     | Min | Std | Max        | Unit |
|---------------------|------------|-----|-----|------------|------|
| Supply voltage      | $V_{DD33}$ | 2.6 | 2.8 | 3.6        | V    |
| Input voltage range | $V_{IN}$   | 0   | -   | $V_{DD33}$ | V    |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### 3) DC characteristics : Input/output level at $V_{SS} = 0V$ , $V_{DD} = 2.6V$ to $3.6V$ , $T_a = -30$ to $70^\circ C$

| Item                     | Symbol   | Condition                 | Min | Std | Max | Unit | Applicable pins |
|--------------------------|----------|---------------------------|-----|-----|-----|------|-----------------|
| High-level input voltage | $V_{IH}$ | CMOS compliant<br>Schmidt | 1.4 |     |     | V    | I2CCK, I2CDT,   |
| Low-level input voltage  | $V_{IL}$ |                           |     |     | 0.4 | V    |                 |
| Low-level output voltage | $V_{OL}$ | $I_{OL} = 2mA$            |     |     | 0.4 | V    | I2CDT           |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### 4) Driver output (OUT1, OUT2) at $V_{SS} = 0V$ , $V_{DD} = 2.8V$ , $T_a = 25^\circ C$

| Item                  | Symbol      | Condition         | Min | Std | Max | Unit     | Applicable pins |
|-----------------------|-------------|-------------------|-----|-----|-----|----------|-----------------|
| Maximum current       | $I_{full}$  |                   | 108 |     | 137 | mA       | OUT1, OUT2      |
| Output ON resistance  | $R_{onu}$   | $I_o = 120mA$ Pch |     | 2.8 |     | $\Omega$ |                 |
| Compliance voltage    | $V_{comp}$  |                   | 0.5 |     |     | V        |                 |
| Output leak current   | $I_{oleak}$ |                   |     | 1   |     | $\mu A$  |                 |
| Diode forward voltage | $V_D$       | $I_D = -120mA$    |     | 0.9 |     | V        |                 |

Actuator resistance ( $R_{act}$ ) =  $(V_M - (R_{onu} \cdot I_o + V_{comp})) / I_o$  [ $\Omega$ ]

### 5) Non-volatile Memory Characteristics

| Item           | Symbol | Condition | Min | Std | Max  | Unit   | Applicable pins |
|----------------|--------|-----------|-----|-----|------|--------|-----------------|
| Endurance      | EN     |           |     |     | 1000 | Cycles | E2PROM          |
| Data retention | RT     |           | 10  |     |      | Years  |                 |

## Hall element position

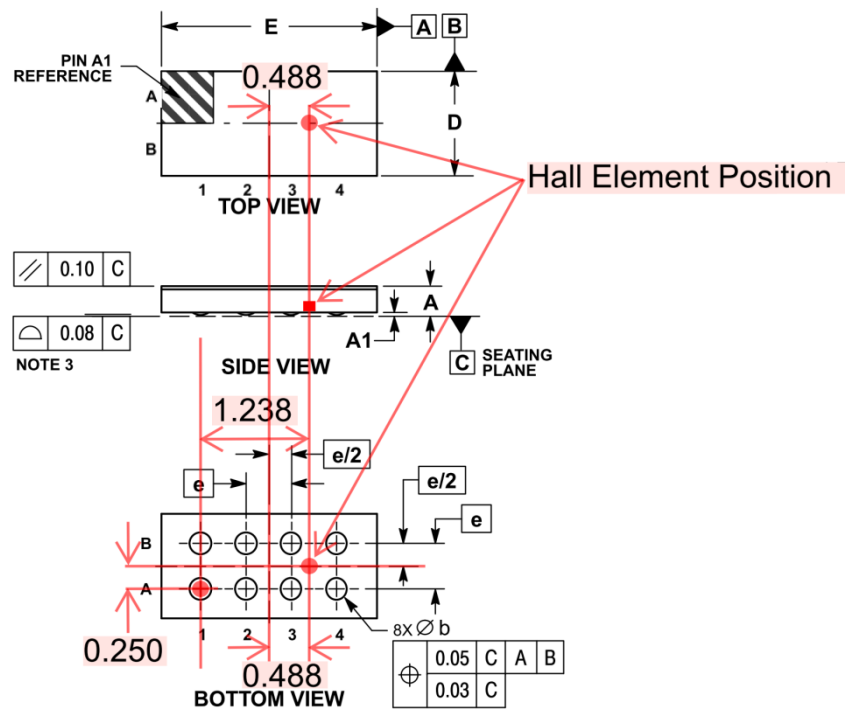


Figure 1 : Hall element position

Please refer to package diagram for each dimension.

## AC Characteristics

### V<sub>DD</sub> supply timing

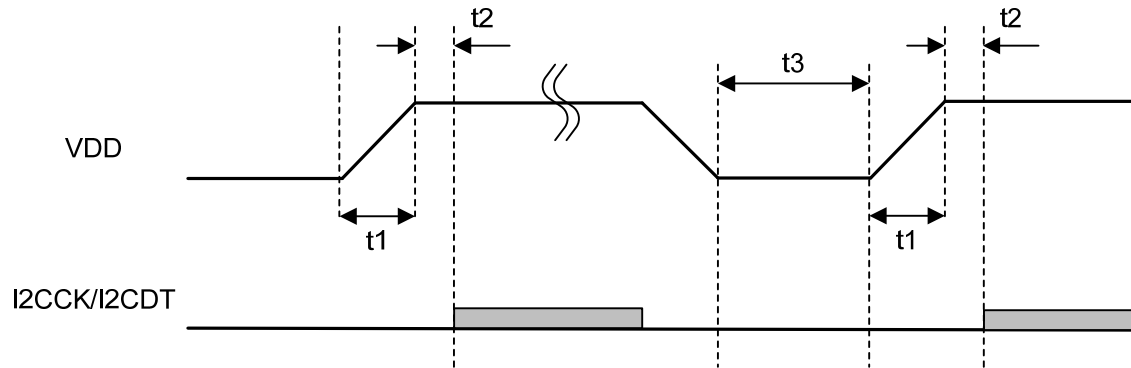


Figure 2 : V<sub>DD</sub> supply timing

It is available to use I<sup>2</sup>C 2ms later for Power On Reset of V<sub>DD</sub>.

| Item                                    | Symbol | Min | Typ | Max | Unit |
|-----------------------------------------|--------|-----|-----|-----|------|
| VDD turn on time                        | t1     |     |     | 3   | ms   |
| I <sup>2</sup> C start time from VDD on | t2     | 2   |     |     | ms   |
| VDD off time                            | t3     | 10  |     |     | ms   |

## AC specification

Figure 2 shows interface timing definition and Table 1 shows electric characteristics.

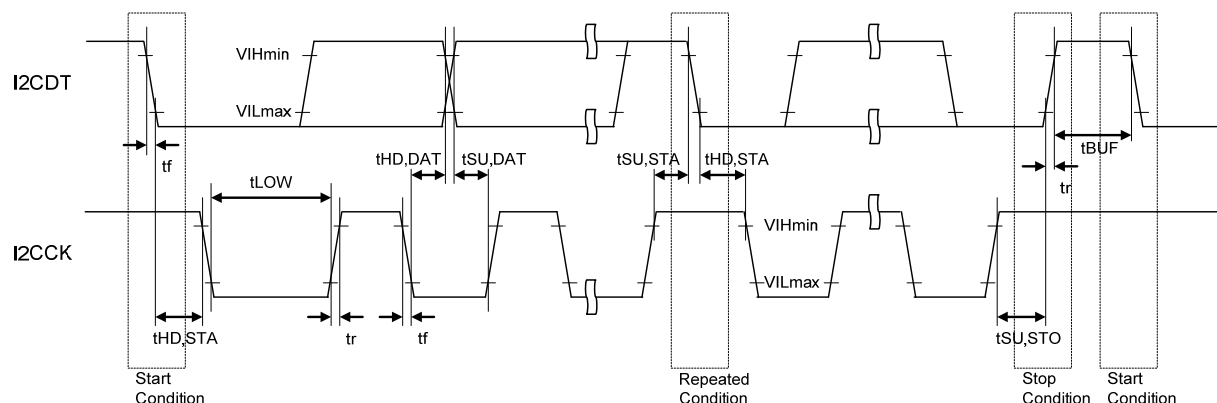


Figure 3 : I<sup>2</sup>C interface timing definition

Table 1 : Electric characteristics for I<sup>2</sup>C interface (AC characteristics)

| Item                                      | Symbol  | Pin name       | Min   | Typ | Max | Unit |
|-------------------------------------------|---------|----------------|-------|-----|-----|------|
| I2CCK clock frequency                     | Fi2cck  | I2CCK          |       |     | 400 | kHz  |
| START condition hold time                 | tHD,STA | I2CCK<br>I2CDT | 0.6   |     |     | μs   |
| I2CCK clock Low period                    | tLOW    | I2CCK          | 1.3   |     |     | μs   |
| I2CCK clock High period                   | tHIGH   | I2CCK          | 0.6   |     |     | μs   |
| Setup time for repetition START condition | tSU,STA | I2CCK<br>I2CDT | 0.6   |     |     | μs   |
| Data hold time                            | tHD,DAT | I2CCK<br>I2CDT | 0 (*) |     | 0.9 | μs   |
| Data setup time                           | tSU,DAT | I2CCK<br>I2CDT | 100   |     |     | ns   |
| I2CDT, I2CCK rising time                  | tr      | I2CCK<br>I2CDT |       |     | 300 | ns   |
| I2CDT, I2CCK falling time                 | tf      | I2CCK<br>I2CDT |       |     | 300 | ns   |
| STOP condition setup time                 | tSU,STO | I2CCK<br>I2CDT | 0.6   |     |     | μs   |
| Bus free time between STOP and START      | tBUF    | I2CCK<br>I2CDT | 1.3   |     |     | μs   |

\* : Although the I<sup>2</sup>C specification defines a condition that 300 ns of hold time is required internally, LC898214XD is designed for a condition with typ. 20 ns of hold time. If I2CDT signal is unstable around falling point of I2CCK signal, please implement an appropriate treatment on board, such as inserting a resistor.

**ORDERING INFORMATION**

| Device        | Package                                             | Shipping (Qty / Packing) |
|---------------|-----------------------------------------------------|--------------------------|
| LC898214XD-MH | WLCSP8, 1.15x2.37, 0.5P<br>(Pb-Free / Halogen Free) | 5000 / Tape & Reel       |

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