

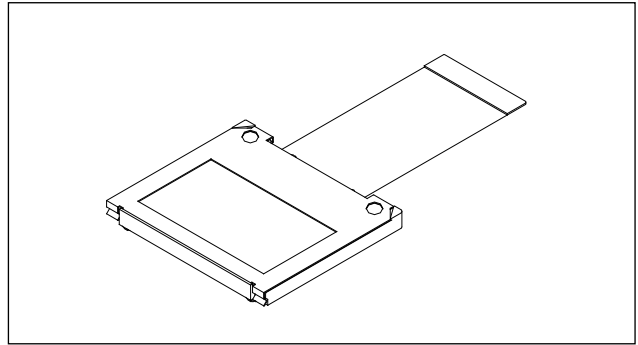
3.4cm (1.35-inch) Black-and-White LCD Panel

Description

The LCX007BNB is a 3.4cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with built-in peripheral driving circuit. This panel, with polarizers on the both faces, displays black-and-white images suitable to video-photographic printers and other applications.

This panel provides a wide aspect ratio of 16 : 9, such as those represented in HD. The built-in side-black function also allows an aspect ratio of 4 : 3 in the NTSC/PAL mode.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing system and control signals.



Features

- The number of active dots: 512,880 (1.35-inch; 3.4cm in diagonal)
- Horizontal resolution: 600 TV lines
- High optical transmittance: 16.5% (typ.)
- High contrast ratio with normally white mode: 190 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- NTSC/NTSC-WIDE/HD (band: 20MHz) mode selectable
(PAL/PAL-WIDE mode also available through conversion of scanned dot numbers by an external IC)
- Up/down and/or right/left inverse display function
- Side-black function
- 16 : 9 and 4 : 3 aspect-ratio switching function

Element Structure

- Dots

| | | |
|----------------|---|--------------------------------|
| 16 : 9 display | : | 1068.5 (H) × 480 (V) = 512,880 |
| 4 : 3 display | : | 799.5 (H) × 480 (V) = 383,760 |

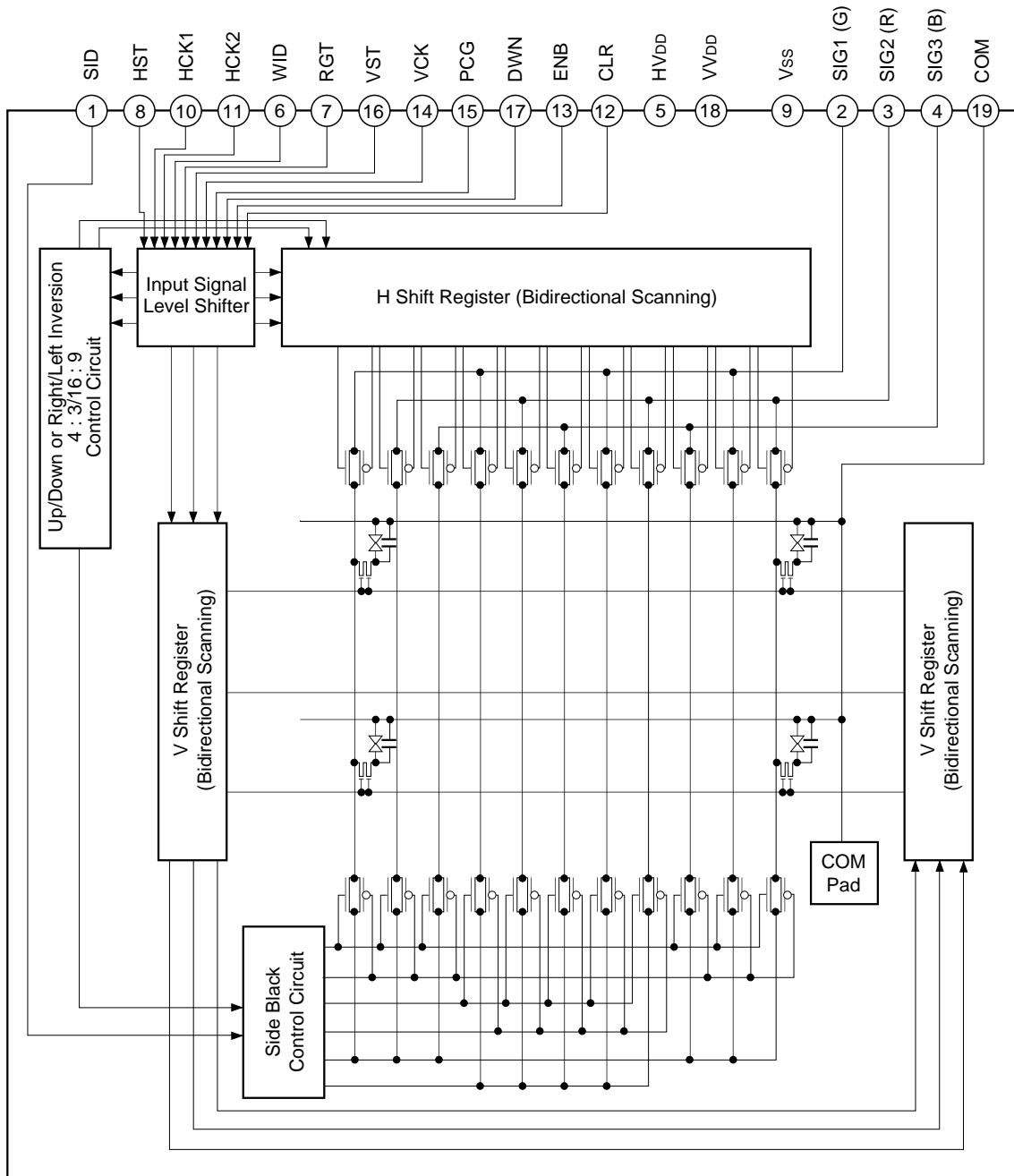
- Built-in peripheral driver using polycrystalline silicon super thin film transistors.

Applications

Video-photographic printers etc.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram



Absolute Maximum Ratings ($V_{SS} = 0V$)

| | | | |
|--------------------------------------|--------------------------------|-------------|----|
| • H driver supply voltage | HV _{DD} | -1.0 to +20 | V |
| • V driver supply voltage | VV _{DD} | -1.0 to +20 | V |
| • Common pad voltage | COM | -1.0 to +17 | V |
| • H shift register input pin voltage | HST, HCK1, HCK2 RGT, WID | -1.0 to +17 | V |
| • V shift register input pin voltage | VST, VCK, PCG CLR, ENB, DWN | -1.0 to +17 | V |
| • Video signal input pin voltage | SIG1, SIG2, SIG3, SID | -1.0 to +15 | V |
| • Operating temperature | Topr | -10 to +70 | °C |
| • Storage temperature | Tstg | -30 to +85 | °C |

Operating Conditions ($V_{SS} = 0V$)

Supply voltage

| | | |
|------------------|--------------------------------------|---|
| HV _{DD} | 15.7 ^{+0.3} _{-0.4} | V |
| VV _{DD} | 15.7 ^{+0.3} _{-0.4} | V |

Input pulse voltage (V_{p-p} of all input pins except video signal and side black signal input pins)

| | | |
|-----------------|-----------|---|
| V _{in} | 5.0 ± 0.5 | V |
|-----------------|-----------|---|

Pin Description

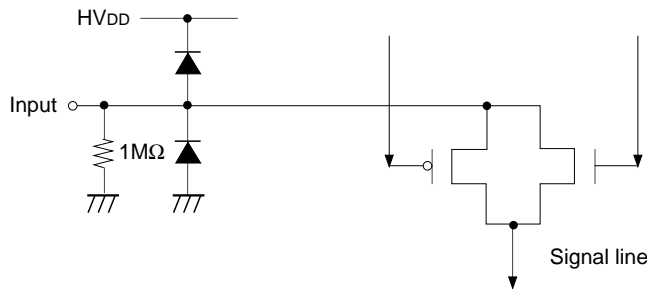
| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
|---------|------------------|--|---------|------------------|--|
| 1 | SID | Side black signal for 4:3 display | 11 | HCK2 | Clock pulse for H shift register drive |
| 2 | SIG1 (G) | Video signal (G* ¹) to panel | 12 | CLR | Improvement pulse (1) for uniformity |
| 3 | SIG2 (R) | Video signal (R* ¹) to panel | 13 | ENB | Enable pulse for gate selection |
| 4 | SIG3 (B) | Video signal (B* ¹) to panel | 14 | VCK | Clock pulse for V shift register drive |
| 5 | HV _{DD} | Power supply for H driver | 15 | PCG | Improvement pulse (2) for uniformity |
| 6 | WID | Aspect-ratio switching (H: 16:9, L: 4:3) | 16 | VST | Start pulse for V shift register drive |
| 7 | RGT | Drive direction pulse for H shift register (H: normal, L: reverse) | 17 | DWN | Drive direction pulse for V shift register (H: normal, L: reverse) |
| 8 | HST | Start pulse for H shift register drive | 18 | VV _{DD} | Power supply for V driver |
| 9 | V _{SS} | GND (H, V drivers) | 19 | COM | Common voltage of panel |
| 10 | HCK1 | Clock pulse for H shift register drive | 20 | TEST | Test; Open |

*1 (R), (G) and (B) are indicated for convenience to show the correspondence with the dot arrangement diagram.

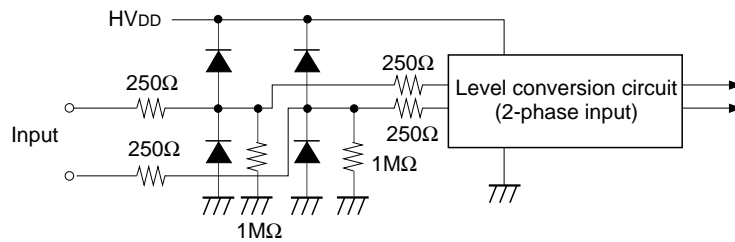
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supply. In addition, protective resistors are added to all pins except video signal input. All pins are connected to V_{SS} with a high resistance of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (The resistor value: typ.)

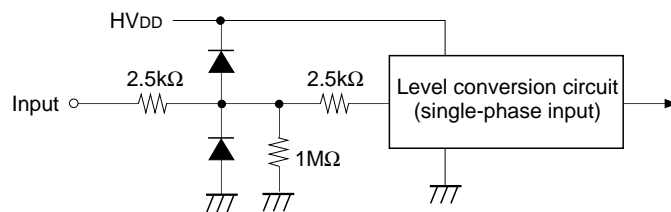
(1) SIG1, SIG2, SIG3, SID



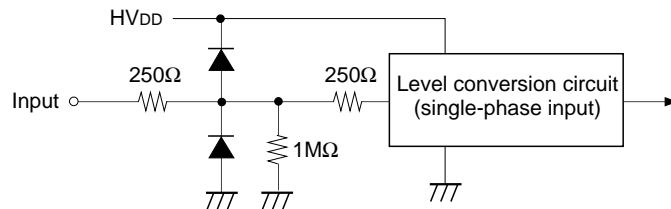
(2) HCK1, HCK2



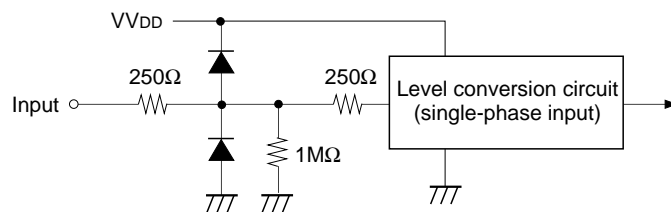
(3) RGT, WID



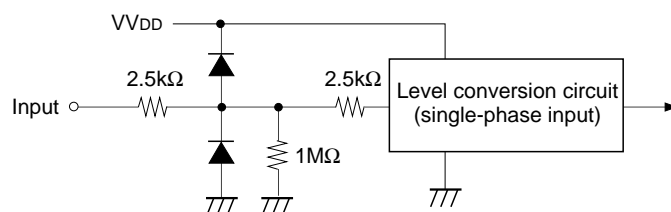
(4) HST



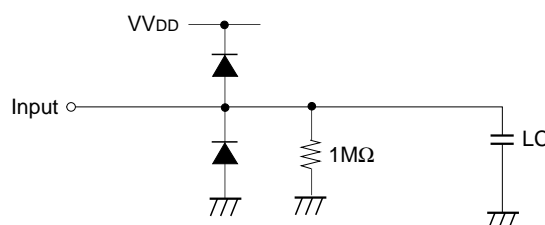
(5) PCG, VCK



(6) VST, CLR, ENB, DWN



(7) COM



Input Signals

1. Input signal voltage conditions ($V_{ss} = 0V$)

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|--|--------|--------|-------------|-------------|-------------|------|
| H driver input voltage WID, RGT, HST, HCK1, HCK2 | (Low) | VHIL | -0.5 | 0.0 | 0.3 | V |
| | (High) | VHIH | 4.5 | 5.0 | 5.5 | V |
| V driver input voltage CLR, ENB, VCK, PCG, VST, DWN | (Low) | VVIL | -0.5 | 0.0 | 0.3 | V |
| | (High) | VVIH | 4.5 | 5.0 | 5.5 | V |
| Video signal center voltage | | VVC | 6.5 | 7.0 | 7.2 | V |
| Video signal input range*1 | | Vsig | $VVC - 4.5$ | — | $VVC + 4.5$ | V |
| Common voltage of panel*2 | | Vcom | $VVC - 0.5$ | $VVC - 0.4$ | $VVC - 0.3$ | V |

*1 Video input signal shall be symmetrical to VVC.

*2 Common voltage of the panel shall be adjusted to $VVC - 0.4V$.

Level Conversion Circuit

The LCX007BNB has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to HV_{DD} or VV_{DD} . The V_{cc} of external ICs are applicable to $5 \pm 0.5V$.

2. Clock timing conditions (Ta = 25°C) (fHCKn = 7.5MHz, fVCK = 15.7kHz)

| | Item | Symbol | Min. | Typ. | Max. | Unit |
|-----|--------------------------------|--------|------|------|------|------|
| HST | Hst rise time | trHst | — | — | 30 | ns |
| | Hst fall time | tfHst | — | — | 30 | |
| | Hst data set-up time | tdHst | 20 | 67 | 100 | |
| | Hst data hold time | thHst | −40 | 0 | 40 | |
| HCK | Hckn ^{*3} rise time | trHckn | — | — | 30 | |
| | Hckn ^{*3} fall time | tfHckn | — | — | 30 | |
| | Hck1 fall to Hck2 rise time | to1Hck | −15 | 0 | 15 | |
| | Hck1 rise to Hck2 fall time | to2Hck | −15 | 0 | 15 | |
| CLR | Clr rise time | trClr | — | — | 100 | |
| | Clr fall time | tfClr | — | — | 100 | |
| | Clr pulse width | twClr | 3000 | 3100 | 3200 | |
| | Vck rise/fall to Clr fall time | tdClr | −50 | 0 | 50 | |
| VST | Vst rise time | trVst | — | — | 100 | μs |
| | Vst fall time | tfVst | — | — | 100 | |
| | Vst data set-up time | tdVst | −25 | 15 | 25 | |
| | Vst data hold time | thVst | 5 | 15 | 25 | |
| VCK | Vck rise time | trVck | — | — | 100 | ns |
| | Vck fall time | tfVck | — | — | 100 | |
| ENB | Enb rise time | trEnb | — | — | 100 | |
| | Enb fall time | tfEnb | — | — | 100 | |
| | Vck rise/fall to Enb rise time | tdEnb | 350 | 400 | 450 | |
| | Enb pulse width | twEnb | 3450 | 3500 | 3550 | |
| PCG | Pcg rise time | trPcg | — | — | 20 | |
| | Pcg fall time | tfPcg | — | — | 20 | |
| | Pcg fall to Vck rise/fall time | toVck | 650 | 700 | 750 | |
| | Pcg pulse width | twPcg | 1150 | 1200 | 1250 | |

^{*3} Hckn means Hck1 and Hck2.

<Horizontal Shift Register Driving Waveform>

| Item | | Symbol | Waveform | Conditions |
|------|--------------------------------|--------|----------|--|
| HST | Hst rise time | trHst | | O Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns |
| | Hst fall time | tfHst | | |
| | Hst data set-up time | tdHst | | |
| | Hst data hold time | thHst | | |
| HCK | Hckn*3 rise time | trHckn | | O Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns |
| | Hckn*3 fall time | tfHckn | | |
| | Hck1 fall to Hck2 rise time | to1Hck | | |
| | Hck1 rise to Hck2 fall time | to2Hck | | |
| CLR | Clr rise time | trClr | | O Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns |
| | Clr fall time | tfClr | | |
| | Clr pulse width | twClr | | |
| | Vck rise/fall to Clr fall time | tdClr | | |

<Vertical Shift Register Driving Waveform>

| Item | | Symbol | Waveform | Conditions |
|------|--------------------------------|--------|----------|------------|
| VST | Vst rise time | trVst | | |
| | Vst fall time | tfVst | | |
| | Vst data set-up time | tdVst | | |
| | Vst data hold time | thVst | | |
| VCK | Vck rise time | trVck | | |
| | Vck fall time | tfVck | | |
| ENB | Enb rise time | trEnb | | |
| | Enb fall time | tfEnb | | |
| | Vck rise/fall to Enb rise time | tdEnb | | |
| | Enb pulse width | twEnb | | |
| PCG | Pcg rise time | trPcg | | |
| | Pcg fall time | tfPcg | | |
| | Pcg fall to Vck rise/fall time | toVck | | |
| | Pcg pulse width | twPcg | | |

*4 Definitions: The right-pointing arrow ($\bullet \rightarrow$) means +.
 The left-pointing arrow ($\leftarrow \bullet$) means -.
 The black dot at an arrow (\bullet) indicates the start of measurement.

Electrical Characteristics ($T_a = 25^\circ\text{C}$, $HV_{DD} = 15.7\text{V}$, $VV_{DD} = 15.7\text{V}$)

1. Horizontal drivers

| Item | Symbol | Min. | Typ. | Max. | Unit | Condition | |
|------------------------------------|----------|-------|-------|------|------|---------------------------|----------------|
| Input pin capacitance | HCKn | CHckn | — | 7 | 10 | pF | |
| | HST | CHst | — | 7 | 10 | pF | |
| Input pin current | HCK1 | | -500 | -120 | — | μA | HCK1 = GND |
| | HCK2 | | -1000 | -450 | — | μA | HCK2 = GND |
| | HST | | -500 | -160 | — | μA | HST = GND |
| | WID, RGT | | -150 | -30 | — | μA | WID, RGT = GND |
| Video signal input pin capacitance | Csig | — | 250 | — | pF | | |
| Current consumption | IH | — | 7.5 | 10 | mA | HCKn: HCK1, HCK2 (7.5MHz) | |

2. Vertical drivers

| Item | Symbol | Min. | Typ. | Max. | Unit | Condition | |
|------------------------|--------|------|-------|------|------|----------------|------------------------------|
| Input pin capacitance | VCK | CVck | — | 7 | 10 | pF | |
| | VST | CVst | — | 7 | 10 | pF | |
| Input pin current | VCK | | -1000 | -160 | — | μA | VCK = GND |
| PCG, VST, EN, CLR, DWN | | | -150 | -30 | — | μA | PCG, VST, EN, CLR, DWN = GND |
| Current consumption | IV | — | 1.5 | 4 | mA | VCK: (15.7kHz) | |

3. Total power consumption of the panel

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|--------|------|------|------|------|
| Total power consumption of the panel (NTSC) | PWR | — | 150 | 250 | mW |

4. Pin input resistance

| Item | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------|--------|------|------|------|------------------|
| Pin-Vss input resistance | Rpin | 0.4 | 1 | — | $\text{M}\Omega$ |

5. Side signal input pin capacitance

| Item | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------------------|--------|------|------|------|------|
| Side signal input pin capacitance | CSIDon | 8 | 10 | 12 | nF |

Electro-optical Characteristics

(Ta = 25°C, NTSC mode)

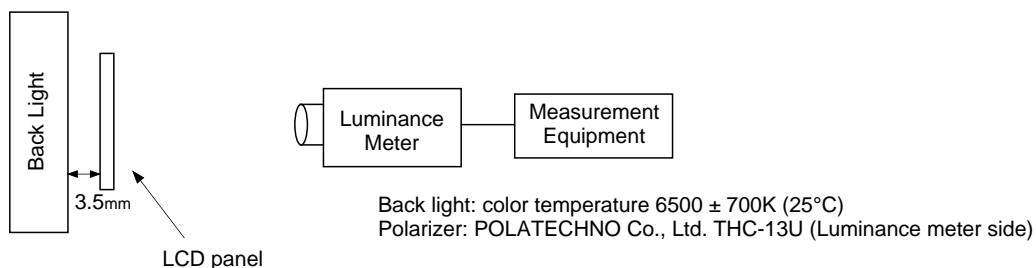
| Item | | Symbol | Measurement method | Min. | Typ. | Max. | Unit | |
|-----------------------|-----------------|--------|---------------------|------|------|------|------|----|
| Contrast ratio | | 60°C | CR60 | 1 | 130 | 190 | — | |
| Optical transmittance | | 60°C | T | 2 | 14.0 | 16.5 | — | |
| V-T characteristics | V ₉₀ | 25°C | RV ₉₀₋₂₅ | 3 | 1.2 | 1.5 | 1.8 | V |
| | | | GV ₉₀₋₂₅ | | 1.4 | 1.7 | 2.0 | |
| | | | BV ₉₀₋₂₅ | | 1.7 | 2.0 | 2.3 | |
| | | 60°C | RV ₉₀₋₆₀ | | 1.1 | 1.4 | 1.7 | |
| | | | GV ₉₀₋₆₀ | | 1.2 | 1.5 | 1.8 | |
| | | | BV ₉₀₋₆₀ | | 1.4 | 1.7 | 2.0 | |
| | V ₅₀ | 25°C | RV ₅₀₋₂₅ | | 1.7 | 2.0 | 2.3 | |
| | | | GV ₅₀₋₂₅ | | 1.8 | 2.1 | 2.4 | |
| | | | BV ₅₀₋₂₅ | | 2.0 | 2.3 | 2.6 | |
| | | 60°C | RV ₅₀₋₆₀ | | 1.5 | 1.8 | 2.1 | |
| | | | GV ₅₀₋₆₀ | | 1.6 | 1.9 | 2.2 | |
| | | | BV ₅₀₋₆₀ | | 1.8 | 2.1 | 2.4 | |
| | V ₁₀ | 25°C | RV ₁₀₋₂₅ | | 2.3 | 2.6 | 2.9 | |
| | | | GV ₁₀₋₂₅ | | 2.4 | 2.7 | 3.0 | |
| | | | BV ₁₀₋₂₅ | | 2.6 | 2.9 | 3.2 | |
| | | 60°C | RV ₁₀₋₆₀ | | 2.1 | 2.4 | 2.7 | |
| | | | GV ₁₀₋₆₀ | | 2.2 | 2.5 | 2.8 | |
| | | | BV ₁₀₋₆₀ | | 2.4 | 2.7 | 3.0 | |
| Response time | ON time | 0°C | ton0 | 4 | — | 50 | 100 | ms |
| | | 25°C | ton25 | | — | 15 | 40 | |
| | OFF time | 0°C | toff0 | | — | 52 | 150 | |
| | | 25°C | toff25 | | — | 16 | 60 | |
| Flicker | | 60°C | F | 5 | — | — | -30 | dB |
| Image retention time | | 25°C | YT60 | 6 | — | — | 0 | s |
| Cross talk | | 25°C | CTK | 7 | — | — | 5 | % |

<Electro-optical Characteristics Measurement>

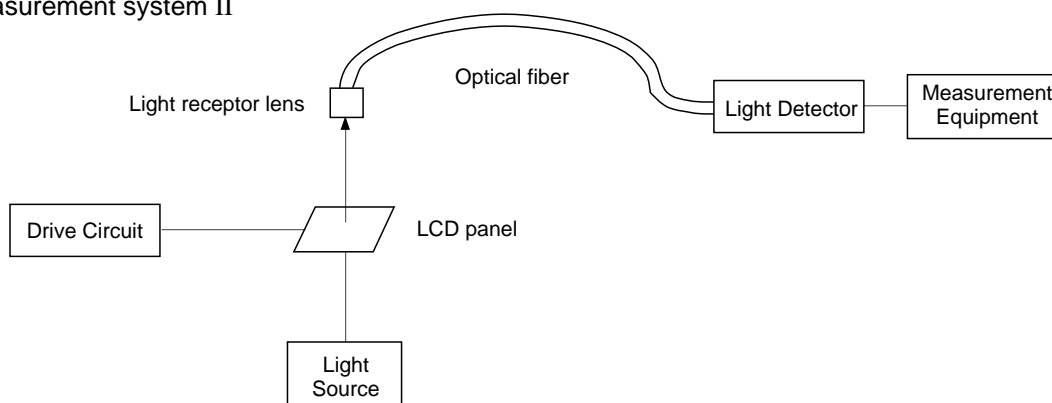
Basic measurement conditions

- (1) Driving voltage
 $HV_{DD} = 15.7V, VV_{DD} = 15.7V$
 $VVC = 7.0V, V_{com} = 6.6V$
- (2) Measurement temperature
 25°C unless otherwise specified.
- (3) Measurement point
 One point in the center of screen unless otherwise specified.
- (4) Measurement systems
 Two types of measurement system are used as shown below.
- (5) Video input signal voltage (V_{sig})
 $V_{sig} = 7.0 \pm V_{AC} [V]$ (V_{AC} : signal amplitude)

* Measurement system I



* Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L (White)}{L (Black)} \dots (1)$$

L (White): Surface luminance of the TFT-LCD panel at the input signal amplitude $V_{AC} = 0.5V$.

L (Black): Surface luminance of the panel at $V_{AC} = 4.5V$.

Both luminosities are measured by System I.

2. Optical Transmittance

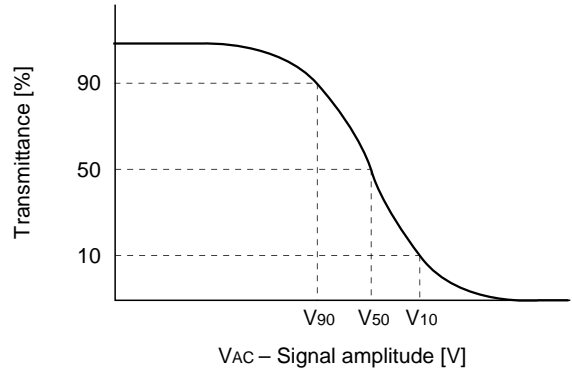
Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{L \text{ (White)}}{\text{Luminance of Back Light}} \times 100 \text{ [%] ... (2)}$$

L (White) is the same expression as defined in the 'Contrast Ratio' section.

3. V-T Characteristics

V-T characteristics, the relationship between signal amplitude and the transmittance of the panels, are measured by System II. V₉₀, V₅₀ and V₁₀ correspond to the each voltage which defines 90%, 50% and 10% of transmittance respectively.



4. Response Time

Response time 'ton' and 'toff' are defined by the formula (5) and (6) respectively.

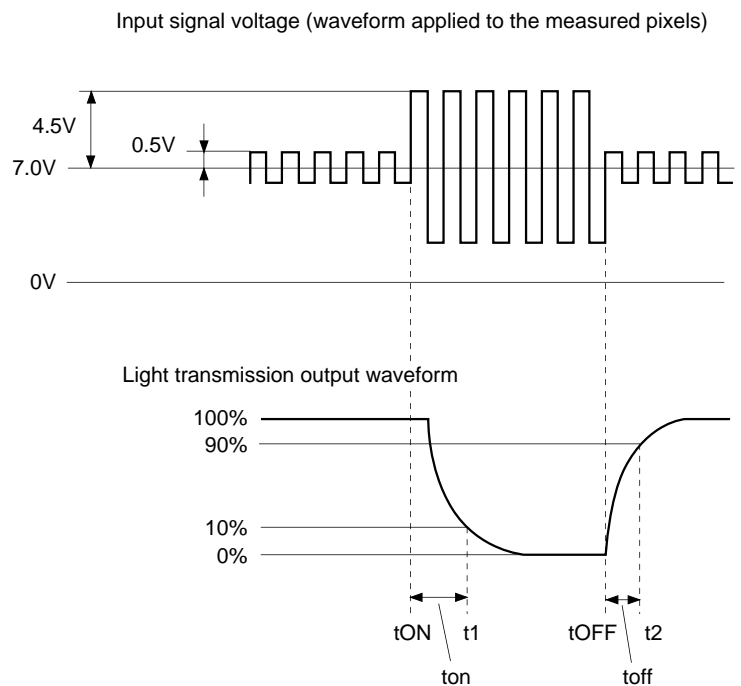
$$t_{on} = t_1 - t_{ON} \text{ ... (5)}$$

$$t_{off} = t_2 - t_{OFF} \text{ ... (6)}$$

t₁: time which gives 10% transmittance of the panel.

t₂: time which gives 90% transmittance of the panel.

The relationships between t₁, t₂, t_{ON} and t_{OFF} are shown in the right figure.



5. Flicker

Flicker (F) is given by the formula (7). DC and AC (NTSC: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster*1 mode are measured by a DC voltmeter and a spectrum analyzer in System II.

$$F [dB] = 20 \log \left\{ \frac{\text{AC component}}{\text{DC component}} \right\} \dots (7)$$

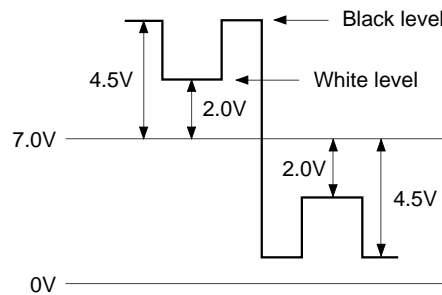
*1 Each input signal condition for gray raster mode is given by $V_{sig} = 7.0 \pm V_{50}$ [V]
 where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T characteristics.

6. Image Retention Time

Image Retention time is given by following procedures.

Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of $V_{sig} = 7.0 \pm V_{AC}$ (V_{AC} : 3 to 4V). Hold V_{AC} that maximizes image retention judging by sight. Measure the time till the residual image becomes indistinct.

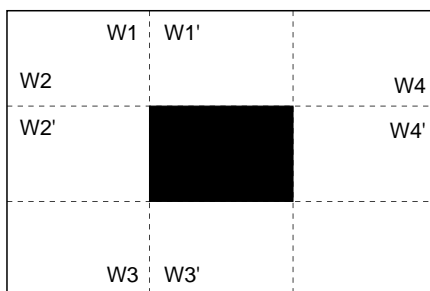
* Monoscope signal conditions:
 $V_{sig} = 7.0 \pm 4.5$ or ± 2.0 [V]
 (shown in the right figure)
 $V_{com} = 6.6V$



Vsig waveform

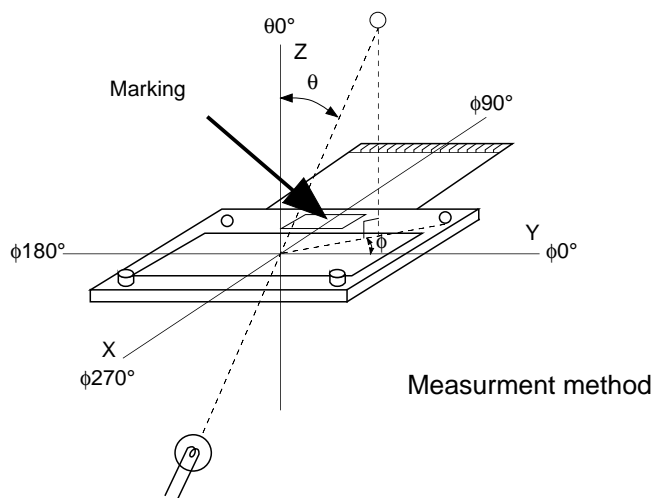
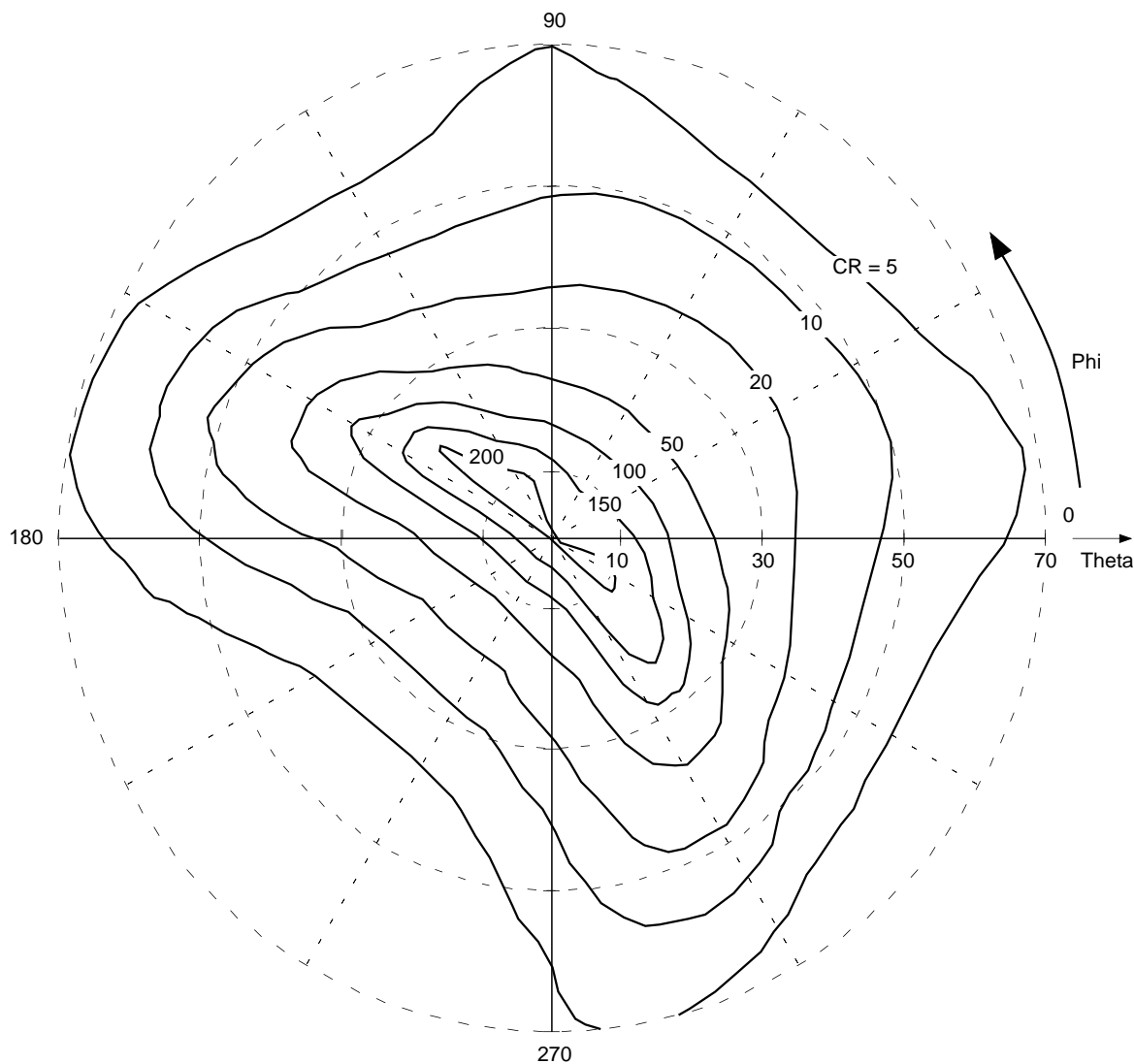
7. Cross talk

Cross talk is determined by the luminance differences between adjacent areas represented W_i' and W_i ($i = 1$ to 4) around black window ($V_{sig} = 4.5V/1V$).

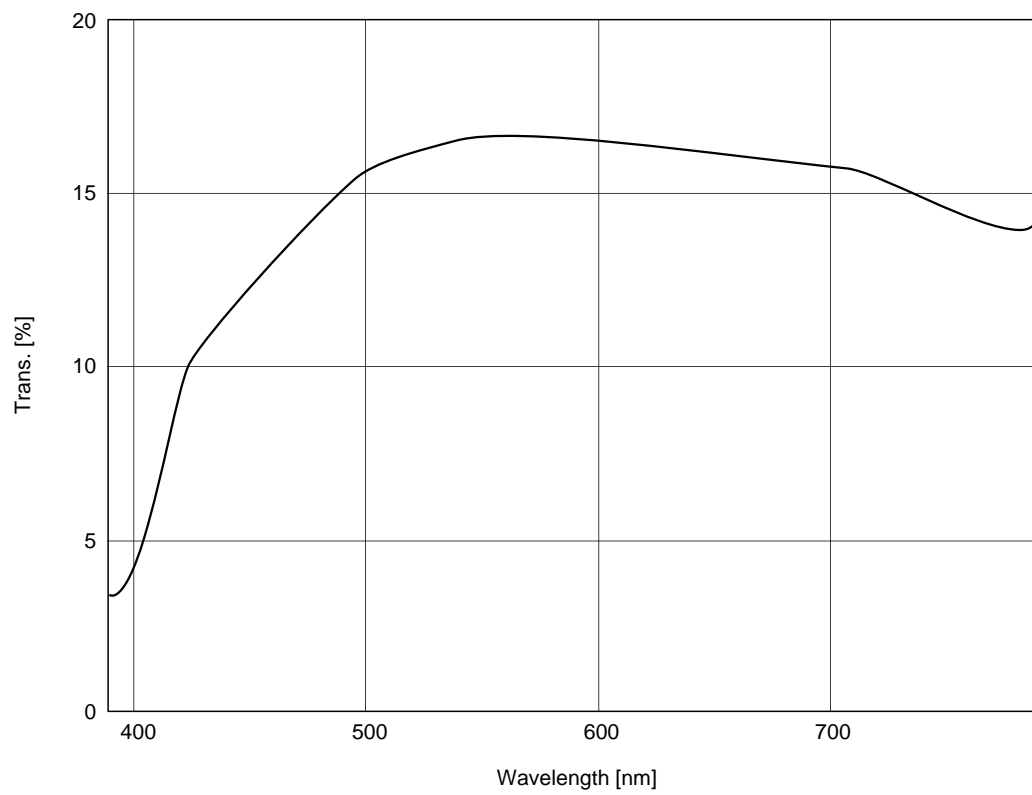


$$\text{Cross talk CTK} = \left| \frac{W_i' - W_i}{W_i} \right| \times 100 [\%]$$

Viewing angle characteristics



Optical transmittance of LCD panel (Typical Value)

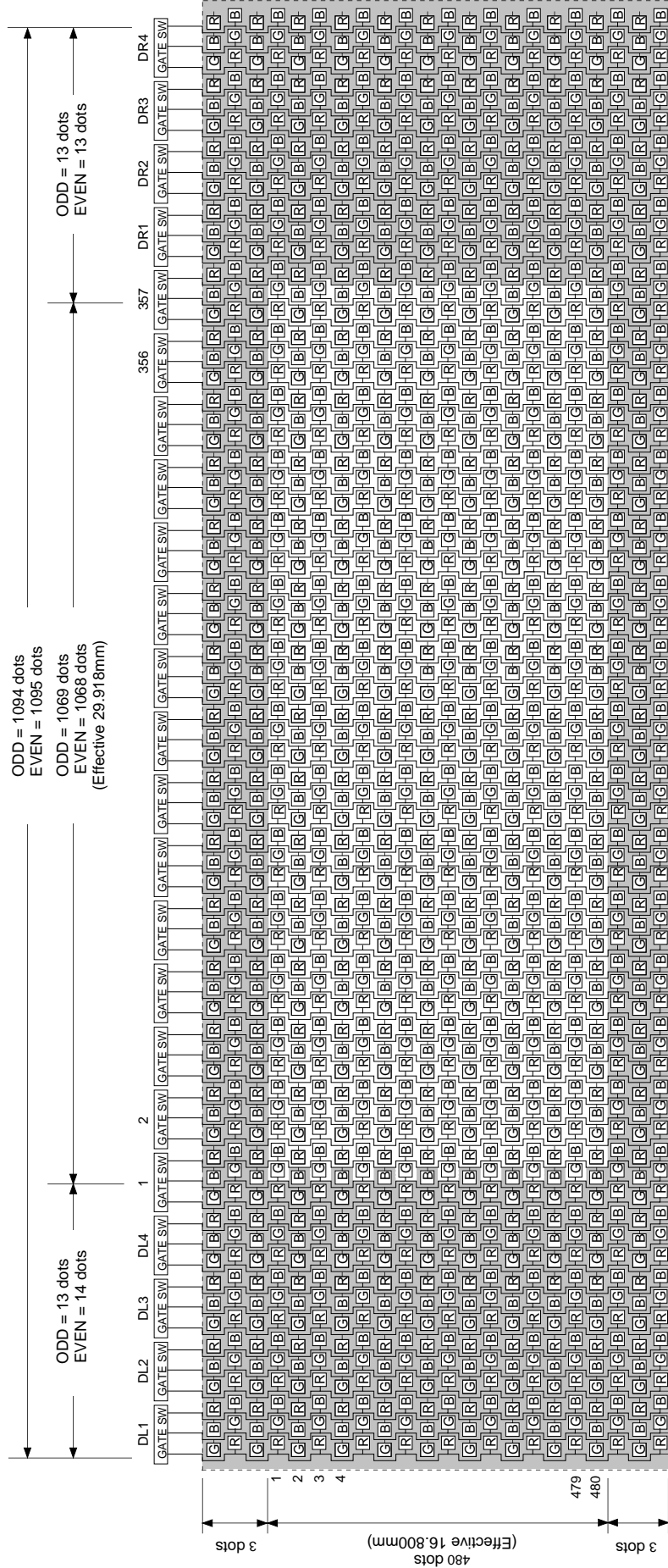


Measurement method: Measurement system II

Description of Operation

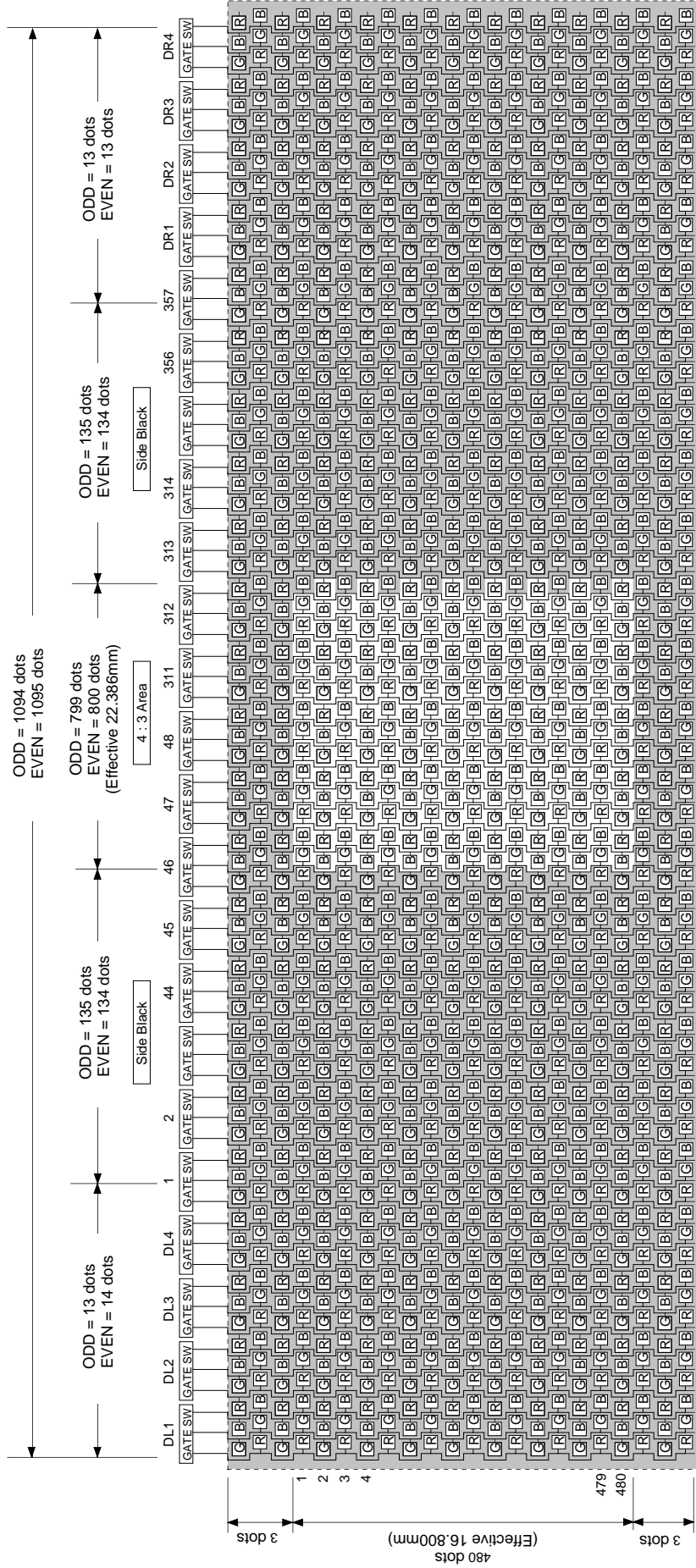
1. Dot Arrangement (1) (16:9 display)

The dots are arranged in a delta pattern. The shaded area is used for the dark border around the display. The R corresponds to SIG2, G to SIG1, and B to SIG3, respectively.



Dot Arrangement (2) (4:3 display)

The dots are arranged in a delta pattern. The shaded area is used for the dark border around the display. The R corresponds to SIG2, G to SIG1, and B to SIG3, respectively.



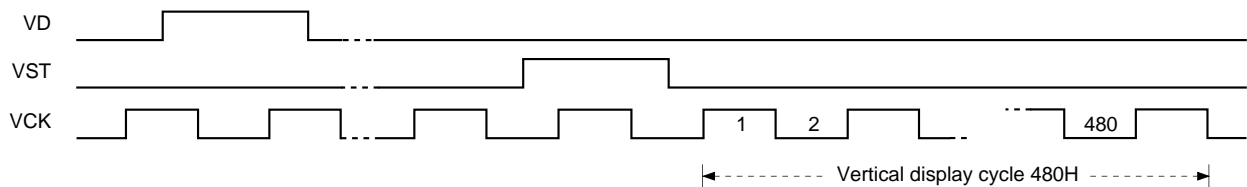
2. LCD Panel Operations

[Description of basic operations]

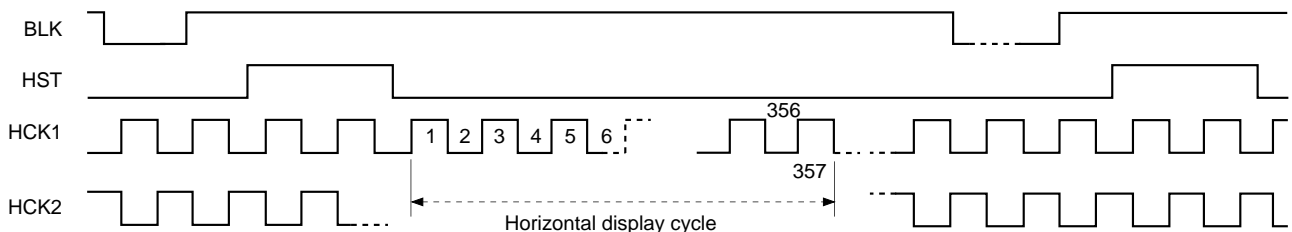
The basic operations of the LCD panel are shown below based on the wide-display mode.

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 480 gate lines sequentially in every horizontal scanning period.
- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 1068.5 signal electrodes sequentially in a single horizontal scanning period.
- Vertical and horizontal shift registers address one pixel, and then turn on Thin Film Transistors (TFTs; two TFTs) to apply a video signal to the dot. The same procedures lead to the entire 480 × 1068.5 dots to display a picture in a single vertical scanning period.
- The LCD pixel dots are arranged in a delta pattern, where the dots connected to the identical signal line are positioned with 1.5-dot offset against those of the adjacent horizontal line. Horizontal Start Pulse (HST) is generated with 1.5-bit offset between the horizontal lines to regulate the above offset. HCK and sample-and-hold (S/H) pulses follow the same 1.5-bit offset scheme.
- The CLR pin is provided to eliminate the shading effect caused by the coupling of selected pulses. While maintaining the CLR at High level, the V_{DD} potential drops to approximately 9.5V. This pin shall be grounded when not in use.
- The video signal shall be input with polarity-inverted system in every horizontal cycle.
- Timing diagrams of the vertical and the horizontal display cycle are shown below:

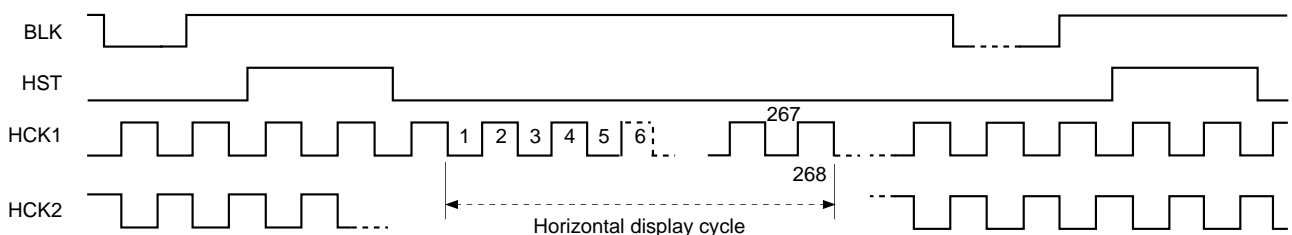
(1) Vertical display cycle



(2) Horizontal display cycle (16:9)



(3) Horizontal display cycle (4:3)



[Description of operating mode]

The LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode
- 4:3 display mode with side-black display

These modes are controlled by three signals (RGT, DWN, and WID). The setting mode is shown below:

| WID | RGT | Mode |
|-----|-----|-----------------|
| H | H | 16:9 right scan |
| H | L | 16:9 left scan |
| L | H | 4:3 right scan |
| L | L | 4:3 left scan |

| DWN | Mode |
|-----|-----------|
| H | Down scan |
| L | Up scan |

The direction of the right/left and/or up/down mean when Pin 1 marking is located at right side with the pin block upside.

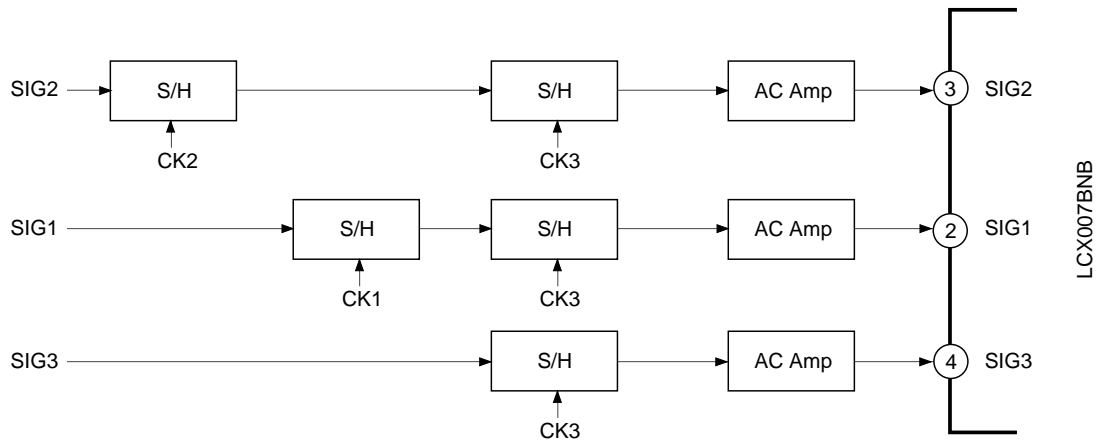
- The analog signal (SID) to display side-black shall be input by 1H inversion synchronized with the signal.

3. 3-dot Simultaneous Sampling

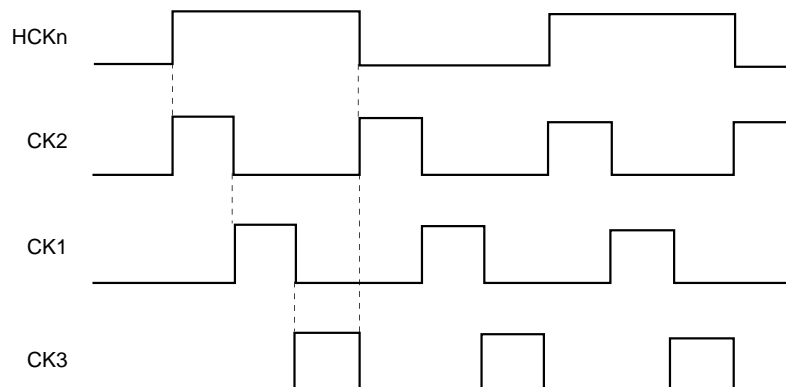
Horizontal driver samples SIG1, SIG2 and SIG3 signal simultaneously, which requires the phase matching between SIG1, SIG2, and SIG3 signals to prevent horizontal resolution from deteriorating. Thus phase matching between each signal is required using an external signal delaying circuit before applying video signal to the LCD panel.

The block diagram of the delaying procedure using sample-and-hold method is as follows.

The LCX007 has the right/left inverse function. The following phase relationship diagram indicates the phase setting for the right scan (RGT = High level). For the left scan (RGT = Low level), the phase setting shall be inverted between SIG2 and SIG3 signals.



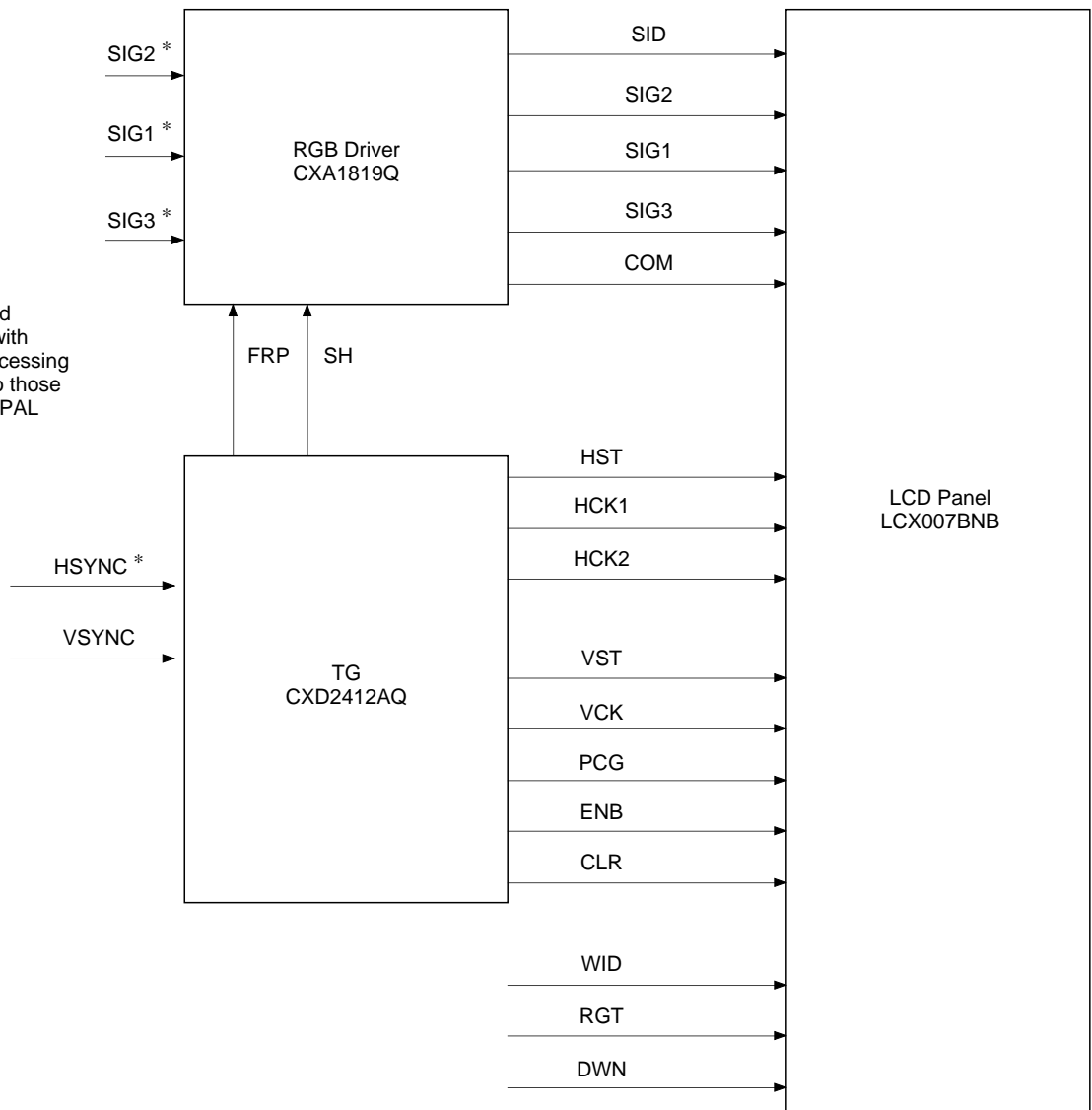
<Phase relationship of delaying sample-and-hold pulses> (right scan)



Display System Block Diagram

An example of display system is shown below.

* The SIG1, 2, 3 and H SYNC signals with double-speed processing shall be applied to those pins in the NTSC/PAL modes.



Reliability test conditions

| Items | Test conditions | Time | |
|--|---|---------------------------|---|
| High temperature operation | Ta = 70°C HV _{DD} = 15.7V VV _{DD} = 15.7V | 250h | Panel appearance and performance after those tests must conform with the standards. |
| High temperature storage | Ta = 85°C | 250h | |
| High temperature & high humidity storage | Ta = 40°C 95% RH | 250h | |
| Temperature cycle | Ta = -30 to +85°C | 10cy | |
| Vibration | X, Y, Z, 1.5mm 10 to 55Hz (1min. reciprocation) | 20min. for each direction | |

Anti-electrostatic discharge test results

Conditions: C = 200pF, Rs = 0Ω

Result:

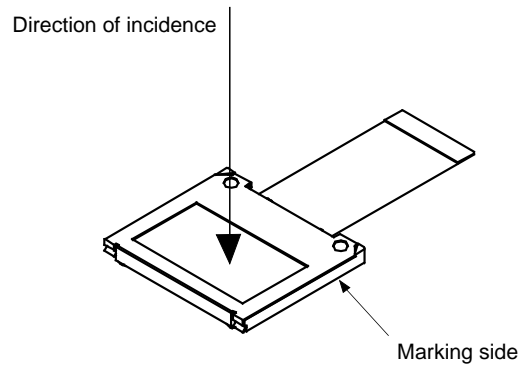
| Breakdown voltage | Up to 100V | 101 to 200V |
|-------------------|------------|-------------|
| + | - | - |
| - | - | Pin 8 |

Pins except pin no.8 have the strength more than 200V.

Important

(1) Direction of incident light

Allow incident light to hit upon an opposite side of a mark-indicated surface.



(2) Polarizer

This LCD is attached with a polarizer. A suitable heat-dissipation method shall be incorporated to suppress optical degradation of a polarizer.

(3) Light source

- Use visible light (wavelength $\lambda = 400$ to 780nm) as a light source. Do not use a light source containing infrared or ultraviolet components.
- Suppress leakage light (reflection light) into a backside of a panel to sufficiently weak level or shut it out completely.

Notes on Handling

(1) Static charge prevention

Be sure to take following protective measures. TFT-LCD panels are easily damaged by static charge.

- a) Use non-chargeable gloves, or simply use bare hands.
- b) Use an earth-band when handling.
- c) Do not touch any electrodes of a panel.
- d) Wear non-chargeable clothes and conductive shoes.
- e) Install conductive mat on the working floor and working table.
- f) Keep panels away from any charged materials.
- g) Use ionized air to discharge the panels.

(2) Protection from dust and dirt

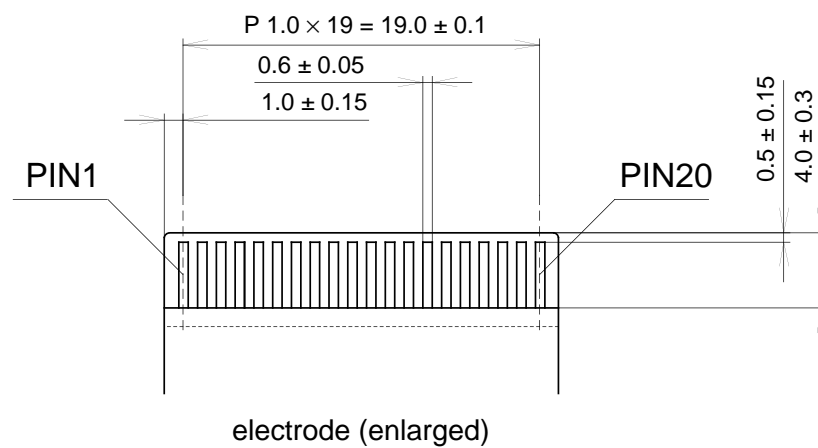
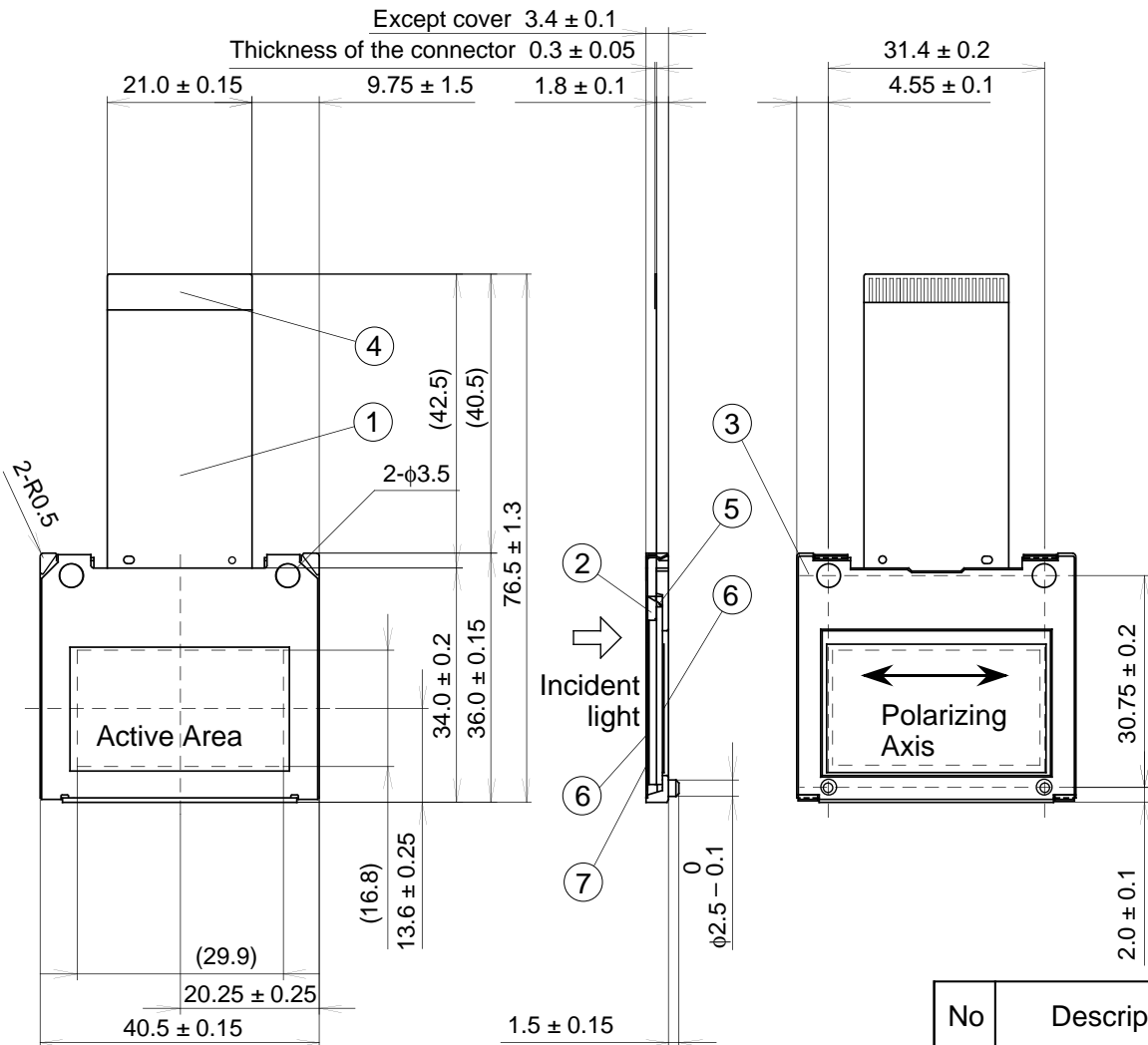
- a) Handle in clean environment.
- b) When delivered, a surface of a panel (Polarizer) is covered by a protective sheet.
Peel off the protective sheet carefully not to damage the panel.
- c) Do not touch the surface of a panel. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stain on the surface.
- d) Use ionized air to blow off dust at a panel.

(3) Other handling precautions

- a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
- b) Do not drop a panel.
- c) Do not twist or bend a panel or a panel frame.
- d) Keep a panel away from heat source.
- e) Do not dampen a panel with water or other solvents.
- f) Avoid to store or to use a panel in a high temperature or in a high humidity, which may result in panel damages.
- g) Minimum bent radius rating for flexible substrates is 1mm.
- h) Panel screw torque should not exceed 3kg · cm.

Package Outline

Unit: mm



electrode (enlarged)

| No | Description |
|----|----------------------|
| 1 | F P C |
| 2 | Molding material |
| 3 | Outside frame |
| 4 | Reinforcing board |
| 5 | Reinforcing material |
| 6 | Polarizing film |
| 7 | Cover |

The rotation angle of the active area relative to H and V is ± 1°.

weight 7g