

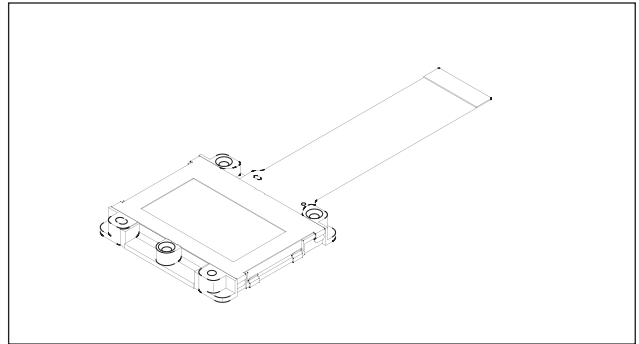
## 3.4cm (1.35 Type) Black-and-White LCD Panel

### Description

The LCX037BLT is a 3.4cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with a built-in peripheral driving circuit. Use of three LCX037BLT panels provides a full-color representation. The striped arrangement suitable for data display is capable of displaying fine text and vertical lines.

The adoption of a new developed dot-line inverse drive system, CMP (Chemical Mechanical Polish) and OCS (On Chip Spacer) structures contribute to high picture quality.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.



### Features

- Number of active dots: 1,049,088 (1.35 Type, 3.4cm in diagonal)
- High optical transmittance: 16% (typ.)
- Dot-line inverse drive circuit
- OCS structure
- CMP (Chemical Mechanical Polish) structure
- High contrast ratio with normally white mode: 300 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function
- Antidust glass package

### Element Structure

- Dots: 1366 (H) × 768 (V) = 1,049,088
- Built-in peripheral driver using polycrystalline silicon super thin film transistors

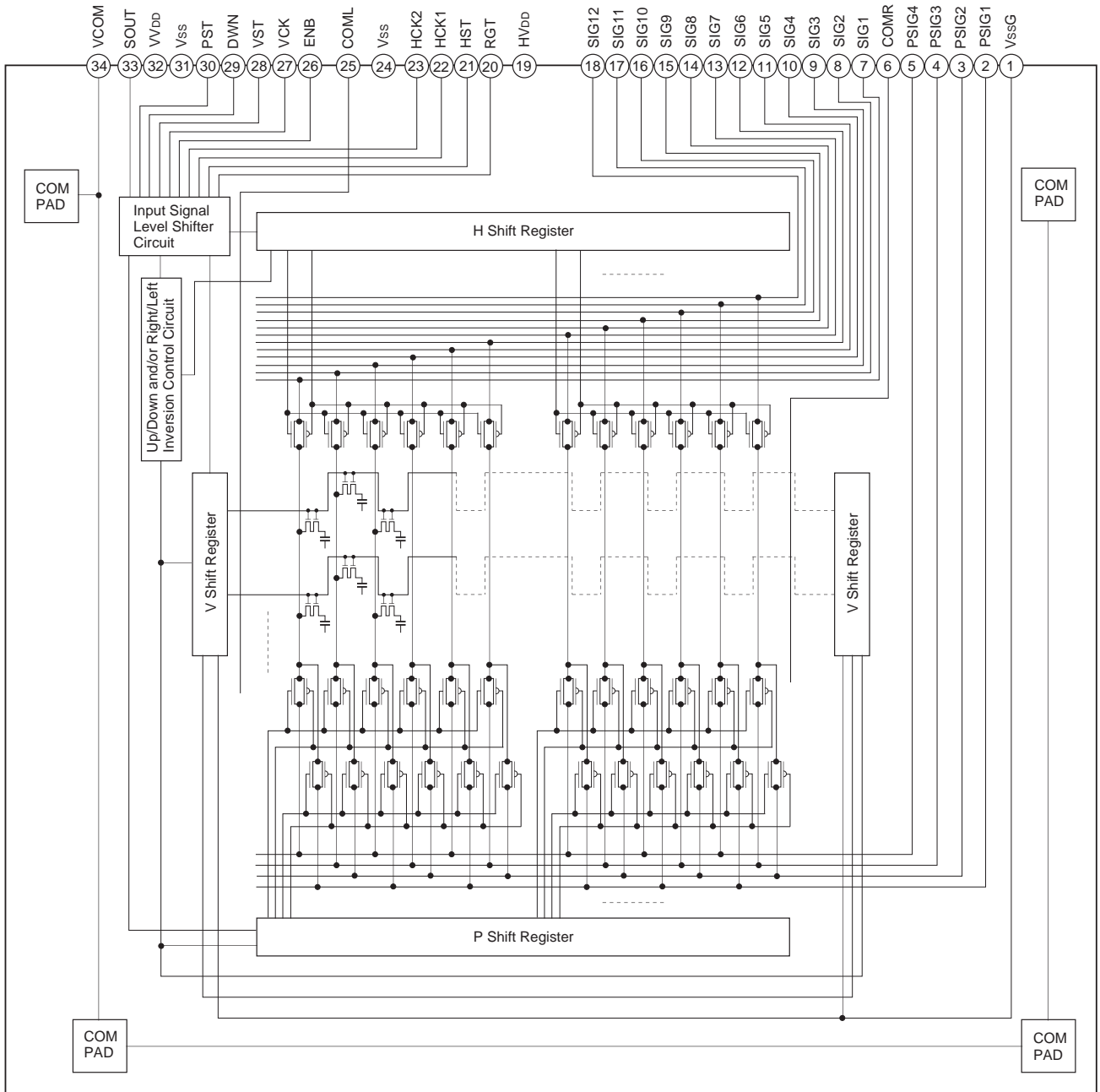
### Applications

- Liquid crystal data projectors
- Liquid crystal multimedia projectors
- Liquid crystal rear-projector TVs, etc.

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Block Diagram



**Absolute Maximum Ratings** ( $V_{SS} = 0V$ )

• H driver supply voltage	HV <sub>DD</sub>	-1.0 to +20	V
• V driver supply voltage	VV <sub>DD</sub>	-1.0 to +20	V
• Common pad voltage	COM, COML, COMR	-1.0 to +17	V
• H shift register input pin voltage	HST, HCK1, HCK2, RGT	-1.0 to +17	V
• V shift register input pin voltage	VST, VCK, PST, ENB, DWN	-1.0 to +17	V
• Video signal input pin voltage	SIG1 to 12, PSIG1 to 4	-1.0 to +15	V
• Operating temperature*	T <sub>opr</sub>	-10 to +70	°C
• Storage temperature	T <sub>stg</sub>	-30 to +85	°C

\* Panel temperature inside the antidust glass

**Operating Conditions** ( $V_{SS} = 0V$ )

- Supply voltage
 

HV <sub>DD</sub>	15.5 ± 0.3V
VV <sub>DD</sub>	15.5 ± 0.3V
- Input pulse voltage (V<sub>p-p</sub> of all input pins except video signal and uniformity improvement signal)
 

V <sub>in</sub>	5.0 ± 0.5V
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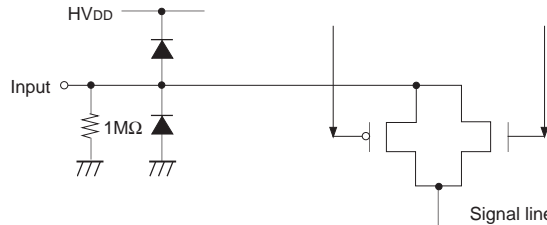
## Pin Description

Pin No.	Symbol	Description
1	VssG	GND for V gate
2	PSIG1	Uniformity improvement signal (for black)
3	PSIG2	Uniformity improvement signal (for black)
4	PSIG3	Uniformity improvement signal (for gray)
5	PSIG4	Uniformity improvement signal (for gray)
6	COMR	Voltage for right CS (Storage capacity) electrode line
7	SIG1	Video signal 1 to panel
8	SIG2	Video signal 2 to panel
9	SIG3	Video signal 3 to panel
10	SIG4	Video signal 4 to panel
11	SIG5	Video signal 5 to panel
12	SIG6	Video signal 6 to panel
13	SIG7	Video signal 7 to panel
14	SIG8	Video signal 8 to panel
15	SIG9	Video signal 9 to panel
16	SIG10	Video signal 10 to panel
17	SIG11	Video signal 11 to panel
18	SIG12	Video signal 12 to panel
19	HV <sub>DD</sub>	Power supply for H driver
20	RGT	Drive direction pulse for H shift register (H: normal, L: reverse)
21	HST	Start pulse for H shift register drive
22	HCK1	Clock pulse for H shift register drive 1
23	HCK2	Clock pulse for H shift register drive 2
24	Vss	GND (H, V, drivers)
25	COML	Voltage for left CS (storage capacity) electrode line
26	ENB	Enable pulse for gate selection
27	VCK	Clock pulse for V shift register drive
28	VST	Start pulse for V shift register drive
29	DWN	Drive direction pulse for V shift register (H: normal, L: reverse)
30	PST	Start pulse for P shift register drive
31	Vss	GND (H, V, P drivers)
32	VV <sub>DD</sub>	Power supply for V, P drivers
33	SOUT	Test pin; leave this pin open.
34	VCOM	Common voltage of panel

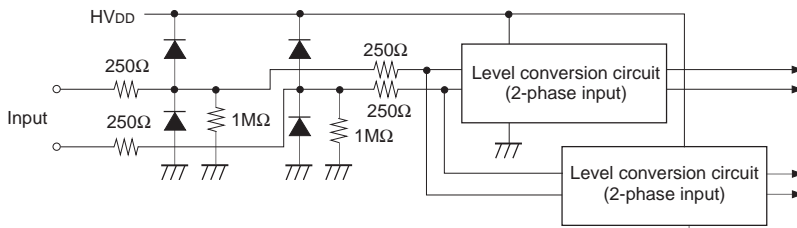
**Input Equivalent Circuit**

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal inputs. All pins are connected to Vss with a high resistor of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistance value: typ.)

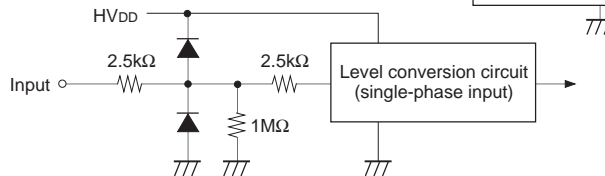
(1) VSIG1 to VSIG12, PSIG



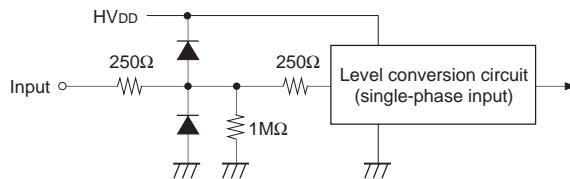
(2) HCK1, HCK2



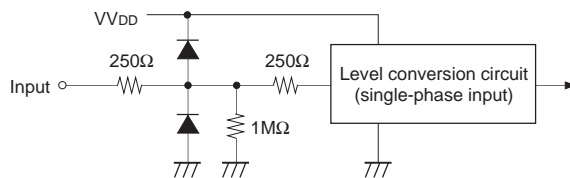
(3) RGT



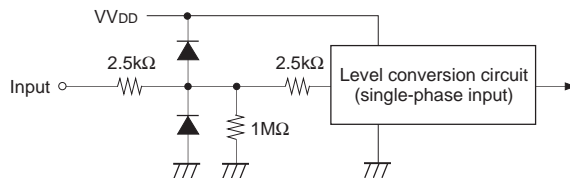
(4) HST



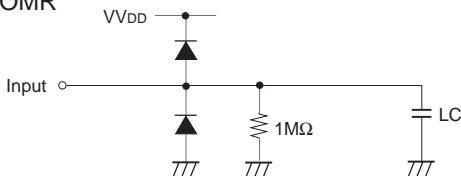
(5) PST, VCK



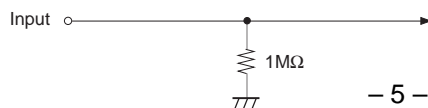
(6) VST, ENB, DWN



(7) VCOM, COML, COMR



(8) HVDD, VssG, VVDD



are all Vss.

## Input Signals

### 1. Input signal voltage conditions ( $V_{SS} = 0V$ )

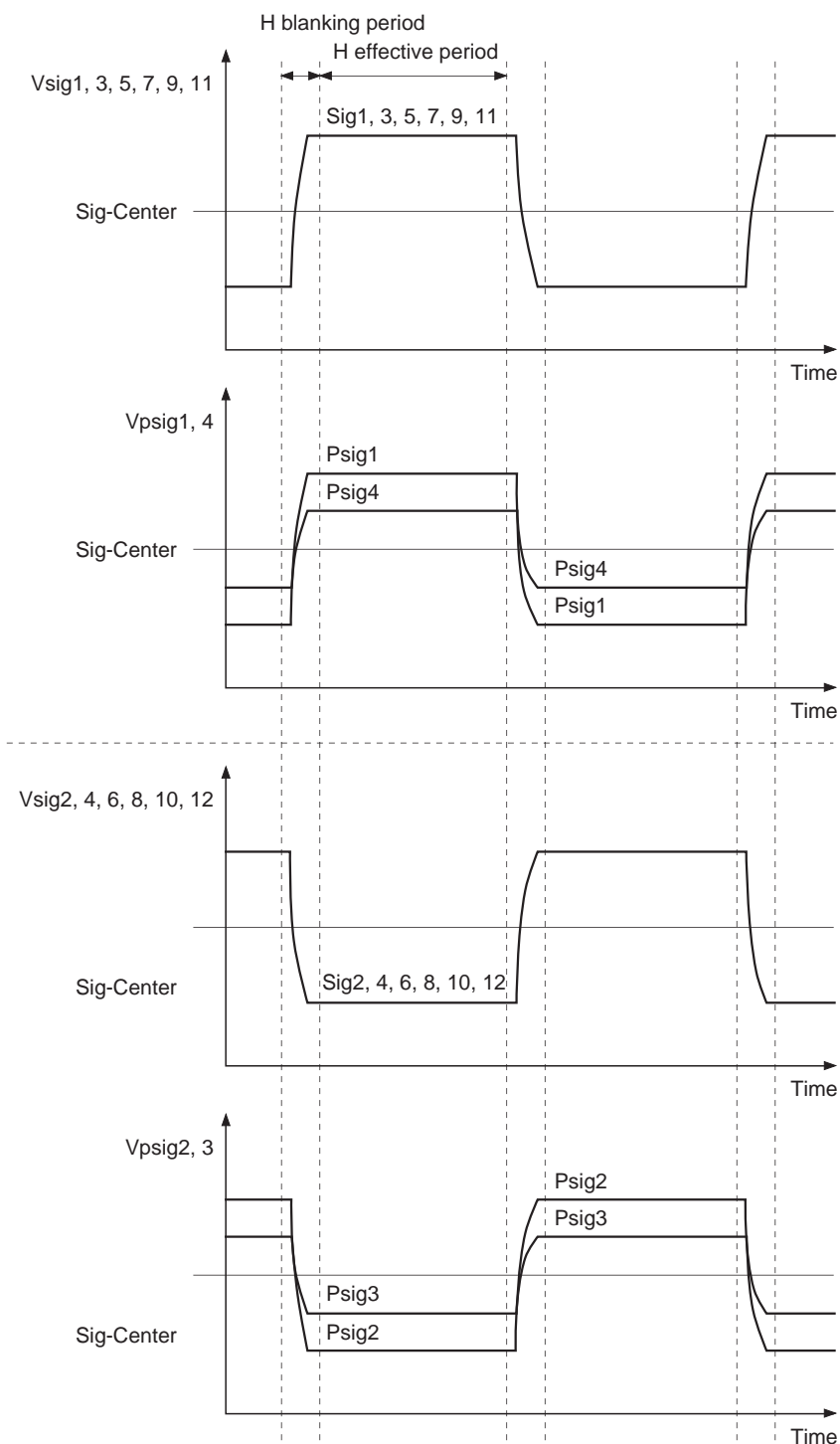
Item		Symbol	Min.	Typ.	Max.	Unit
H shift register input voltage HST, HCK1, HCK2, RGT	(Low)	VHIL	-0.5	0.0	0.4	V
	(High)	VHIH	4.5	5.0	5.5	V
V shift register input voltage VB1, VB2, BLK, VST, VCK, PCG, ENB, DWN	(Low)	VVIL	-0.5	0.0	0.4	V
	(High)	VVIH	4.5	5.0	5.5	V
Video signal center voltage		VVC	7.4	7.5	7.6	V
Video signal input range*1		Vsig1, 3, 5, 7, 9, 11	$VVC \pm 4.4$	$VVC \pm 4.5$	$VVC \pm 4.6$	V
		Vsig2, 4, 6, 8	$VVC \pm 4.4$	$VVC \pm 4.5$	$VVC \pm 4.6$	V
Common voltage of panel*2		Vcom	$VVC - 0.8$	$VVC - 0.7$	$VVC - 0.6$	V
Uniformity improvement signal input voltage*3		Vpsig1, 3	$VVC \pm 4.4$	$VVC \pm 4.5$	$VVC \pm 4.6$	V
		Vpsig2, 4	$VVC \pm 2.3$	$VVC \pm 2.5$	$VVC \pm 2.7$	V

\*1 Input video signal shall be symmetrical to VVC.

\*2 The typical value of the common pad voltage may lower its suitable voltage according to the set construction to use. In this case, use the voltage of which has maximum contrast as typical value. When the typical value is lowered, the maximum and minimum values may lower.

\*3 Input video signal, and a uniformity improvement signal as shown phase like below. And the rise time  $tr_{Psig}$  and the fall time  $tf_{Psig}$  of  $P_{sig1}$  to 4 are suppressed within 400ns.

**Phase relationship between video signal and uniformity improvement signal**



**Level Conversion Circuit**

The LCX037BLT has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to  $HV_{DD}$  or  $VV_{DD}$ . The  $V_{CC}$  of external ICs are applicable to  $5 \pm 0.5V$ .

## 2. Clock timing conditions (Ta = 25°C)

(fHckn = 6.67MHz, fVck = 25.6kHz, fv = 60Hz)

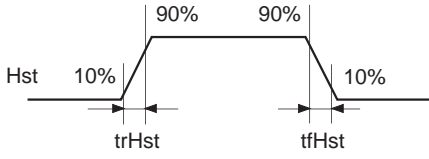
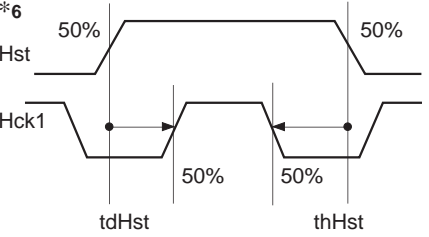
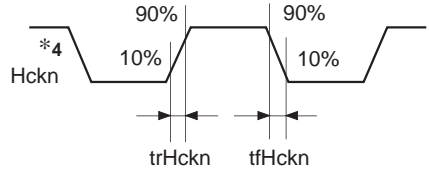
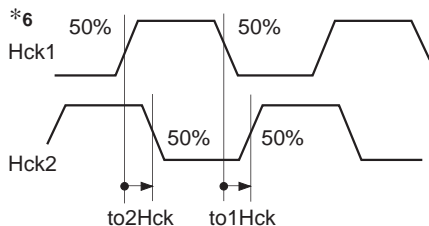
	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst	—	—	30	ns
	Hst fall time	tfHst	—	—	30	
	Hst data set-up time	tdHst	-10	0	10	
	Hst data hold time	thHst	65	75	85	
HCK	Hckn rise time*4	trHckn	—	—	30	ns
	Hckn fall time*4	tfHckn	—	—	30	
	Hck1 fall to Hck2 rise time	to1Hck	-15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	-15	0	15	
VST	Vst rise time	trVst	—	—	100	μs
	Vst fall time	tfVst	—	—	100	
	Vst data set-up time	tdVst	5	10	15	
	Vst data hold time	thVst	5	10	15	
VCK	Vck rise time	trVck	—	—	100	ns
	Vck fall time	tfVck	—	—	100	
ENB	Enb rise time	trEnb	—	—	100	ns
	Enb fall time	tfEnb	—	—	100	
	Horizontal video period completed to Enb fall time	tdEnb	800*5	1000	1200	
	Enb width	twEnb	900	1000	1100	
	Vck rise/fall to Enb rise time	toEnb	300	400	500	
	Enb rise to Pst rise time	toPst	390	400	410	
PST	Pst rise time	trPst	—	—	30	×4 cycles of Hck
	Pst fall time	tfPst	—	—	30	
	Pst data set-up time	tdPst	-10	0	10	
	Pst data hold time	thPst	65	75	85	
	Pst rise to Hst rise time	toHst	—	4	—	

\*4 Hckn means Hck1 and Hck2.

\*5 The minimum value of tdEnb is 800ns. When H-BLK has a long period and has some time to spare, take more time prior to other value.



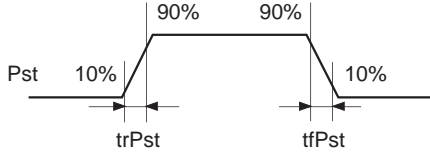
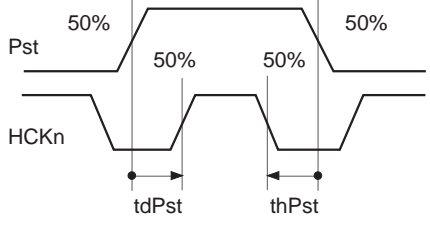
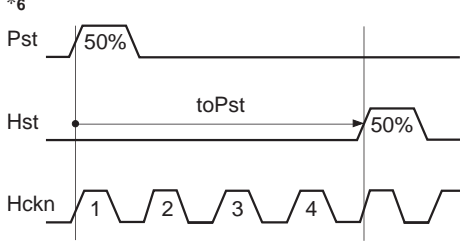
<Horizontal Shift Register Driving Waveform>

Item	Symbol	Waveform	Conditions	
HST	Hst rise time	trHst		<ul style="list-style-type: none"> <li>• Hckn*4</li> <li>duty cycle 50%</li> <li>to1Hck = 0ns</li> <li>to2Hck = 0ns</li> </ul>
	Hst fall time	tfHst		
	Hst data set-up time	tdHst		
	Hst data hold time	thHst		
HCK	Hckn rise time*4	trHckn		<ul style="list-style-type: none"> <li>• Hckn*4</li> <li>duty cycle 50%</li> <li>to1Hck = 0ns</li> <li>to2Hck = 0ns</li> </ul>
	Hckn fall time*4	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		
	Hck1 rise to Hck2 fall time	to2Hck		

\*6 Definitions: The right-pointing arrow ( •→ ) means +.  
 The left-pointing arrow ( ←• ) means -.  
 The black dot at an arrow ( • ) indicates the start of measurement.

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
VST	Vst rise time	trVst		
	Vst fall time	tfVst		
	Vst data set-up time	tdVst		
	Vst data hold time	thVst		
VCK	Vck rise time	trVck		
	Vck fall time	tfVck		
ENB	Enb rise time	trEnb		
	Enb fall time	tfEnb		
	Horizontal video period completed to Enb fall time	tdEnb		
	Enb width	twEnb		
	Vck rise/fall to Enb fall time	toEnb		
Enb rise to Pst rise time	toPst			

	Item	Symbol	Waveform	Conditions
PST	Pst rise time	trPst		
	Pst fall time	tfPst		
	Pst data set-up time	tdPst		
	Pst data set-up time	thPst		
	Pst rise to Hst rise time	toHst	<p>*6</p> 	

**Electrical Characteristics** ( $T_a = 25^\circ\text{C}$ ,  $HV_{DD} = 15.5\text{V}$ ,  $V_{DD} = 15.5\text{V}$ )**1. Horizontal drivers**

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	
Input pin capacitance	HCKn	CHckn	—	15	20	pF	
	HST	CHst	—	15	20	pF	
Input pin current	HCK1		-1000	-500	—	$\mu\text{A}$	HCK1 = GND
	HCK2		-1000	-500	—	$\mu\text{A}$	HCK2 = GND
	HST		-500	-170	—	$\mu\text{A}$	HST = GND
	RGT		-150	-40	—	$\mu\text{A}$	RGT = GND
Video signal input pin capacitance	Csig	—	180	250	pF		
Current consumption	IH	—	15	25	mA	HCKn: HCK1, HCK2 (6.67MHz)	

**2. Vertical drivers**

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	
Input pin capacitance	VCK	CVck	—	15	20	pF	
	VST, PST	CVst	—	15	20	pF	
Input pin current	VCK, PST		-500	-150	—	$\mu\text{A}$	VCK = GND, PST = GND
	VST, ENB, DWN		-150	-35	—	$\mu\text{A}$	VST, ENB, DWN = GND
Current consumption	IV	—	20	30	mA	VCK: (25.6kHz)	

**3. Total power consumption of the panel**

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel	PWR	—	550	1000	mW

**4. Pin input resistance**

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – Vss input resistance	Rpin	0.4	1	—	$\text{M}\Omega$

**5. Uniformity improvement signal**

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance for uniformity improvement signal	CPSIG1 to 4	—	0.5	5.0	nF

**Electro-optical Characteristics**

Item		Symbol	Measurement method	Min.	Typ.	Max.	Unit	
Contrast ratio		25°C	CR	1	200	300	—	
Optical transmittance		25°C	T	2	13	16	—	
V-T characteristics	V <sub>90</sub>	25°C	RV <sub>90-25</sub>	3	0.9	1.3	1.6	V
			GV <sub>90-25</sub>		1.0	1.4	1.7	
			BV <sub>90-25</sub>		1.2	1.6	1.9	
		60°C	RV <sub>90-60</sub>		0.9	1.3	1.6	
			GV <sub>90-60</sub>		1.0	1.4	1.7	
			BV <sub>90-60</sub>		1.1	1.5	1.8	
	V <sub>50</sub>	25°C	RV <sub>50-25</sub>		1.3	1.7	2.0	
			GV <sub>50-25</sub>		1.4	1.8	2.1	
			BV <sub>50-25</sub>		1.5	1.9	2.2	
		60°C	RV <sub>50-60</sub>		1.2	1.6	1.9	
			GV <sub>50-60</sub>		1.3	1.7	2.0	
			BV <sub>50-60</sub>		1.4	1.8	2.1	
	V <sub>10</sub>	25°C	RV <sub>10-25</sub>		1.7	2.1	2.4	
			GV <sub>10-25</sub>		1.8	2.2	2.5	
			BV <sub>10-25</sub>		1.9	2.3	2.6	
		60°C	RV <sub>10-60</sub>		1.7	2.1	2.4	
			GV <sub>10-60</sub>		1.8	2.2	2.5	
			BV <sub>10-60</sub>		1.8	2.2	2.5	
Response time	ON time	0°C	ton0	4	—	24.0	80.0	ms
		25°C	ton25		—	9.0	40.0	
	OFF time	0°C	toff0		—	99.0	200.0	
		25°C	toff25		—	27.0	70.0	
Flicker		60°C	F	5	—	-82.0	-40.0	dB
Image retention time		25°C	YT60	6	—	0	—	s
Cross talk		25°C	CTK	7	—	—	5	%

**Reflection Preventive Processing**

When a phase substrate which rotates the polarization axis is used to adjust to the polarization direction of a polarization screen or prism, use a phase substrate with reflection preventive processing on the surface. This prevents characteristic deterioration caused by luminous reflection.

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

$HV_{DD} = 15.5V, VV_{DD} = 15.5V$

$VVC = 7.5V, Vcom = 6.8V$

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of the screen unless otherwise specified.

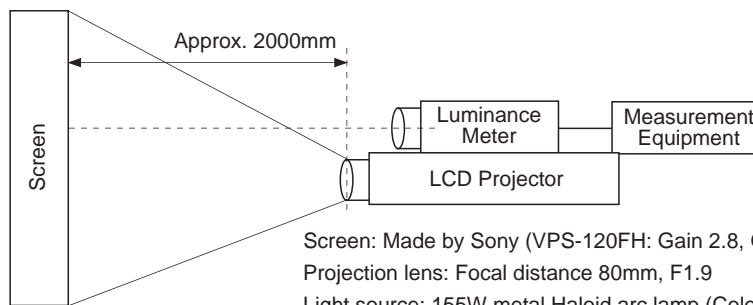
(4) Measurement systems

Two types of measurement systems are used as shown below.

(5) Video input signal voltage ( $V_{sig}$ )

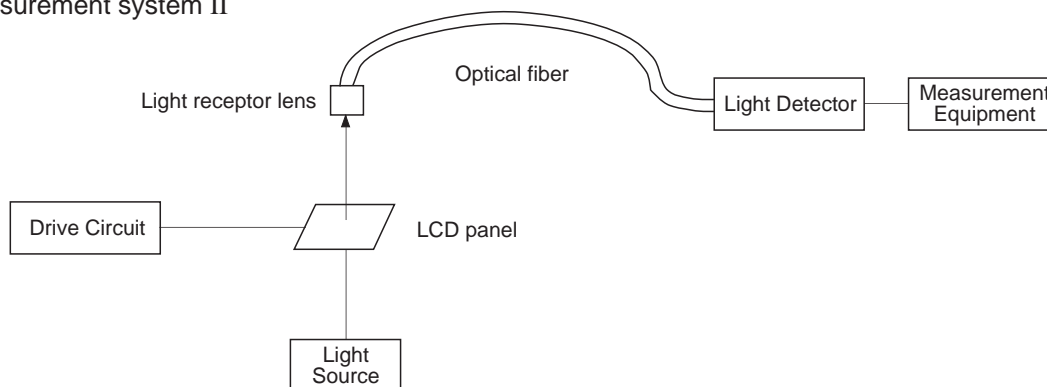
$V_{sig} = 7.5 \pm V_{AC}$  [V] ( $V_{AC}$  = signal amplitude)

• Measurement system I



Screen: Made by Sony (VPS-120FH: Gain 2.8, Glass Beaded Type) or equivalent  
 Projection lens: Focal distance 80mm, F1.9  
 Light source: 155W metal Haloid arc lamp (Color temperature 7500K ± 500)  
 (×24, Sensor area: 7mmφ)  
 Polarizer: Side of incidence-Nitto Denko's EG-1224DU or Polatechno's SKN-18242T  
 Side of output light-Polatechno's SHC-128 or equivalent

• Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L(\text{White})}{L(\text{Black})} \dots (1)$$

L (White): Surface luminance of the center of the screen at the input signal amplitude  $V_{AC} = 0.5V$ .

L (Black): Surface luminance of the center of the screen at  $V_{AC} = 5.5V$ .

Both luminosities are measured by System I.

**2. Optical Transmittance**

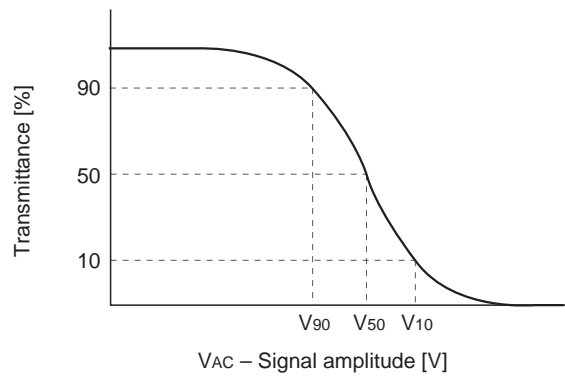
Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{\text{White luminance}}{\text{Luminance of light source}} \times 100 [\%] \dots (2)$$

"White luminance" means the maximum luminance on the screen at the input signal amplitude  $V_{AC} = 0.5V$  on Measurement System I.

**3. V-T Characteristics**

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panels, are measured by System II by inputting the same signal amplitude  $V_{AC}$  to each input pin.  $V_{90}$ ,  $V_{50}$ , and  $V_{10}$  correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.



**4. Response Time**

Response time  $t_{on}$  and  $t_{off}$  are defined by formulas (5) and (6) respectively.

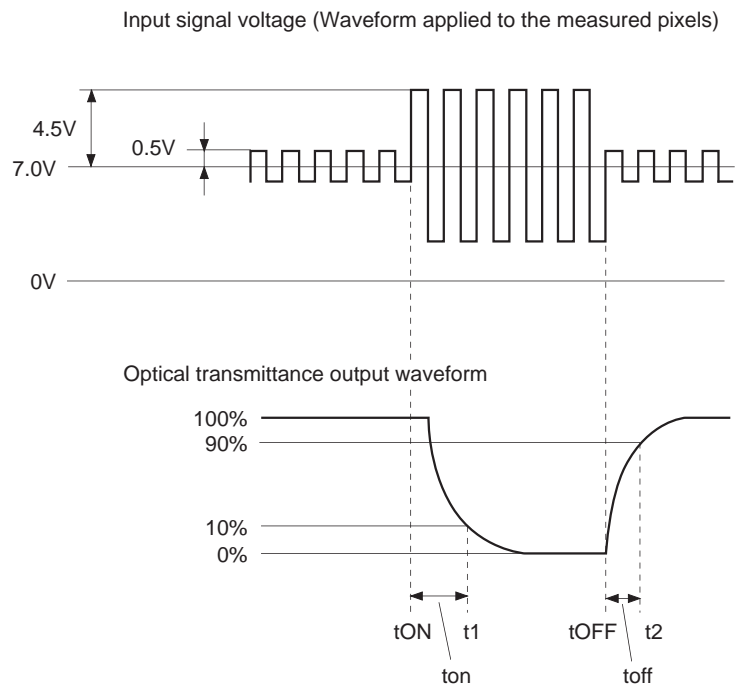
$$t_{on} = t_1 - t_{ON} \dots (5)$$

$$t_{off} = t_2 - t_{OFF} \dots (6)$$

$t_1$ : time which gives 10% transmittance of the panel.

$t_2$ : time which gives 90% transmittance of the panel.

The relationships between  $t_1$ ,  $t_2$ ,  $t_{ON}$  and  $t_{OFF}$  are shown in the right figure.



**5. Flicker**

Flicker (F) is given by formula (7). DC and AC (SXGA: 30Hz, rms) components of the panel output signal for gray raster\* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

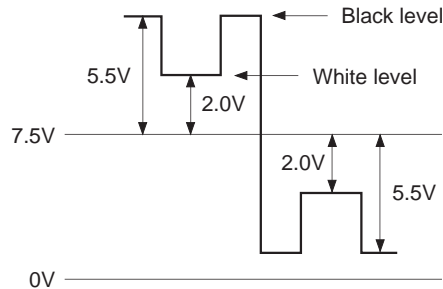
$$F \text{ [dB]} = 20\log \left\{ \frac{\text{AC component}}{\text{DC component}} \right\} \dots(7)$$

\* Each input signal voltage for gray raster mode is given by  $V_{sig} = 7.0 \pm V_{50}$  [V] where:  $V_{50}$  is the signal amplitude which gives 50% of transmittance in V-T characteristics.

**6. Image Retention Time**

Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of  $V_{sig} = 7.5 \pm V_{AC}$  ( $V_{AC}$ : 3 to 4V). Judging by sight at the  $V_{AC}$  that holds the maximum image retention, measure the time till the residual image becomes indistinct.

\* Monoscope signal conditions:  
 $V_{sig} = 7.5 \pm 4.5$  or  $\pm 2.0$  [V]  
 (shown in the right figure)  
 $V_{com} = 6.8V$

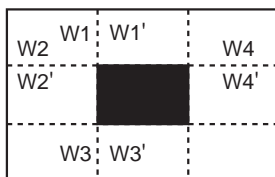


Vsig waveform

**7. Cross Talk**

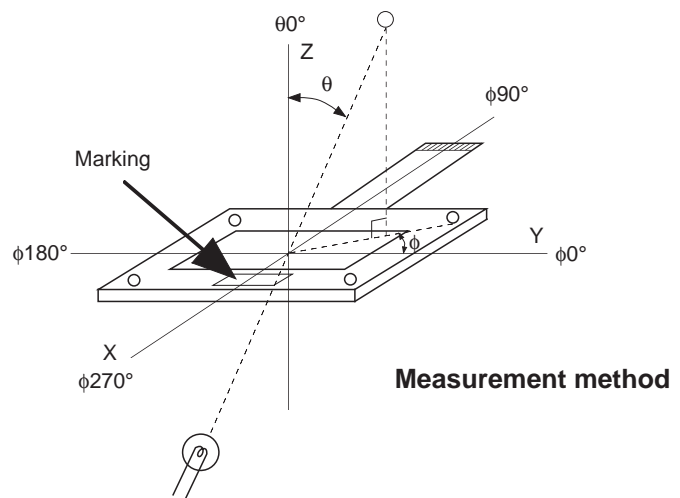
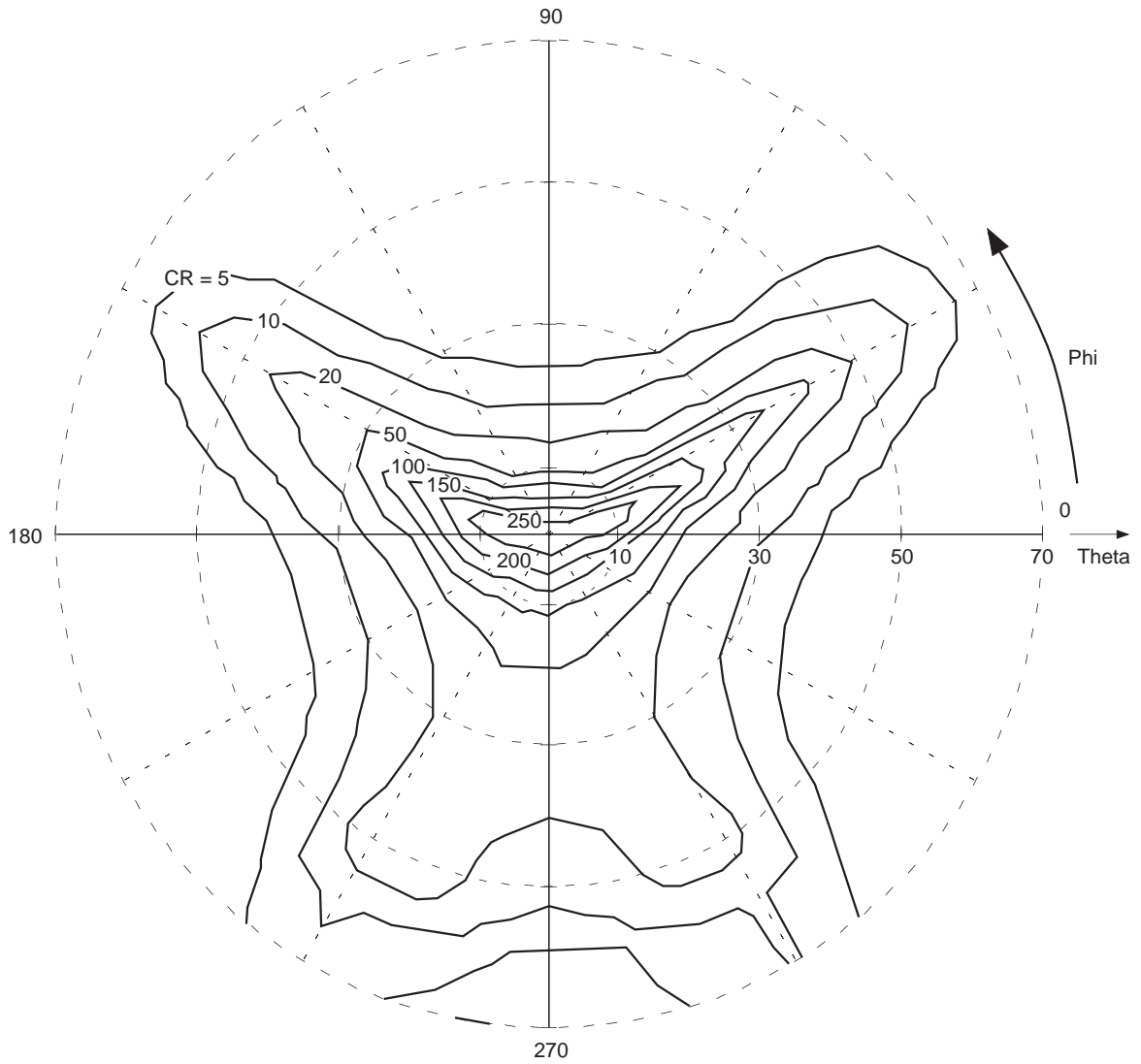
Cross talk is determined by the luminance differences between adjacent areas represented by  $W_i'$  and  $W_i$  ( $i = 1$  to 4) around a black window ( $V_{sig} = 4.5 V/1V$ ).

$$\text{Cross talk value CTK} = \left| \frac{W_i' - W_i}{W_i} \right| \times 100 \text{ [%]}$$

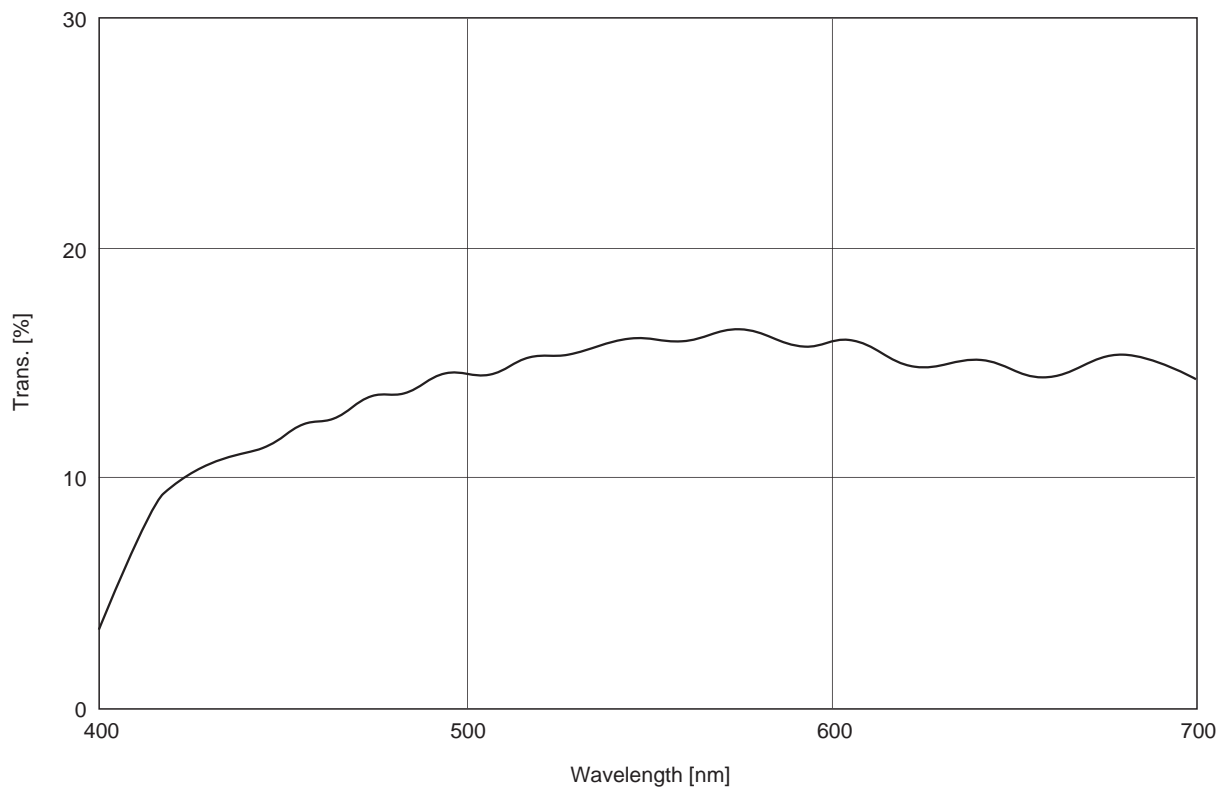




Viewing angle characteristics (Typical Value)



Optical transmittance of LCD panel (Typical Value)



Measurement method: Measurement system II



## 2. LCD Panel Operations

### [Description of basic operations]

- To perform dot-line inverse drive, the pixel arrangement of the same gate is as shown in the diagram. Therefore, the input signal matched to respective arrangement is required for input signals SIG1 to 12.
- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 768 gate lines sequentially in a single horizontal scanning period.
- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 1366 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.
- Vertical and horizontal shift registers address one pixel, and then Thin Film Transistors (TFTs; two TFTs) turn on to apply a video signal to the dot. The same procedures lead to the entire  $1366 \times 768$  dots to display a picture in a single vertical scanning period.

This LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode

These modes are controlled by two signals (RGT and DWN). The right/left and/or up/down setting modes are shown below.

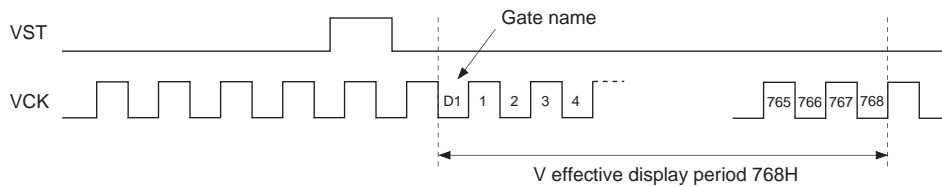
RGT	Mode
H	Right scan
L	Left scan

DWN	Mode
H	Down scan
L	Up scan

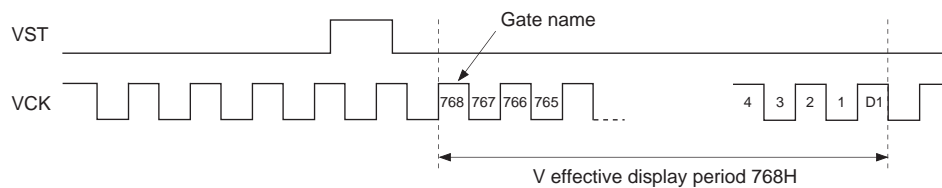
Right/left and/or up/down mean the direction when the Pin 1 marking is located at the right side with the pin block upside.

To locate the active area in the center of the panel in each mode, polarity of the start pulse and clock phase for the H system must be varied. The phase relationship between the start pulse and the clock for each mode is shown below.

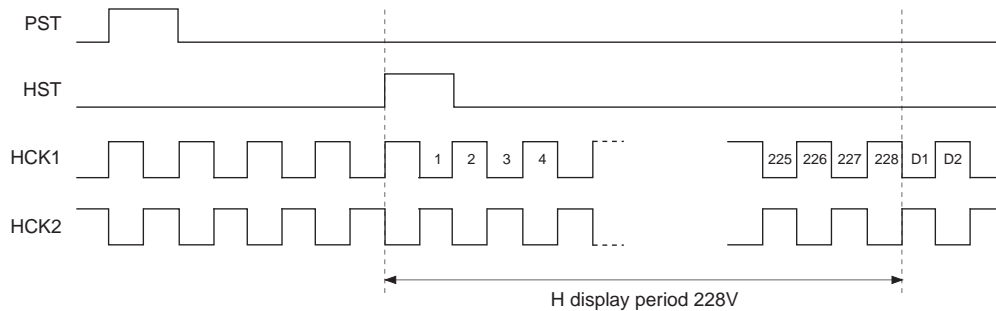
**Vertical direction display period (DWN = H)**



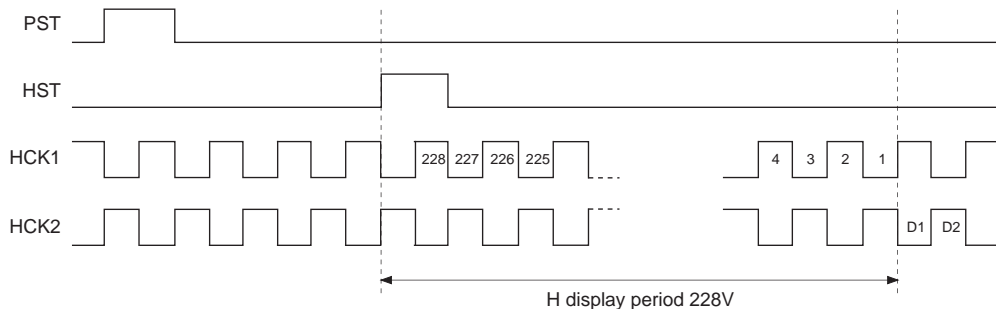
**Vertical direction display period (DWN = L)**



**Horizontal direction display period (RGT = H)**



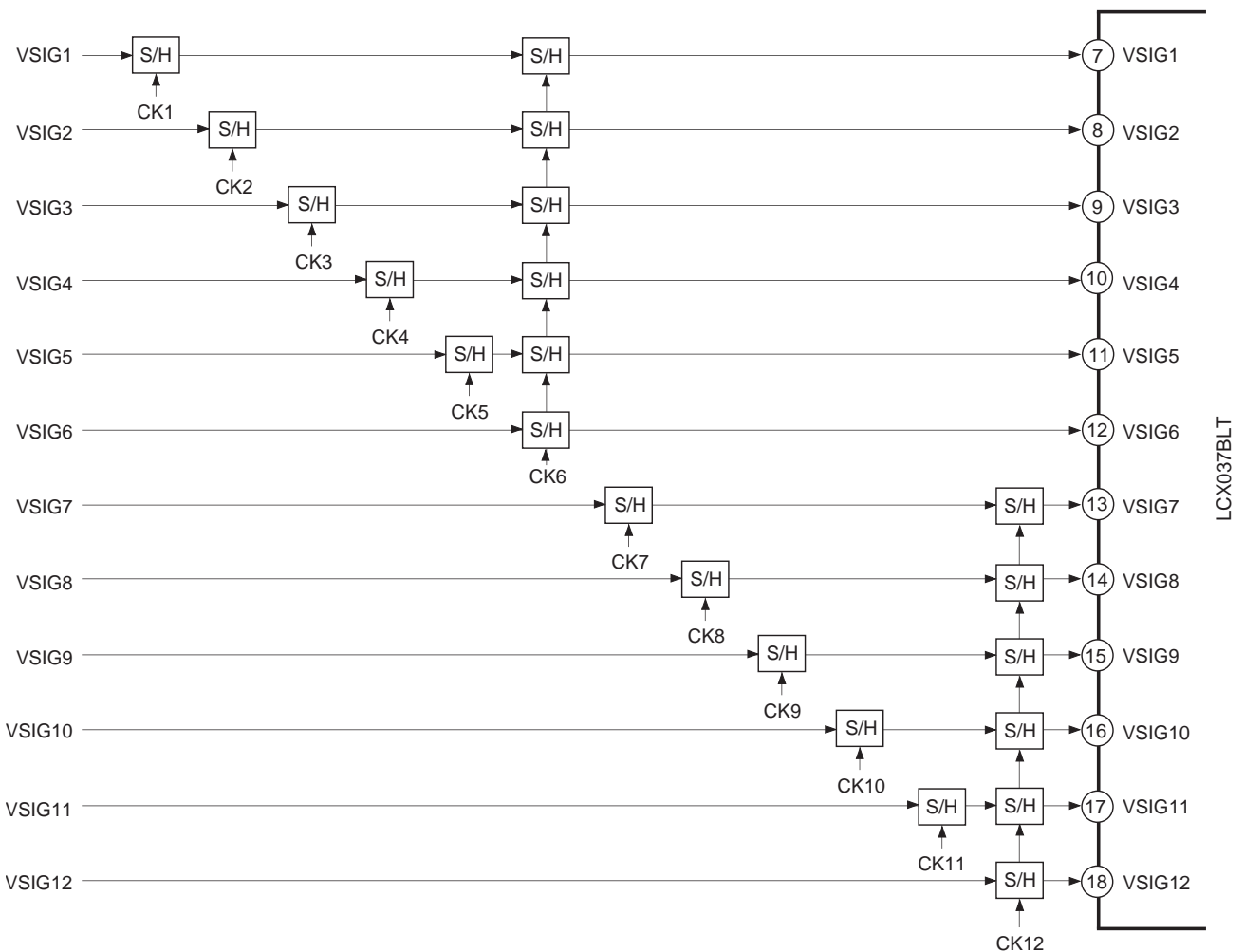
**Horizontal direction display period (RGT = L)**



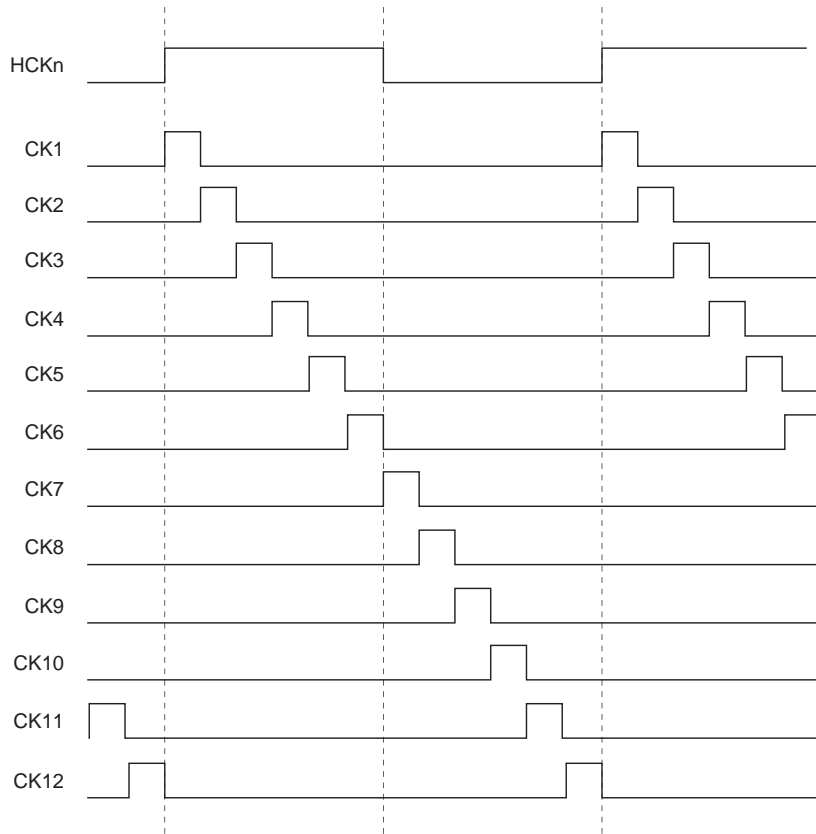
### 3. 12-dot Simultaneous Sampling

The horizontal shift register samples signals VSIG1 to VSIG6, VSIG7 to VSIG12 simultaneously. This requires phase matching between signals VSIG1 to VSIG12 to prevent the horizontal resolution from deteriorating. Thus, phase matching between each signal is required using an external signal delaying circuit before applying the video signal to the LCD panel.

The block diagram of the delaying procedure using the sample-and-hold method is as follows. The following phase relationship diagram indicates the phase setting for right scan (RGT = High). For left scan (RGT = Low), the phase settings for signals VSIG1 to VSIG12 are exactly reversed.

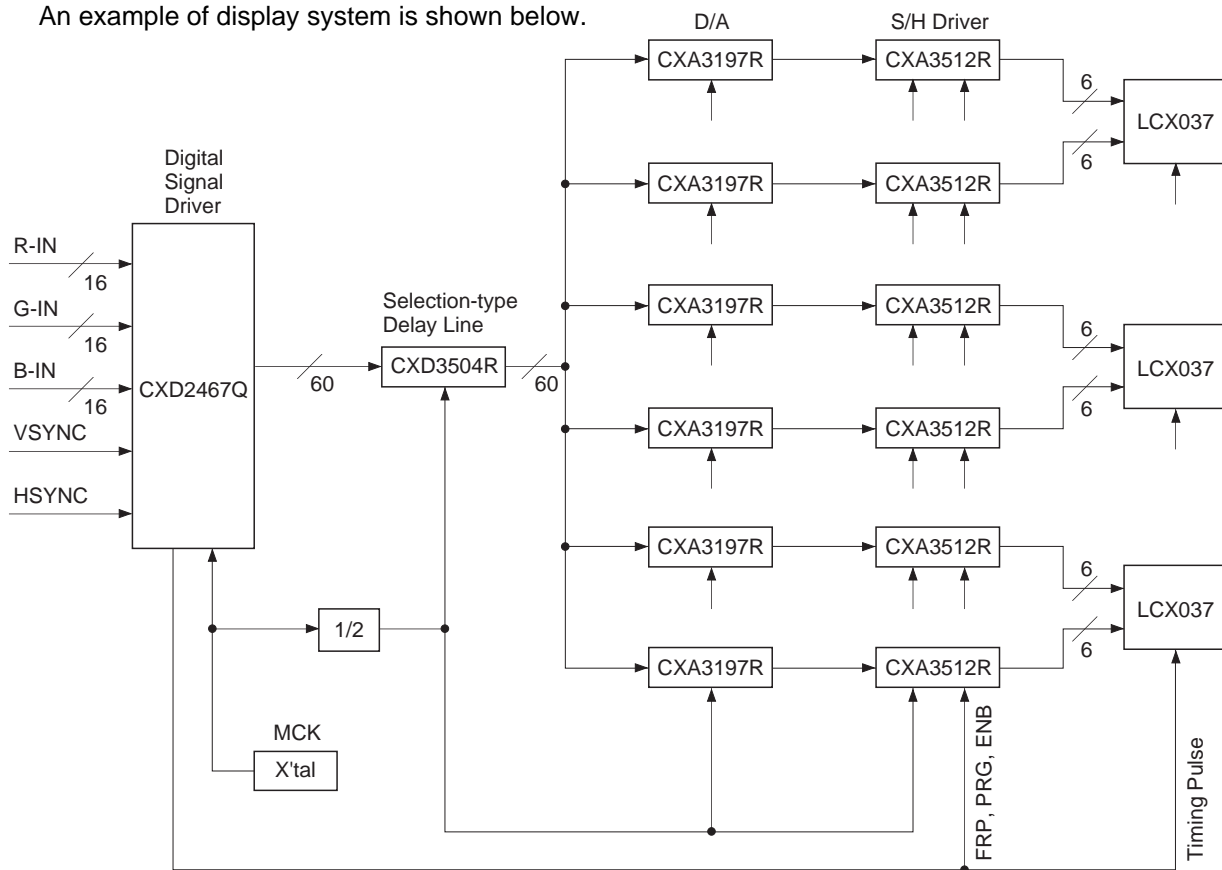


<Phase relationship of delaying sample-and-hold pulses> (right scan)



Display System Block Diagram

An example of display system is shown below.



## Notes on Handling

### (1) Static charge prevention

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

- a) Use non-chargeable gloves, or simply use bare hands.
- b) Use an earth-band when handling.
- c) Do not touch any electrodes of a panel.
- d) Wear non-chargeable clothes and conductive shoes.
- e) Install conductive mats on the working floor and working table.
- f) Keep panels away from any charged materials.
- g) Use ionized air to discharge the panels.

### (2) Protection from dust and dirt

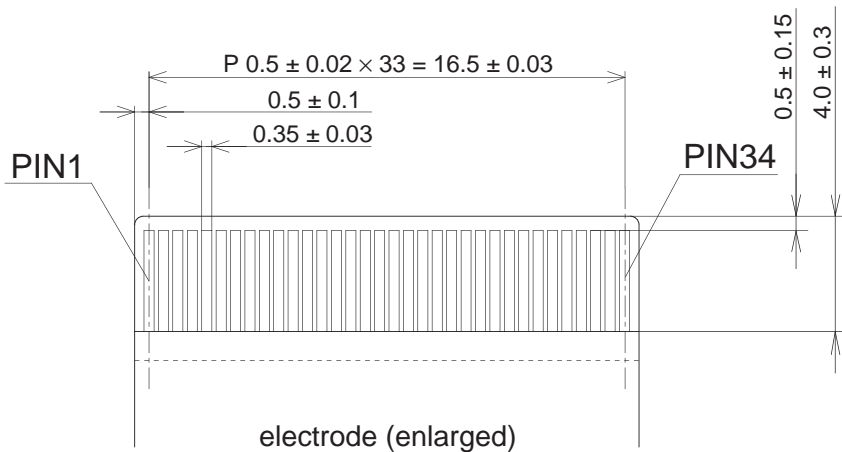
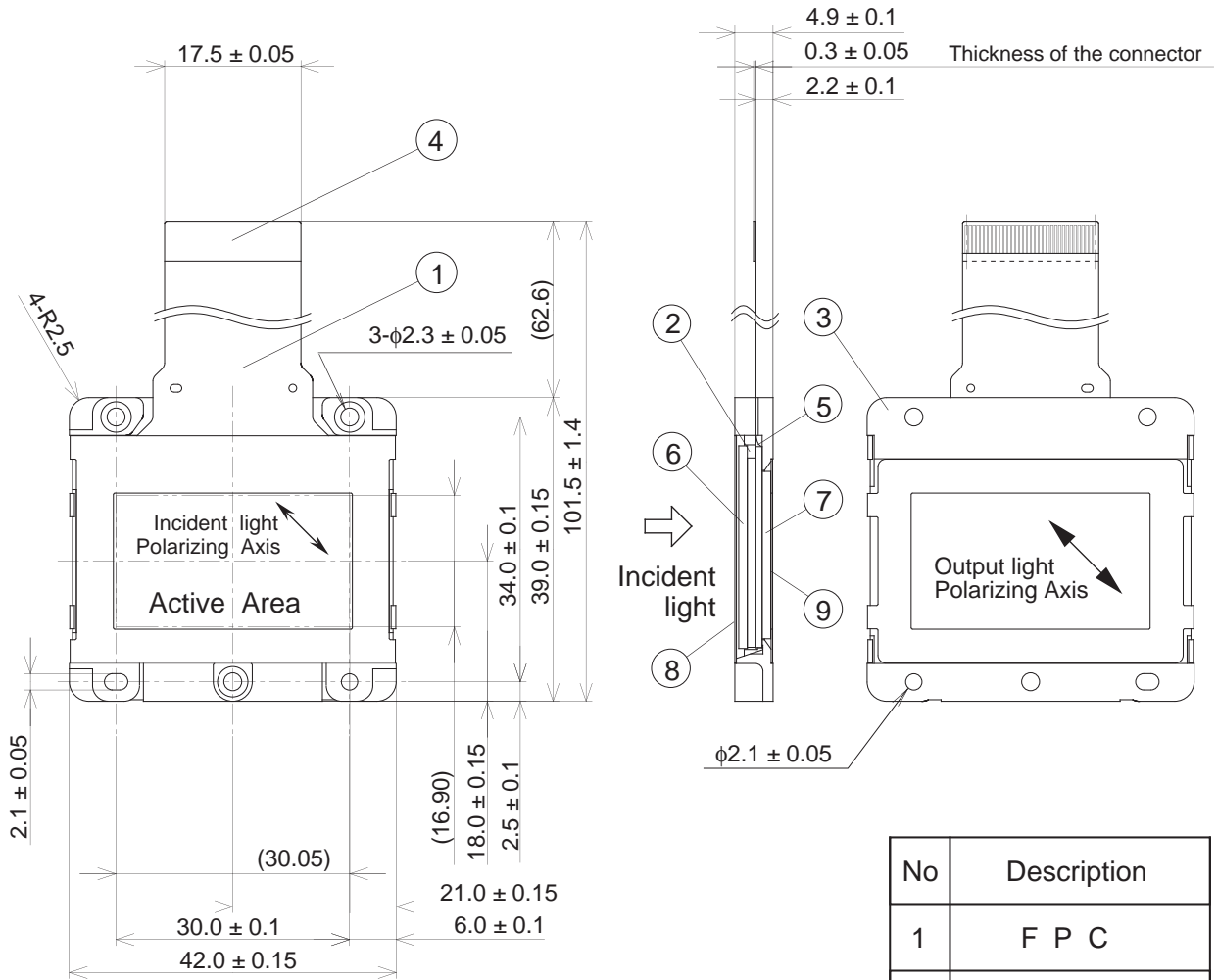
- a) Operate in a clean environment.
- b) When delivered, the panel surface (glass panel) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the glass panel.
- c) Do not touch the glass panel surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave a stain on the surface.
- d) Use ionized air to blow dust off the glass panel.

### (3) Other handling precautions

- a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
- b) Do not drop the panel.
- c) Do not twist or bend the panel or panel frame.
- d) Keep the panel away from heat sources.
- e) Do not dampen the panel with water or other solvents.
- f) Avoid storing or using the panel at a high temperature or high humidity, which may result in panel damages.
- g) Minimum radius of bending curvature for a flexible substrate must be 1mm.
- h) Torque required to tighten screws on a panel must be 3kg · cm or less.
- i) Use appropriate filter to protect a panel.
- j) Do not pressure the portion other than mounting hole (cover).



Package Outline Unit: mm



The rotation angle of the active area relative to H and V is  $\pm 1^\circ$ .

No	Description
1	F P C
2	Molding material
3	Outside frame
4	Reinforcing board
5	Reinforcing material
6	Glass 1
7	Glass 2
8	Cover 1
9	Cover 2

weight 13.7g